National Semiconductor

NMOS RAMs

MM5290*16,384-Bit (16,384 x 1) Dynamic RAM

General Description

The MM5290 is a 16,384 x 1 bit dynamic RAM. It features a multiplexed address input with separate row and column strobes. This added flexibility allows the MM5290 to be used in page mode operation.

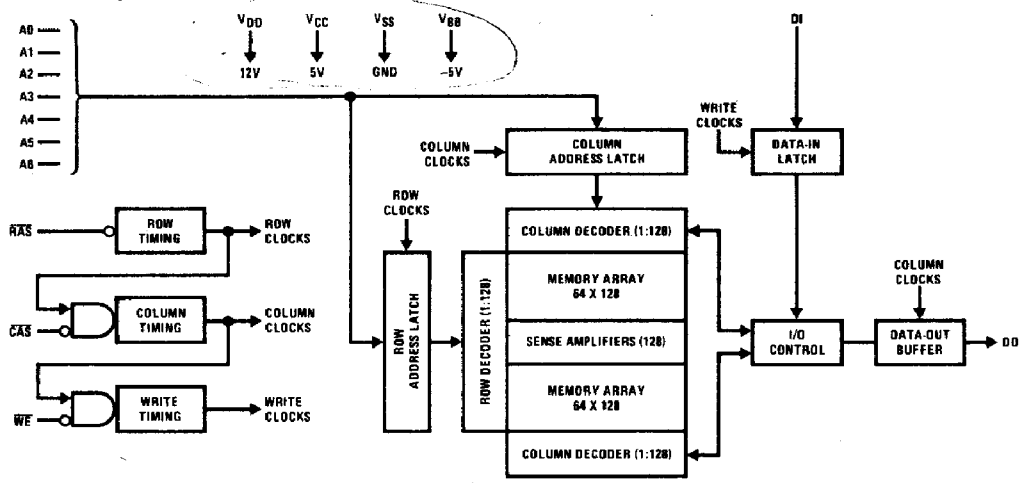
The MM5290 must be refreshed every 2 ms. This can be accomplished by performing any cycle which brings the Row Address Strobe active including a $\overline{RAS}$-only cycle at each of the 128 row addresses.

N-channel double-poly silicon gate technology, developed by National, is used in the manufacture of the MM5290. This process combines high density and performance with reliability. Greater system densities are achievable by the use of a 16-pin dual-in-line package for the MM5290.

Features

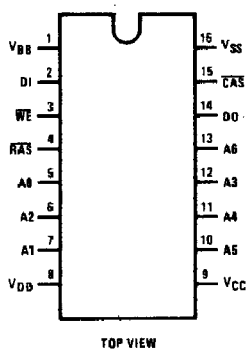
- Access times: 150 ns, 200 ns, 250 ns
- Low power: 528 mW max
- TTL compatible: all inputs and output
- Gated $\overline{CAS}$—noncritical timing
- Read, Write, Read-Modify-Write and $\overline{RAS}$-only Refresh cycles
- Page mode operation
- Industry standard 16-pin configuration

Block Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

*See the MST™ Program page 3.

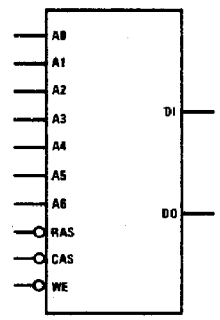
Pin Names

$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0—A6	Address Inputs
DI	Data Input
DO	Data Output
V_{DD}	Power (12V)
V_{CC}	Power (5V)
V_{SS}	Ground
V_{BB}	Power (−5V)

Order Number MM5290J-2, MM5290J-3, or MM5290J-4
See NS Package J16A

Order Number MM5290N-2, MM5290N-3, or MM5290N-4
See NS Package N16A

Logic Diagram



Absolute Maximum Ratings (Note 1)

Storage Temperature −65°C to +150°C
Power Dissipation 1W
Voltage on Any Pin Relative to V_{BB} −0.3V to +20V
($V_{SS} - V_{BB} \geq 4.5V$)
Lead Temperature (Soldering, 10 seconds) 300°C

Recommended DC Operating Conditions

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
T_A	Ambient Temperature	0	70	°C	
V_{DD}	Supply Voltages	10.8	13.2	V	2, 3
V_{CC}		4.5	5.5	V	2, 3
V_{SS}		0	0	V	2, 3
V_{BB}		−4.5	−5.5	V	2, 3
V_{IHC}	Input High Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	2.7	7.0	V	2
V_{IH}	Input High Voltage, A0–A6, DI	2.4	7.0	V	2
V_{IL}	Input Low Voltage, All Inputs	−1.0	0.8	V	2

DC Electrical Characteristics Over the range of Recommended DC Operating Conditions unless otherwise noted

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{DD1}	**Operating Current**		35	mA	4
I_{CC1}	Average Power Supply Operating Current				5
I_{BB1}	($\overline{RAS}$, $\overline{CAS}$ Cycling; t_{RC} = t_{RC} MIN)		200	μA	
I_{DD2}	**Standby Current**		1.5	mA	
I_{CC2}	Power Supply Standby Current ($\overline{RAS}$ = V_{IHC},	−10	10	μA	
I_{BB2}	DO = High Impedance)		100	μA	
I_{DD3}	**Refresh Current**		25	mA	4
I_{CC3}	Average Power Supply Current, Refresh Mode	−10	10	μA	
I_{BB3}	($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = t_{RC} MIN)		200	μA	
I_{DD4}	**Page Mode Current**		27	mA	4
I_{CC4}	Average Power Supply Current, Page Mode				5
I_{BB4}	($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling; t_{PC} = 225 ns)		200	μA	
$I_{I(L)}$	**Input Leakage**	−10	10	μA	
	Input Leakage Current, Any Input				
	(V_{BB} = −5V, 0V ≤ V_{IN} ≤ 7V, All Other				
	Pins not Under Test = 0V)				
$I_{O(L)}$	**Output Leakage**	−10	10	μA	
	Output Leakage Current (DO is Disabled,				
	0V ≤ V_{OUT} ≤ 5.5V)				
	Output Levels				
V_{OH}	Output High Voltage (I_{OUT} = −5 mA)	2.4		V	
V_{OL}	Output Low Voltage (I_{OUT} = 4.2 mA)		0.4	V	
CAPACITANCE					
C_I	Input Capacitance A0–A6, DI		5	pF	6
C_C	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$		10	pF	6
C_O	Output Capacitance, DO		7	pF	6

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Recommended DC Operating Conditions" provides conditions for actual device operation.

Note 2: All voltages referenced to V_{SS}. When applying voltages to the device, V_{DD}, V_{CC} or V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Several cycles are required after power-up before proper device operation is achieved. Any 8 RAS cycles are adequate for this purpose.

Note 4: I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate.

Note 5: I_{CC} depends on output load.

Note 6: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation C = IΔt/ΔV. Capacitance is guaranteed by periodic testing.

AC Electrical Characteristics

Over the range of Recommended DC Operating Conditions unless otherwise noted

SYMBOL	PARAMETER	MM5290-2		MM5290-3		MM5290-4		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	375		375		410		ns	7, 8
t_{RWC}	Read-Write Cycle Time	375		375		515		ns	7, 8
t_{PC}	Page Mode Cycle Time	170		225		275		ns	
t_{RAC}	Access Time from $\overline{RAS}$		150		200		250	ns	9, 11
t_{CAC}	Access Time from $\overline{CAS}$		100		135		165	ns	10, 11
t_{OFF}	Output Buffer Turn-Off Delay	0	40	0	50	0	60	ns	12
t_T	Transition Time (Rise and Fall)	3	35	3	50	3	50	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	100		120		150		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	150	10,000	200	10,000	250	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	100		135		165		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	150		200		250		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	100	10,000	135	10,000	165	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	25	65	35	85	ns	9
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	−20		−20		−20		ns	
t_{ASR}	Row Address Set-Up Time	0		0		0		ns	
t_{RAH}	Row Address Hold Time	20		25		35		ns	
t_{ASC}	Column Address Set-Up Time	−10		−10		−10		ns	
t_{CAH}	Column Address Hold Time	45		55		75		ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	95		120		160		ns	
t_{RCS}	Read Command Set-Up Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
t_{WCH}	Write Command Hold Time	45		55		75		ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	95		120		160		ns	
t_{WP}	Write Command Pulse Width	45		55		75		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	60		80		100		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	60		80		100		ns	
t_{DS}	Data-In Set-Up Time	0		0		0		ns	13, 14
t_{DH}	Data-In Hold Time	45		55		75		ns	13, 14
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	95		120		160		ns	
t_{CP}	$\overline{CAS}$ Precharge Time (for Page Mode Cycle Only)	60		80		100		ns	
t_{REF}	Refresh Period		2		2		2	ms	
t_{WCS}	$\overline{WE}$ to $\overline{CAS}$ Set-Up Time	−20		−20		−20		ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	70		95		125		ns	15
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	120		160		200		ns	15

Note 7: The specifications for $t_{RC(MIN)}$ and $t_{RWC(MIN)}$ are used only to indicate cycle time at which proper operation over the full temperature range is guaranteed.

Note 8: Transition times are measured between V_{IHC} or V_{IH} and V_{IL}. Timing measurements are made between $V_{IHC(MIN)}$ or $V_{IH(MIN)}$ and $V_{IL(MAX)}$, and assume $t_T = 5$ ns.

Note 9: Assumes row-limited access, i.e., $t_{RCD} \leq t_{RCD(MAX)}$. If this condition is not satisfied, then note 10 applies.

Note 10: Assumes column-limited access, i.e., $t_{RCD} > t_{RCD(MAX)}$.

Note 11: Equivalent load is 2 standard TTL inputs plus 100 pF.

Note 12: $\overline{CAS}$ going high disables the Data Output. t_{OFF} is the delay to the high impedance state.

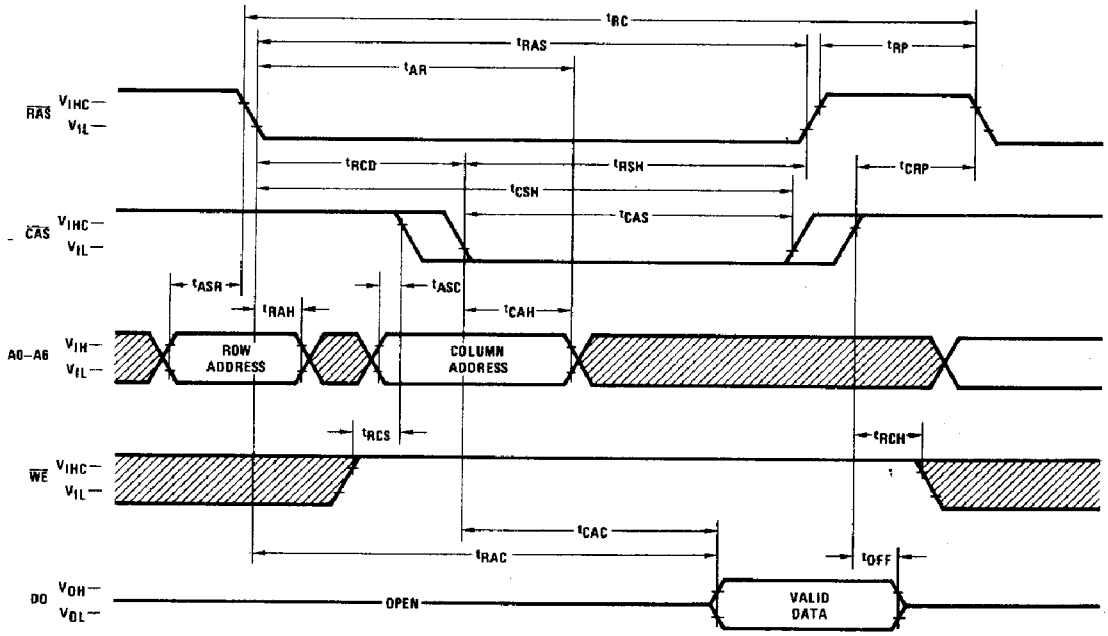
Note 13: These parameters are referenced to the negative edge of $\overline{CAS}$ in an early-write cycle and to the negative edge of $\overline{WE}$ in a Read-Modify-Write cycle. (See Note 12).

Note 14: If $t_{WCS} \geq t_{WCS(MIN)}$, the Data Output is guaranteed to remain in the high impedance state for the duration of the cycle. This is the "early-write" cycle.

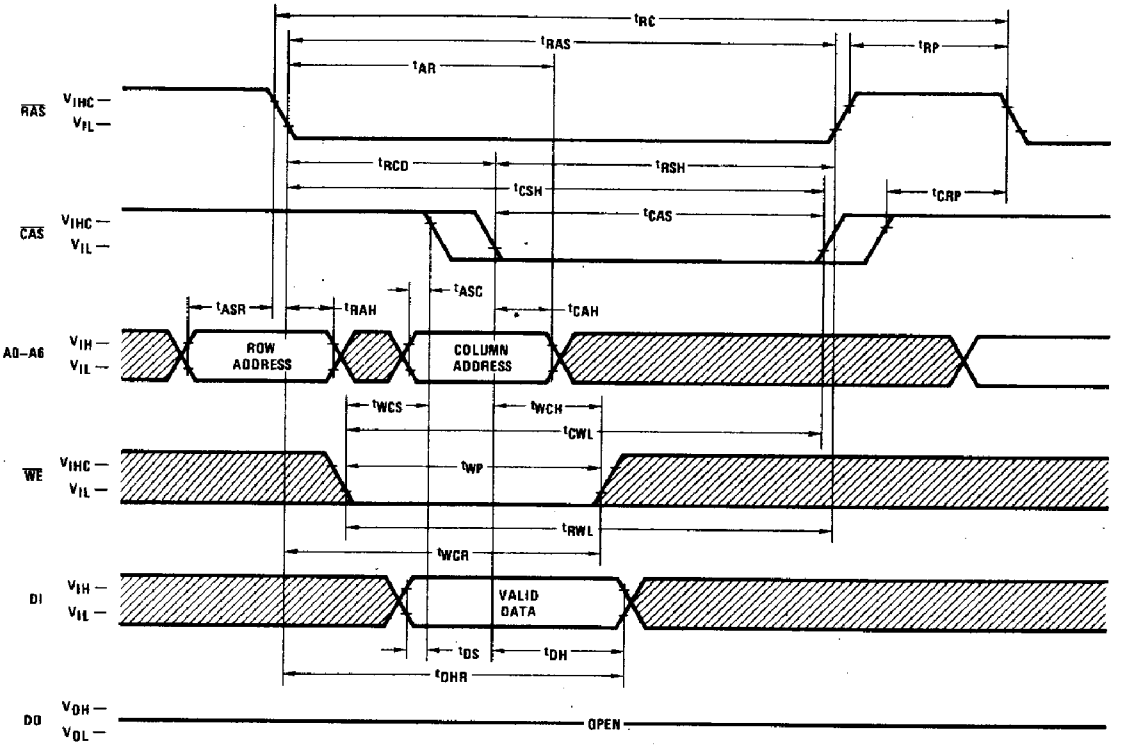
Note 15: If $t_{CWD} \geq t_{CWD(MIN)}$ and $t_{RWD} \geq t_{RWD(MIN)}$, the Data Output will contain the original data in the selected cell. This is the Read-Modify-Write cycle. If either of these conditions is not satisfied, the output will be indeterminate unless the early-write condition of Note 12 is met.

Switching Time Waveforms

Read Cycle

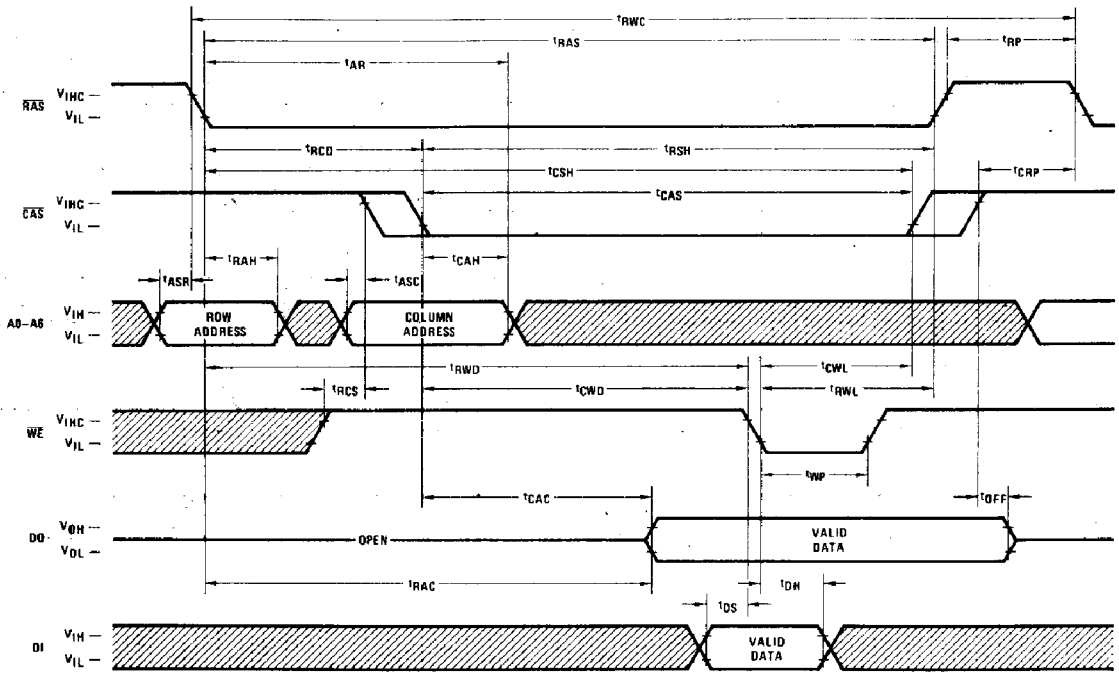


Write Cycle (Early Write)

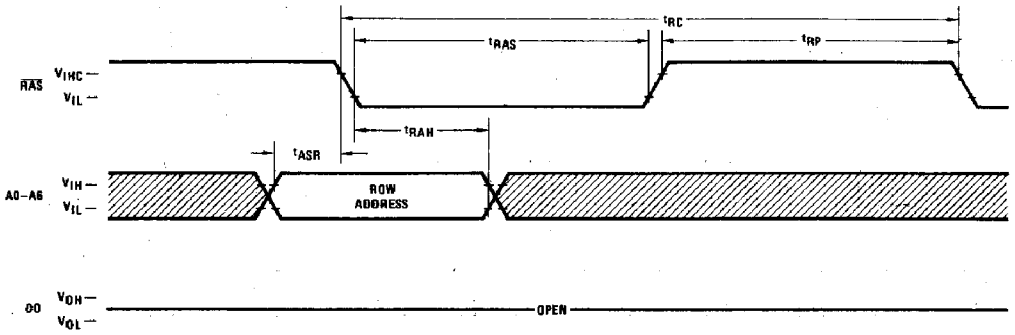


Switching Time Waveforms (Continued)

Read-Write Cycle, Read-Modify-Write Cycle



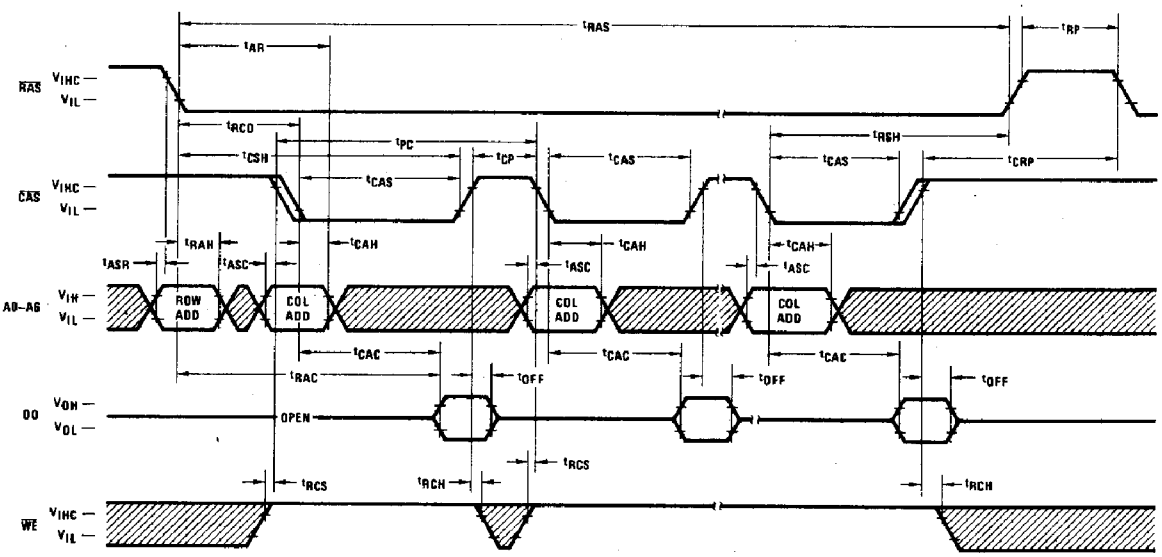
RAS-Only Refresh Cycle



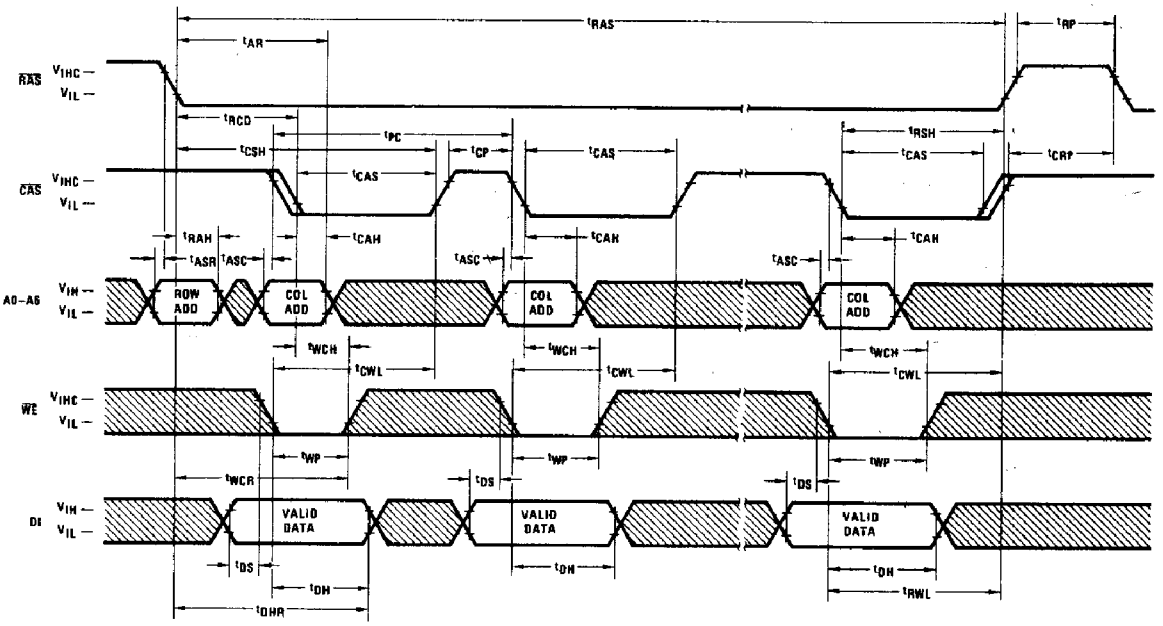
Note. $\overline{CAS}$ = V_{IHC}, $\overline{WE}$ = don't care

Switching Time Waveforms (Continued)

Page Mode Read Cycle



Page Mode Write Cycle



Note. Standard part not tested for page mode