PRODUCT SUMMARY

INTRODUCTION

S5D2510 is a stand-alone OSD Processor, which is used to display monitor adjustment or status information as a certain character or symbol on screen. Its basic operation includes making the R/ G/ B signal for the character or symbol by controlling the internal memory, synchronizing it with the horizontal flyback signal, and mixing it with the main video signal in the video AMP IC. The font data for making the character or symbol is stored in the internal ROM. It is accessed and controlled by the control data, transmitted from the micro controller through the I^2C bus. The chip contains internal PLL circuitry, so all timing control signals, including the system clock, are synchronized with the horizontal flyback signal.

FEATURES

- Enough font to support multiple language :
- Wide Operating (Horizontal) Frequency Range : 30kHz 120kHz
- 640, 800, 1024 and 1280 Dots/ Line
- Pixel Frequency provided by On-Chip PLL : 19.2MHz — 153.6MHz
- General Font Matrix : 12 × 18
- Fully Programmable Display Area : 15 Rows × 30 Columns
- Popular MCU Interface : I^2C Protocol
- Built in 1K-byte SRAM
- Selectable Character Color (Up to 16 Color) : Font basis
- Selectable Raster Color (Up to 16 Color) : Font basis
- Programmable and Auto-adjustable Vertical Height of Character : Range 18 — 63
- Character Blinking and Shadowing : Font basis
- Programmable Symmetrical Row to Row Spacing : Range 0 — 31
- Horizontal Starting Position : 256 different positions (6 dots for each step)
- Vertical Starting Position : 256 different positions (4 scan line for each step)
- Scrolling : Effect where 1 character line is scrolled up or down
- 4 Programmable Window Function and Window Priority Control
- Selectable Window Shadow Width : H/ V 2, 4, 6 and 8 Dots
- Supports Background Video Transparency : Font basis or Window basis
- Full White Pattern Generation for Manufacturing Mode
- Auto Character Height Control
- Full-Screen Display RAM Erasing
- OSD Vertical Bouncing Auto-Detecting & Correction

BLOCK DIAGRAM

The OSD Processor consists of 8 blocks on the top level as shown "Figure 1: Functional block diagram".

There are 4 input signals for the OSD Processor, which are serial data (SDA), clock (SCL) form a micro controller and sync signals (HFLB and VFLB) from the H/ V sync processor. Through the serial data line, all information for the OSD operation are transferred. Here, the protocol is I^2C bus.

The data receiver block is a decoder for decoding the serial input data from a micro controller. The serial data is converted to a 16-bit parallel format at the data receiver block. The parallel data are transported to the RAM or registers by the bus line. The internal bus is a kind of star-bus type.

Control data comes from the data receiver is used to generate the control signals that control the character size, character position, blank mode, blink mode, background color, and etc, in timing controller and display unit block. All timing signals to read/ write data from/ to the internal RAM and ROM are also generated in the timing controller block. In the PLL block, the internal system clock that is synchronized with HFLB is generated, which is used as a timing reference signal for the OSD processor.

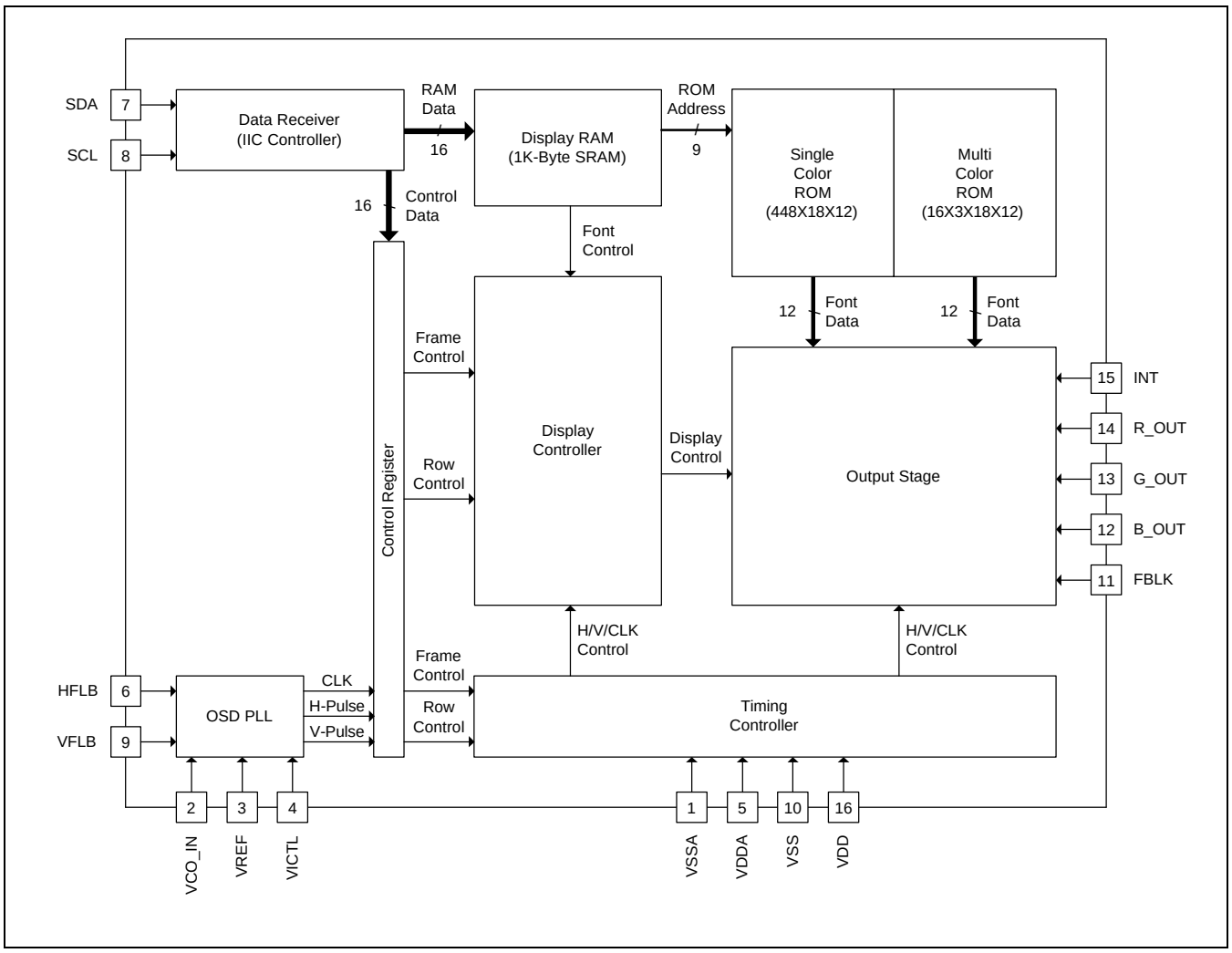


Figure 1. Functional Block Diagram

PIN CONFIGURATIONS

Package Type of the S5D2510 is 16-DIP-300.
Pin Configuration is shown in the figure bellow.

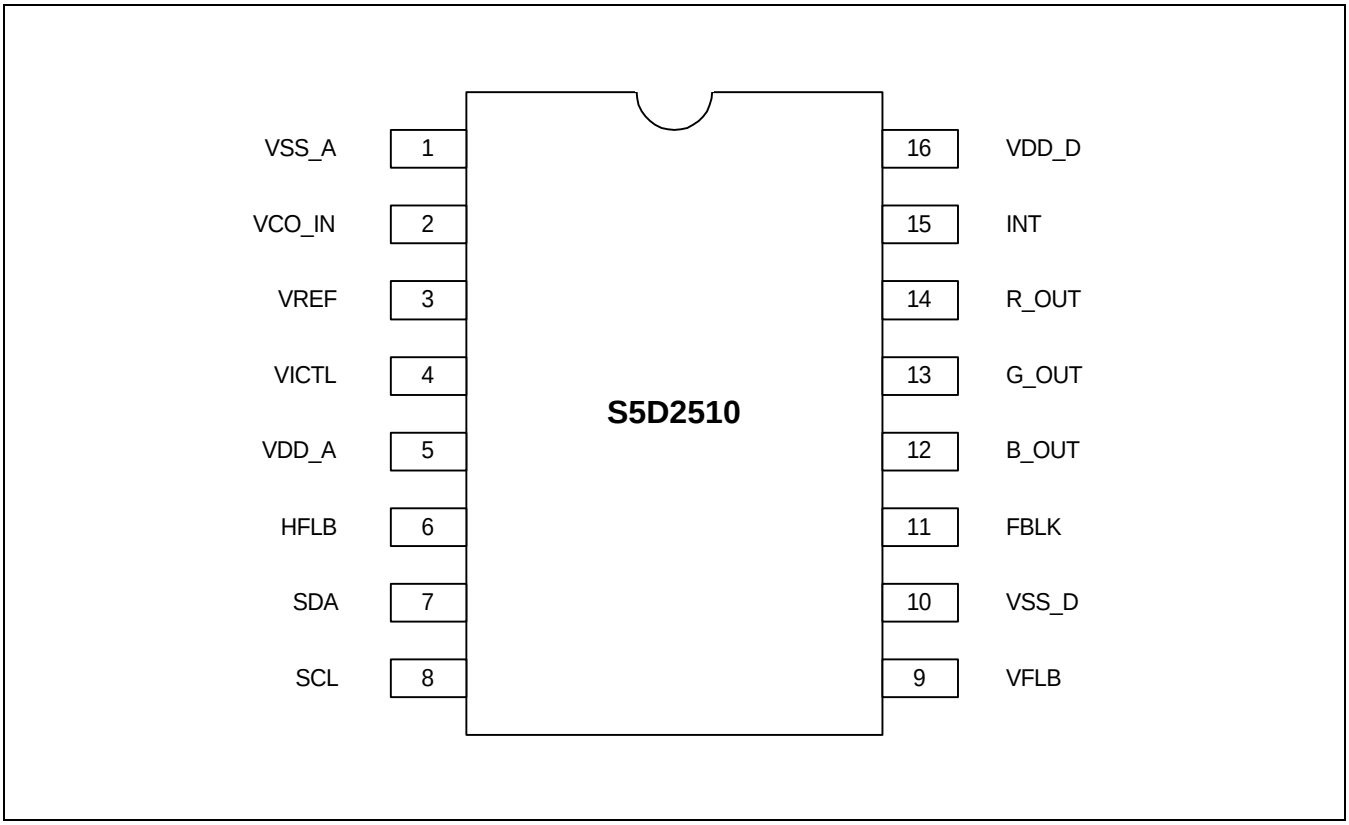


Figure 2. Pin configuration

PIN DESCRIPTIONS

Table 1. Pin Description

Pin No.	Signal	Active	I/ O	Description
1	VSSA	-	-	This pin provides the signal ground to the PLL circuit. We recommend that you separate the analog ground from the digital ground as shown in 'Figure 3 : S5D2510 Application Circuit' (6p) for optimum performance (S5D2510's built-in PLL is sensitive to noise due to wide range PLL characteristics).
2	VCO_IN	-	-	This voltage is made in an external loop filter and sent to VCO's input block. Operation voltage range is about 1 — 4V, and you can raise immunity against external noise if you want lower the VCO sensitivity by allowing the max operation voltage range possible at 5V power voltage. Refer to 'PLL Control' (29p).
3	VREF	-	-	Connect to ground using resistance in order to make the reference current that need to operate internal PLL (PLL region control). Refer to 'PLL Control' (29p)'.
4	VICTL	-	-	PLL gain controlled by controlling VCO Current.
5	VDDA	-	-	This pin supplies +5V supply voltage to the PLL circuit. We recommend that you divide the digital and analog power for PLL as you did in 'Figure 3 : S5D2510 Application Circuit (6p)' to prevent the influence of clock noise on the digital block.
6	HFLB	LOW	Input	Horizontal Flyback : This pin is reference signal source of the internal PLL.
7	SDA	-	In/ Out	Serial Data (I^2C). We recommend that you use the serial resistor about 1/ 10 value of 5V pull-up resistor as I^2C protocol.
8	SCL	-	In/ Out	Serial Clock (I^2C). We recommend that you use the serial resistor about 1/ 10 value of 5V pull-up resistor as I^2C protocol.
9	VFLB	LOW	Input	Vertical Flyback signal : Similar to pin #6, this inputs the negative polarity vertical flyback signal for syncronizing the vertical control circuit.
10	VSS	-	-	Ground for Digital Part
11	FBLK	-	Output	Fast Blank Signal : OSD R/ G/ B output is recognized in the Pre-AMP only when this output pin is high. In other words, if FBLK is low, the OSD R/ G/ B output is not selected in the Pre-AMP.
12	B_OUT	-	Output	OSD Signal Output (B).
13	G_OUT	-	Output	OSD Signal Output (G)
14	R_OUT	-	Output	OSD Signal Output (R)

Table 1. Pin Description (Continued)

Pin No.	Signal	Active	I/ O	Description
15	INT	-	Output	This output pin signifies the color intensity. If you set the intensity control bit to '1' (high) and use with the Pre-AMP supporting intensity function, this pin outputs logic high while the specified character or raster is being displayed. If this pin's output is high, the color level is reduced to half and shows a difference in color level from when it is low, allowing a 16-color choice when this intensity pin and R/ G/ B output are combined. For example, if R, G, B are all high, white is output. If you set the INT bit to '1' (high), the color level becomes reduced to half and outputs gray.
16	VDD	-	Output	+5V Supply Voltage for Digital Part

* In the table above, only HFLB and VFLB's active column is low. This means that HFLB and VFLB are set so that they are inputted as active low in default. For more information, please refer to 'Register Descriptions (13p)'.

APPLICATION CIRCUIT

— When you are doing PCB Art Work, separate analog VDD and digital VDD.

— Using PCB pattern, separate analog Ground and main ground, and then connect two ground with Bead as following figure.

— Because communication noise influences the operation of PLL, I^2C communication line keep away from analog block (Pin #1 — #5) as possible as.

— You can improve the monitor's video characteristics (OSD ringing, OSD smear) and regulation characteristics by adding serial resistance to S5D2510's output pins (Pin #11 — Pin #15).

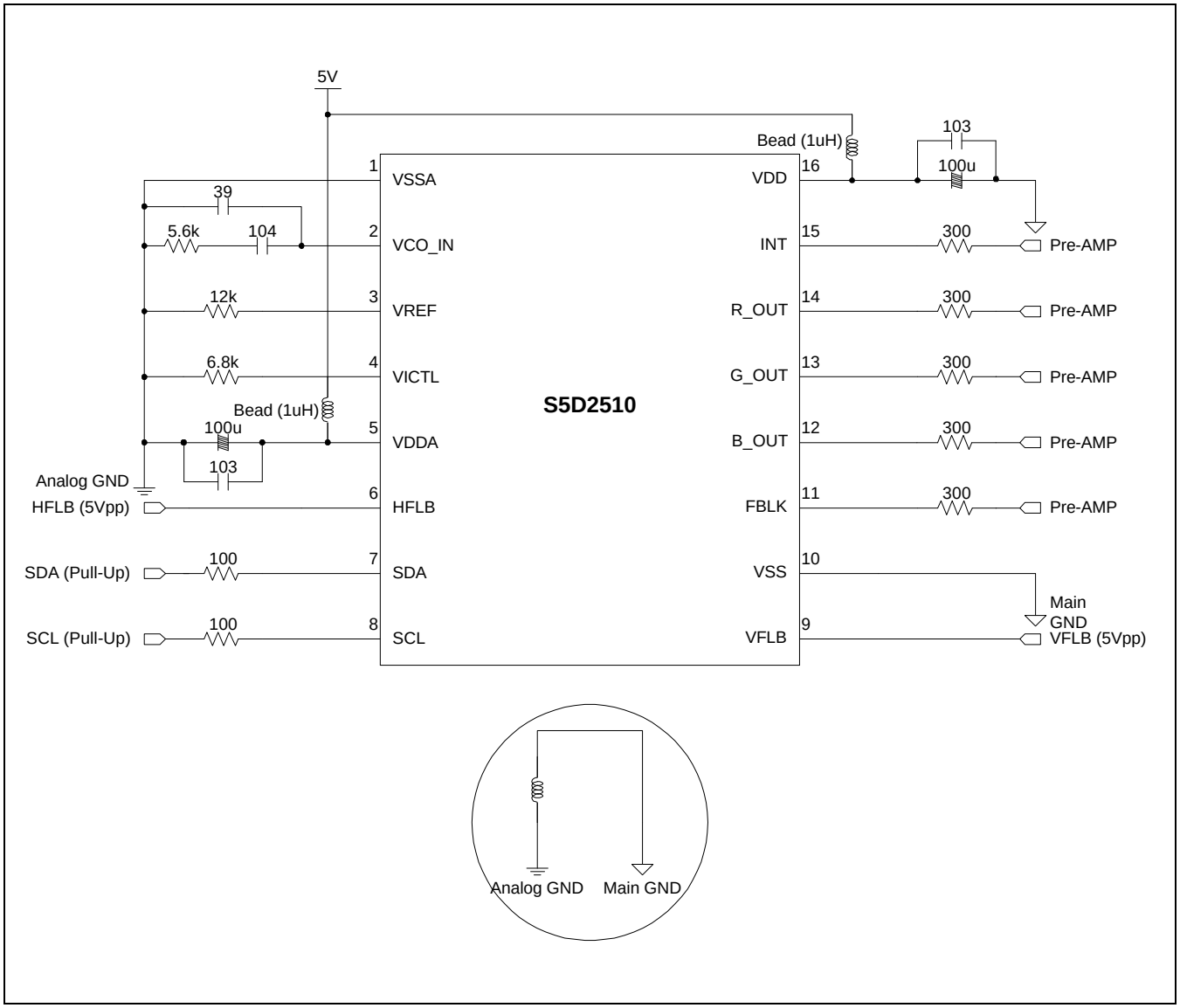
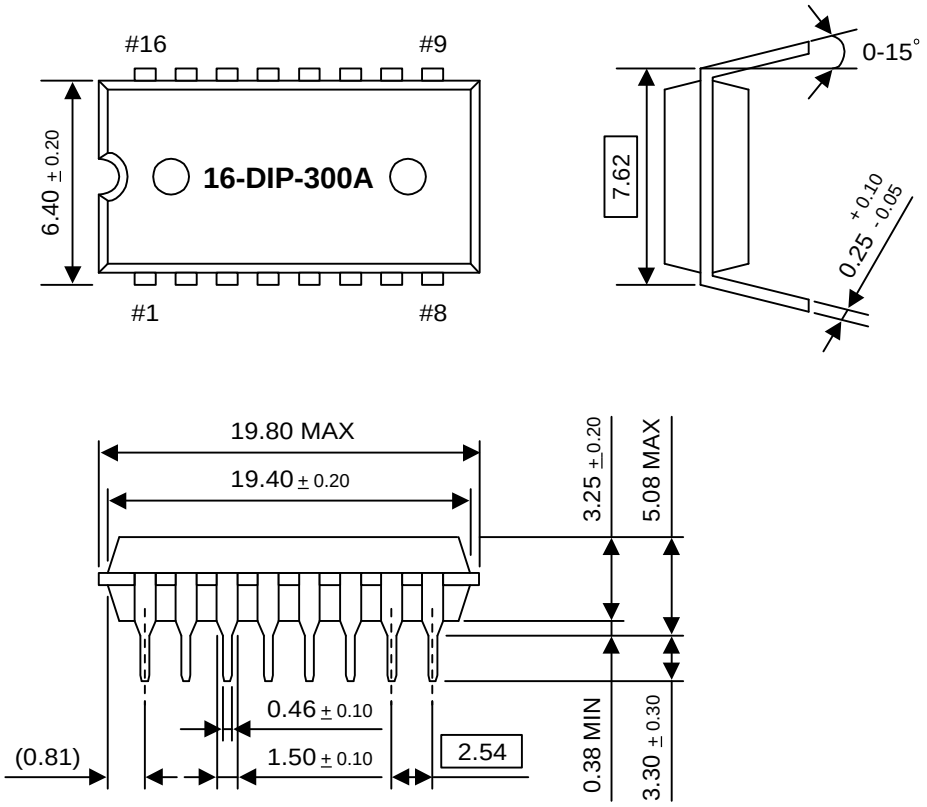


Figure 3 : S5D2510 Application Circuit

PACKAGE INFORMATION



NOTE: Dimensions are in millimeters.

Figure 4 : S5D2510 Package Information

SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply Voltage	VDD	0 — 6.5	V
Input Voltage	VI	0 — 5.25	V
Power Dissipation	Pd	1200	mW
Operating Temperature Range	Topr	-20 — 70	°C
Storage Temperature Range	Tstg	-40 — 125	°C

♣ PKG Thermal Resistance : 64.2°C / W

ELECTRICAL CHARACTERISTICS

DC Electrical Characteristics

Table 3. DC Electrical Characteristics

(Ta = 25°C, VDD_A = VDD_D = 5V)

Parameters (Conditions)	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VDD	4.75	5.00	5.25	V
Supply Current (No load on any output)	IDD	-	-	25	mA
Input Voltage	VIH	0.8VDD	-	-	V
	VIL	-	-	VSS+0.4	V
Output Voltage	VOH	0.8VDD	-	-	V
(Iout = ± 1mA)	VOL	-	-	VSS+0.4	V
Input Leakage Current	IIL	-10	-	10	uA
VCO Input Voltage	VVCO	-	2.5	-	V

OPERATION TIMING

OUTPUT SIGNAL R/ G/ B_OUT, INT, FBLK

Table 4: Rise/ Fall Time of Output Signal

(Ta = 25°C, VDDA = VDD=5V, CLOAD = 30pF)

Parameters (Conditions)	Symbol	Min.	Typ.	Max.	Unit
Rise Time	tR	-	-	2	nsec
Fall Time	tF	-	-	2	nsec

Input Signal HFLB, VFLB

Table 5: Frequency of Input Signal

Parameters(Conditions)	Symbol	Min.	Typ.	Max.	Unit
Horizontal Flyback Signal Frequency	fHFLB	-	-	120	kHz
Vertical Flyback Signal Frequency	fVFLB	-	-	200	Hz

C Interface SDA, SCL

Table 6: Operating Time of I^2C Interface

Parameters (Conditions)	Symbol	Min.	Typ.	Max.	Unit
SCL Clock Frequency	fSCL	-	-	300	kHz
Hold Time for start condition	ths	500	-	-	ns
Set Up Time for stop condition	tsus	500	-	-	ns
Low Duration of clock	tlow	400	-	-	ns
High Duration of clock	thigh	400	-	-	ns
Hold Time for data	thd	0	-	-	ns
Set Up Time for data	tsud	500	-	-	ns
Time between 2 access	tss	500	-	-	ns
Fall Time of SDA	tfSDA	-	-	20	ns
Rise Time of both SCL and SDA	trSDA	-	-	-	ns

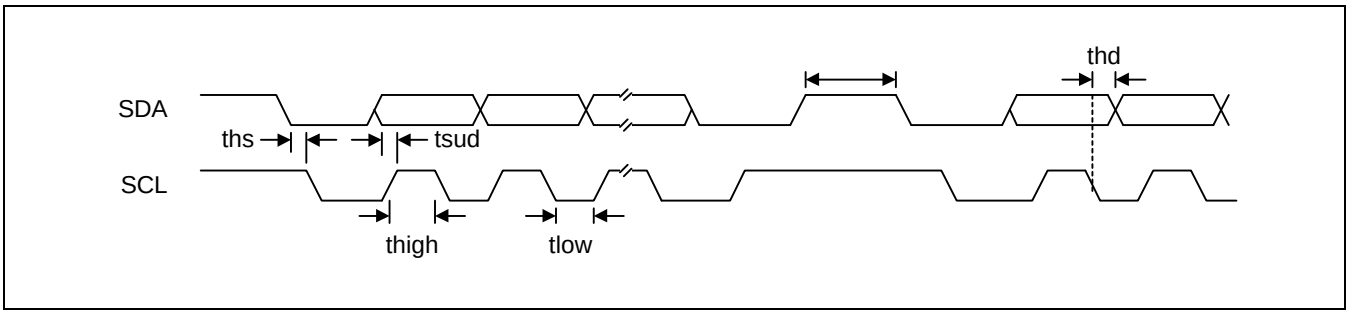


Figure 5 : Operation Timing - SDA and SCL

FUNCTIONAL DESCRIPTIONS

DATA TRANSMISSION

The communication interface between S5D2510 and MCU follows the I^2C protocol. As shown in "Figure 6 : Data Transmission Format", It supports two formats to transmit 16-bits register values effectively. After the starting pulse, the transmission takes place in the following order: Slave address with R/ W bit, each 1-byte row/ column address, 2-byte data, and stop condition. An acknowledge signal is received for each byte, excluding only the start/ stop condition. It assigns 8-bits out of 16-bits to font address for selecting character code, because attribute bits of the "Character & Attribute Registers" is composed of 8-bits for convenient adjustment with font unit. By the way, S5D2510 needs 9-bits for addressing 464-fonts by reason that it supports 464-fonts.
Therefore, the needed 1-bit is assigned to the RMSB of column address bit pattern as follows "Address Bit Pattern for Display Registers Data". For using the RMSB, it must be enabled the COLEN bit of row address bit pattern.
S5D2510's slave address is BAh. It is BBh in read mode, and BAh in write mode.

Address Bit Pattern for Display Registers Data

(a) Row Address Bit Pattern — R3 - R0 : Valid Data for Row Address

A15	A14	A13	A12	A11	A10	A9	A8
COLEN	X	X	C4	R3	R2	R1	R0

COLEN : Column Data Format Enable

(b) Column Address Bit Pattern — C4 - C0 : Valid Data for Column Address

A7	A6	A5	A4	A3	A2	A1	A0
RMSB	X	X	C4	C3	C2	C1	C0

RMSB : ROM Address MSB Bit — 'X' : Don't care bit

Data Transmission Format

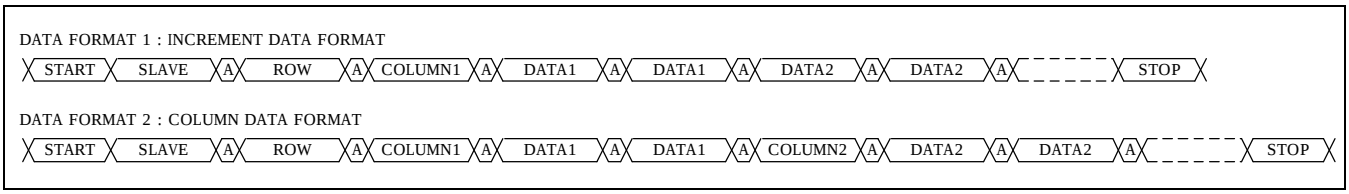


Figure 6: Data Transmission Formats

SDA / SCL Signal at Communication

Data Format 1 : Auto Increment Data Format

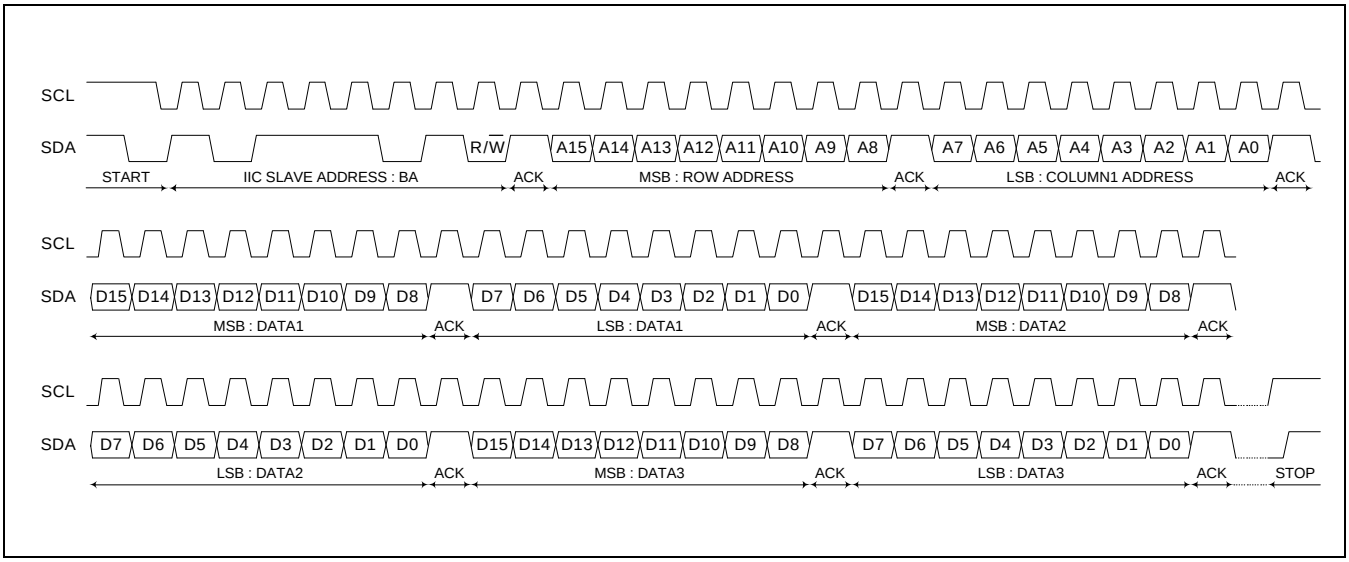


Figure 7 : SDA/ SCL Timing Chart (Format 1)

Data Format 2 : Column Data Format

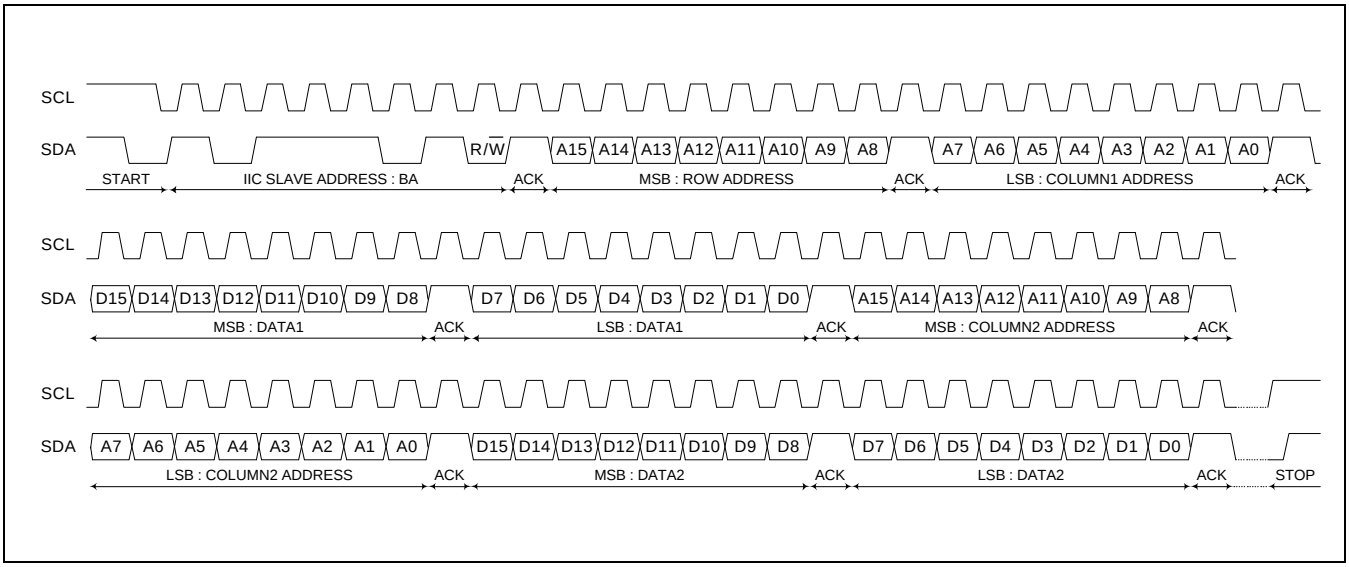


Figure 8 : SDA/ SCL Timing Chart (Format 2)

* As you can see the "Figure 7, 8 : SDA/ SCL Timing Chart", just the time when the SCL is low, the SDA can be occurred transition. Therefore, you must program MCU not to occur timing violation.

MEMORY MAP

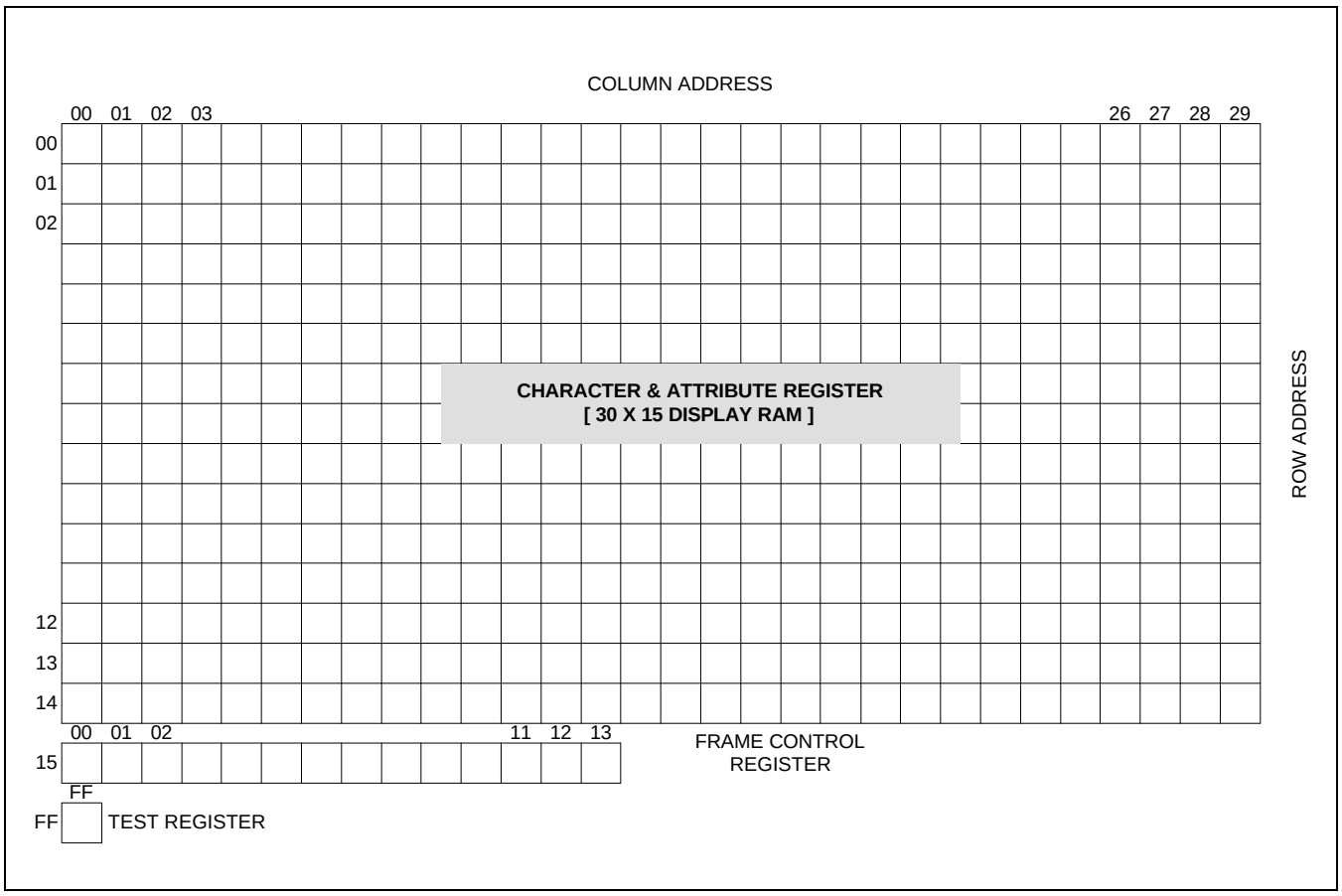


Figure 9: Memory Map of Display Registers

The display RAM's address of the row and column number are assigned in order. The display RAM is composed of 2 register groups (Character & Attribute Register, Frame Control Register).

The display area in the monitor screen is 30 columns X 15 rows, so the related "Character & Attribute Registers" are also 30 columns X 15 rows. Each register has a character address and characteristics corresponding to the display location on the screen, and one register is composed of 16-buts. The lower 8-bits and the extended 1-bit (the MSB of row/ column address) are used for selecting a font out of 464 ROM fonts, and upper 8-bits are assigned to give a character attribute to a selected font.

"Frame Control Registers" are in the 15th row. "Frame Control Register 0 — 2" control with frame unit display position of the OSD, height of character, blinking, scrolling, and etc function. "Frame Control Register 3" select extended codes to control 'Blink', 'Shadow', 'Character intensity', and 'Raster intensity'. "Frame Control Register 4" specify the reference value for "Auto height control" and "Row to row space". "Frame Control Register 5 — 13" control in relation to 4-windows.

Each register's configurations shown in "Figure 10 : Register Description (13p) ". For more detailed information, refer to "Table 7 : Register Description (14p) ".

REGISTER DESCRIPTION

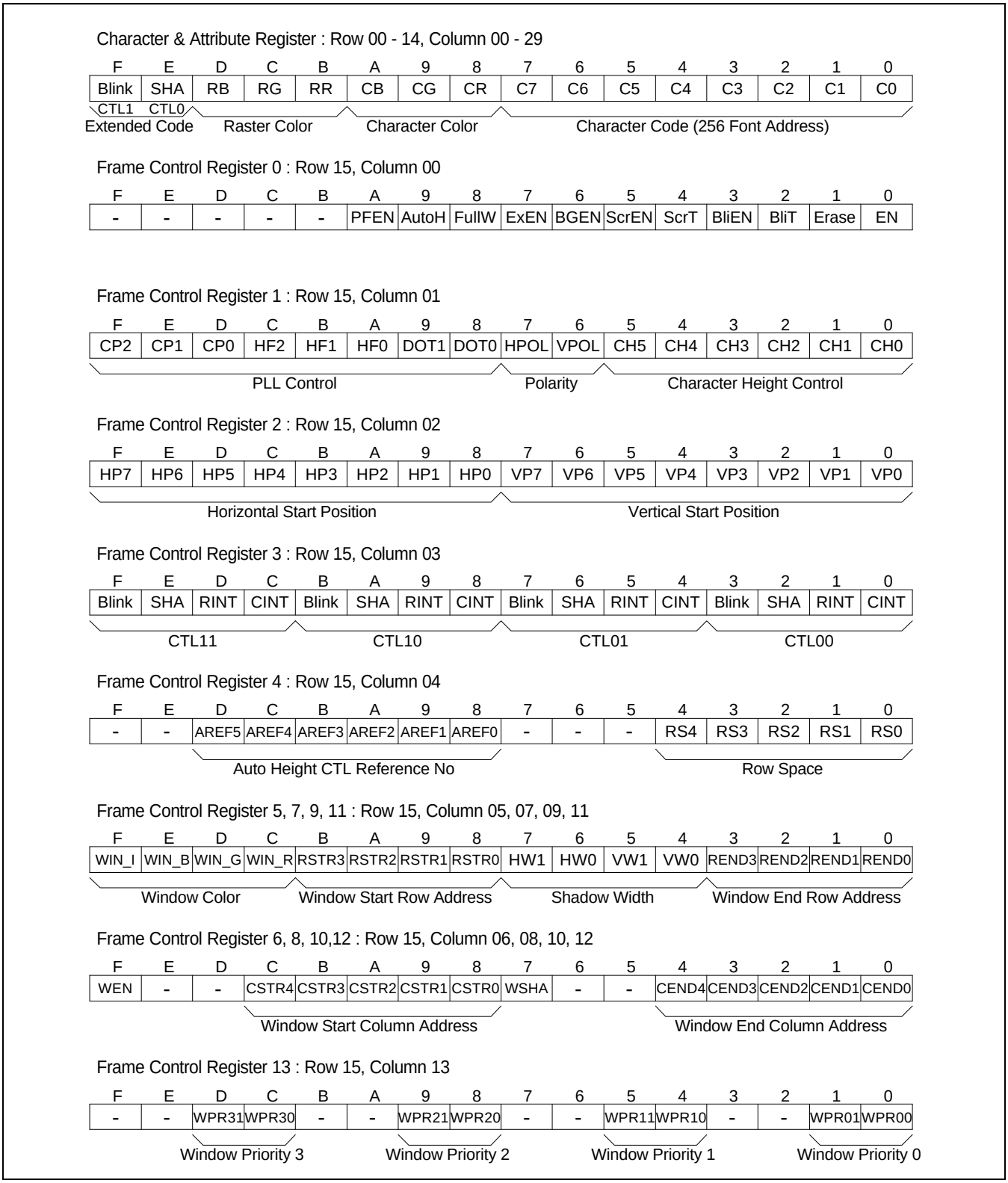


Figure 10: Register Description

Table 7: Register Description

Registers	Bits	Description
Character & Attribute Registers (Row 00 — 14, Column 00 — 29)	Blink (Bit F)	**Character Blink** Set this bit to activate character blinking effect or use as 'CTL1' bit for selecting "Extended code set".
	SHA (Bit E)	**Character Shadow** Set this bit to activate character shadowing effect or use as 'CTL0' bit for selecting "Extended code set".
	RB, RG ,RR (Bit D — B)	**Raster Color** A color out of 16-colors is selected by these 3-bits and 'RINT' bit in "Frame Control Register 3" as raster color.
	CB, CG, CR (Bit A — 8)	**Character Color** A color out of 16-colors is selected by these 3-bits and 'CINT' bit in "Frame Control Register 3" as character color.
	C7 — C0 (Bit 7 — 0)	**Character Code Address** These 8-bits is used for accessing 256 ROM fonts. If you access over 256 FOM fonts, Column data format must be used. Column address MSB 'RMSB' bit is used for MSB of 9-bits ROM fonts address.
Frame Control Registers-0 (Row15, Column00)	Bit F — B	Reserved.
	PFEN (Bit A)	**Programmable Full White Pattern Enable** As size as you want, you can determine full white pattern by using "Window size" at 320 OSD resolution. On the other hand, 'FullW' bit is used automatic "Full white pattern generation".
	AutoH (Bit 9)	**Auto Adjustable Vertical Font Height Control** If this bit is high, height of font is sustained as 'AREF' Bits regardless of video input mode.
	FullW (Bit 8)	**Full White Pattern Generation** If this bit is set high, OSD outputs full white pattern automatically.
	ExEN (Bit 7)	**Extended Code Enable** If this bit is set high, Bit F/ E in "Character & Attribute Registers" are used for selecting extended code set 'CTL00 — CTL11'.
	BGEN (Bit 6)	**Back Ground Enable** If you set this bit to '1', black color of OSD raster area is transparent. This control bit is aimed for round-type OSD window generation.
	Scrl (Bit 5)	Scroll Enable Refer to 'Scrolling (28p)'.
	ScrT (Bit 4)	Scroll Time Control If this bit is '1', the scroll time is 0.5sec, otherwise 1.0sec.
	BliEN (Bit 3)	Blink Enable If you set this bit to high, blink the font with 'Blink' attribute.
	BliT (Bit 2)	Blink Time Control If this bit is '1', the blink time is 0.5sec, otherwise 1.0sec.
	Erase (Bit 1)	RAM Erasing RAM data are erased by setting this bit. Refer to 'Display RAM (19p)'.
	EN (Bit 0)	OSD Enable The character display is controlled by this bit. If this bit is high, OSD is enable. Otherwise, disable. When this bit is disabled, OSD isn't output inspite of writing control data.

Table 7: Register Description (Continued)

<table>
<tr><th>Registers</th><th>Bits</th><th>Description</th></tr>
<tr><td rowspan="8">Frame Control Registers-1 (Row15, Column01)</td><td>CP2 — CP0 (Bit F — D)</td><td>Charge Pump Output Current Control
This is the PLL block's internal phase detector output status, converted into current. The output is determined by these 3-bits.
<table><tr><th>CP2</th><th>CP1</th><th>CP0</th><th>Current</th><th>CP2</th><th>CP1</th><th>CP0</th><th>Current</th></tr><tr><td>0</td><td>0</td><td>0</td><td rowspan="2">40µA</td><td>1</td><td>0</td><td>0</td><td>160µA</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>200µA</td></tr><tr><td>0</td><td>1</td><td>0</td><td>80µA</td><td>1</td><td>1</td><td>0</td><td>240µA</td></tr><tr><td>0</td><td>1</td><td>1</td><td>120µA</td><td>1</td><td>1</td><td>1</td><td>280µA</td></tr></table></td></tr>
<tr><td>HF2 — HF0 (Bit C — A)</td><td>Horizontal Frequency
PLL's horizontal frequency is decided by the combination of these 3-bits. This is related to the selection of DOT[1:0], so you can't numerically express the frequency range with only the HF[2:0] selection. For more information, please refer to 'Separating region of frequency (30p)'.</td></tr>
<tr><td>DOT1, DOT0 (Bit 9,8)</td><td>Resolution Control (Dots/ Line)
<table><tr><th>Dot1</th><th>dot0</th><th>No. Of Dots</th></tr><tr><td>0</td><td>0</td><td>640 dots/line</td></tr><tr><td>0</td><td>1</td><td>800 dots/line</td></tr><tr><td>1</td><td>0</td><td>1024 dots/line</td></tr><tr><td>1</td><td>1</td><td>1280 dots/line</td></tr></table>As shown above, the number of dots per horizontal line is decided by a combination of these two bits.</td></tr>
<tr><td>HPOL (Bit 7)</td><td>Polarity of Horizontal Fly Back Signal
If this bit is '1', HFLB's polarity is positive, and if '0', it is negative. In other words, this bit is set to '1' if active high, and '0' if active low.</td></tr>
<tr><td>VPOL (Bit 6)</td><td>Polarity of Vertical Fly Back Signal
If this bit is '1', VFLB's polarity is positive, and if '0', it is negative. In other words, this bit is set to '1' if active high, and '0' if active low.</td></tr>
<tr><td>CH5 — CH0 (Bit 5 — 0)</td><td>Character Height Control
The purpose of CH[5:0] is to output OSD of a uniform size even if the resolution changes. If you adjust the value in the range of CH = 18 — CH = 63, each line's repeating number is decided (standard height CH = 18 is the reference value), by which the line is repeated. For more information on repeating number selection, refer to 'Character Height (26p)'.</td></tr>
<tr><td rowspan="2">Frame Control Registers-2
(Row15, Column02)</td><td>VP7 — VP0</td><td>Vertical Start Position Control (= VP[7:0] × 4)
Signifies top margin height from the V-Sync reference edge.</td></tr>
<tr><td>HP7 — HP0</td><td>Horizontal Start Position Control (= HP[7:0] × 6)
Signifies delay of the horizontal display from the H-Sync reference edge to the character's 1st pixel location.</td></tr>
</table>

* The purpose of bits 'HPOL', and 'VPOL' is to provide flexibility when using the S5D2510 IC. No matter which polarity you choose for the input signal, the IC will handle them identically, so you can select active high or active low according to your convenience.

Table 7: Register Description (Continued)

Registers	Bits	Description
Frame Control Registers-3 (Row15, Column03)	CTL11 (Bit F — C)	**Extended Code Set 11** If 'ExEN' bit of "Frame Control Register 0" is set to high, when Bit F (CTL1) and Bit E (CTL0) of "Character & Attribute Registers" are set to '11', these extended code set is referred as the combination of 'Blink', 'SHA', 'RINT', and 'CINT'. That is, you may set previously the combination that you want. and then select the extended code set by 'CTL1' and 'CTL0' bits.
	CTL10 (Bit B — 8)	**Extended Code Set 10** If 'ExEN' bit of "Frame Control Register 0" is set to high, when Bit F (CTL1) and Bit E (CTL0) of "Character & Attribute Registers" are set to '10', these extended code set is referred as the combination of 'Blink', 'SHA', 'RINT', and 'CINT'. That is, you may set previously the combination that you want. and then select the extended code set by 'CTL1' and 'CTL0' bits.
	CTL01 (Bit 7 — 4)	**Extended Code Set 01** If 'ExEN' bit of "Frame Control Register 0" is set to high, when Bit F (CTL1) and Bit E (CTL0) of "Character & Attribute Registers" are set to '01', these extended code set is referred as the combination of 'Blink', 'SHA', 'RINT', and 'CINT'. That is, you may set previously the combination that you want. and then select the extended code set by 'CTL1' and 'CTL0' bits.
	(Bit 3 — 0)	**Extended Code Set 00** If 'ExEN' bit of "Frame Control Register 0" is set to high, when Bit F (CTL1) and Bit E (CTL0) of "Character & Attribute Registers" are set to '00', these extended code set is referred as the combination of 'Blink', 'SHA', 'RINT', and 'CINT'. That is, you may set previously the combination that you want. and then select the extended code set by 'CTL1' and 'CTL0' bits.
Frame Control Registers-4 (Row15, Column04)	Bit F — E	Reserved.
	AREF (Bit D — 8)	**Auto Height Control** Reference Number If 'AutoH' bit of "Frame Control Register 0" is set to '1', must set these AREF[5:0] from 1 to 63. These control bits means the number of font that you want to display in direction of vertical monitor line. In this case, that is, 'AutoH' bit is set to '1' and AREF[5:0] bits is set, OSD fonts sustain constant vertical height regardless of video input mode change. If calculated font height is smaller than 18, font height is displayed by 18 lines. In other hands, if 'AutoH' Bit is set to '0', this function is ignored and character height is determined by CH[5:0] of "Frame Control Register 1". Refer to 'Character Height (26p)'.
	Bit 7 — 5	Reserved.
	RS (Bit 4 — 0)	**Row Space Number** It means the line number between a character row and the next row. The default value is 0. For obtaining symmetrical row space, first and last line are extended in each row. (line number for spacing = RS[4:0] 2) Refer to 'Figure 15 : OSD window area(24p)'.

Table 7: Register Description (Continued)

Registers	Bits	Description
Frame Control Registers-5, 7, 9, 11 (Row15, Column05, 07, 09, 11)	WIN_I, WIN_B, WIN_G, WIN_R (Bit F — C)	Window Raster Color Attribute The priority of raster color is determined by these bits is higher than raster color is determined by RB/ RG/ RR bits of "Character & Attribute Registers". 'WIN_I' bit may make 16-colors with the pre-AMP that support intensity function as like as 'CINT' or 'RINT'.
	RSTR3 — RSTR0 (Bit B — 8)	Window Start Row Address : Range 0 — 15 It means the row address that window starts from. About actually start point, refer to 'III-6.3 Window Generation'(27p).
	HW1,HW0 (Bit 7 — 6)	Horizontal Width of Window Shadowing The horizontal width of window shadow is determined by these HW[1:0] bits setting as follows : (Horizontal Width = HW 2 Dots)
	VW1,VW0 (Bit 5 — 4)	Vertical Width of Window Shadowing The vertical width of window shadow is determined by these VW[1:0] bits setting as follows : (Vertical Width = VW × 2 Lines)
	REND3 — REND0 (Bit 3 — 0)	Window End Row Address : Range 0 — 15 It means the row address that window stops on. About actually stop point, refer to 'III-6.3 Window Generation'(27p).
Frame Control Registers-6, 8, 10, 12 (Row15, Column06, 08, 10, 12)	WIN_EN (Bit F)	Window Enable Set this bit to activate window.
	Bit E — D	Reserved.
	CSTR4 — CSTR0 (Bit C — 8)	Window Start Column Address : Range 0 — 29 It means the column address that window starts from. About actually start point, refer to 'III-6.3 Window Generation'(27p).
	WSHA (Bit 7)	Window Shadowing Enable If this bit is set '1', activate the area of window shadow as width as HW and VW.
	Bit 6 — 5	Reserved.
	CEND4 — CEND0 (Bit 3 — 0)	Window End Column Address : Range 0 — 29 It means the column address that window stops on. About actually stop point, refer to 'III-6.3 Window Generation'(27p).

* That "Frame Control Register 5" pair with "Frame Control Register 6" control the function about window. As like above, that the odd register pair with the even register in "Frame Control Register 7 — 12" control about each "Window 1 — 3".

Table 7: Register Description (Continued)

Registers	Bits	Description
Frame Control Registers-13 (Row15, Column13)	Bit F — E	Reserved.
	WPR31, WPR30 (Bit D — C)	Window Priority 3 Determine a window out of 4 windows that has the lowest priority. The selected window area may be overlapped by a area of the window that has higher priority.
	Bit B — A	Reserved.
	WPR21, WPR20 (Bit 9 — 8)	Window Priority 2 Determine a window out of 4 windows that has the 3rd priority.
	Bit 7 — 6	Reserved.
	WPR11, WPR10 (Bit 5 — 4)	Window Priority 1 Determine a window out of 4 windows that has the 3rd priority.
	Bit 3 — 2	Reserved.
	WPR01, WPR00 (Bit 1 — 0)	Window Priority 0 Determine a window out of 4 windows that has the highest priority. The selected window area overlaps lower priority windows.

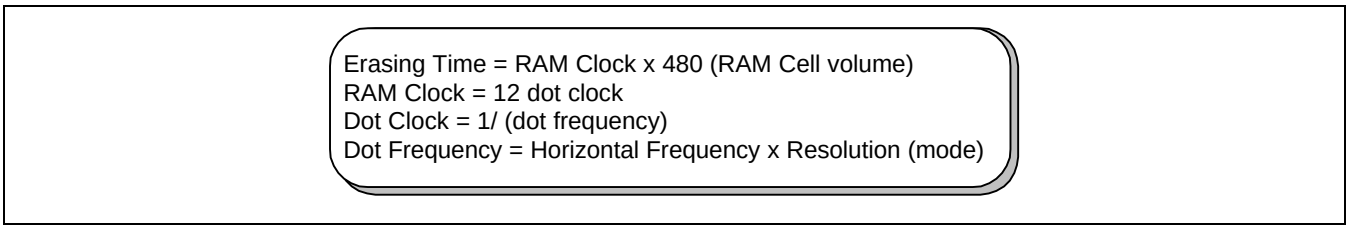
* If you determine window priorities with "Frame Control Register 13", each window overlaps lower priority windows. So you can make pop-up window OSD. Refer to 'Transparency (23p)'.

ADDRESSING

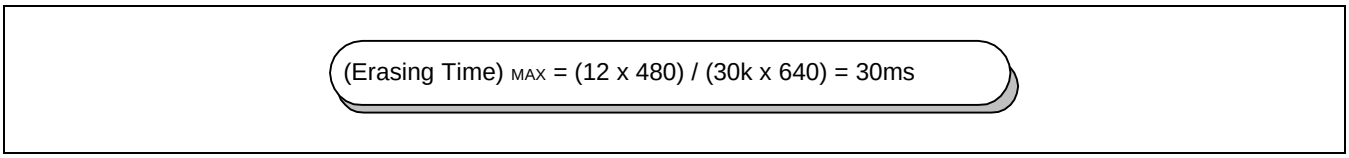
DISPLAY RAM

1 k-Byte SRAM (512 × 16 bits) is built in S5D2510. Registers are distributed within 16 rows × 30 columns. But, for facilitating internal calculation, addressing is done using exponents of 2, and the S5D2510 is composed of 16 rows × 32 columns RAM Cell.
if 'Erase' Bit of "Frame Control Register 0" is enabled by setting '1' and erased RAM, 480 RAM cells are erased excepting only 16th row (Frame Control Registers). Therefore, the 'Erasing Time' is measured with 480 RAM cells as the standard.

* Erasing Time



So, the maximum value of the 'Erasing Time' is as follows.



When you are programming with MCU, you have not to give the S5D2510 other operation or command during the $(\text{Erasing Time})_{MAX}$ at a minimum, if you hope that timing violation isn't happened.

ROM FONTS

S5D2510 provides 464 ROM fonts for displaying OSD icons, which allows the use of multi-language OSD icons. Out of the 464 ROM fonts, 448 are standard fonts, and 16 are multi-color fonts. The standard font is placed at 000h address is reserved for blank data. Each multi-color font is composed of 4 color attribute ROM fonts are as shown "Figure III-4.2 : Composition of ROM Fonts".
A multi-color font is made by 'OR operating with these 3 fonts. When you want to access this multi-color font, you may call the address of R-color attribute font. In example, the addresses of 1C0h, 1D0h and 1E0h mean respectively R, G, B color attribute fonts. and that the multi-color font is accessed by addressing 1C0h is made with 1C0h, 1D0h, and 1E0h through 'OR' operation.

To do addressing 464 ROM fonts, as explained at "Memory Map (12p)", the S5D2510 uses 9 bits added 1 extended bit which use the MSB of row/ column address and 8 bits for character code bits in "Character & Attribute Registers".

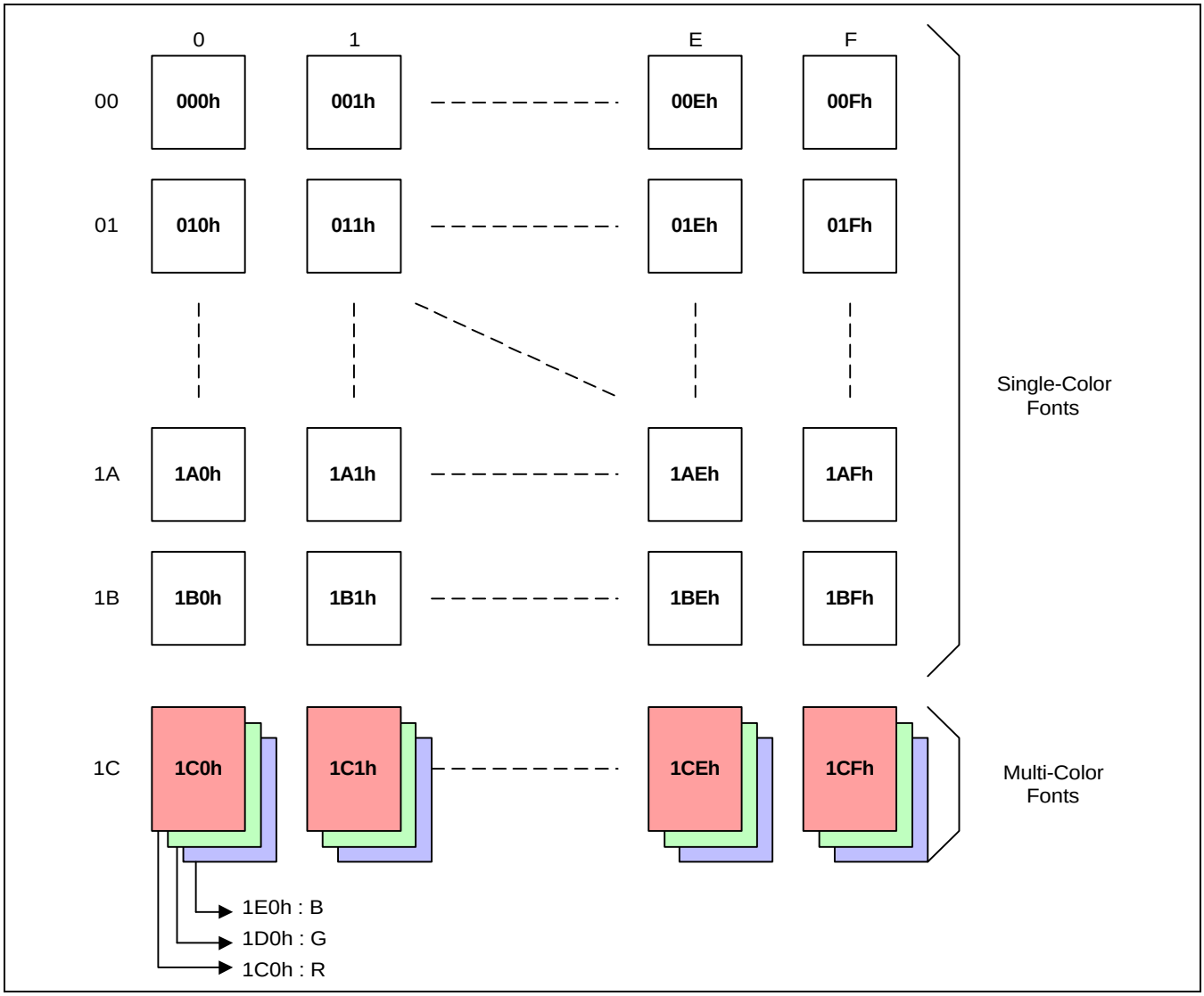


Figure 11: Composition of ROM Fonts

Notes for when making S5D2510 Fonts

Address 000h is appointed as blank data. RAM's initial values are all 0, and all bits are written as 0 when you erase the RAM, so blank data means the initial value. In other words, blank data means 'do nothing'. You don't need to write any data for the space font, except for 000h. It just needs to be an undotted area.

If you want to express a font image color the way you want according to the multi-color font characteristics, you must keep in mind that you are using a multi-color font when selecting the character or raster color. When you select a character or raster color, the color that was 'OR' operation to the original color is expressed. You should also consider the multi-color font's raster part. Since raster color is applied to '0' areas even with 'OR' operation, you can express many different background colors even with one multi-color font. The best thing to do is to set any part that you don't want to change color as the character part, and the changeable parts as the raster part when using a multi-color font.

COLORING

If you have an intensity feature, the number of possible colors you can express becomes doubled. In other words, the number of colors you can represent with three colors blue, green, and red is 8 (= 2^3), but with the intensity feature, it is 16 (= 2^4).

Character Color

Character Color is assigned for each font, and the 4 components for expressing a color are listed below.

Blue	CB bit [A] of "Character & Attribute Registers"
Green	CG bit [9] of "Character & Attribute Registers"
Red	CR bit [8] of "Character & Attribute Registers"
Intensity	CINT bit of extended code set in "Frame Control Register 3" which is set by CTL1:CTL0 bits [F:E] in "Character & Attribute Registers".

Raster Color

Blue	RB bit [D] of "Character & Attribute Registers"
Green	RG bit [C] of "Character & Attribute Registers"
Red	RR bit [B] of "Character & Attribute Registers"
Intensity	RINT bit of extended code set in "Frame Control Register 3" which is set by CTL1:CTL0 bits [F:E] in "Character & Attribute Registers".

If the extended code is enabled by setting ExEN bit in "Frame Control Register 0" to '1', that the extended code is set in "Frame Control Register 3" is selected by [F:E] bits of "Character & Attribute Registers". So, you can select attribute with font unit by the various composition of Blink, Shadow, Raster Color Intensity, and Character Color Intensity. Otherwise, you can select just blink and shadow attributes with font base. Therefore, if you want to express 16 colors, you must enable ExEN bit and also set RINT and CINT bits of extended code set in "Frame Control Register 3" to '1'.

Multi-Color Font

The multi-color fonts supported in S5D2510 is composed of 3 fonts (red, green, and blue) as the structure in "III-4.2 ROM Fonts"(21p) and can express 16 colors as single-color fonts is did 'OR' operation.

The reason for using such multi-color fonts is that it makes it possible to express different colors within one font. Therefore, if one font's character, symbol and background (raster) are each composed of a single color, you don't need to use a multi-color font. Let's take a look at an example.

When making a single-color font, the dots make up a font's character or symbol, and the other undotted areas are called raster (background without character or symbol). If we think of this in a binary format, the dotted areas are '1', and the undotted areas are '0'. If we decide upon a character color, it will only influence the areas that are '1', and if you select a raster color, it will only influence the areas that are '0'.

For example, in the standard font file, the font of 020h doesn't have any part that is '1'. So even if you select a character color for this font, there will be no changes since there are no '1' areas. But if you select a raster color for this font, since all areas are '0', the entire font area will become the selected raster color.

We do 'OR' operation for the 3 fonts after masking IC that express red/ green/ blue to make one font (multi-color). In other words, when making a multi-color font using a font editor, the 3 fonts are handled as separated fonts before they are combined, but when the combination is done and used in programming or in an actual display, it is handled as one font. The '1' area of the multi-color font is influenced by the character color selection, and the '0' area is influenced by the raster color selection.

That is, if you call the address of R-color attribute font, the '1' area of R/ G/ B color attribute fonts in the left side combined and the font did 'OR' operation in the right side is displayed as shown in following figure.

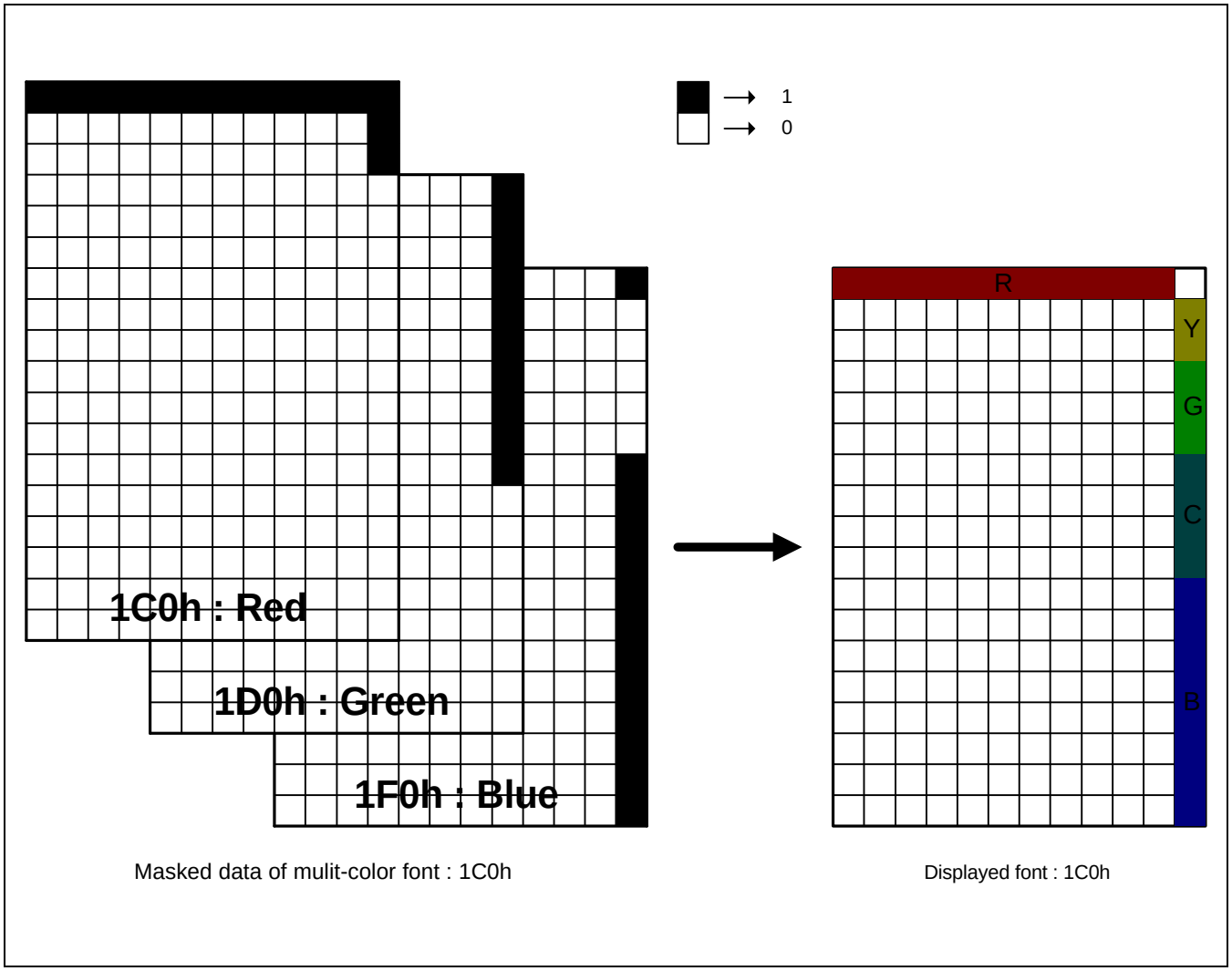


Figure 12 : Multi-Color Font's composition

Transparency

If BGEN bit of "Frame Control Register 0" is enabled, the part that raster color is a black within OSD becomes transparent, and video displayes at the part of OSD raster. Therefore, if you use this bit, you can make OSD window various OSD shapes with perfect freedom, which the shapes are not only rectangle but also rounded rectangle, circle, or etc. That is, when you design fonts, at first design OSD, and then make fonts to include character in designed OSD window as like the character part of fonts indicated 1 and 2 in "Figure 13 : Various OSD window by setting BGEN bit", and then set raster color of the fonts to black, and then enable BGEN bit, in the long run, you can express various OSD shapes. At this time, if you set shadow attribute, raster part of the fonts that enabled back ground enabled by BGEN bit is the area except character part and shadowed area as like "Figure 14 : The part influenced by BGEN bit".

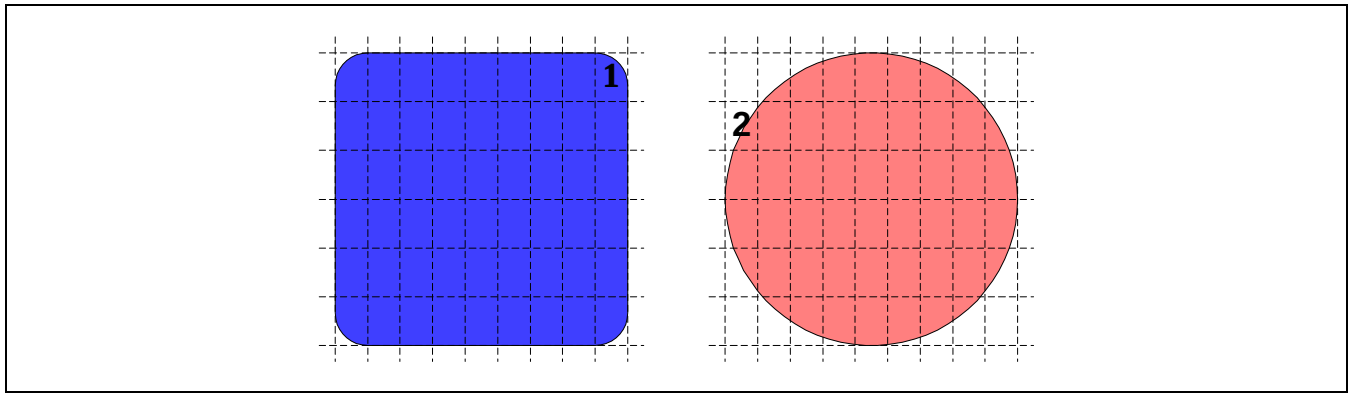


Figure 13 : Various OSD window by setting BGEN Bit

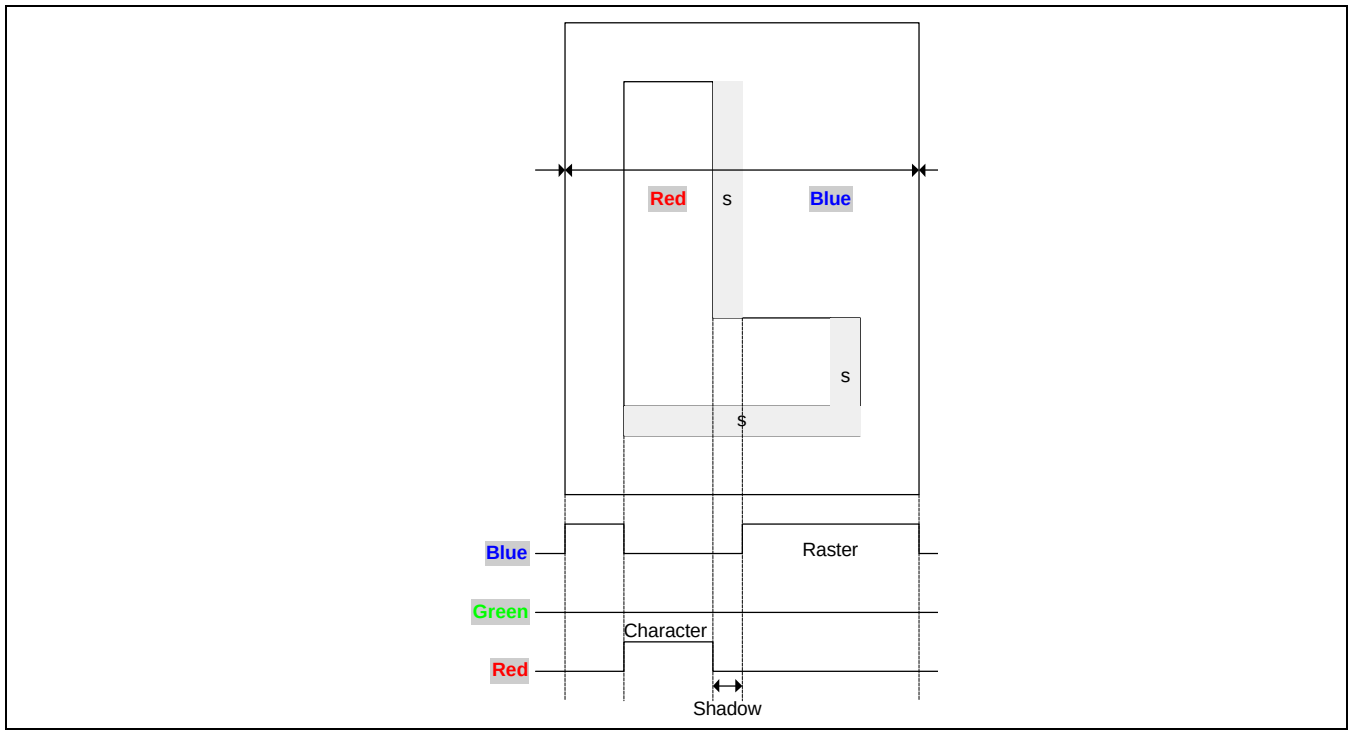


Figure 14: The part influenced by BGEN Bit

SIZING / POSITIONING

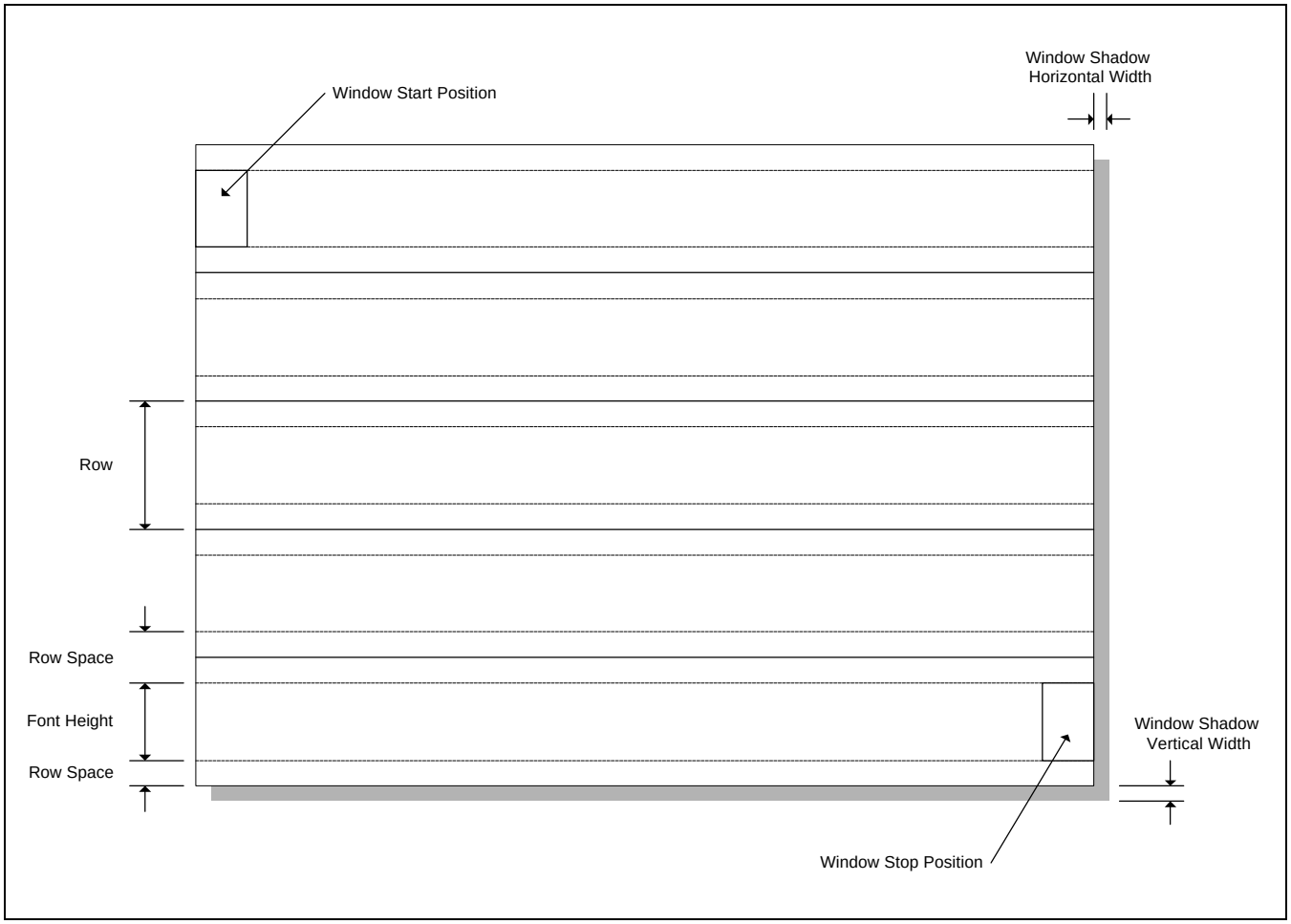


Figure 15 : OSD window area

Positioning

The "Frame Control Register 2"'s HP[F:8] bits signify delay of the horizontal display from the H-Sync reference edge to the character's 1st pixel location, and is controlled by multiplying HP[F:8]'s range value by 6. Also, VP[7:0] bits signify the top margin height from the V-Sync reference edge, and is controlled by multiplying 4 to the VP[7:0]'s range value. Therefore, it is "HP × 6 = 256 × 6 = 1536, VP × 4 = 256 × 4 = 1024" that correspond to the maximum resolution (1600 × 1200 mode) of the current monitor.

Whereas VP and HP explained above set the initial reference point of the OSD display area (15 rows × 30 columns), As like "Figure III-6 : OSD window area", RSTR, CSTR, REND and CEND bits in "Frame Control Register 5 — 12" decide each window area from the left-top point of OSD display area. But RSTR and REND are controlled by 4 bits, they have a range 0 — 14 actually because window area is within OSD display area. In the same reason, CSTR and CEND are controlled by 5 bits, but they have a range 0 — 29.

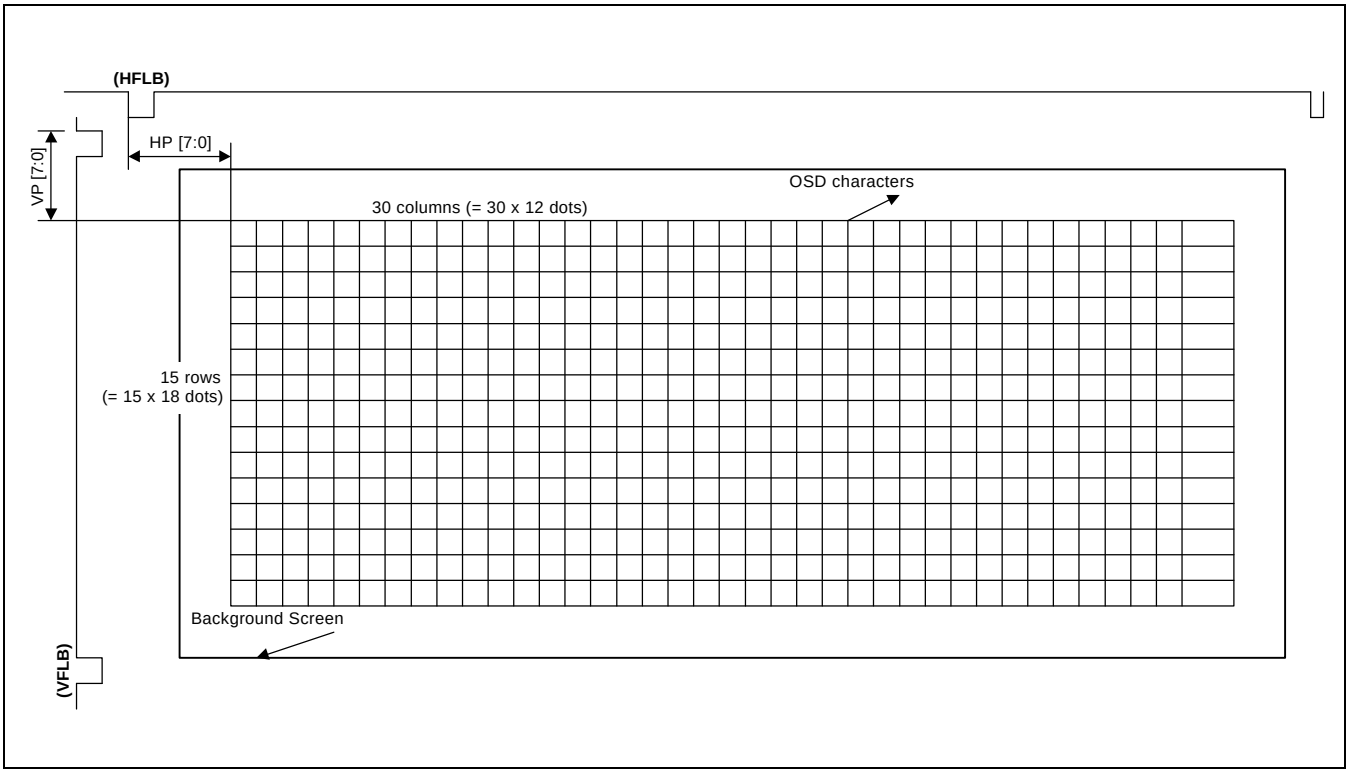


Figure 16: Frame Composition with the OSD Characters

Windows shadow width

HW and VW bits in "Frame Control Register 5, 7, 9, 11" mean each horizontal and vertical width of window shadow as shown in "Figure 15 : OSD window area". The actual value is calculated by (HW × 2 Dots) and (VW × 2 Lines). Shadow color is set by only black for the characteristics of shadowing. Also, it can display not only OSD area (15 rows × 30 columns) but also the extended area by window shadow. That is, to use window shadow function, you may not construct the window less than the maximum OSD area.

Window Generation

As shown in "Figure III-6 : OSD window area", window size is determined by setting CSTR, RSTR, CEND, and REND bits, which mean as a address with font unit in window area. The actual and physical start point of window is the left-top point of the font area indicated 'Window Start Position' in "Figure 15 : OSD window area". Also, the actual stop point of window is the right-bottom point of the font area indicated 'Window Stop Point'. If 'WEN' bit in each window is enabled by setting to high, the window generated as above is displayed with the window priority determined by 'WPR' bits in "Frame Control Register 13".

Character Height

The purpose of CH[5:0] (Character Height) is to output a uniformly sized OSD even if the resolution changes. To express a character height of CH = 18 — CH = 63 after receiving CH[5:0]'s input from the "Frame Control Register 1", decide on each line's repeating number(standard height CH = 18) and repeat the lines. The following figure shows two examples of a height-controlled character. Height control is control is carried out by repeating some of the lines.

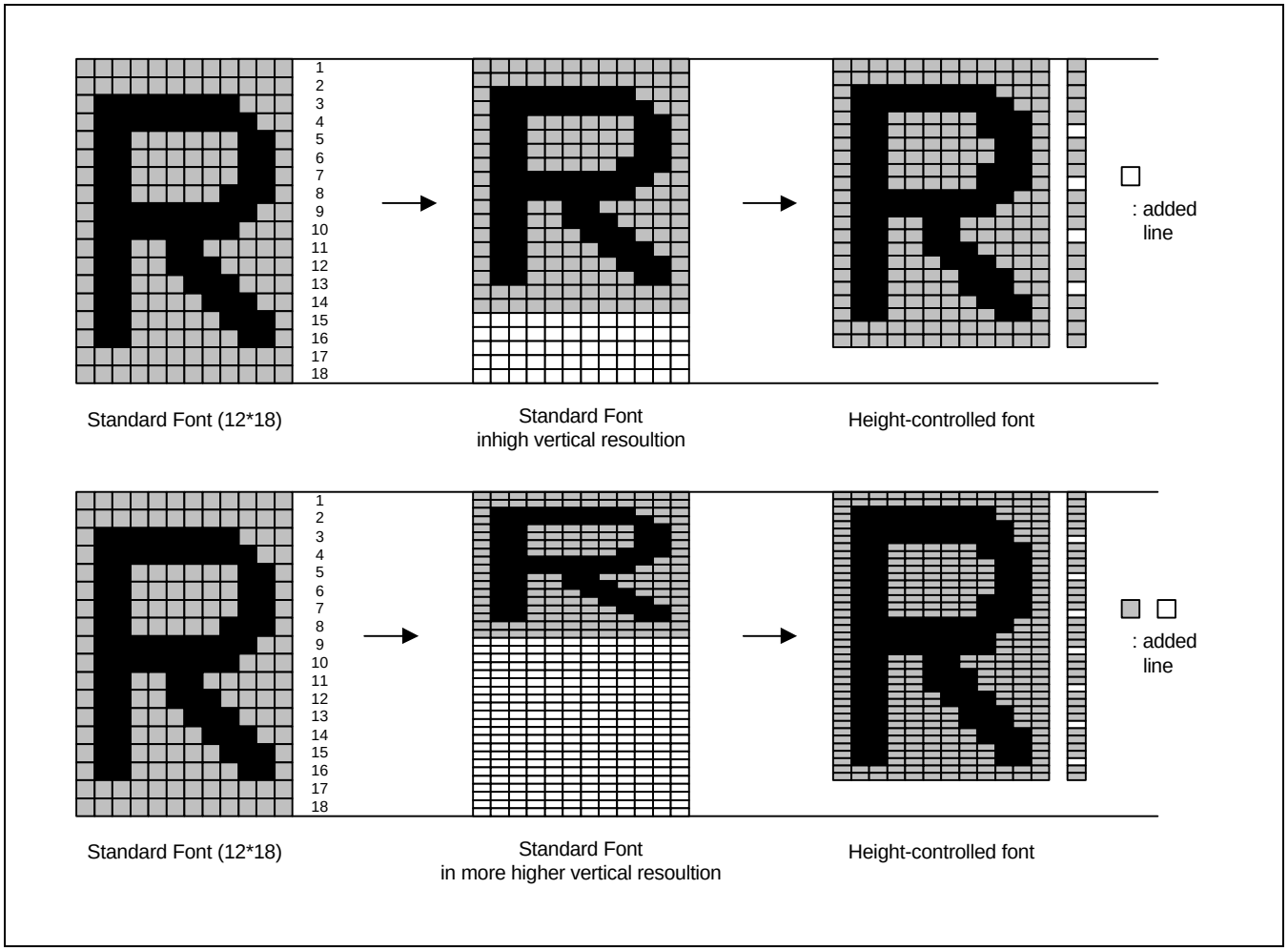


Figure 17: Character Height Control

Repeating line-number can be found by the following formula.

[# of the repeating lines = 2 + N x M] ,

where N = 1, 2, 3, ... and M = round { 14 / (CH[5:0] - 18) }.

(i) If CH[5:0] is greater than 32 and less than or equal to 46 (32 < CH[5:0] ≤ 46), all lines are repeated once or twice. The lines that are repeated twice are chosen by the following formula.

where N = 1, 2, 3, ... and M = round { 14 / (CH*[5:0] - 32) }*.

(ii) If CH[5:0] is greater than 46 and less than or equal to 60 (46 < CH[5:0] ≤ 60), all lines are

repeated tow or three times. The lines that are repeated three times are chosen by the following formula.

where N = 1, 2, 3, ... and M = round { 14 / (CH[5:0] - 46) }.

(iii) If CH[5:0] is greater than 60 and less than or equal to 64 (60 < CH[5:0] ≤ 64), all lines are repeated three or four times. The lines that are repeated four times are chosen by the following formula.

where N = 1, 2, 3, ... and M = round { 14 / (CH[5:0] - 60) }.

CH's reference value is 18, and even if you input 0, it operates in the same way as when CH=18. The repeating line-number is limited to 16. If the M value is less than or equal to 1, all lines of the standard font are repeated more than once.

Auto Height Control function is executed by enabling 'AutoH' bit in "Frame Control Register 0" and setting the number of OSD fonts that you need vertically at 'AREF' bits in "Frame Control Register 4".
At this time, the reason of that 'AREF' are 6 bits is as follows : At first, we suppose that the maximum of vertical resolution is 1200 lines on Monitor. In case that the minimum of font height is 18 lines, the number of OSD font is vertically 67 (=1200/ 18). Therefore, it is satisfied that 'Auto Height Control Reference Number' is 63 (=2^6).
That is, if you enable 'AutoH' bit and set 20 to 'AREF' bits, height lines in a font is determined to display 20 fonts vertically at maximum resolution as shown in the figure below, and the same size of OSD display regardless of changing resolution. If the font height calculated by AREF value is less than 18 lines, the font height displayes as many as 18 lines.

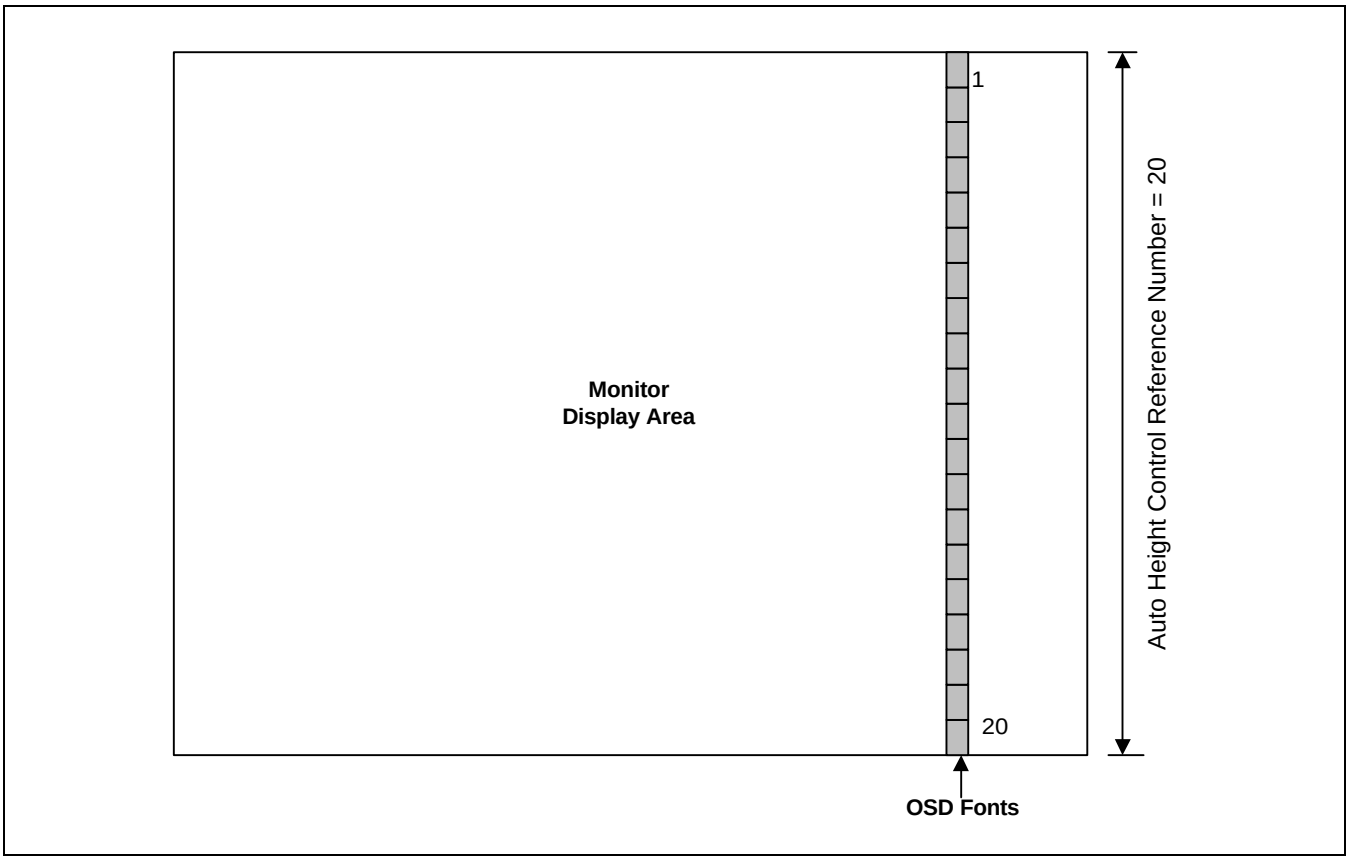


Figure 18 : Auto Height control

VISUAL EFFECT

Shadowing

Character 'R' Font appear the effect shown in figure below by character shadowing. the principle that 1 pixel to the right, below, and diagonal below the character makes black.

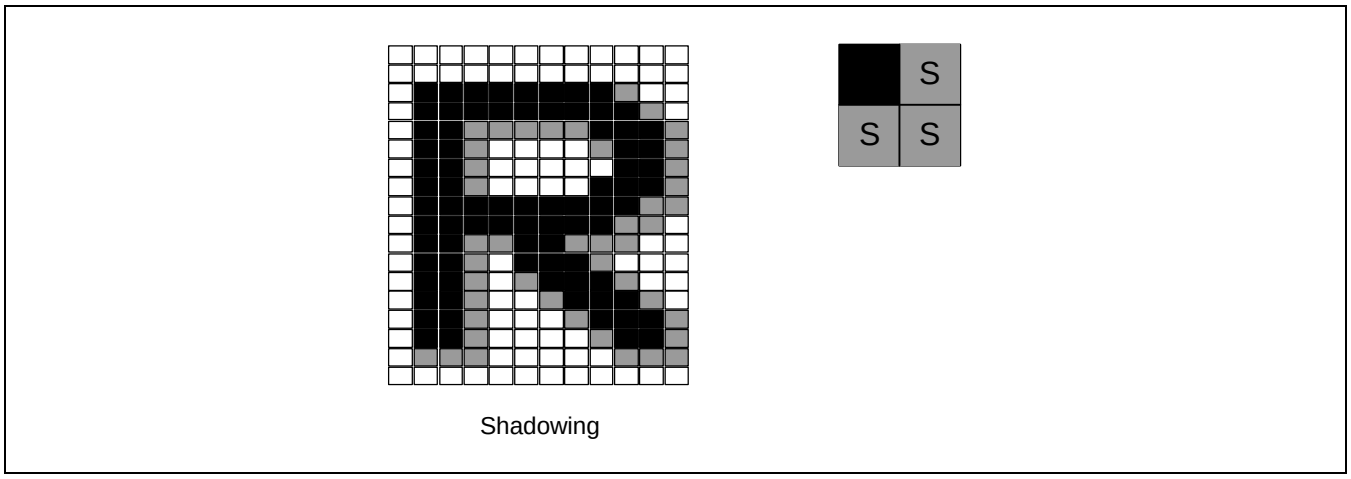


Figure 19 : Character Shadowing

As shown in "Figure 15 : OSD window area" , windows shadowing is started after delay as much as, "VW" and "HW".
Window shadow is also composed of block as like as character shadow.

Scrolling

Scrolling is slowly displaying or erasing a character from the top line to the bottom. This effect makes it look as if 1 character line is scrolling up or down. However, you must remember that scrolling is on/ off only when OSD is enabled/ disabled.

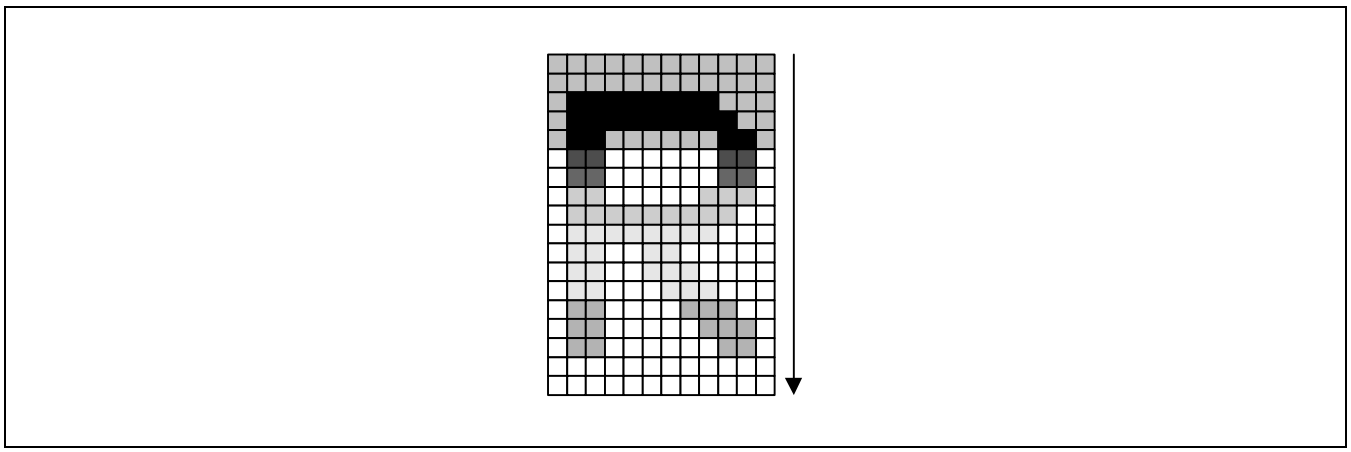


Figure 20 : Scrolling

PLL CONTROL

PLL (Phase Lock Loop) is feedback controlled circuit that maintains a constant phase difference between a reference signal and an oscillator output signal. The PLL of S5D2510 is charge-pump PLL , and is generally composed PFD, charge pump, VCO, and Divider.

To support VGA — UXGA grade, divider has the ratio of 640/ 800/ 1024/ 1280, and the range of the HFLB input frequency for reference is 30kHz — 120kHz. At this time, needed the output frequency of VCO is 19.2 MHz —153.6MHz.

H/ W and S/ W setting is needed for optimal operation of PLL. The application circuit of Pin #2 and Pin #3 is representative of H/ W setting. CP, FHF, and DOT bits in "Frame Control Register 1" is representative of S/ W setting.

You had better set the tuning factor explained above by referring to the following reference.

Locking Range

As you can see the figure below, it is 2.5V that measured voltage at Pin #2 to optimize OSD quality. Also, locking voltage range of PLL is 1.0V — 4.0V, and the proper voltage range of PLL to capture well is 1.7V — 3.3V.

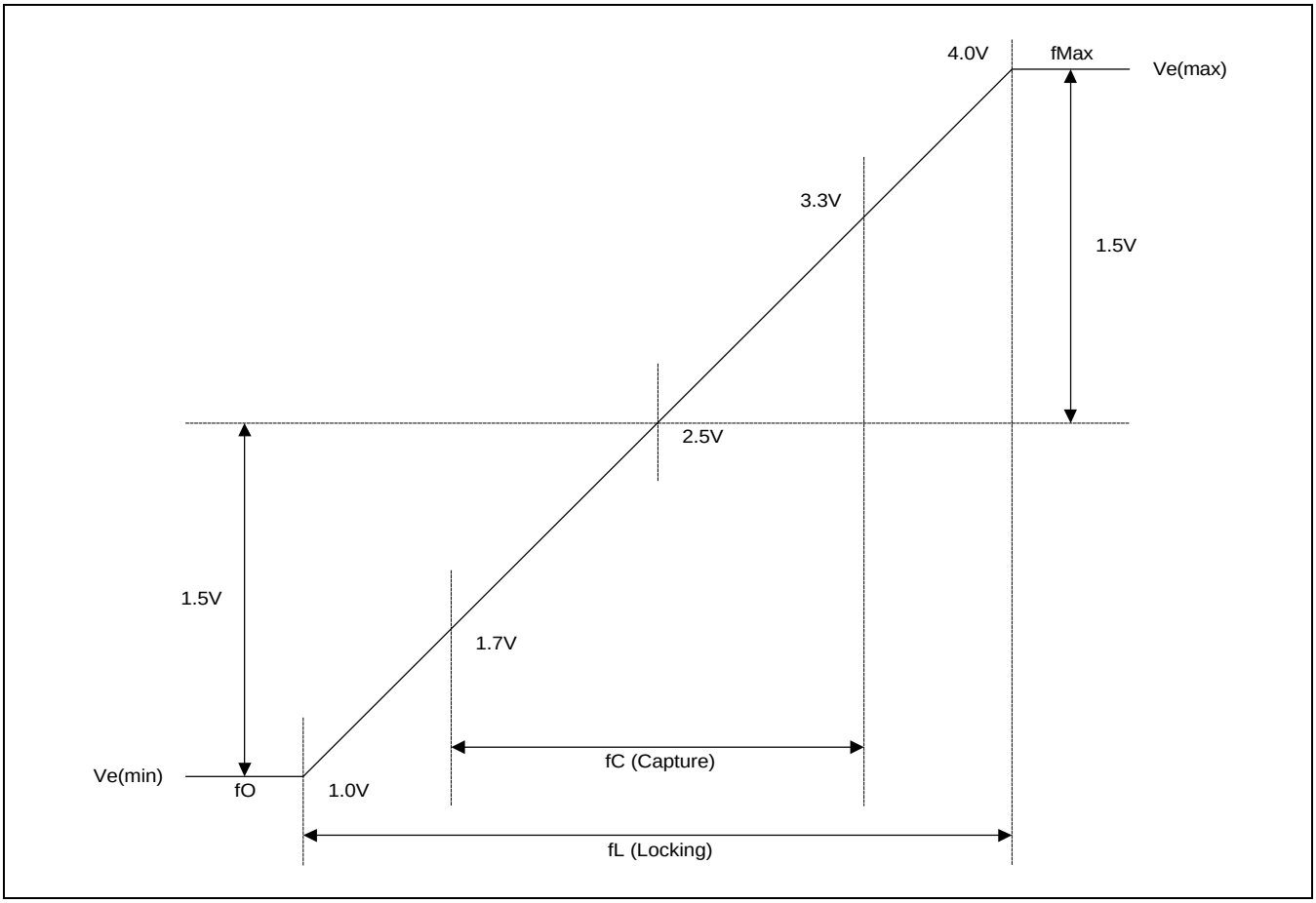


Figure 21 : PLL Locking Range

Separating region of frequency

To reduce influence of the noise that exist in VCO input voltage, because it is desirable that VCO gain is small, each region of frequency is separated in 2 — 5 EA. Each region is overlapped for thermal characteristics and parameter variation in a process of manufacture.

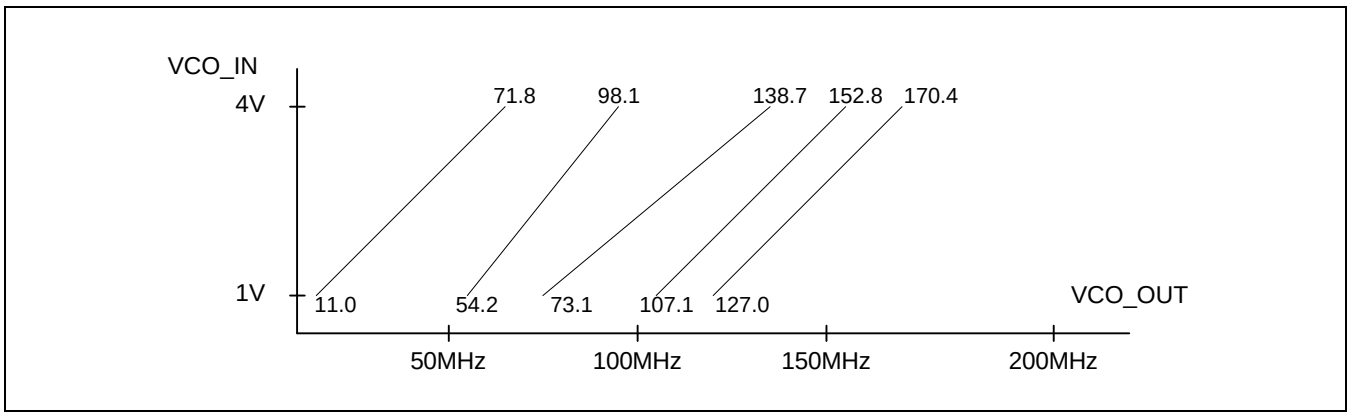


Figure 22 : PLL frequency range (Type 1)

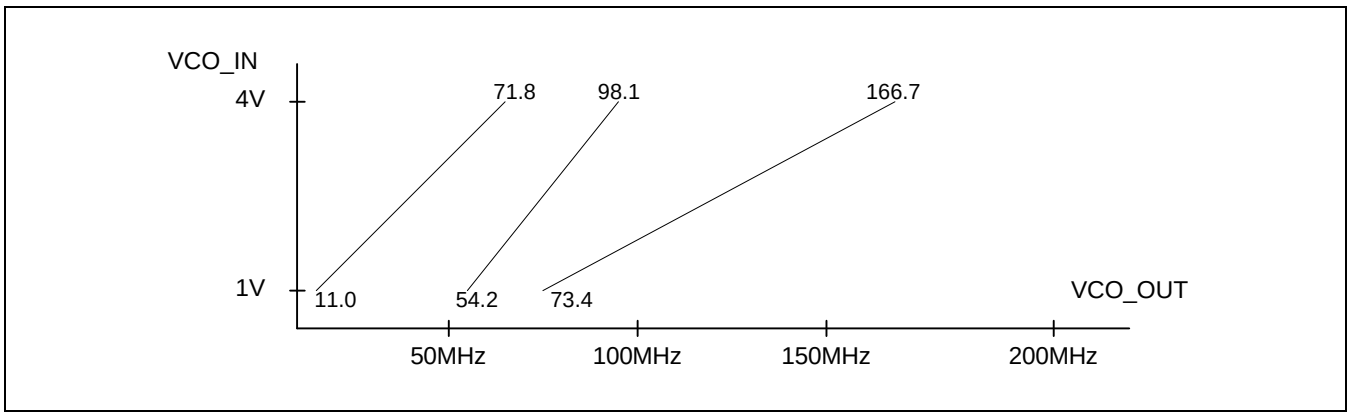


Figure 23 : PLL frequency range (Type 2)

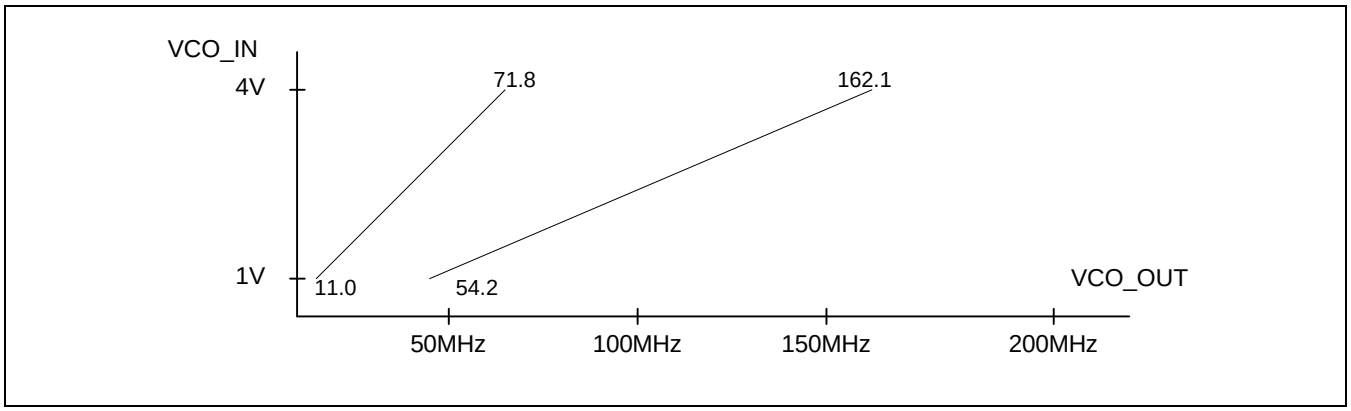


Figure 24: PLL frequency range (Type 3)

Separation of frequency region is in need of the multifarious consideration about PLL tuning factors as explained before.

HF bits in "Frame Control Register 1" are not selecting from out of 8 (2_3)steps uniformly, but selecting 3 types shown in table below as you can see "9.2 Separating region of frequency". In 'Type 1', HF2/HF1/HF0 bits are setting each 0/0/0, 0/0/1, 0/1/0, 0/1/1, 1/0/0 (1/0/1), in 'Type 2' 0/0/0, 1/1/1, and in 'Type 3' 0/0/0, 0/0/1, 1/1/0.

HF2	HF1	HF0	PLL Dot Frequency Range
0	0	0	19.2 MHz < Fdot < 70 MHz
0	0	1	70 MHz ≤ Fdot < 90 MHz
0	1	0	90 MHz ≤ Fdot < 128 MHz
0	1	1	128 MHz ≤ Fdot < 140 MHz
1	0	0	140 MHz ≤ Fdot < 160 MHz
1	0	1	
1	1	0	90 MHz ≤ Fdot < 160 MHz
1	1	1	70 MHz ≤ Fdot < 160 MHz

After fixing time constants of the external circuit and PLL control bits except HF bits, if HF bits are stepped up, the voltage measured at Pin #2 drops. On the contrary, if HF bits are stepped down, the voltage rises. The voltage measured at Pin #2 don't change by changing CP bits.

As changing the external register in Pin #3, the range is shiftted without changing slope in the figures shown before about 'PLL frequency region'. In other words, if the value of the external register in Pin #3 rises, the voltage measured at Pin #2 (VCO_IN) is shiftted upward without changing slope shown in figures before.

If the external register in Pin #4, the slope is changed without shifting shown in figures before. That is, if the value of the external register in Pin #4 rises, the slope shown in figures before rises.

After initial setting refferred to the table below in the side view of S/W and the figure "S5D2510 Application Circuit" in the side view of H/W.

Table 8: Recommand setting of PLL control bits

Range	CP2	CP1	CP0	HF2	HF1	HF0	DOT1	DOT0	Hexa	V (Pin #2)
30kHz — 40kHz	0	1	1	0	0	0	1	1	63h	2.18V — 2.68V
40kHz — 50kHz	1	0	1	0	0	0	1	1	A3h	2.68V — 3.16V
50kHz — 70kHz	1	1	1	0	0	1	1	1	E7h	1.34V — 2.64V
70kHz — 110kHz	1	1	1	0	1	0	1	1	EBh	1.42V — 3.10V
110kHz — 120kHz	1	1	1	0	1	1	1	1	EFh	1.92V — 2.44V

NOTES