DATASHEET

Low Power Clock for Intel Atom®-Based Systems

ICS9LPRS436C

Recommended Application:

NM10 Express Chipset + N450/D410/D510 Atom® CPUs

Output Features:

- 2 - 0.8V push-pull differential CPU pairs
- 2 - 0.8V push-pull differential PCIEX pairs
- 1 - 0.8V push-pull differential SATA75 pair
- 1 - 0.8V push-pull differential DOT96 pair
- 1 - 0.8V push-pull differential CPU/PCIEX selectable pair
- 1 - PCI (33MHz)
- 1 - PCICLK_F, (33MHz) free-running
- 1 - USB, 48MHz
- 1 - 12/48MHz
- 1 - 25MHz
- 1 - REF, 14.318MHz
- 1 - 12.288MHz

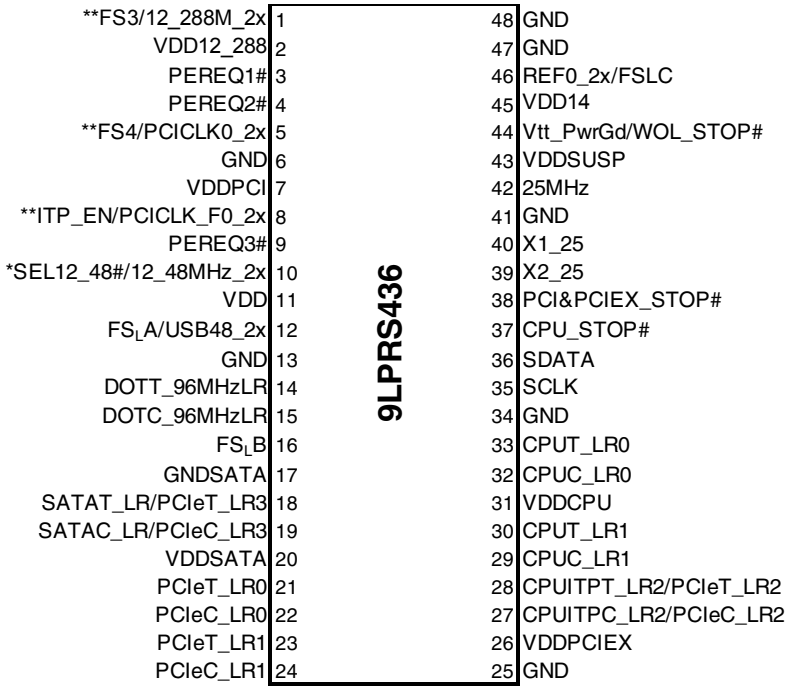
Key Specifications:

- CPU outputs cycle-cycle jitter < 85ps
- PCIEX outputs cycle-cycle jitter < 125ps
- SATA outputs cycle-cycle jitter < 125ps
- PCI outputs cycle-cycle jitter < 500ps
- +/- 100ppm frequency accuracy on all clocks

Features/Benefits:

- VDDSUSP allows 25MHz to run in S-states
- Supports programmable spread percentage
- Uses external 25MHz crystal, external crystal load caps are required for frequency tuning
- PEREQ# pins to support PCIEX/SATA power management.
- Low power differential clock outputs (No 50Ω resistor to GND needed)
- Integrated 33Ω series resistor on all differential outputs.

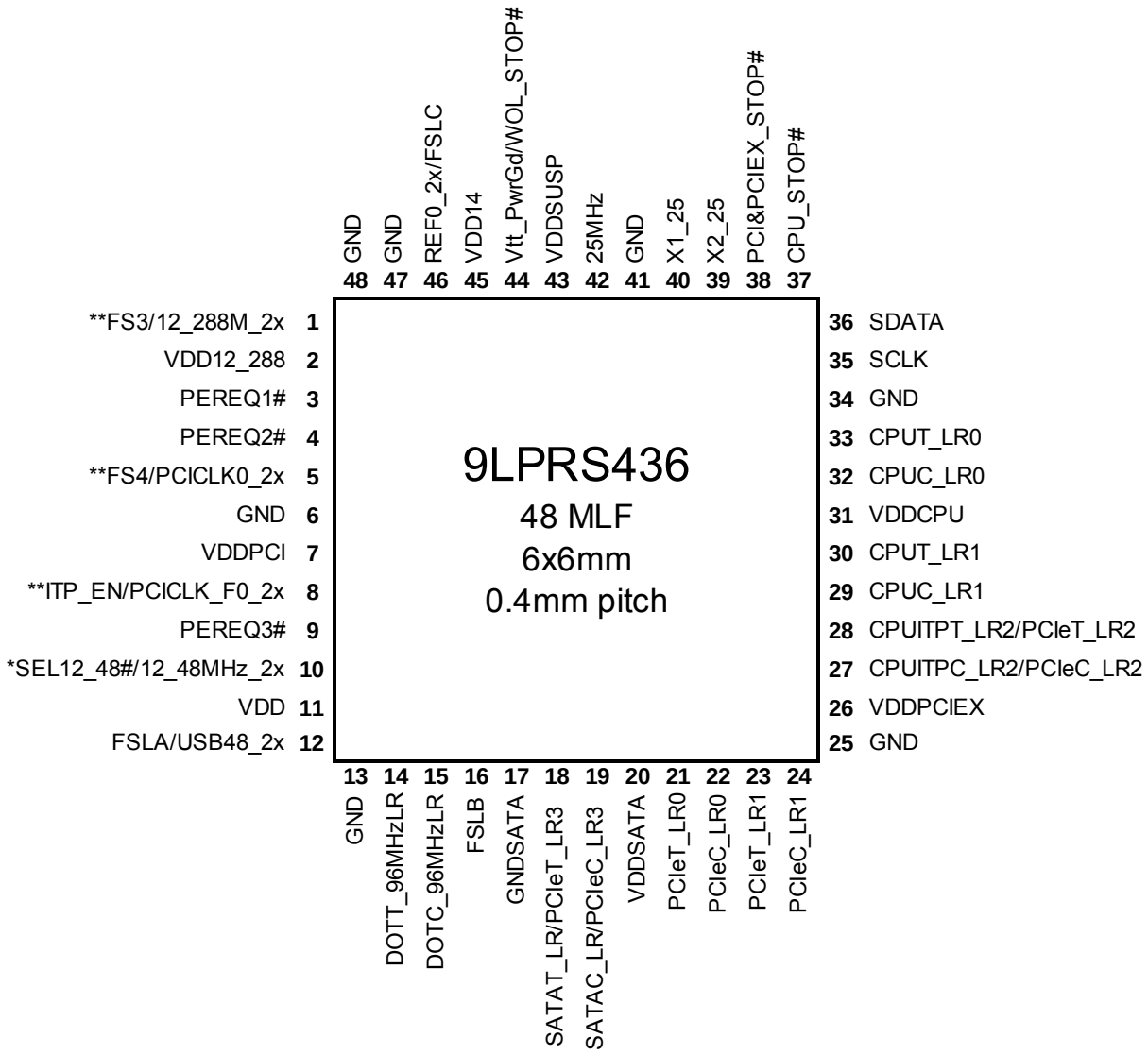
Pin Configuration



48-TSSOP

* Internal Pull-Up Resistor

** Internal Pull-Down Resistor



* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

Pin Description

PIN #	PIN NAME	TYPE	DESCRIPTION
1	**FS3/12_288M_2x	I/O	Frequency select latch input pin / 12.288MHz output, 3.3V
2	VDD12_288	PWR	Power for 12.288MHz PLL and output buffer, nominal 3.3V.
3	PEREQ1#	IN	Real-time input pin that controls SATACLK and PCIEXCLK outputs that are selected through the SMBus. 1 = selected outputs are disabled, 0 = selected outputs are enabled.
4	PEREQ2#	IN	Real-time input pin that controls SATACLK and PCIEXCLK outputs that are selected through the SMBus. 1 = selected outputs are disabled, 0 = selected outputs are enabled.
5	**FS4/PCICLK0_2x	I/O	Frequency select latch input pin / 3.3V PCI clock output.
6	GND	PWR	Ground pin.
7	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
8	**ITP_EN/PCICLK_F0_2x	I/O	ITP Enable Latched Input/Free Running PCI clock output. ITP_Enable Selects the functionality of the CPU_ITP/SRC output as follows: 1 = CPU_ITP output 0 = SRC output
9	PEREQ3#	IN	Real-time input pin that controls PCIEXCLK outputs that are selected through the SMBus. 1 = selected outputs are disabled, 0 = selected outputs are enabled.
10	*SEL12_48#/12_48MHz_2x	I/O	Latched select input for 12/48MHz output. 1=12MHz, 0=48MHz. 12/48MHz clock output.
11	VDD	PWR	Power supply, nominal 3.3V
12	FSLA/USB48_2x	I/O	3.3V tolerant input for CPU frequency selection. Low voltage threshold inputs, see input electrical characteristics for Vil_FS and Vih_FS values. / 48.00MHz USB clock
13	GND	PWR	Ground pin.
14	DOTT_96MHzLR	OUT	True clock of low power differential pair for 96.00MHz DOT clock. No 50ohm to GND needed. No Rs needed.
15	DOTC_96MHzLR	OUT	Complementary clock of low power differential pair for 96.00MHz DOT clock. No 50ohm resistor to GND needed. No Rs needed.
16	FSLB	IN	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values.
17	GNDSATA	PWR	Ground pin for the SATA outputs
18	SATAT_LR/PCIeT_LR3	OUT	True clock of differential SATA pair. / True clock of differential PCI-Express pair - selectable by FS(4:3) ; both are 0.8V differential push pull outputs with integrated 33ohm series resistor.
19	SATAC_LR/PCIeC_LR3	OUT	Complementary clock of differential SATA pair. / Complementary clock of differential PCI-Express pair - selectable by FS(4:3); both are 0.8V differential push pull outputs with integrated 33ohm series resistor.
20	VDDSATA	PWR	Supply for SATA clocks, 3.3V nominal
21	PCIeT_LR0	OUT	True clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor
22	PCIeC_LR0	OUT	Complementary clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor
23	PCIeT_LR1	OUT	True clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor
24	PCIeC_LR1	OUT	Complementary clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor

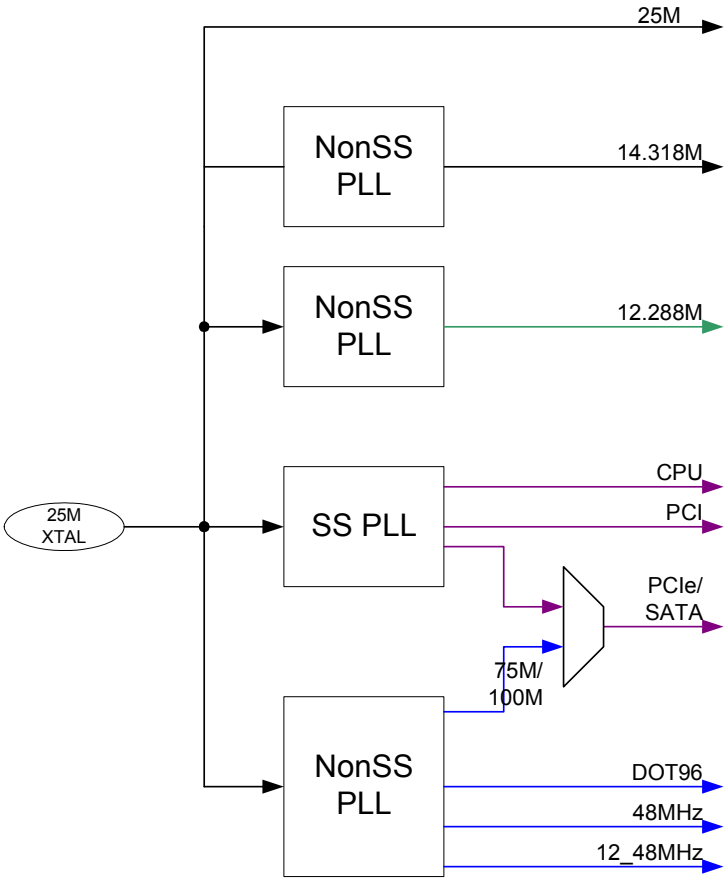
Pin Description (Continued)

25	GND	PWR	Ground pin.
26	VDDPCIEX	PWR	Power supply for PCI Express clocks, nominal 3.3V
27	CPUITPC_LR2/PCIeC_LR2	OUT	Complementary clock of differential pair CPU output. / Complementary clock of differential PCIEX pair. These are 0.8V push pull outputs. No external 50ohm resistor to GND or 33ohm series resistor needed.
28	CPUITPT_LR2/PCIeT_LR2	OUT	True clock of differential pair CPU output. / True clock of differential PCIEX pair. These are 0.8V push pull outputs. No external 50ohm resistor to GND or 33ohm series resistor needed.
29	CPUC_LR1	OUT	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor.
30	CPUT_LR1	OUT	True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor.
31	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
32	CPUC_LR0	OUT	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor.
33	CPUT_LR0	OUT	True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor.
34	GND	PWR	Ground pin.
35	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
36	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.
37	CPU_STOP#	IN	Stops CPU0 clock when enabled.
38	PCI&PCIEX_STOP#	IN	Stops all PCICLKs at logic 0 level, when low. Free running PCICLKs are not effected by this input.
39	X2_25	OUT	Crystal output, Nominally 25.00MHz.
40	X1_25	IN	Crystal input, Nominally 25.00MHz.
41	GND	PWR	Ground pin.
42	25MHz	OUT	25MHz clock output, 3.3V
43	VDDSUSP	PWR	Supply for suspend mode, powers 25MHz PLL, 25M output and XTAL oscillator. 3.3V Nominal
44	Vtt_PwrGd/WOL_STOP#	IN	This active high 3.3V LVTTL input is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled / Asynchronous active low input pin that stops all outputs except free running 25Mhz
45	VDD14	PWR	Power for 14.31818MHz PLL and REF output, nominal 3.3V.
46	REF0_2x/FSLC	I/O	2x strength 14.318 MHz reference clock./ 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values.
47	GND	PWR	Ground pin.
48	GND	PWR	Ground pin.

General Description

The **ICS9LPRS436C** is a low power CK505-compatible clock targeted at Intel-based Netbooks and Nettops. This clock synthesizer provides a single chip solution for systems using the Intel NM10 chipset paired with the Intel N450/D410/D510 Atom® CPUs. The **ICS9LPRS436C** is driven with a 25MHz crystal.

Block Diagram



Series Resistors for Single Ended Outputs

D.C.Drive Strength	Number of Loads to Drive	Match Point for N & P Voltage / Current (mA)	Number of Loads Actually Driven.		
			1 Load Rs=	2 Loads Rs=	3 Loads Rs=
	1	0.56 / 33 (17Ω)	33Ω [39Ω]	-	-
	2	0.92 / 66 (14Ω)	39Ω [43Ω]	22Ω [27Ω]	-

Notes:

1. Preferred drive strengths using CK505 clock sources. Transmission lines to load do not share series resistors.
2. Desktop/Mobile Platforms with Zo = 50/55 ohms use the first resistor value.
3. Systems with Zo = 60 ohms use the resistor values in brackets [ ].

Table 1: CPU/SRC/PCI PLL Spread Frequency Selection Table for 9LPRS436C

	FS4 (B0b4)	FS3 (B0b3)	FS_LC (B0b2)	FS_LB (B0b1)	FS_LA (B0b0)	CPU MHz	SRC	PCI	SATA
0	0	0	0	0	0	100.00	100.00	33.33	Follows SRC
1	0	0	0	0	1	100.00	100.00	33.33	Follows SRC
2	0	0	0	1	0	83.33	100.00	33.33	Follows SRC
3	0	0	0	1	1	83.33	100.00	33.33	Follows SRC
4	0	0	1	0	0	133.33	100.00	33.33	Follows SRC
5	0	0	1	0	1	133.33	100.00	33.33	Follows SRC
6	0	0	1	1	0	166.67	100.00	33.33	Follows SRC
7	0	0	1	1	1	166.67	100.00	33.33	Follows SRC
8	0	1	0	0	0	100.00	100.00	33.33	100MHz Non-Spread
9	0	1	0	0	1	100.00	100.00	33.33	100MHz Non-Spread
10	0	1	0	1	0	83.33	100.00	33.33	100MHz Non-Spread
11	0	1	0	1	1	83.33	100.00	33.33	100MHz Non-Spread
12	0	1	1	0	0	133.33	100.00	33.33	100MHz Non-Spread
13	0	1	1	0	1	133.33	100.00	33.33	100MHz Non-Spread
14	0	1	1	1	0	166.67	100.00	33.33	100MHz Non-Spread
15	0	1	1	1	1	166.67	100.00	33.33	100MHz Non-Spread
16	1	0	0	0	0	100.00	100.00	33.33	75MHz Non-Spread
17	1	0	0	0	1	100.00	100.00	33.33	75MHz Non-Spread
18	1	0	0	1	0	83.33	100.00	33.33	75MHz Non-Spread
19	1	0	0	1	1	83.33	100.00	33.33	75MHz Non-Spread
20	1	0	1	0	0	133.33	100.00	33.33	75MHz Non-Spread
21	1	0	1	0	1	133.33	100.00	33.33	75MHz Non-Spread
22	1	0	1	1	0	166.67	100.00	33.33	75MHz Non-Spread
23	1	0	1	1	1	166.67	100.00	33.33	75MHz Non-Spread
24	1	1	0	0	0	100.00	100.00	33.33	75MHz Non-Spread
25	1	1	0	0	1	100.00	100.00	33.33	75MHz Non-Spread
26	1	1	0	1	0	83.33	100.00	33.33	75MHz Non-Spread
27	1	1	0	1	1	83.33	100.00	33.33	75MHz Non-Spread
28	1	1	1	0	0	133.33	100.00	33.33	75MHz Non-Spread
29	1	1	1	0	1	133.33	100.00	33.33	75MHz Non-Spread
30	1	1	1	1	0	166.67	100.00	33.33	75MHz Non-Spread
31	1	1	1	1	1	166.67	100.00	33.33	75MHz Non-Spread

Table 2: Slew Rate Selection Table

Bit 1	Bit 0	Slew Rate
0	0	Hi-Z
0	1	0.6X (1.2V/ns)
1	0	0.8X (1.6V/ns)
1	1	1X (2.0V/ns)

CPU Power Management Table

WOL_STOP#	SMBus Register OE	CPU_STOP#	PCI&PCIEX_ STOP#	CPU(1:0)/ITP	CPU#(1:0)/ITP
1	Enable	**1**	X	Running	Running
1	Enable	**0**	X	High	Low
0	Enable	X	X	Low	Low
X	**Disable**	X	X	Low	Low

Differential Power Management Table

WOL_STOP#	SMBus Register OE	CPU_STOP#	PCI&PCIEX_ STOP#	PCIEX/SATA	PCIEX/SATA#	PCIEX/SATA	PCIEX/SATA#	DOT	DOT#
				PCI Stoppable		Free-Run			
1	Enable	X	**1**	Running	Running	Running	Running	Running	Running
1	Enable	X	**0**	High	Low	Running	Running	Running	Running
0	Enable	X	X	Low	Low	Low /20K	Low	Low /20K	Low
X	**Disable**	X	X	Low	Low	Low /20K	Low	Low /20K	Low

Singled-ended Power Management Table

WOL_STOP#	SMBus Register OE	CPU_STOP#	PCI&PCIEX_ STOP#	PCIF/PCI	PCIF/PCI	REF	12/48MHz 12.288MHz	25MHz	25MHz
				Free-run	Stoppable			Free-run	Stoppable
1	Enable	X	**1**	Running	Running	Running	Running	Running	Running
1	Enable	X	**0**	Running	Low	Running	Running	Running	Running
0	Enable	X	X	Low	Low	Low	Low	Running	Low
X	**Disable**	X	X	Low	Low	Low	Low	Low	Low

PEREQ# Control Table:

PEREQ#	PCIe controlled
1	0, SATA/PCIe3
2	SATA/PCIe3, 1
3	1, 2

Electrical Characteristics - Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
3.3V Core Supply Voltage	VDDA				4.6	V	1,2
3.3V Logic Supply Voltage	VDD				4.6	V	1,2
Input Low Voltage	V_{IL}		GND-0.5			V	1
Input High Voltage	V_{IH}	Except for SMBus interface			V_{DD}+0.5V	V	1
Input High Voltage	V_{IHSMB}	SMBus clock and data pins			5.5V	V	1
Storage Temperature	Ts		-65		150	°C	1
Case Temperature	Tcase				115	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics - Input/Supply/Common Output DC Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Ambient Operating Temp	T_{ambC}	Standard Device	0		85	°C	
	T_{ambI}	Industrial Temperature Range Device	-40		85	°C	
Supply Voltage	VDDxxx	Supply Voltage	3.135		3.465	V	
Input High Voltage	V_{IHSE}	Single-ended 3.3V inputs	2		V_{DD} + 0.3	V	7
Input Low Voltage	V_{ILSE}	Single-ended 3.3V inputs	V_{SS} - 0.3		0.8	V	7
FS(4:3) Input High Voltage	V_{IH_FS4}	Single-ended 3.3V FS(4:3) Inputs	2		VDD + 0.3	V	
FS(4:3) Input Low Voltage	V_{IL_FS4}	Single-ended 3.3V FS(4:3) Inputs	V_{SS} - 0.3		0.8	V	
Low Threshold Input-High Voltage	V_{IH_FS}	3.3 V +/-5%	0.7		VDD+0.3	V	
Low Threshold Input-Low Voltage	V_{IL_FS}	3.3 V +/-5%	V_{SS} - 0.3		0.35	V	
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5		5	uA	6
Input Leakage Current	I_{INRES}	Inputs with pull up or pull down resistors $V_{IN} = V_{DD}$, V_{IN} = GND	-200		200	uA	
Output High Voltage	V_{OHSE}	Single-ended outputs, I_{OH} = -1mA	2.4			V	5
Output Low Voltage	V_{OLSE}	Single-ended outputs, I_{OL} = 1 mA			0.4	V	5
Operating Supply Current	$I_{DDVDD3.3}$	Full Active, C_L = Full load; IDD 3.3V			100	mA	
	$I_{DDVDDSUSP3.3}$	Full Active, C_L = Full load; IDD 3.3V			13	mA	
Powerdown Current	$I_{DDPDVDD3.3}$	3.3V Main Rail			0	mA	
	$I_{DDPDSUSP3.3w}$	VDD_SUSP Rail. 25MHz Running (WOL)			13	mA	
	$I_{DDPDSUSP3.3}$	VDD_SUSP Rail. 25MHz Off			2	mA	
Input Frequency	F_i	V_{DD} = 3.3 V			27	MHz	8
Pin Inductance	L_{pin}				7	nH	
Input Capacitance	C_{IN}	Logic Inputs	1.5		5	pF	
	C_{OUT}	Output pin capacitance			6	pF	
	C_{INX}	X1 & X2 pins			6	pF	
SMBus Voltage	V_{DD}		2.7		5.5	V	
Low-level Output Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	
Current sinking at V_{OLSMB} = 0.4 V	I_{PULLUP}	SMB Data Pin	4			mA	
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	
Maximum SMBus Operating Frequency	F_{SMBUS}				100	kHz	
Spread Spectrum Modulation Frequency	f_{SSMOD}	Triangular Modulation	30		33	kHz	

NOTES on DC Parameters: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

[1] Operation at these points is not recommended

[2] Maximum VIH is not to exceed VDD

[3] Human Body Model

[4] Operation under these conditions is neither implied, nor guaranteed.

[5]Signal is required to be monotonic in this region.

[6] Input leakage current does not include inputs with pull-up or pull-down resistors

[7] 3.3V referenced inputs are: PCI&PCIEX_STOP#, CPU_STOP#, ITP_EN, SCLK, SDATA, VTT_PWR_GD/PD#, SEL12_48# and PEREQ# inputs if selected.

[8] For margining purposes only. Normal operation should have Fin = 25MHz +/-50ppm

AC Electrical Characteristics - Input/Common Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Clk Stabilization	T_{STAB}	From VDD Power-Up or de-assertion of PD to 1st clock			1.8	ms	
Tdrive_PEREQ_off	$T_{DRPEROFF}$	Output stop after PEREQ# deasserted			3	clocks	
Tdrive_PEREQ_on	$T_{DRPERON}$	Output run after PEREQ# asserted			3	clocks	
Tdrive_CPU	T_{DRSRC}	CPU output enable after CPU_STOP# de-assertion			10	ns	
Tdrive_PCIEX	$T_{DRPCIEX}$	PCIEX output enable after PCI&PCIEX_STOP# de-assertion			15	ns	1
Tfall_SE	T_{FALL}	Fall/rise time of all 3.3V control inputs from 20-80%			10	ns	
Trise_SE	T_{RISE}				10	ns	
Tdrive_PD#	T_{DRPD}	Differential output enable after PD# de-assertion			300	us	1

AC Electrical Characteristics - CPU, PCIEX, SATA, DOT96MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Rising Edge Slew Rate	tSLR	Differential Measurement	2.5		4	V/ns	1,2
Falling Edge Slew Rate	tFLR	Differential Measurement	2.5		4	V/ns	1,2
Slew Rate Variation	tSLVAR	Single-ended Measurement			20	%	1
Maximum Output Voltage	VHIGH	Includes overshoot			1150	mV	1
Minimum Output Voltage	VLOW	Includes undershoot	-300			mV	1
Differential Voltage Swing	VSWING	Differential Measurement	300			mV	1
Crossing Point Voltage	VXABS	Single-ended Measurement	300		550	mV	1,3,4
Crossing Point Variation	VXABSVAR	Single-ended Measurement			140	mV	1,3,5
Duty Cycle	DCYC	Differential Measurement	45		55	%	1
CPU Jitter - Cycle to Cycle	CPUJC2C	Differential Measurement			85	ps	1
SRC Jitter - Cycle to Cycle	SRCJC2C	Differential Measurement			125	ps	1
SATA Jitter - Cycle to Cycle	SATAJC2C	Differential Measurement			125	ps	1
DOT Jitter - Cycle to Cycle	DOTJC2C	Differential Measurement			250	ps	1
CPU[1:0] Skew	CPUSKEW10	Differential Measurement			100	ps	1,6
CPU[2_ITP:0] Skew	CPUSKEW20	Differential Measurement			150	ps	1,6
SRC Skew	SRCSKEW	Differential Measurement			250	ps	1

Electrical Characteristics - PCICLK/PCICLK_F

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	12		55	Ω	1
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	2
Clock period	T_{period}	33.33MHz output no spread	29.99700		30.00300	ns	2
		33.33MHz output spread	30.08421		30.23459	ns	2
Absolute min/max period	T_{abs}	33.33MHz output no spread	29.49700		30.50300	ns	2
		33.33MHz output nominal/spread	29.56617		30.58421	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH}@MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1		4	V/ns	1
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1		4	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Pin to Pin Skew	t_{skew}	V_T = 1.5 V			250	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L=5pF, Rs=22Ω (unless specified otherwise)

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3] Slew rate emastured through V_swing voltage range centered about differential zero

[4] Vcross is defined at the voltage where Clock = Clock#.

[5] Only applies to the differential rising edge (Clock rising, Clock# falling.)

[6] CPU group skew is nominally 0ps.

Electrical Characteristics - USB48MHz, 12/48MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2
Clock period	T_{period}	48.00MHz output nominal	20.83125		20.83542	ns	2,3
Absolute min/max period	T_{abs}	48.00MHz output nominal	20.48125		21.18542	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Rising Edge Slew Rate (USB48M)	t_{SLR}	Measured from 0.8 to 2.0 V	1		2	V/ns	1
Falling Edge Slew Rate (USB48M)	t_{FLR}	Measured from 2.0 to 0.8 V	1		2	V/ns	1
Rising Edge Slew Rate (12/48M)	t_{SLR}	Measured from 0.8 to 2.0 V	1		4	V/ns	1
Falling Edge Slew Rate (12/48M)	t_{FLR}	Measured from 2.0 to 0.8 V	1		4	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			350	ps	1

Electrical Characteristics - 25MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2
Clock period	T_{period}	25.00MHz output nominal	39.99600		40.00400	ns	2,3
Absolute min/max period	T_{abs}	25.00MHz output nominal	39.32360		40.67640	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1		2	V/ns	1
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1		2	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps	1

Electrical Characteristics - 12.288MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2
Clock period	T_{period}	12.288MHz output nominal	81.37207		81.38835	ns	2,3
Absolute min/max period	T_{abs}	12.288MHz output nominal	80.87207		81.88835	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1		2	V/ns	1
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1		2	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps	1

Electrical Characteristics - REF-14.318MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2
Clock period	Tperiod	14.318MHz output nominal	69.82033		69.86224	ns	2,3
Absolute min/max period	Tabs	14.318MHz output nominal	69.83400		70.84800	ns	2
Output High Voltage	VOH	IOH = -1 mA	2.4			V	1
Output Low Voltage	VOL	IOL = 1 mA			0.4	V	1
Rising Edge Slew Rate	tSLR	Measured from 0.8 to 2.0 V	1		4	V/ns	1
Falling Edge Slew Rate	tFLR	Measured from 2.0 to 0.8 V	1		4	V/ns	1
Duty Cycle	dt1	VT = 1.5 V	45		55	%	1
Jitter, Cycle to cycle	tjcyc-cyc	VT = 1.5 V			1000	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L=5pF, Rs=22Ω (unless specified otherwise)

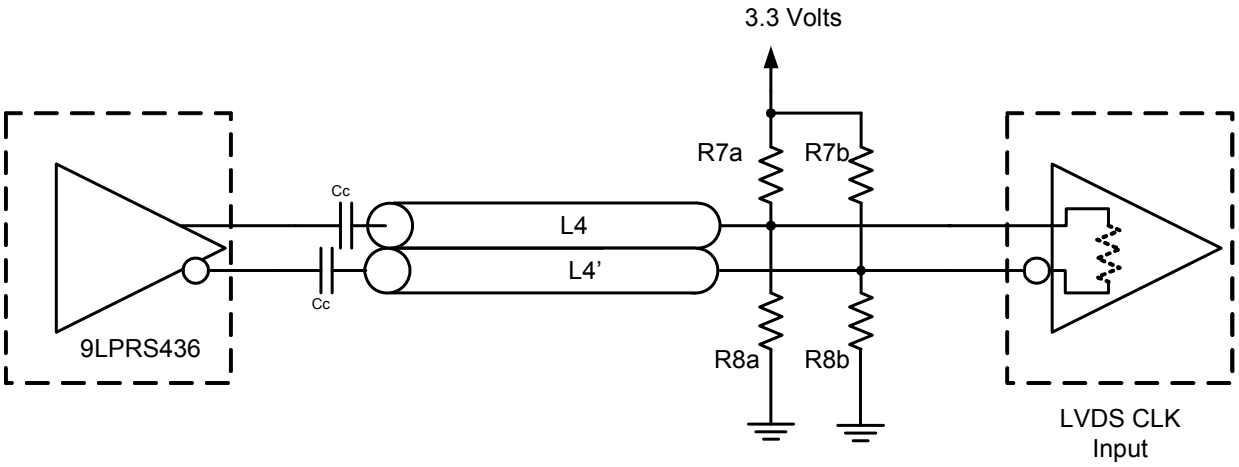
[1] Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3] The average period over any 1us period of time

Driving LVDS inputs with the 9LPRS436

Component	Value		Note
	Receiver has termination	Receiver does not have termination	
R7a, R7b	10K ohm	140 ohm	
R8a, R8b	5.6K ohm	75 ohm	
Cc	0.1 uF	0.1 uF	
Vcm	1.2 volts	1.2 volts	



General SMBus serial interface information for the ICS9LPRS436C

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the beginning byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address $D2_{(H)}$		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
Data Byte Count = X		
		ACK
Beginning Byte N	X Byte	
		ACK
O		
O		O
O		O
		O
Byte N + X - 1		
		ACK
P	stoP bit	

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address $D3_{(H)}$			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
			Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Table: Frequency Select Register

Byte 0	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Spread Enable	Enables Spread for CPU/SRC/PCI outputs	RW	Off	0.5% down spread	0
Bit 4	FS4	Freq Select Bit 4	RW	See Table 1: CPU/SRC/PCI PLL Frequency Selection Table		Latch
Bit 3	FS3	Freq Select Bit 3	RW			Latch
Bit 2	FSLC	Freq Select Bit 2	RW			Latch
Bit 1	FSLB	Freq Select Bit 1	RW			Latch
Bit 0	FSLA	Freq Select Bit 0	RW			Latch

SMBus Table: Output Control Register

Byte 1	Name	Control Function	Type	0	1	PWD
Bit 7	DOT96Mhz	Output Enable	RW	Disable	Enable	1
Bit 6	SATA/PCIe3	Output Enable	RW	Disable	Enable	1
Bit 5	ITP/PCIe2	Output Enable	RW	Disable	Enable	1
Bit 4	PCIe1	Output Enable	RW	Disable	Enable	1
Bit 3	PCIe0	Output Enable	RW	Disable	Enable	1
Bit 2	12.288MHz	Output Enable (Disabling This output also disables the 12.288M PLL).	RW	Disable	Enable	1
Bit 1	25MHz	25MHz free running during VDD Suspend (S-states). If this bit is set to 0, the XTAL OSC will also be powered down in the Suspend States)	RW	Does Not Run	Runs	1
Bit 0	CPU PLL MN_EN	CPU PLL M/N Enable	RW	Disable	Enable	0

SMBus Table: Output Control Register

Byte 2	Name	Control Function	Type	0	1	PWD
Bit 7	USB_48MHz	Output Enable	RW	Disable	Enable	1
Bit 6	Reserved					0
Bit 5	REF0	Output Enable	RW	Disable	Enable	1
Bit 4	25MHz	Output Enable	RW	Disable	Enable	1
Bit 3	12_48MHz	Output Enable	RW	Disable	Enable	1
Bit 2	PCICLK_F0	Output Enable	RW	Disable	Enable	1
Bit 1	PCICLK0	Output Enable	RW	Disable	Enable	1
Bit 0	Reserved					0

SMBus Table: Output Control Register

Byte 3	Name	Control Function	Type	0	1	PWD
Bit 7	CPUCLK1	Output Enable	RW	Disable	Enable	1
Bit 6	CPUCLK0	Output Enable	RW	Disable	Enable	1
Bit 5	PEREQ3# Control	PCIEX1 is controlled	RW	Not Controlled	Controlled	0
Bit 4	PEREQ3# Control	PCIEX2 is controlled	RW	Not Controlled	Controlled	0
Bit 3	PEREQ2# Control	PCIEX1 is controlled	RW	Not Controlled	Controlled	0
Bit 2	PEREQ2# Control	SATACLK is controlled	RW	Not Controlled	Controlled	0
Bit 1	PEREQ1# Control	PCIEX0 is controlled	RW	Not Controlled	Controlled	0
Bit 0	PEREQ1# Control	SATACLK is controlled	RW	Not Controlled	Controlled	0

NOTE: Only 1 PEREQ at a time can be selected to control an output.

SMBus Table: Output Control and Readback Register

Byte 4	Name	Control Function		0	1	PWD
Bit 7	Reserved					0
Bit 6	CPU_1	Free-Running Control	RW	Free-Running	Stoppable	0
Bit 5	SEL_12_48	SEL12_48MHz readback	R	48MHz	12MHz	latch
Bit 4	CPUCLK_2/ITP	Free-Running Control	RW	Free-Running	Stoppable	0
Bit 3	ITP_EN	ITP_EN readback	R	PCIEX6	CPU_ITP	latch
Bit 2	Reserved					0
Bit 1	CPUCLK_0	Free-Running Control	RW	Free-Running	Stoppable	0
Bit 0	Reserved					0

SMBus Table: Output Control Register

Byte 5	Name	Control Function		0	1	PWD
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	SATA/PCIe3	Free- Running Control	RW	Free-Running	Stoppable	1
Bit 3	PCIe2	Free- Running Control	RW	Free-Running	Stoppable	0
Bit 2	PCIe1	Free- Running Control	RW	Free-Running	Stoppable	0
Bit 1	PCIe0	Free- Running Control	RW	Free-Running	Stoppable	0
Bit 0	Load Control	IIC Load control	RW	Load	Do not Load	0

SMBus Table: Amplitude Control Register

Byte 6	Name	Control Function	Type	0	1	PWD
Bit 7	Diff AMP	PCIe(2:0) Differential output	RW	00 = 700mV	10 = 900mV	0
Bit 6	Diff AMP	Amplitude Control	RW	01 = 800mV	11 = 1000mV	1
Bit 5	Diff AMP	DOT96 Differential output	RW	00 = 700mV	10 = 900mV	0
Bit 4	Diff AMP	Amplitude Control	RW	01 = 800mV	11 = 1000mV	1
Bit 3	Diff AMP	SATA/PCIe3 Differential output	RW	00 = 700mV	10 = 900mV	0
Bit 2	Diff AMP	Amplitude Control	RW	01 = 800mV	11 = 1000mV	1
Bit 1	Diff AMP	CPU Differential output	RW	00 = 700mV	10 = 900mV	0
Bit 0	Diff AMP	Amplitude Control	RW	01 = 800mV	11 = 1000mV	1

SMBus Table: Revision and Vendor ID Register

Byte 7	Name	Control Function	Type	0	1	PWD
Bit 7	RID3	Revision ID	R	0010 = C Rev		x
Bit 6	RID2		R			x
Bit 5	RID1		R			x
Bit 4	RID0		R			x
Bit 3	VID3	VENDOR ID	R	0001 = ICS		0
Bit 2	VID2		R			0
Bit 1	VID1		R			0
Bit 0	VID0		R			1

SMBus Table: Byte Count Register

Byte 8	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	BC4	Byte Count Programming	RW	Writing to this register will configure how many bytes will be read back, default is 0F = 15 bytes.		0
Bit 3	BC3		RW			1
Bit 2	BC2		RW			1
Bit 1	BC1		RW			1
Bit 0	BC0		RW			1

SMBus Table: Watch Dog Timer Control Register

Byte 9	Name	Control Function	Type	0	1	PWD
Bit 7	HWD_EN	Watchdog Hard Alarm Enable	RW	Disable	Enable	0
Bit 6	WD Hard Status	WD Hard Alarm Status	R	Normal	Alarm	X
Bit 5	WDTCtrl	Watch Dog Alarm Time base Control	R	290ms Base		0
Bit 4	HWD3	WD Hard Alarm Timer Bit 3	RW	These bits represent X*290ms or X*1.16s. The watchdog timer waits before it goes to alarm mode. Default is 15 X 290ms = 4.35s.		1
Bit 3	HWD2	WD Hard Alarm Timer Bit 2	RW			1
Bit 2	HWD1	WD Hard Alarm Timer Bit 1	RW			1
Bit 1	HWD0	WD Hard Alarm Timer Bit 0	RW			1
Bit 0	Reserved	Reserved	RW	-	-	0

SMBus Table: Skew programming Register

Byte 10	Name	Control Function	Type	0	1	PWD
Bit 7	CPUSkw3	CPUCLK0 Skew Control (ps)	RW	See CPU Skew Programming Table		0
Bit 6	CPUSkw2		RW			0
Bit 5	CPUSkw1		RW			0
Bit 4	CPUSkw0		RW			0
Bit 3	CPUSkw3	CPUCLK1 Skew Control (ps)	RW	See CPU Skew Programming Table		0
Bit 2	CPUSkw2		RW			0
Bit 1	CPUSkw1		RW			0
Bit 0	CPUSkw0		RW			0

CPU Skew Programming Table

Byte 10 bits [7:4] or bits [3:0]	Skew Value (ps)
0000	0
0001	100
0010	200
0011	300
0100	400
0101	500
0110	600
0111	700
1000	800
1001	900
1010	1000
1011	1100
1100	1200
1101	1300
1110	1400
1111	1500

SMBus Table: CPU/SRC/PCI PLL Frequency Control Register

Byte 11	Name	Control Function	Type	0	1	PWD
Bit 7	N Div2	N Divider Prog bit 2	RW	The decimal representation of M and N Divider in Byte 11 and 12 will configure the CPU PLL VCO frequency. Default at power up = latch-in or Byte 0 ROM table. VCO Frequency = 50 x Ndiv(10:0)/Mdiv(5:0)		X
Bit 6	N Div1	N Divider Prog bit 1	RW			X
Bit 5	M Div5	M Divider Programming bit (5:0)	RW			X
Bit 4	M Div4		RW			X
Bit 3	M Div3		RW			X
Bit 2	M Div2		RW			X
Bit 1	M Div1		RW			X
Bit 0	M Div0		RW			X

SMBus Table: CPU/SRC/PCI PLL Frequency Control Register

Byte 12	Name	Control Function	Type	0	1	PWD
Bit 7	N Div10	N Divider Programming Byte12 bit(7:0) and Byte11 bit(7:6)	RW	The decimal representation of M and N Divider in Byte 11 and 12 will configure the CPU PLL VCO frequency. Default at power up = latch-in or Byte 0 ROM table. VCO Frequency = 50 x Ndiv(10:0)/Mdiv(5:0)		X
Bit 6	N Div9		RW			X
Bit 5	N Div8		RW			X
Bit 4	N Div7		RW			X
Bit 3	N Div6		RW			X
Bit 2	N Div5		RW			X
Bit 1	N Div4		RW			X
Bit 0	N Div3		RW			X

SMBus Table: CPU/SRC/PCI PLL Frequency Control Register

Byte 13	Name	Control Function	Type	0	1	PWD
Bit 7	SSP7	Spread Spectrum Programming bit(7:0)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread percentage of CPU PLL		X
Bit 6	SSP6		RW			X
Bit 5	SSP5		RW			X
Bit 4	SSP4		RW			X
Bit 3	SSP3		RW			X
Bit 2	SSP2		RW			X
Bit 1	SSP1		RW			X
Bit 0	SSP0		RW			X

SMBus Table: CPU/SRC/PCI PLL Frequency Control Register

Byte 14	Name	Control Function	Type	0	1	PWD
Bit 7	SSP15	Spread Spectrum Programming bit(15:8)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread percentage of CPU PLL		0
Bit 6	SSP14		RW			X
Bit 5	SSP13		RW			X
Bit 4	SSP12		RW			X
Bit 3	SSP11		RW			X
Bit 2	SSP10		RW			X
Bit 1	SSP9		RW			X
Bit 0	SSP8		RW			X

Bytes [15:22] Are reserved

SMBus Table: SE Slew Rate Control Register

Byte 23	Name	Control Function	Type	0	1	PWD
Bit 7	48M Slew	Slew Rate Control	RW	00 = Hi-Z	01 = 0.6x (1.2V/ns)	1
Bit 6			RW	10 = 0.8x (1.6V/ns)	11 = 1x (2.0V/ns)	0
Bit 5	REF Slew	Slew Rate Control	RW	00 = Hi-Z	01 = 0.6x (1.2V/ns)	1
Bit 4			RW	10 = 0.8x (1.6V/ns)	11 = 1x (2.0V/ns)	0
Bit 3	12_48M Slew	Slew Rate Control	RW	00 = Hi-Z	01 = 0.6x (1.2V/ns)	1
Bit 2			RW	10 = 0.8x (1.6V/ns)	11 = 1x (2.0V/ns)	0
Bit 1	25M Slew	Slew Rate Control	RW	00 = Hi-Z	01 = 0.6x (1.2V/ns)	1
Bit 0			RW	10 = 0.8x (1.6V/ns)	11 = 1x (2.0V/ns)	0

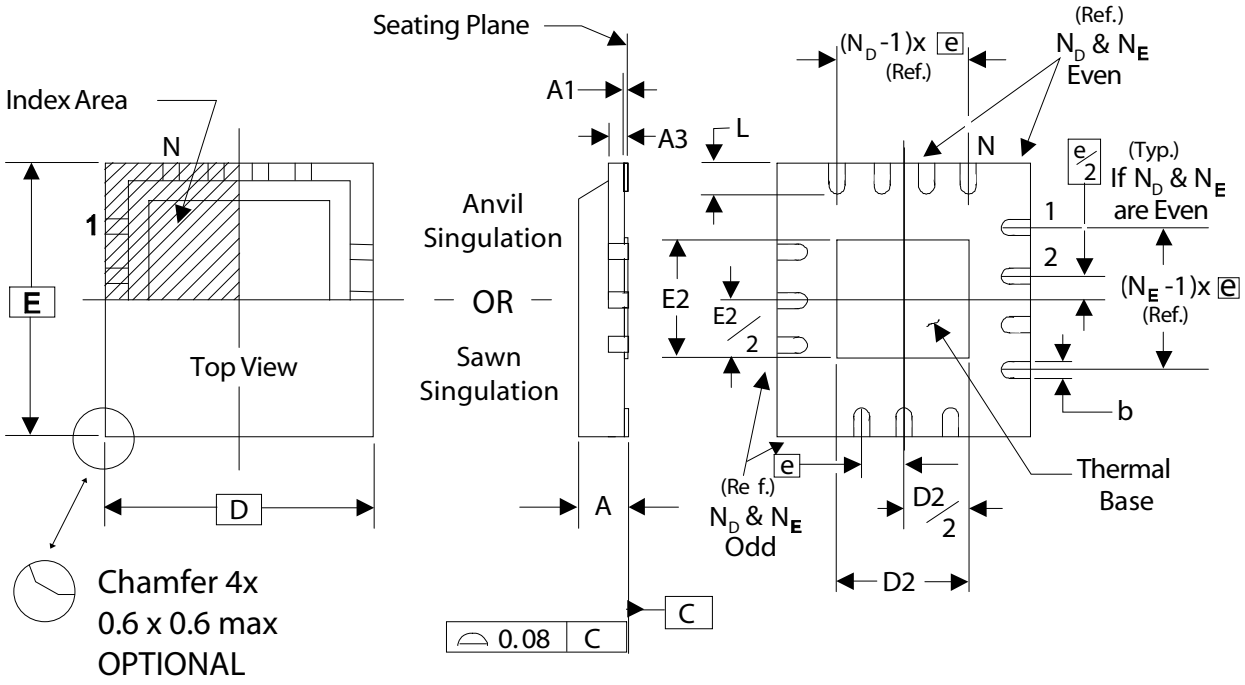
Byte [24] is reserved

SMBus Table: SE OutputControl Register

Byte 25	Name	Control Function	Type	0	1	PWD
Bit 7	12.288M Slew	Slew Rate Control	RW	00 = really Hi-Z	01 = 0.6x (1.2V/ns)	1
Bit 6			RW	10 = 0.8x (1.6V/ns)	11 = 1x (2.0V/ns)	0
Bit 5	PCICLK_F0	Free- Running Control	RW	Free-Running	Stoppable	0
Bit 4	PCICLK0	Free- Running Control	RW	Free-Running	Stoppable	1
Bit 3	PCICLK0 Slew	Slew Rate Control	RW	00 = really Hi-Z	01 = 0.6x (1.2V/ns)	1
Bit 2			RW	10 = 0.8x (1.6V/ns)	11 = 1x (2.0V/ns)	0
Bit 1	PCICLK_F0 Slew	Slew Rate Control	RW	00 = really Hi-Z	01 = 0.6x (1.2V/ns)	1
Bit 0			RW	10 = 0.8x (1.6V/ns)	11 = 1x (2.0V/ns)	0

Byte [26:30] are reserved

48-pin MLF Package Drawing and Dimensions



THERMALLY ENHANCED, VERY THIN, FINE PITCH
QUAD FLAT / NO LEAD PLASTIC PACKAGE

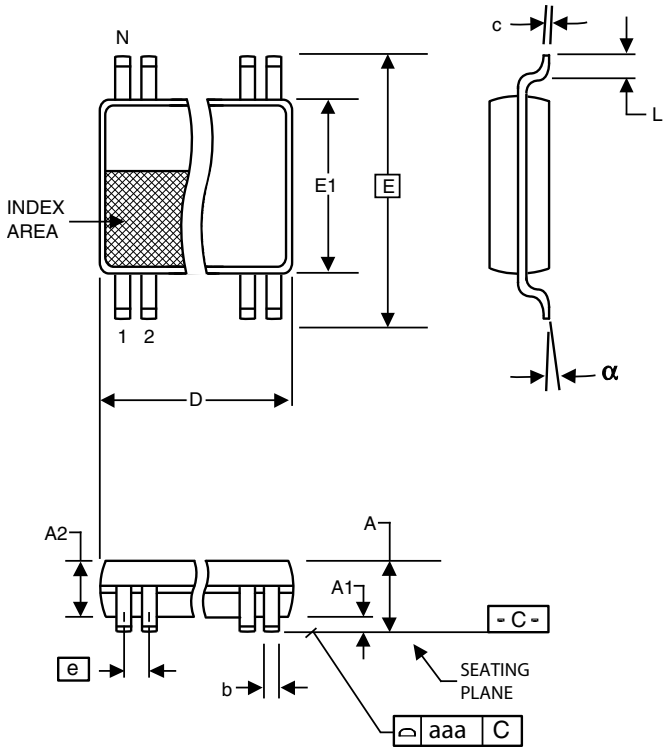
DIMENSIONS

SYMBOL	MIN.	MAX.
A	0.8	1.0
A1	0	0.05
A3	0.20 Reference	
b	0.18	0.3
e	0.40 BASIC	

DIMENSIONS

SYMBOL	48L TOLERANCE
N	48
N_D	12
N_E	12
D x E BASIC	6.00 x 6.00
D2 MIN. / MAX.	3.95 / 4.25
E2 MIN. / MAX.	3.95 / 4.25
L MIN. / MAX.	0.30 / 0.50

48-pin TSSOP Package Drawing and Dimensions



6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

Part / Order Number	Shipping Package	Package	Temperature
9LPRS436CKLF	Tubes	48-pin MLF	0 to +85° C
9LPRS436CKLFT	Tape and Reel	48-pin MLF	0 to +85° C
9LPRS436CKILF	Tubes	48-pin MLF	-40 to +85° C
9LPRS436CKILFT	Tape and Reel	48-pin MLF	-40 to +85° C
9LPRS436CGLF	Tubes	48-pin TSSOP	0 to +85° C
9LPRS436CGLFT	Tape and Reel	48-pin TSSOP	0 to +85° C
9LPRS436CGILF	Tubes	48-pin TSSOP	-40 to +85° C
9LPRS436CGILFT	Tape and Reel	48-pin TSSOP	-40 to +85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.
"C" is the revision designator (will not correlate to the datasheet revision)

Revision History

Rev.	Issue Date	Requestor	Description	Page #
0.1	12/14/2009	RDW	Initial Release of C rev with updated Frequency Select Table and Updated Idd specs for Suspend State. 48 MLF pinout also added.	-
0.2	12/18/2009	RDW	Corrected IDDPDVDD3.3 parameter to be 0 mA	
0.3	1/18/2010	RDW	Updated block diagram	5
0.4	6/1/2010	RDW	Corrected SMBus as follows: 1. Byte0, bits (4:0) are Read/Write not Read only 2. Byte 6 is as follows: b(7:6) control PCIe(2:0), b(5:4) control DOT96, b(3:2) control PCIe3/SATA, b(1:0) control CPU. 3. Added '0010 = C rev' to Byte 7 description for C rev. 4. Updated Absolute Max ratings to indicate max SMBus Vhigh is 5.5V. 5. Removed IOH and IOL specifications from Single Ended output Electrical Characteristics tables. These values are indirectly determined by the Output Termination Table. 6. Typical column added to Electrical Characteristics Tables. 7. General Description updated. 8. References to I2C clarified to refer to SMBus 9. Minor formatting updated to SMBus Bytes 23, and 25.	5, 8-11, 13,14
A	6/1/2010	RDW	Released to Final	

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