20W Stereo Digital Class-D Audio Power Amplifier with EQ and DRC

Features

- **Operating Voltage: 8.0V~24V for PVDD**
  – 3.0V~3.6V for DVDD and AVDD
- **High Efficiency Class-D Operation Eliminate the Need of Heatsinks**
- **Digital Serial Audio Input (Stereo Output)**
- **I²C Control Interface**
- **Sampling Rate can Support from 32kHz to 192kHz**
- **Separated Volume Control from 24dB to Mute**
- **Soft Mute (50% Duty Cycle)**
- **Shutdown and Mute Function**
- **Thermal and Over-Current Protections with Auto-Recovery**
- **Space Saving Package TQFP7x7-48P**
- **Lead Free and Green Devices Available (RoHS Compliant)**

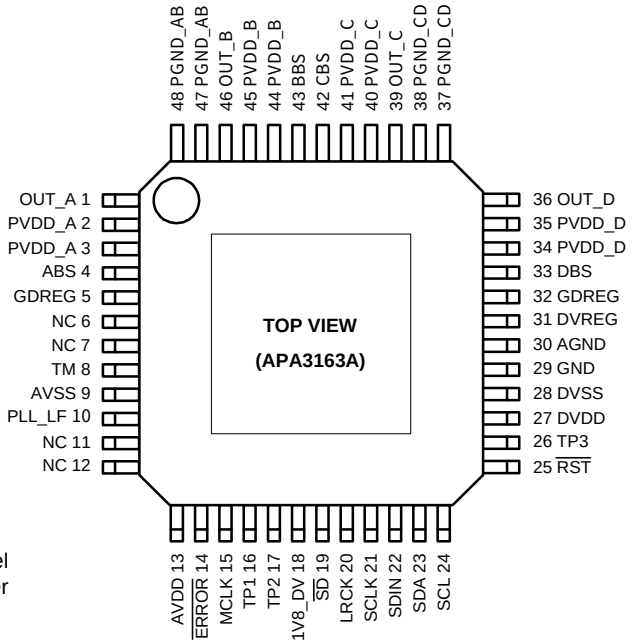
General Description

The APA3163A is a digital input, stereo, high efficiency, Class-D audio amplifier available in a TQFP7x7-48P package.

The APA3163A accepts the digital serial audio data and using the digital audio processor to convert the audio data becomes the stereo Class-D output speaker amplifier. This provides the seamless integration between the codec and the speaker amplifier.

The APA3163A is a slave device receiving clocks from external source, and the Class-D's PWM switching frequency is 352.8kHz for the sampling rate 44.1kHz or 384 kHz for sampling 48kHz, depend on the input signal's sampling rate.

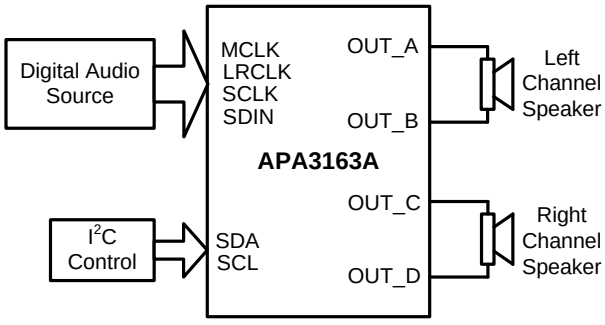
Pin Configuration



Applications

- **LCD TV**

Simplified Application Circuit



ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

APA3163A □□□□-□□ □ Assembly Material Handling Code Temperature Range Package Code	Package Code QCA : TQFP7x7-48P Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APA3163A QCA : 	XXXXX - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
	Supply Voltage (PVDD_X to PGND_XX)	-0.3 to 26	V
	Supply Voltage (DVDD to DVSS)	-0.3 to 3.6	
	Supply Voltage (AVDD to AVSS)	-0.3 to 3.6	
	Input Voltage (MCLK to AVSS)	-0.5 to AVDD+2.5	
	Input Voltage ($\overline{SD}$, $\overline{RST}$, LRCLK, SCLK, SDIN, SDA, SCL to DVSS)	-0.5 to DVDD+2.5	
	Input Voltage (OUT_X to PGND_XX)	-0.3 to +26	
	Input Voltage (XBS to PGND_XX)	-0.3 to +31	
	Input Voltage (AVSS, DVSS, AGND to PGND_XX)	-0.3 to +0.3	
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_{SDR}	Soldering Temperature Range, 10 seconds	260	°C
P_D	Power Dissipation	Internally Limited	W

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air (Note 2) TQFP7x7-48P	25	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of TQFP7X7-48P is soldered directly on the PCB.

Note 3: The case temperature is measured at the center of the exposed pad on the underside of the TQFP7X7-48P package.

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Recommended Operating Conditions

Symbol	Parameter		Range		Unit
			Min.	Max.	
V_{DD}	Supply Voltage		3	3.6	V
PV_{DD}	Full Bridge Stage Supply Voltage (PVDD_X)		8	24	
V_{IH}	High Level Threshold Voltage	$\overline{SD}$, MCLK, LRCLK, SCLK, SDIN, SDA, SCL, $\overline{RST}$	2	5	
V_{IL}	Low Level Threshold Voltage	$\overline{SD}$, MCLK, LRCLK, SCLK, SDIN, SDA, SCL, $\overline{RST}$	0	1	
T_A	Ambient Temperature Range		-40	85	°C
T_J	Junction Temperature Range		-40	125	
R_L	Speaker Resistance		6	-	Ω
L_O	Output Low Pass Filter Inductance		10	-	μH

PWM Operating Conditions

Symbol	Parameter	Test Conditions	Value	Unit
f_S	Output Sample Rate	32 kHz Data Rate ±2%	256	kHz
		44.1k/88.2k/176.4 kHz Data Rate ±2%	352.8	
		48k/96k/192 kHz Data Rate ±2%	384	

PLL Input Parameters and External Filter Components

Symbol	Parameter	Test Conditions	APA3163A			Unit
			Min.	Typ.	Max.	
f_{MCLK}	MCLK Frequency		2.8224	-	24.576	MHz
	MCLK Duty Cycle		40	50	60	%
tr/tf (MCLK)	Rise/Fall Time for MCLK		-	-	5	ns
	LRCLK Allowable Drift before LRCLK Reset		-	-	4	MCLKs
	External PLL Filter Capacitor C1	SMD 0603 Y5V	-	47	-	nF
	External PLL Filter Capacitor C2	SMD 0603 Y5V	-	4.7	-	
	External PLL Filter Resistor R		-	470	-	Ω

Electrical Characteristics

T_A=25°C, PV_{DD}=18V, V_{DD}=3.3V (AVDD and DVDD), R_L=8Ω, BD Mode, f_S=48kHz (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA3163A			Unit
			Min.	Typ.	Max.	
DC CHARACTERISTICS						
I_{DD}	3.3V Supply Current (AVDD, DVDD)	Normal Mode (No load)	-	10	20	mA
		Reset (No load)	-	7.2	14.5	
I_{PVDD}	Full Bridge Stage Supply Current (PVDD_X)	Normal Mode (No load)	-	18	36	
		Reset (No load)	-	0.5	1	
I_{IL}	Low Level Input Current	V_I<V_{IL}, V_{DD}=3.6V (AVDD and DVDD)	-	150	-	μA

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Electrical Characteristics (Cont.)

T_A=25°C, PV_{DD}=18V, V_{DD}=3.3V (AVDD and DVDD), R_L=8Ω, BD Mode, f_S=48kHz (unless otherwise noted)

Symbol	Parameter	Test Conditions		APA3163A			Unit
				Min.	Typ.	Max.	
DC CHARACTERISTICS (CONT.)							
I_{IH}	High Level Input Current	V_I>V_{IH}, V_{DD}=3.6V (AVDD and DVDD)		-	150	-	μA
$r_{DS(ON)}$	Drain to source resistance,LS	T_J=25°C, includes metallization resistance		-	180	-	mΩ
	Drain to source resistance,HS	T_J=25°C, includes metallization resistance		-	180	-	mΩ
T_{TP}	Thermal Protection Threshold			-	160	170	°C
	Thermal Protection Threshold Hysteresis			-	25	-	
η	Efficiency	Stereo, R_L=8Ω, P_O=18W		-	88	-	%
R_{OUT}	Internal Pull-Down Resistance at Each OUT_X			-	3	-	kΩ
AC CHARACTERISTICS							
P_O	Output Power	THD+N=1% f_{in}=1kHz, R_L=8Ω	PV_{DD}=18V	14.5	16	-	W
			PV_{DD}=12V	6.5	7.2	-	
			PV_{DD}=8V	2.9	3.2	-	
		THD+N=1% f_{in}=1kHz, R_L=6Ω	PV_{DD}=12V	8.1	9	-	
		THD+N=10% f_{in}=1kHz, R_L=8Ω	PV_{DD}=18V	-	20	-	
			PV_{DD}=12V	-	9	-	
			PV_{DD}=8V	-	4	-	
		THD+N=10% f_{in}=1kHz, R_L=6Ω	PV_{DD}=12V	-	11	-	
THD+N	Total Harmonic Distortion Plus Noise	f_{in}=1kHz, R_L=8Ω	PV_{DD}=18V, P_O=1W	-	0.06	-	%
			PV_{DD}=12V, P_O=1W	-	0.13	-	
			PV_{DD}=8V, P_O=1W	-	0.2	-	
Crosstalk	Channel Separation	P_O=0.25W, R_L=8Ω, f_{in}=1kHz		-	-82	-	dB
Att_{Mute}	Mute Attenuation	f_{in}=1kHz, R_L=8Ω, V_O=1V_{rms}		-	-70	-	
$Att_{shutdown}$	Shutdown Attenuation	f_{in}=1kHz, R_L=8Ω, V_O=1V_{rms}		-	-110	-	
S/N	Signal to Noise Ratio	R_L=8Ω, P_O=16W, With A-Weighting Filter (A_V=0dB)		-	97	-	
V_n	Noise Output Voltage	With A-Weighting Filter (A_V=0dB)		-	150	-	μV_{rms}

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Serial Audio Ports Slave Mode

Over recommended operating conditions (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA3163A			Unit
			Min.	Typ.	Max.	
f_{SCLK}	Frequency, SCLK $32xf_S$, $48xf_S$, $64xf_S$	C_L=30pF	1.024	-	12.288	MHz
t_{Setup1}	Setup Time, LRCLK to SCLK Rising Edge		10	-	-	ns
t_{Hold1}	Hold Time, LRCLK to SCLK Rising Edge		10	-	-	

Serial Audio Ports Slave Mode

Over recommended operating conditions (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA3163A			Unit
			Min.	Typ.	Max.	
t_{Setup2}	Setup Time, SDIN to SCLK Rising Edge		10	-	-	ns
t_{Hold}	Hold Time, SDIN to SCLK Rising Edge		10	-	-	
	LRCLK Frequency		8K	48K	48K	kHz
	LRCLK Duty Cycle		40	50	60	%
	SCLK Duty Cycle		40	50	60	
	SCLK Rising Edges Between LRCLK Riding Edges		32	-	64	SCLK edges
$t_{(edge)}$	LRCLK Clock Edge With Respect To The Falling Edge of SCLK		-1/4	-	1/4	SCLK period
tr/tf (SCLK/LRCLK)	Rise/Fall Time for SCLK/LRCLK		-	-	8	ns

Reset Timing

Control signal parameters over recommended operating conditions (unless otherwise noted). Please refer to “Recommended Use Model” section on usage of all terminals.

Symbol	Parameter	Test Conditions	APA3163A			Unit
			Min.	Typ.	Max.	
$t_{p(\overline{RST})}$	Pulse Duration, $\overline{RST}$ Active.	No Load	100	-	-	µs
$t_{d(12C_Ready)}$	Time to Enable I^2C		-	-	13.5	ms

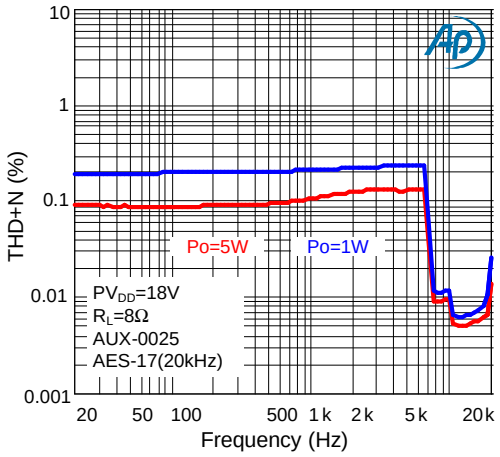
I²C Serial Control Port Operation

Timing characteristics for I²C Interface signals over recommended operating conditions (unless otherwise noted)

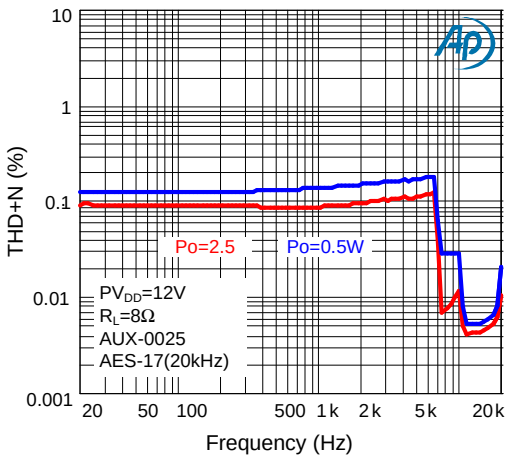
Symbol	Parameter	Test Conditions	APA3163A			Unit
			Min.	Typ.	Max.	
f_{SCL}	Frequency, SCL	No Wait States	-	-	400	kHz
$t_{W(H)}$	Pulse Duration, SCL High		0.6	-	-	µs
$t_{W(L)}$	Pulse Duration, SCL Low		1.3	-	-	
t_r	Rise Time, SCL and SDA		-	-	300	ns
t_f	Fall Time, SCL and SDA		-	-	300	
t_{setup1}	Setup Time, SCL to SDA		100	-	-	
t_{hold1}	Hold Time, SCL to SDA		0	-	-	
$t_{(buf)}$	Bus Free Time Between Stop and Start Condition		1.3	-	-	µs
t_{setup2}	Setup Time, SCL to Start Condition		0.6	-	-	
t_{hold2}	Hold Time, Start condition to SCL		0.6	-	-	
t_{setup3}	Setup Time, SCL to Stop Condition		0.6	-	-	
C_L	Load Capacitance for Each Bus Line		-	-	400	pF

Typical Operating Characteristics

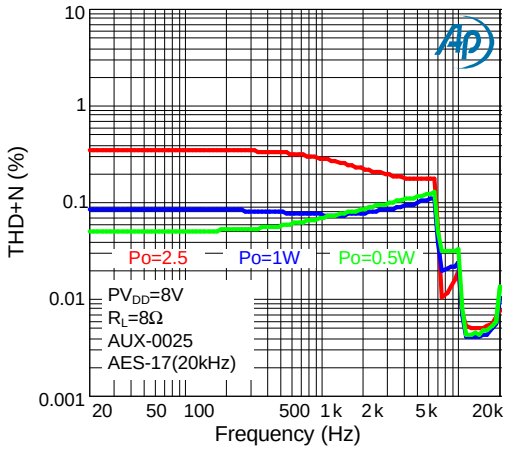
THD+N vs. Frequency



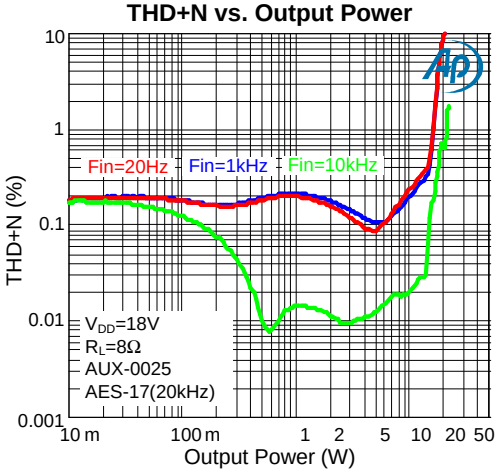
THD+N vs. Frequency



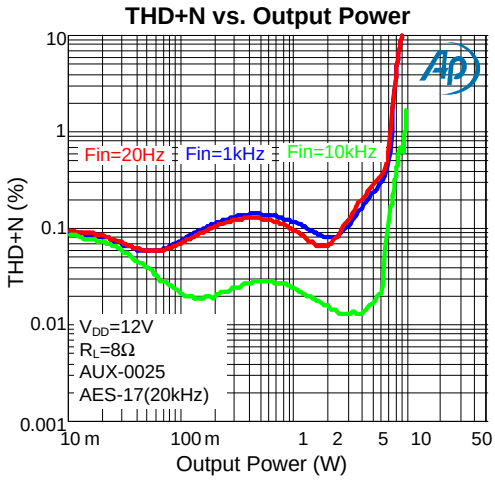
THD+N vs. Frequency



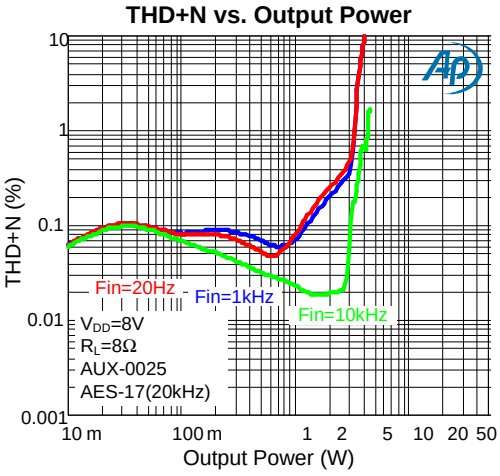
THD+N vs. Output Power



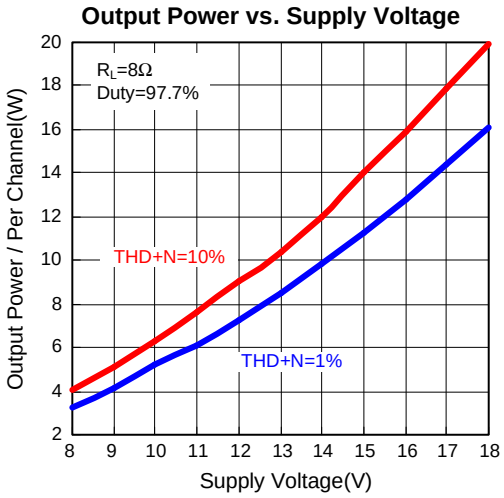
THD+N vs. Output Power

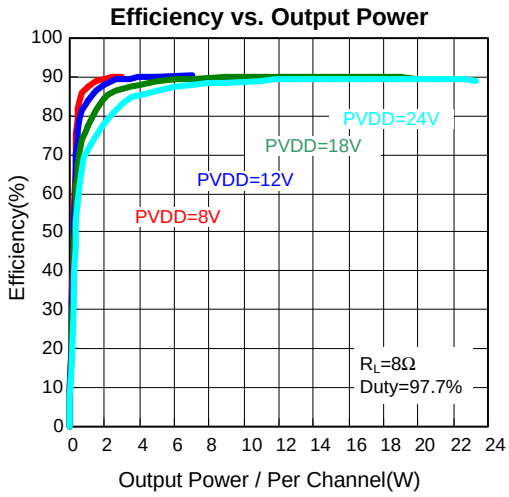


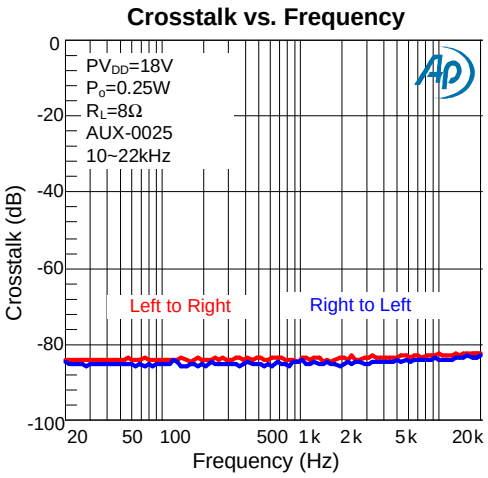
THD+N vs. Output Power

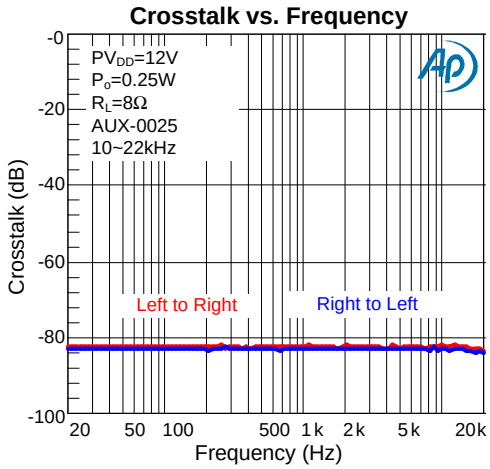


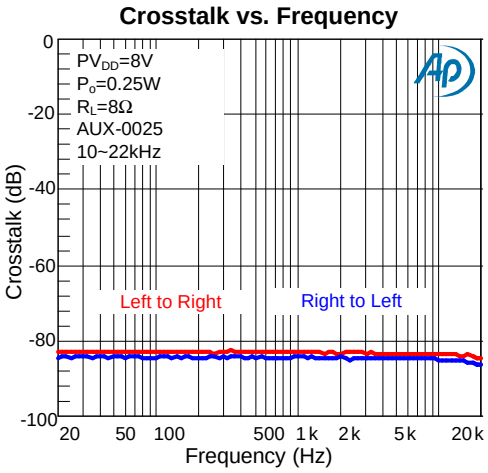
Typical Operating Characteristics (Cont.)











Pin Description

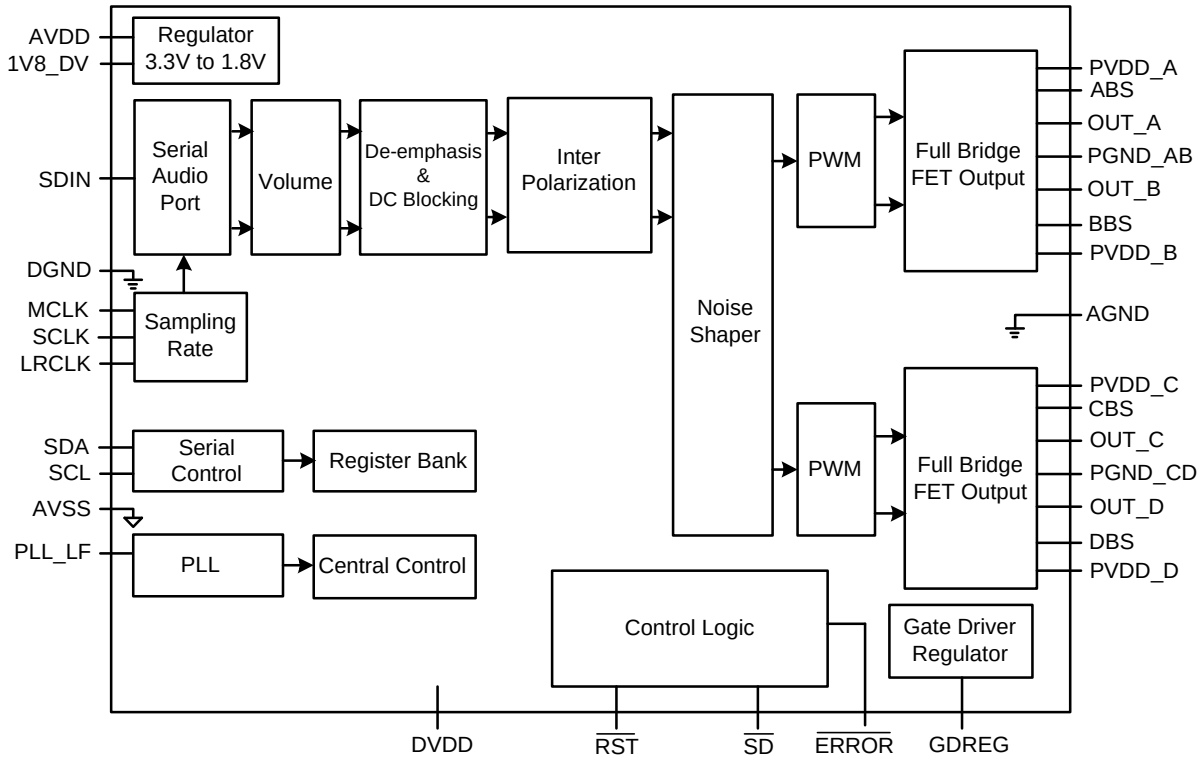
PIN		I/O/P	FUNCTION
NO.	NAME		
1	OUT_A	O	Output of half bridge A.
2, 3	PVDD_A	P	Power supply for half bridge A.
4	ABS	I/O	High side bootstrap supply for half bridge A.
5, 32	GDREG	O/P	Internal regulator output of gate driver.
6	NC	-	No connection.
7	NC	-	No connection.
8	TM	I	Test mode digital input pin.
9, 11	AVSS	P	Analog power supply's ground.
10	PLL_LF	O	PLL negative loop filter pin.
12	2V5_AV	O/P	Internal regulated 2.5V for analog block's supply, Not for power external device.
13	AVDD	P	Analog powers supply and connects to 3.3V.
14	$\overline{\text{ERROR}}$	O	When over temperature, over current over voltage and under voltage occur, this pin will be pull low; and it will be reset to high when the fault condition has be remove.
15	MCLK	I	Master clock input.
16	TP1	I/O	Test mode digital input/output pin.
17	TP2	I/O	Test mode digital input/output pin.
18	1V8_DV	O/P	Internal regulated 1.8V for digital block's supply, Not for power external device.
19	$\overline{\text{SD}}$	I	Active LOW, Shutting down the noise shaper and initiating PWM stop sequence.
20	LRCLK	I	Input serial audio data left/right clock. (Sample rate clock), it's weak pull down terminal.
21	SCLK	I	Serial audio data clock (shift clock). SCLK is the serial audio port input data bit clock.
22	SDIN	I	Serial audio data input.
23	SDA	IO	I^2C serial control data interface input/output.
24	SCL	I	I^2C serial control clock input.
25	$\overline{\text{RST}}$	I	Reset control, place a logic low to this pin, will reset the APA3163A to its default condition. It's weak pull-up terminal.
26	TP3	I/O	Test mode digital input/output pin.
27	DVDD	P	Digital powers supply and connects to 3.3V.
28	DVSS	P	Digital power supply's ground.
29	GND	P	Power stage's analog ground.
30	AGND	P	Power stage's analog ground.
31	DVREG	O/P	Digital voltage regulator's output, only for internal used.
33	DBS	I/O	High side bootstrap supply for half bridge D.
34, 35	PVDD_D	P	Power supply for half bridge D.
36	OUT_D	O	Output of half bridge D.
37, 38	PGND_CD	P	Power Ground connection for half bridge C and D.
39	OUT_C	O	Output of half bridge C.
40, 41	PVDD_C	P	Power supply for half bridge C.
42	CBS	I/O	High side bootstrap supply for half bridge C.
43	BBS	I/O	High side bootstrap supply for half bridge B.

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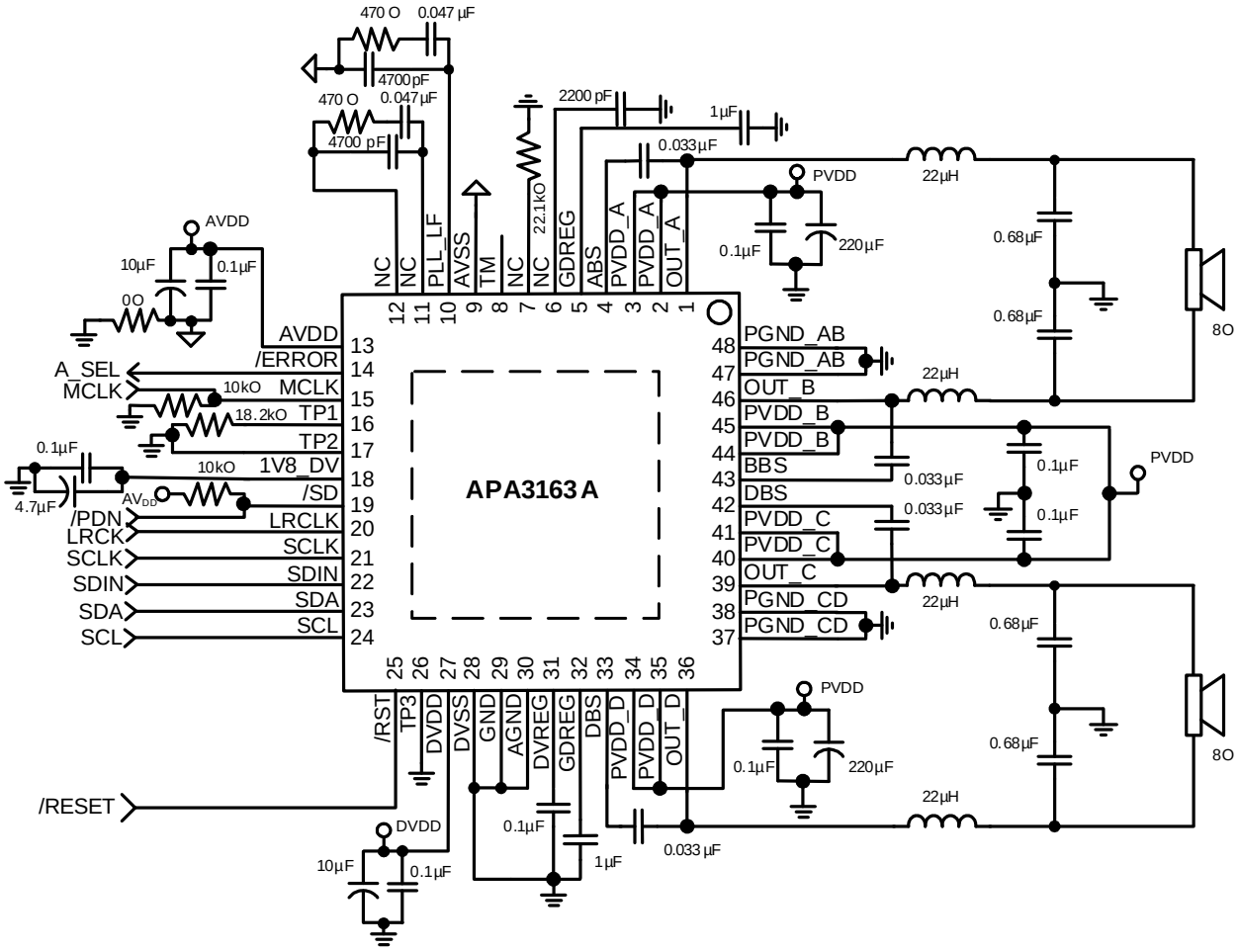
Pin Description (Cont.)

PIN		I/O/P	FUNCTION
NO.	NAME		
44, 45	PVDD_B	P	Power supply for half bridge B.
46	OUT_B	O	Output of half bridge B.
47, 48	PGND_AB	P	Power Ground connection for half bridge A and B.

Block Diagram



Typical Application Circuit



Function Description

Clock And PLL

The APA3163A is a slave device and receives signals from MCLK, SCLK, and LRCLK. The digital audio processor (DAP) provides all sample rates and MCLK rates which defined in the clock control register.
The APA3163A checks to verify that SCLK is a particular value of $32f_S$, $48f_S$, or $64f_S$. The DAP only provides a $1\times f_S$ LRCLK. The timing relationship of these clocks to SDIN is shown in subsequent sections.

Serial Data Interface

Serial data is an input transmitted to SDIN. The PWM outputs are derived from SDIN. Besides, the APA3163A DAP receives left-justified, right-justified, and I²S serial data formats with 16, 20, or 24 bit.

PWM Section

The APA3163A DAP device is a high power efficiency and high-performance digital audio reproduction. A noise shaper is used to increase dynamic range and SNR in the audio band. The PWM section receives 24bit PCM data from the DAP and outputs two BTL PWM audio output channels.
The PWM section has individual channel dc blocking filters that can be enabled and disabled. The low pass filter cutoff frequency is less than 1Hz. Besides, the PWM section includes individual channel de-emphasis filters for 44.1 and 48 kHz and can be enabled and disabled.
The adjustable maximum modulation limit of PWM section is from 93.8% to 98.4%.

I²C Compatible Serial Control Interface

The APA3163A DAP receives commands from a system controller through an I²C serial control slave interface. The serial control interface supports both normal-speed 100kHz and high-speed 400kHz operations without waiting states. As an added feature, even though the MCLK is absent, the interface operates.
For status registers, the serial control interface provides both single-byte and multi-byte read and write operations; and for the general control registers, they associated with the PWM.

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Function Description (Cont.)

Serial Interface Control And Timing

I²S Timing

I²S timing uses LRCLK to define the data for the left channel and the right channel when the data being transmitted. For the left channel, the LRCLK is low; for the right channel, the LRCLK is high. A bit clock running at 32, 48, or 64 × f_S is used to clock in the data. When the LRCLK signal changes state, there is a delay of one bit clock from the time which the first bit of data on the data lines. The data is written MSB first and is valid on the rising edge of bit clock. The DAP masks unused trailing data bit positions.

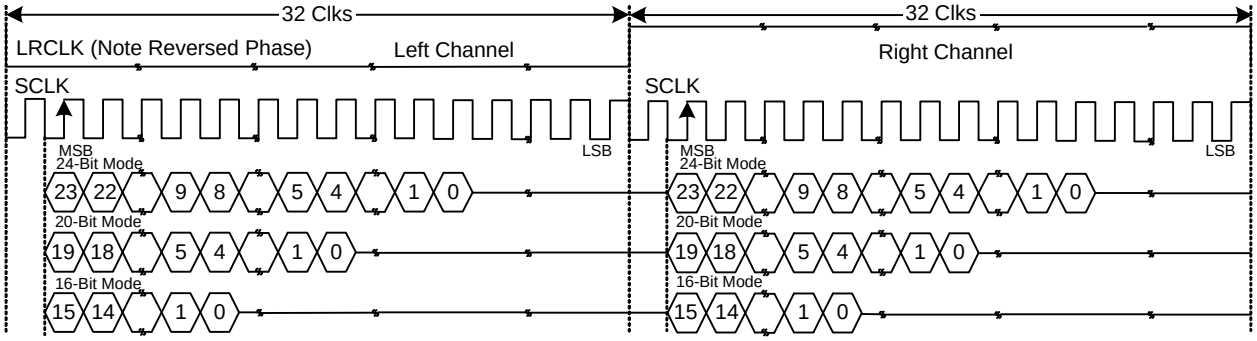


Figure 1. I²S 64 f_S Format

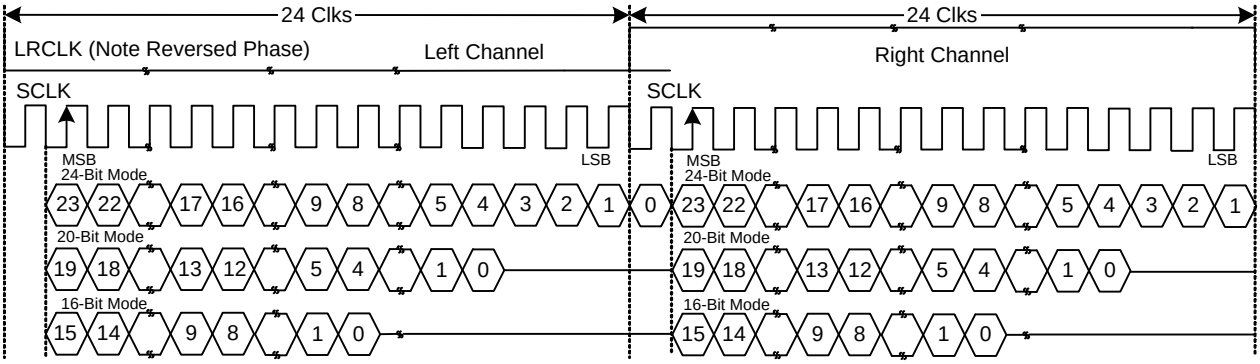


Figure 2. I²S 48 f_S Format

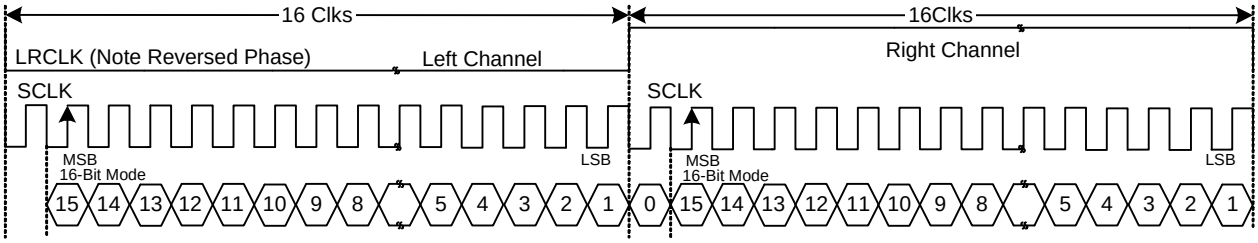


Figure 3. I²S 32 f_S Format

Function Description (Cont.)

Left-Justified

Left-justified (LJ) timing uses LRCLK to define the data for the left channel and the right channel when the data being transmitted. For the left channel, the LRCLK is high; for the right channel, the LRCLK is low. A bit clock running at 32, 48, or 64 × f_S is used to clock in the data. The first bit of data appears on the data lines when LRCLK toggles. The data is written MSB first and is valid on the rising edge of the bit clock. The DAP masks unused trailing data bit positions.

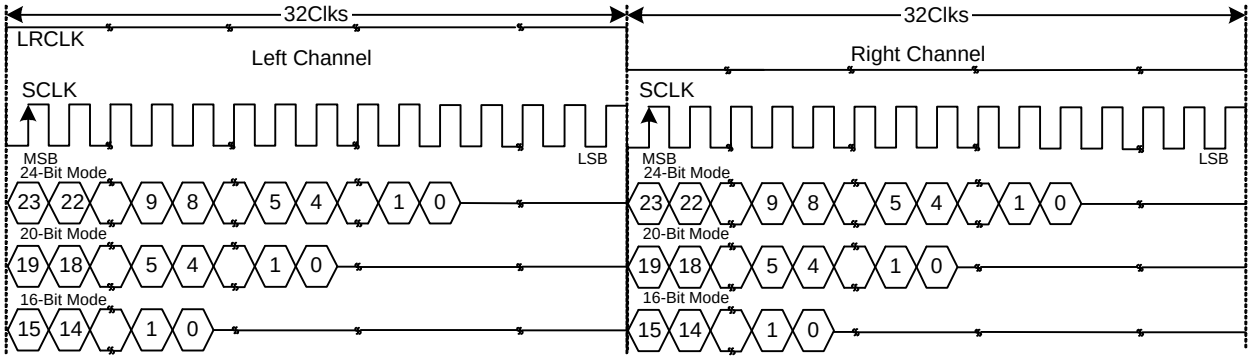


Figure 4. Left-Justified 64 f_S Format

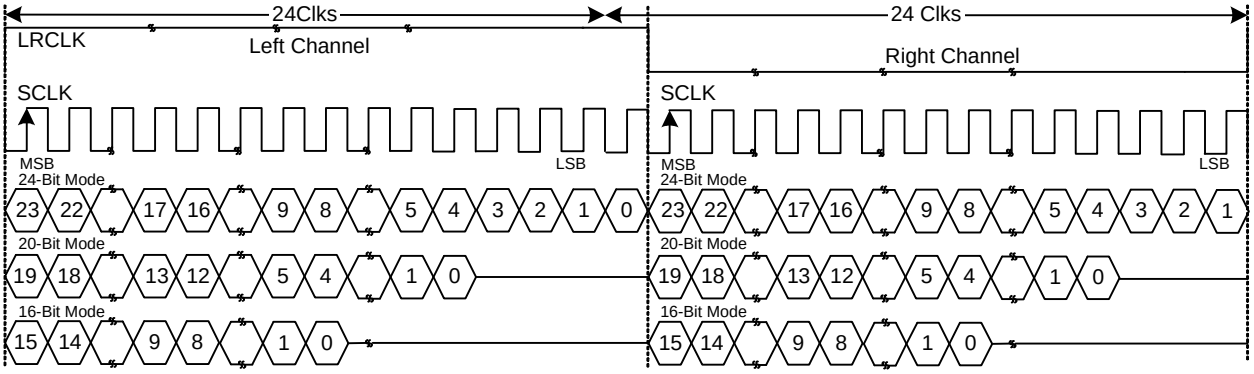


Figure 5. Left-Justified 48 f_S Format

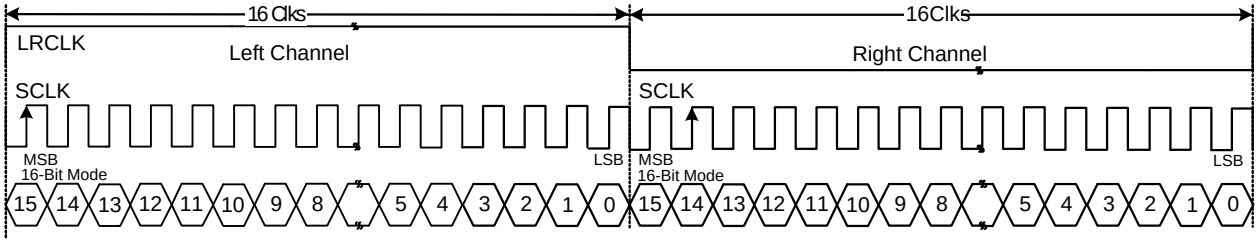


Figure 6. Left-Justified 32 f_S Format

Function Description (Cont.)

Right-Justified

Right-justified (RJ) timing uses LRCLK to define the data for the left channel and the right channel when the data being transmitted. For the left channel, the LRCLK is high; for the right channel, the LRCLK low. A bit clock running at 32, 48, or 64 × f_S is used to clock in the data. After LRCLK toggles, for 24bit data, the first bit of data appears on the data 8 bit-clock. In RJ mode, the LSB of data is always clocked by the last bit clock before LRCLK transitions. The data is written MSB first and is valid on the rising edge of bit clock. The DAP masks unused leading data bit positions.

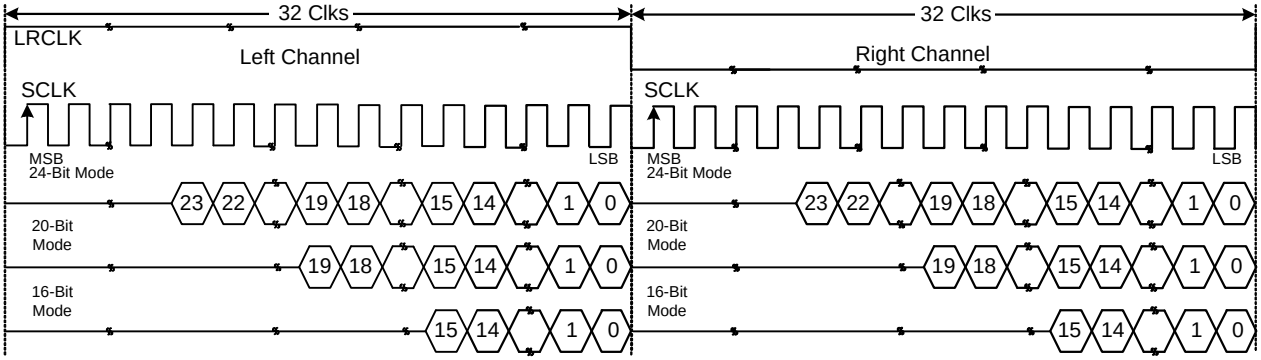


Figure 7. Right-Justified 64 f_S Format

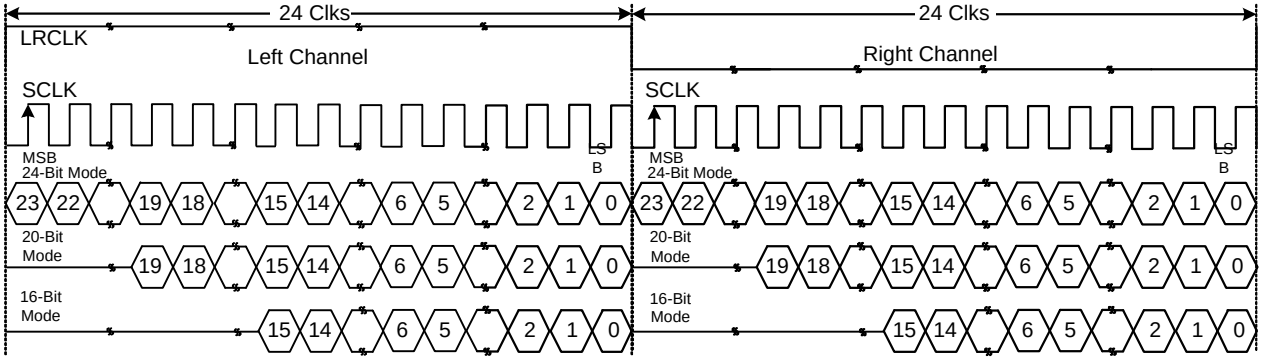


Figure 8. Right-Justified 48 f_S Format

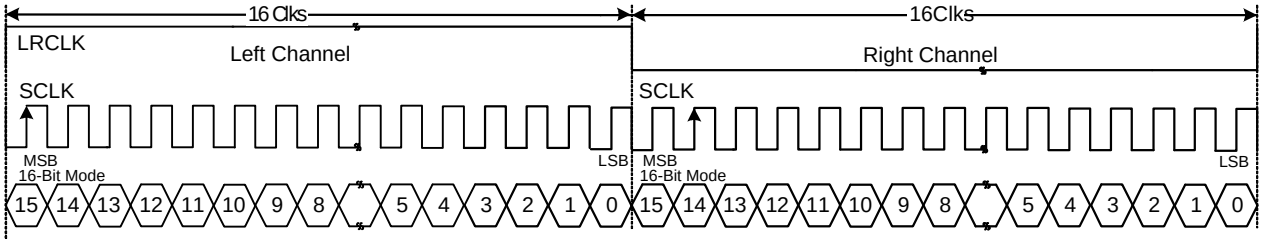


Figure 9. Right-Justified 32 f_S Format

Function Description (Cont.)

I²C Serial Control Interface

The APA3163A DAP has a bidirectional I²C interface that compatible with the I²C (Inter IC) bus protocol. Besides, it provides both 100kHz and 400kHz data transfer rates to single and multiple bytes write and read operations.
This is a slave only device, and it doesn't support a multi-master bus environment or wait state insertion. The function of the control interface is to read device status and to program the registers of the device.
The DAP supports the standard-mode I²C bus operation (100kHz maximum) and the fast I²C bus operation (400kHz maximum). Without I²C wait cycles, the DAP performs I²C operations.

General I²C Operation

The I²C bus uses SDA (data) and SCL (clock) to communicate between integrated circuits in a system. Data is transferred on the bus serially one bit at a time. With the most significant bit (MSB) transferred first, the address and data can be transferred in byte (8bit) format. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus.
The bus uses transitions on the SDA when the clock is high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data bit transitions must occur within the low time of the clock. These conditions are shown in Figure 10. The master generates the 7bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The APA3163A holds SDA low during the acknowledge clock to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence.
Each device is addressed by a unique 7bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pull-up resistor must be used for the SDA and SCL signals to set the high level for the bus.

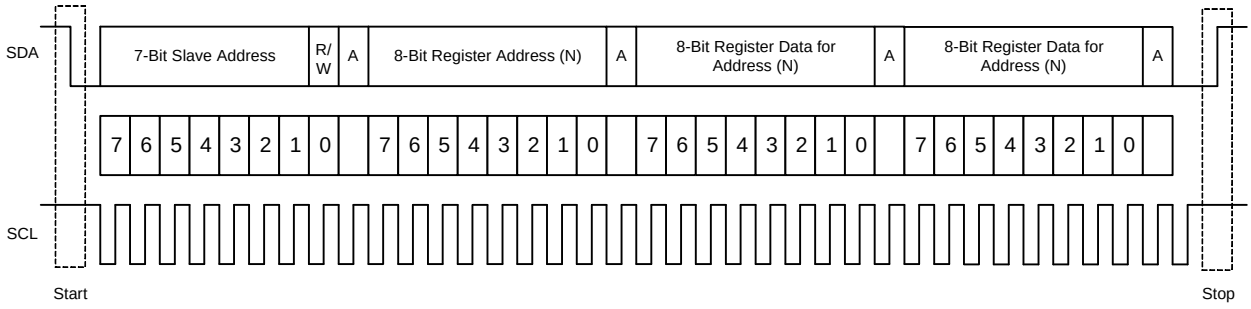


Figure 10. Typical I²C Sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 10.
The 7bit address for APA3163A is 0011 010 (0x34). APA3163A address can be changed from 0x34 to 0x38 by writing 0x38 to device address register 0xF9.

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Function Description (Cont.)

Single- and Multiple-Byte Transfers

The serial control interface supports single-byte and multiple-byte (R/W) operations for sub-addresses 0x00 to 0x1F. However, for the sub-addresses 0x20 to 0xFF, the serial control interface supports only multiple-byte read/write operations (in multiples of 4 bytes).

During multiple-byte read operations, the DAP responds with data, a byte at a time, starting at the sub-address assigned, as long as the master device continues to respond with acknowledges. If a particular sub-address does not contain 32 bits, the unused bits are read as logic 0.

During multiple-byte write operations, the DAP compares the number of bytes transmitted to the number of bytes that are required for each specific sub-address.

Supplying a sub-address for each sub-address transaction is referred to as random I²C addressing. The APA3163A also supports sequential I²C addressing. For write transactions, if a sub-address is issued and followed by data for that sub-address and the 15 sub-addresses that follow, a sequential I²C write transaction has taken place, and the data for all 16 sub-addresses is successfully received by the APA3163A. For I²C sequential write transactions, the sub-address then serves as the start address, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many sub-addresses are written. As was true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last sub-address, the data for the last sub-address is discarded. However, if all other data written is accepted, only the incomplete data is discarded.

Single-Byte Write

As shown in Figure 11, a single-byte data write transfer begins with the master device transmitting a start condition followed by the I²C device address and the R/W bit. The R/W bit determines the direction of the data transfer. For a write data transfer, the R/W bit will be a 0. After receiving the correct I²C device address and the R/W bit, the DAP responds with an acknowledge bit. And then, the master transmits the address byte or bytes corresponding to the APA3163A internal memory address being accessed. After receiving the address byte, the APA3163A responds with an acknowledge bit again. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the APA3163A again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data write transfer.

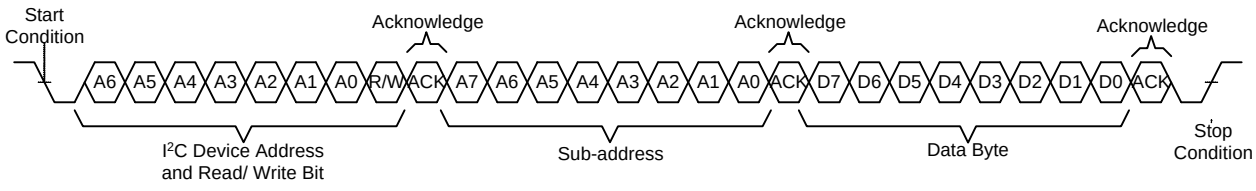


Figure 11. Single-Byte Write Transfer

Function Description (Cont.)

Multiple-Byte Write

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the DAP as shown in Figure 12. After receiving each data byte, the APA3163A responds with an acknowledge bit.

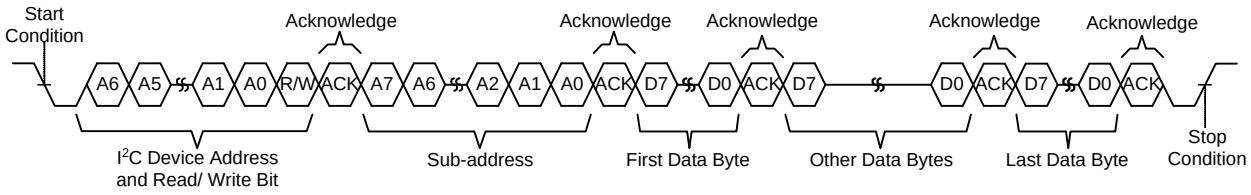


Figure 12. Multiple-Byte Write Transfer

Single-Byte Read

As shown in Figure 13, a single-byte data read transfer begins with the master device transmitting a start condition followed by the I²C device address and the R/W bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the R/W bit becomes a 0. After receiving the APA3163A address and the read/write bit, APA3163A responds with an acknowledge bit. Besides, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the APA3163A address and the read/write bit again. This time the read/ write bit becomes a 1, indicating a read transfer. After receiving the address and the read/write bit, the APA3163A again responds with an acknowledge bit. And then, the APA3163A transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not acknowledge followed by a stop condition to complete the single byte data read transfer.

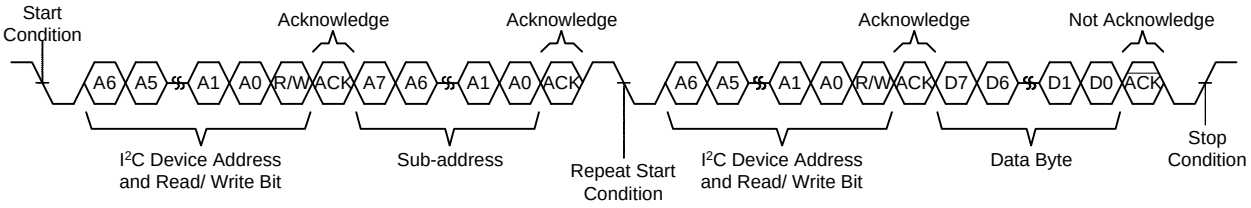


Figure 13. Single-Byte Read Transfer

Multiple-Byte Read

A multiple-byte data read transfer is identical to a single-byte data read transfer except that multiple data bytes are transmitted by the APA3163A to the master device as shown in Figure 14. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

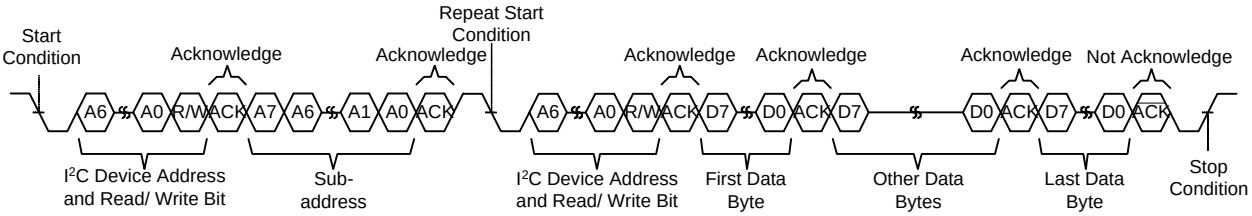


Figure 14. Multiple-Byte Read Transfer

Function Description (Cont.)

Dynamic Range Control (DRC)

The DRC scheme has a single threshold, offset, and slope (all programmable). There is one ganged DRC for the left/ right channels.

The DRC input/output diagram is shown in Figure 15.

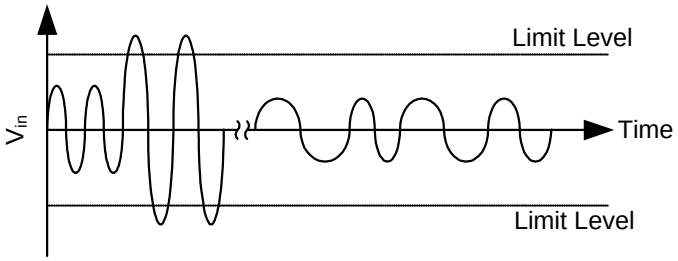


Figure 15. Dynamic Range Control

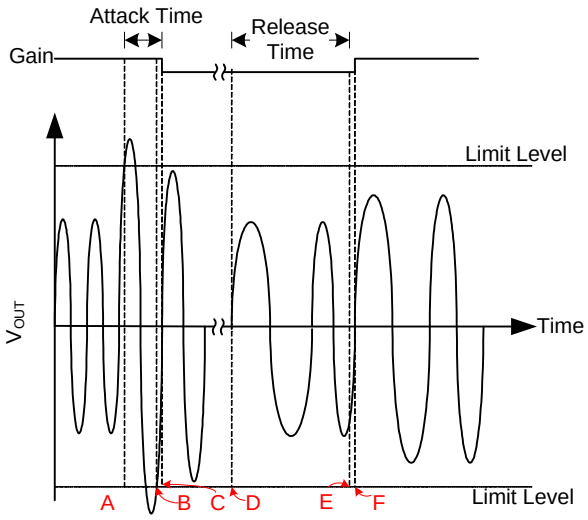


Figure 16. DRC Structure

Function Description (Cont.)

Recommended Use Model

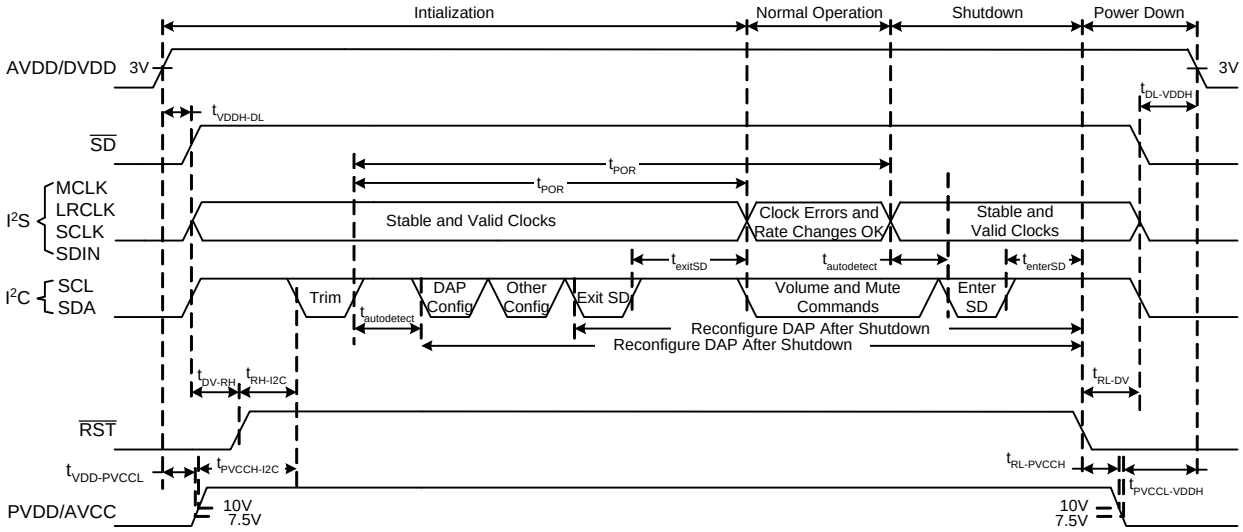


Figure 17. Recommended Command Sequence

Parameter	Description	APA3163A			Unit
		Min.	Typ.	Max.	
$t_{VDDH-DL}$	Time digital inputs must remain low after AVDD/DVDD goes above 3V	0	-	-	µs
$t_{DL-VDDH}$	Time digital inputs must be low before AVDD/DVDD goes below 3V	0	-	-	
$t_{VDDH-PVDDL}$	Time PVDD/AVCC remains below 7.5V after AVDD/DVDD goes above 3V	100	-	-	
$t_{PVDDL-VDDH}$	Time PVDD/AVCC must be below 7.5V before AVDD/DVDD goes below 3V	0	-	-	
$t_{PVDDH-I2C}$	Time PVDD/AVCC must be above 10V before I²C commands may address device	10	-	-	
$t_{RL-PVDDH}$	Time PVDD/AVCC must remain above 10V after $\overline{RST}$ goes low	2	-	-	
t_{RH-I2C}	Time RESET must be high before I²C commands may address device	13.5	-	-	ms
t_{DV-RH}	Time digital inputs must be valid (driven as recommended) before $\overline{RST}$ goes high	100	-	-	µs
t_{RL-DV}	Time digital inputs must remain valid (driven as recommended) after $\overline{RST}$ goes low	2	-	-	
$t_{autodetect}$	Auto-detect completion wait time (given stable and valid clocks) before issuing further commands	50	-	-	ms
t_{exitSD}	Exit shutdown wait time before issuing further commands to device (t start given by register 0x1A)	1+1.3 x t_{start}	-	-	
$t_{enterSD}$	Enter shutdown wait time before issuing further commands to device (t stop given by register 0x1A)	1+1.3 x t_{stop}	-	-	
t_{POR}	Power-on-reset wait time after 1st trim following AVDD/DVDD power-up (t_{start} given by register 0x1A) (does not apply to trim commands following subsequent resets)	240 + 1.3 x t_{start}	-	-	

Function Description (Cont.)

Recommended Use Model (Cont.)

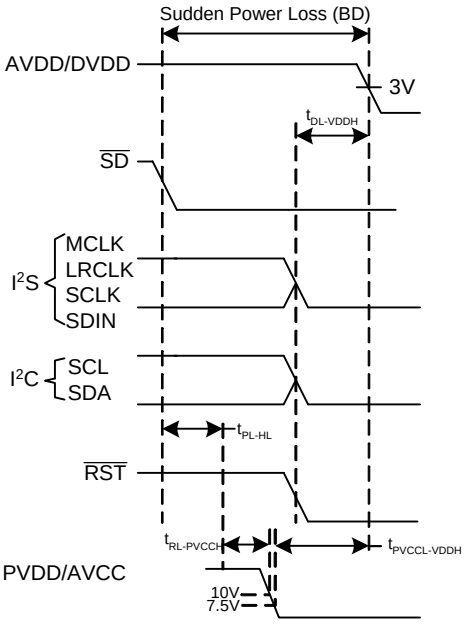


Figure 18. Power Loss Sequence

Parameter	Description	APA3163A			Unit
		Min.	Typ.	Max.	
t_{RL-DV}	Time digital inputs must remain valid (driven as recommended) after $\overline{RST}$ goes low	2	-	-	µs
$t_{DL-VDDH}$	Time digital inputs must be low before AVDD/DVDD goes below 3V	0	-	-	
$t_{RL-PVDDH}$	Time PVDD/AVCC must remain above 10V after $\overline{RST}$ goes low	2	-	-	
$t_{PVDDL-VDDH}$	Time PVDD/AVCC must be below 7.5V before AVDD/DVDD goes below 3V	0	-	-	

Recommended Command Sequences

The DAP has two groups of commands. One set is for configuration and is intended for use only during initialization. The other set has built-in click and pop protection and may be used during normal operation while audio is streaming. The following supported command sequences illustrate how to initialize, operate, and shutdown the device.

Function Description (Cont.)

Initialization Sequence

Use the following sequence to power-up and initialize the device:

1. Hold all digital inputs low and ramp up AVDD/DVDD to at least 3V.
2. Initialize digital inputs and PVDD supply as follows:
   • Drive $\overline{RST}$=0, $\overline{SD}$=1, and other digital inputs to their desired state while ensuring that all are never more than 2.5V above AVDD/DVDD. Provide stable and valid I²S clocks (MCLK, LRCLK, and SCLK). Wait at least 100µs, drive $\overline{RST}$=1, and wait at least another 13.5ms.
   • Ramp up PVDD to at least 8V while ensuring that it remains below 6V for at least 100µs after AVDD/DVDD reaches 3V. Then wait at least another 10µs.
3. Configure the DAP via I²C (see Users's Guide for typical values): DRC parameters (0x46, and 0x60~62).
4. Configure remaining registers.
5. Exit shutdown (sequence defined below).

Normal Operation

The following are the only events supported during normal operation:

(a) Writes to master/channel volume registers

(b) Writes to soft mute register

(c) Enter and exit shutdown (sequence defined below)

(d) Clock errors and rate changes

Note: Events (c) and (d) are not supported for 240ms+1.3xt_0 0after trim following AVDD/DVDD power up ramp (where Tstart is specified by register 0x1A).

Shutdown Sequence

Enter:

1. Ensure I²S clocks have been stable and valid for at least 50ms.
2. Write 0x40 to register 0x05.
3. Wait at least 1ms+1.3xt_{stop} (where t_{stop} is specified by register 0x1A).
4. Once in shutdown, stable clocks are not required while device remains idle.
5. If desired, reconfigure by ensuring that clocks have been stable and valid for at least 50ms before returning to step 4 of initialization sequence.

Exit:

1. Ensure I²S clocks have been stable and valid for at least 50ms.
2. Write 0x00 to register 0x05 (exit shutdown command may not be serviced for as much as 240ms after trim following AVDD/DVDD powerup ramp).
3. Wait at least 1ms+1.3xt_{start} (where t_{start} is specified by register 0x1A).
4. Proceed with normal operation.

Function Description (Cont.)

Power-down Sequence

Use the following sequence to power-down the device and its supplies:

1. If time permits, enter shutdown (sequence defined above); else, in case of sudden power loss, assert $\overline{SD}$=0 and wait at least 2ms.
2. Assert $\overline{RST}$=0.
3. Drive digital inputs low and ramp down PVDD supply as follows:
   - Drive all digital inputs low after $\overline{RST}$ has been low for at least 2µs.
   - Ramp down PVDD while ensuring that it remains above 8V until $\overline{RST}$ has been low for at least 2µs.
4. Ramp down AVDD/DVDD while ensuring that it remains above 3V until PVDD is below 6V and that it is never more than 2.5V below the digital inputs.

Table 1. Serial Control Interface Register Summary

Sub Address	Register Name	No. of Bytes	Contents	Initialization Values
			A u indicates unused bits.	
0x00	Clock control register	1	Description shown in subsequent section	0x6C
0x01	Device ID register	1	Description shown in subsequent section	0x00
0x02	Error status register	1	Description shown in subsequent section	0x00
0x03	System control register 1	1	Description shown in subsequent section	0x80
0x04	Serial data interface	1	Description shown in subsequent section	0x05
0x05		1	Description shown in subsequent section	0x40
0x06	Soft mute register	1	Description shown in subsequent section	0x00
0x07	Master volume	1	Description shown in subsequent section	0xFF (mute)
0x08	Channel 1 vol	1	Description shown in subsequent section	0x30 (0dB)
0x09	Channel 2 vol	1	Description shown in subsequent section	0x30 (0dB)
0x0A	Fine master volume	1	Description shown in subsequent section	0x00 (0dB)
0x0B - 0X0D			Reserved (1)	
0x0E	Volume configuration register	1	Description shown in subsequent section	0x91
0x0F		1	Reserved (1)	
0x10	Modulation limit register	1	Description shown in subsequent section	0x02
0x15-0x19		1	Reserved (1)	
0x1A	Start/stop period register	1	Description shown in subsequent section	0x0A
0x1B		1	Reserved (1)	
0x1C		1	Reserved (1)	
0x1D–0x1F		1	Reserved (1)	
0x20	Input MUX register	4	Description shown in subsequent section	0x 0089 777A
0x21-0x24		4	Reserved (1)	
0x25	PWM MUX register	4	Description shown in subsequent section	0x0102 1345
0x26-0x5F		4	Reserved (1)	

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Function Description (Cont.)

Table 1. Serial Control Interface Register Summary (Cont.)

Sub Address	Register Name	No. of Bytes	Contents	Initialization Values
0x46	DRC Control	4	Description shown in subsequent section	0x0000 0000
0x60	DRC attack threshold	4	u [31:24], attackTh [23:0]	0x0003 2D64
0x61	DRC release threshold	4	u [31:24], attackTh [23:0]	0x0002 FFE4
0x62	DRC WinIdx	1	Description shown in subsequent section	0x01
0x63-0xF8			Reserved (2)	
0xF9	Update Device Address	4	u [31:8], New Dev Id[7:0] (New Dev Id=0x38)	0x00000034
0xFA-0xFF			Reserved (2)	

Note (1): Reserved register should not be accessed.

Note (2): Reserved register should not be accessed.

Note (3): “ae” stands for α of energy filter, “aa” stands for α of attack filter and “ad” stands for α of decay filter and $1-\alpha = \omega$.

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Function Description (Cont.)

Clock Control Register (0x00)

The clocks and data rates are automatically determined by the APA3163A. The clock control register contains the auto-detected clock status. Bits D7-D5 reflect the sample rate. Bits D4-D2 reflect the MCLK frequency.

Table 2. Clock Control Register (0x00)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	-	-	-	-	-	f_S=32kHz sample rate
0	0	1	-	-	-	-	-	f_S=88.2kHz/96kHz sample rate
0	1	0	-	-	-	-	-	f_S=176.4kHz/192kHz sample rate
0	1	1	-	-	-	-	-	f_S=44.1/48kHz sample rate (5)
-	-	-	0	0	0	-	-	MCLK frequency=64xf_S (6)
-	-	-	0	0	1	-	-	MCLK frequency=128xf_S (6)
-	-	-	0	1	0	-	-	MCLK frequency=192xf_S (7)
-	-	-	0	1	1	-	-	MCLK frequency=256xf_S (5) (8)
-	-	-	1	0	0	-	-	MCLK frequency=384xf_S
-	-	-	1	0	1	-	-	MCLK frequency=512xf_S
-	-	-	1	1	0	-	-	Reserved (4)
-	-	-	1	1	1	-	-	Reserved (4)
-	-	-	-	-	-	0	-	Reserved (4)
-	-	-	-	-	-	-	0	Reserved (4)

Note (4): Reserved registers should not be accessed.
Note (5): Italic is default.
Note (6): Only available for 44.1kHz and 48kHz rates.
Note (7): Rate only available for 32/44.1/48kHz sample rates.
Note (8): Not available at 8kHz.

Device Id Register (0x01)

The device ID register contains the ID code for the firmware revision.

Table 3. General Status Register (0x01)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
X	-	-	-	-	-	-	-	Reserved
-	0	0	0	0	0	0	0	Identification code

Note: Italic is default.

Function Description (Cont.)

Error Status Register (0x02)

The error bits are sticky and are not cleared by the hardware. This means that the software must clear the register (write zeroes) and then read them to determine if they are persistent errors. Error Definitions:
MCLK Error : MCLK frequency is changing. The number of MCLKs per LRCLK is changing.
SCLK Error: The number of SCLKs per LRCLK is changing.
LRCLK Error: LRCLK frequency is changing.

Table 4. Error Status Register (0x02)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	-	-	-	-	-	-	-	MCLK error
-	1	-	-	-	-	-	-	PLL auto clock error
-	-	1	-	-	-	-	-	SCLK error
-	-	-	1	-	-	-	-	LRCLK error
-	-	-	-	1	-	-	-	Reserved
-	-	-	-	-	1	-	-	Reserved
-	-	-	-	-	-	1	-	Over temperature warning (sets around 145^{O}C) POR error, OCP, thermal shutdown error
0	0	0	0	0	0	0	0	No errors

Note: Italic is default.

System Control Register 1 (0x03)

The system control register 1 has several functions:
Bit D7: If 0, the dc-blocking filter for each channel is disabled. If 1, the dc-blocking filter (-3dB cutoff < 1Hz) for each channel is enabled (default).
Bit D5: If 0, use soft unmute on recovery from clock error. This is a slow recovery. Unmute takes same time as volume ramp defined in reg 0x0E. If 1, use hard unmute on recovery from clock error (default). This is a fast recovery, a single step volume ramp Bits D1-D0: Select de-emphasis.

Table 5. System Control Register 1 (0x03)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	-	-	-	-	-	-	-	PWM high-pass (dc blocking) disenabled
1	-	-	-	-	-	-	-	PWM high-pass (dc blocking) enabled
-	0	-	-	-	-	-	-	Reserved
-	-	0	-	-	-	-	-	Reserved
-	-	0	-	-	-	-	-	Reserved
-	-	-	0	-	-	-	-	Reserved
-	-	-	-	0	-	-	-	Reserved
-	-	-	-	-	0	-	-	Reserved
-	-	-	-	-	-	0	0	No de-emphasis
-	-	-	-	-	-	0	1	Reserved
-	-	-	-	-	-	1	0	De-emphasis for f_S=44.1kHz
-	-	-	-	-	-	1	1	De-emphasis for f_S=48kHz

Note: Italic is default.

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Function Description (Cont.)

Serial Data Interface Register (0x04)

As shown in Table 6, the APA3163A supports 9 serial data modes. The default is 24bit, I²S mode.

Table 6. Serial Data Interface Control Register (0x04) Format

D7	D6	D5	D4	D3	D2	D1	D0	Word Length	Receive Serial Data Interface Format
0	0	0	0	0	0	0	0	16	Right-justified
0	0	0	0	0	0	0	1	20	Right-justified
0	0	0	0	0	0	1	0	24	Right-justified
0	0	0	0	0	0	1	1	16	I^2S
0	0	0	0	0	1	0	0	20	I^2S
0	0	0	0	0	1	0	1	24	I^2S
0	0	0	0	0	1	1	0	16	Left-justified
0	0	0	0	0	1	1	1	20	Left-justified
0	0	0	0	1	0	0	0	24	Left-justified
0	0	0	0	1	-	1	0	-	Reserved
0	0	0	0	1	-	-	1	-	Reserved
0	0	0	0	1	1	1	1	-	Reserved

Note: Italic is default.

System Control Register 2 (0x05)

When bit D6 is set low, the system exits all channel shutdown and starts playing audio; otherwise, the outputs are shut down (hard mute).

Table 7. System Control Register 2 (0x05)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	-	-	-	-	-	-	-	Reserved
-	1	-	-	-	-	-	-	Enter all channel shut down (hard mute)
-	0	-	-	-	-	-	-	Exit all channel shut down (Normal operation)
-	-	0	0	0	0	0	0	Reserved

Note: Italic is default.

Soft Mute Register (0x06)

Writing a 1 to any of the following bits sets the output of the respective channel to 50% duty cycle (soft mute).

Table 8. Soft Mute Register (0x06)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
-	-	-	-	-	-	-	1	Soft mute channel 1
-	-	-	-	-	-	-	0	Soft un-mute channel 1
-	-	-	-	-	-	1	-	Soft mute channel 2
-	-	-	-	-	-	0	-	Soft un-mute channel 2
0	0	0	0	0	0	-	-	Reserved

Note: Italic is default.

Function Description (Cont.)

Volume Registers (0x07, 0x08, 0x09)

Step size is 0.5 dB.
Master volume - 0x07 (default is mute)
Channel-1 volume - 0x08 (default is 0 dB)
Channel-2 volume - 0x09 (default is 0 dB)

Table 9. Volume Registers (0x07, 0x08, 0x09)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	24dB
0	0	1	1	0	0	0	0	0dB
1	1	0	0	1	1	0	1	-78.5dB
1	1	0	0	1	1	1	0	-79.0dB
1	1	0	0	1	1	1	1	Values between 0xCF and 0xFE are Reserved
1	1	1	1	1	1	1	1	MUTE (default for master volume)

Note: Italic is default.

Master Fine Volume Register (0x0A)

This register can be used to provide precision tuning of master volume.

Table 10. Master Fine Volume Register (0x0A)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
-	-	-	-	-	-	0	0	0dB
-	-	-	-	-	-	0	1	0.125dB
-	-	-	-	-	-	1	0	0.25dB
-	-	-	-	-	-	1	1	0.345dB
1	-	-	-	-	-	-	-	Write enable bit
-	-	-	-	-	-	-	-	Ignore write to register 0x0A

Note: Italic is default.

Volume Configuration Register (0x0E)

Bits Volume slew rate (Used to control volume change and MUTE ramp rates). These bits control the D2-D0: number of steps in a volume ramp. Volume steps occur at a rate that depends on the sample rate of the I^2S data as follows.

Sample Rate (kHz)	Approximate Ramp Rate
8/16/32	125µs/step
11.025/22.05/44.1	90.7µs/step
12/24/48	83.3µs/step

Table 11. Volume Control Register (0x0E)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	0	0	1	0	-	-	-	Reserved
-	-	-	-	-	0	0	0	Volume slew 512 steps (43ms volume ramp time at 48kHz)

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Function Description (Cont.)

Volume Configuration Register (0x0E) (Cont.)

Table 11. Volume Control Register (0x0E)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
-	-	-	-	-	0	0	1	Volume slew 1024 steps (85ms volume ramp time at 48kHz)
-	-	-	-	-	0	1	0	Volume slew 2048 steps (171ms volume ramp time at 48kHz)
-	-	-	-	-	0	1	1	Volume slew 256 steps (21ms volume ramp time at 48kHz)
-	-	-	-	-	1	x	x	Reserved

Note: Italic is default.

Modulation Limit Register (0x10)

Table 12. Modulation Limit Register (0x10)

D7	D6	D5	D4	D3	D2	D1	D0	MODULATION LIMIT
-	-	-	-	-	0	0	0	Reserved
-	-	-	-	-	0	0	1	98.4%
-	-	-	-	-	0	1	0	97.7%
-	-	-	-	-	0	1	1	96.9%
-	-	-	-	-	1	0	0	96.1%
-	-	-	-	-	1	0	1	95.3%
-	-	-	-	-	1	1	0	94.5%
-	-	-	-	-	1	1	1	93.8%
0	0	0	0	0	-	-	-	Reserved

Note: Italic is default.

Start/Stop Period Register (0x1A)

This register is used to control the soft-start and soft-stop period following an enter/exit all channel shut down command or change in the $\overline{SD}$ state. This helps reduce pops and clicks at start-up and shutdown. The times are only approximate and vary depending on device activity level and I^2S clock stability.

Table 13. Start/Stop Period Register (0x1A)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	-	-	-	-	-	Reserved
-	-	-	0	0	-	-	-	No 50% duty cycle start/stop period
-	-	-	0	1	0	0	0	16.5ms 50% duty cycle start/stop period
-	-	-	0	1	0	0	1	23.9ms 50% duty cycle start/stop period
-	-	-	0	1	0	1	0	31.4ms 50% duty cycle start/stop period
-	-	-	0	1	0	1	1	40.4ms 50% duty cycle start/stop period
-	-	-	0	1	1	0	0	53.9ms 50% duty cycle start/stop period
-	-	-	0	1	1	0	1	70.3ms 50% duty cycle start/stop period
-	-	-	0	1	1	1	0	94.2ms 50% duty cycle start/stop period
-	-	-	0	1	1	1	1	125.7ms 50% duty cycle start/stop period

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Function Description (Cont.)

Start/Stop Period Register (0x1A) (Cont.)

Table 13. Start/Stop Period Register (0x1A)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
-	-	-	1	0	0	0	0	164.6ms 50% duty cycle start/stop period
-	-	-	1	0	0	0	1	239.4ms 50% duty cycle start/stop period
-	-	-	1	0	0	1	0	314.2ms 50% duty cycle start/stop period
-	-	-	1	0	0	1	1	403.9ms 50% duty cycle start/stop period
-	-	-	1	0	1	0	0	538.6ms 50% duty cycle start/stop period
-	-	-	1	0	1	0	1	703.4ms 50% duty cycle start/stop period
-	-	-	1	0	1	1	0	942.5ms 50% duty cycle start/stop period
-	-	-	1	0	1	1	1	1256.6ms 50% duty cycle start/stop period
-	-	-	1	1	0	0	0	1728.1ms 50% duty cycle start/stop period
-	-	-	1	1	0	0	1	2513.6ms 50% duty cycle start/stop period
-	-	-	1	1	0	1	0	3299.1ms 50% duty cycle start/stop period
-	-	-	1	1	0	1	1	4241.7ms 50% duty cycle start/stop period
-	-	-	1	1	1	0	0	5655.6ms 50% duty cycle start/stop period
-	-	-	1	1	1	0	1	7383.7ms 50% duty cycle start/stop period
-	-	-	1	1	1	1	0	9897.3ms 50% duty cycle start/stop period
-	-	-	1	1	1	1	0	13196.4ms 50% duty cycle start/stop period

Note: Italic is default.

Input Multiplexer Register (0x20)

This register controls the modulation scheme (BD mode) as well as the routing of I^2S audio to the internal channels.

Table 14. Input Multiplexer Register (0x20)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	0	0	0	0	0	0	0	Reserved
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	-	-	-	-	-	-	-	Reserved
1	-	-	-	-	-	-	-	Channel 1 BD mode
-	0	0	0	-	-	-	-	SDIN-L to Channel 1
-	0	0	1	-	-	-	-	SDIN-R to Channel 1
-	0	1	0	-	-	-	-	Reserved
-	0	1	1	-	-	-	-	Reserved
-	1	0	0	-	-	-	-	Reserved
-	1	0	1	-	-	-	-	Reserved
-	1	1	0	-	-	-	-	Ground (0) to channel 1
-	1	1	1	-	-	-	-	Reserved
-	-	-	-	0	-	-	-	Reserved
-	-	-	-	1	-	-	-	Channel-2 BD mode

Function Description (Cont.)

Input Multiplexer Register (0x20) (Cont.)

Table 14. Input Multiplexer Register (0x20)

D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
-	-	-	-	-	0	0	0	SDIN-L to Channel 2
-	-	-	-	-	0	0	1	SDIN-R to Channel 2
-	-	-	-	-	0	1	0	Reserved
-	-	-	-	-	0	1	1	Reserved
-	-	-	-	-	1	0	0	Reserved
-	-	-	-	-	1	0	1	Reserved
-	-	-	-	-	1	1	0	Ground (0) to channel 2
-	-	-	-	-	1	1	1	Reserved
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	1	1	1	0	1	1	1	Reserved
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	1	1	1	0	0	1	0	Reserved

Note: Italic is default.

Pwm Output Mux Register (0x25)

This DAP output mux selects which internal PWM channel is output to the external pins. Any channel can be output to any external output pin.

Bits D21-D20: Selects which PWM channel is output to OUT_A

Bits D17-D16: Selects which PWM channel is output to OUT_B

Bits D13-D12: Selects which PWM channel is output to OUT_C

Bits D09-D08: Selects which PWM channel is output to OUT_D

Note that channels are enclosed so that channel 1=0x00, channel 2=0x01, $\overline{\text{channel 1}}$=0x02, and $\overline{\text{channel 2}}$=0x03.

Table 15. PWM Output Mux Register (0x25)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	0	0	0	0	0	0	0	Reserved
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	0	-	-	-	-	-	-	Reserved
-	-	0	0	-	-	-	-	Multiplex channel 1 to OUT_A
-	-	0	1	-	-	-	-	Multiplex channel 2 to OUT_A
-	-	1	0	-	-	-	-	Multiplex $\overline{\text{channel 1}}$ to OUT_A
-	-	1	1	-	-	-	-	Multiplex $\overline{\text{channel 2}}$ to OUT_A
-	-	-	-	0	0	-	-	Reserved
-	-	-	-	-	-	0	0	Multiplex channel 1 to OUT_B
-	-	-	-	-	-	0	1	Multiplex channel 2 to OUT_B
-	-	-	-	-	-	1	0	Multiplex $\overline{\text{channel 1}}$ to OUT_B

Function Description (Cont.)

Pwm Output Mux Register (0x25) (Cont.)

Table 15. PWM Output Mux Register (0x25)

D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
-	-	-	-	-	-	1	1	Multiplex $\overline{\text{channel 2}}$ to OUT_B
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	0	-	-	-	-	-	-	Reserved
-	-	0	0	-	-	-	-	Multiplex channel 1 to OUT_C
-	-	0	1	-	-	-	-	Multiplex channel 2 to OUT_C
-	-	1	0	-	-	-	-	Multiplex $\overline{\text{channel 1}}$ to OUT_C
-	-	1	1	-	-	-	-	Multiplex $\overline{\text{channel 2}}$ to OUT_C
-	-	-	-	0	0	-	-	Reserved
-	-	-	-	-	-	0	0	Multiplex channel 1 to OUT_D
-	-	-	-	-	-	0	1	Multiplex channel 2 to OUT_D
-	-	-	-	-	-	1	0	Multiplex $\overline{\text{channel 1}}$ to OUT_D
-	-	-	-	-	-	1	1	Multiplex $\overline{\text{channel 2}}$ to OUT_D
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	1	0	0	0	1	0	1	Reserved

Note: Italic is default.

DRC Control (0x46)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	0	0	0	0	0	0	0	Reserved
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	0	0	0	0	0	0	0	Reserved
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	0	0	0	0	0	0	0	Reserved
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
-	-	-	-	-	-	-	0	DRC turned OFF
-	-	-	-	-	-	-	1	DRC turned ON
0	0	0	0	0	0	0	-	Reserved

Note: Italic is default.

Function Description (Cont.)

Error Reporting

Any fault resulting in device shutdown is signaled by the $\overline{\text{ERROR}}$ pin going low (see Table 18). A sticky version of this pin is available on D1 of register 0X02.

Table 16. $\overline{\text{ERROR}}$ Output States

Fault Description	Error
0	Over-Current (OC) or Under-Voltage (UVP) or Over-Temperature (OTP)
1	No faults (normal operation)

Over-Current (OC) Protection With Current-Limiting

The device has independent, fast-reacting current detectors on all high-side and low-side power-stage FETs. The detector outputs are closely monitored by two protection systems. The first protection system controls the power stage in order to prevent the output current further increasing, i.e., it performs a cycle-by-cycle current-limiting function, rather than prematurely shutting down during combinations of high-level music transients and extreme speaker load impedance drops. If the high-current condition situation persists, i.e., the power stage is being overloaded, a second protection system triggers a latching shutdown, resulting in the power stage being set in the high-impedance (Hi-Z) state. The device returns to normal operation once the fault condition (i.e., a short circuit on the output) is removed. Current limiting and overcurrent protection are not independent for half-bridges.
That is, if the bridge-tied load between half-bridges A and B causes an overcurrent fault, half-bridges A, B, C, and D are shut down.

Over-Temperature Protection

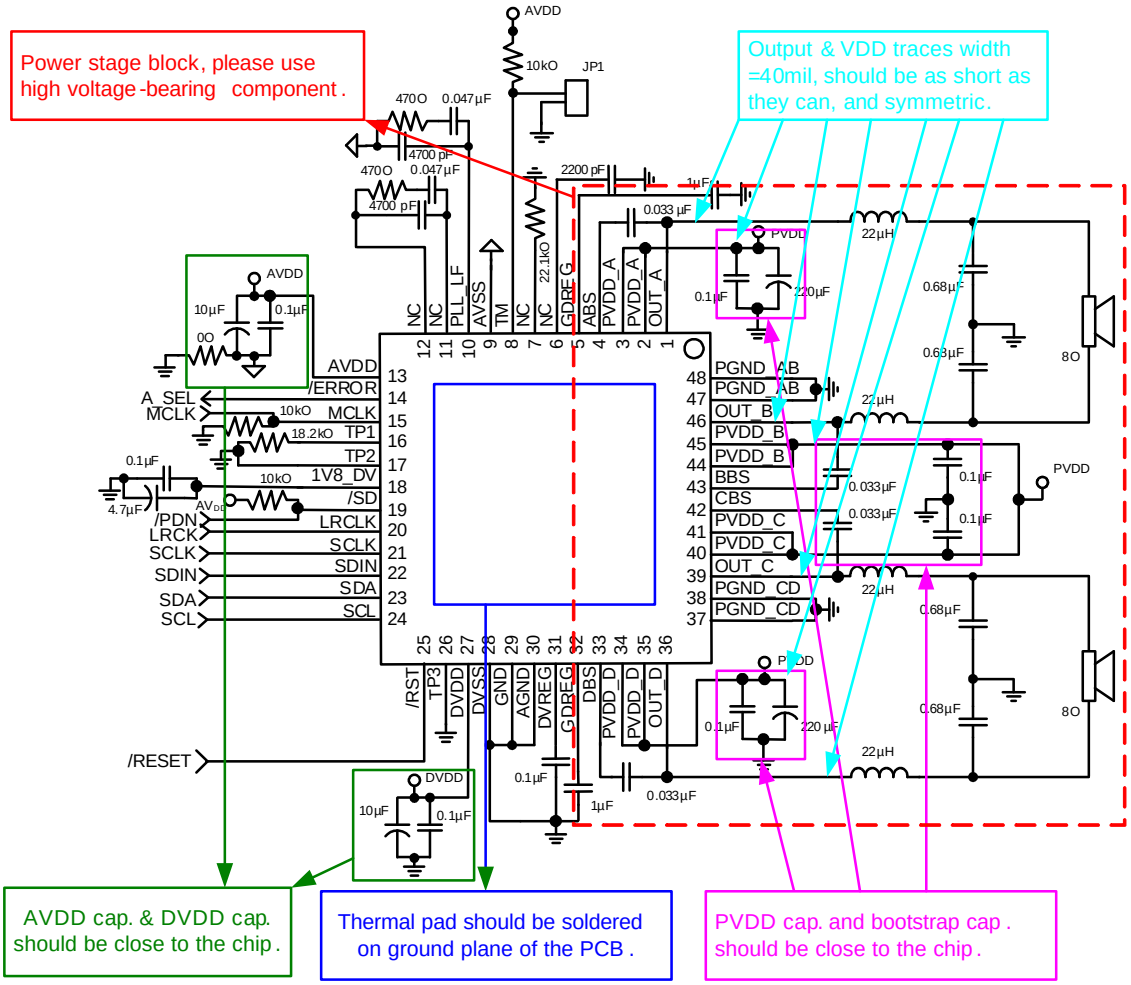
The APA3163A has over-temperatureprotection system. If the device junction temperature exceeds 150°C (nominal), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and FAULT being asserted low. The APA3163A recovers automatically once the temperature drops approximately 30°.

Under-Voltage Protection (UVP) and Power-On-Reset (POR)

The UVP and POR circuits of the APA3163A fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overload circuit (OLP) and ensures that all circuits are fully operational when the PVDD and AVDD supply voltages reach 7.6V and 2.7V, respectively. Although PVDD and AVDD are independently monitored, a supply voltage drop below the UVP threshold on AVDD or either PVDD pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and $\overline{\text{ERROR}}$ being asserted low.

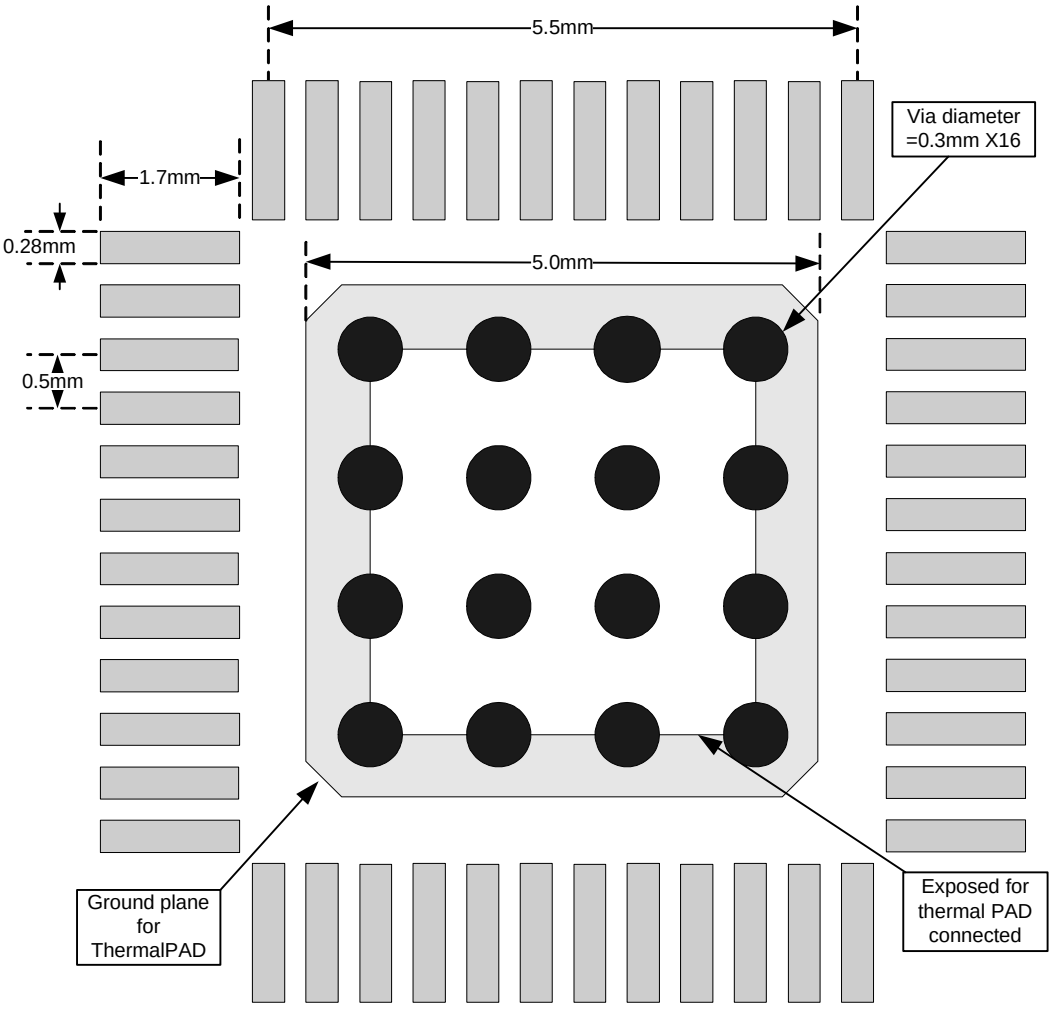
Application Information

Layout Recommendation



Application Information(Cont.)

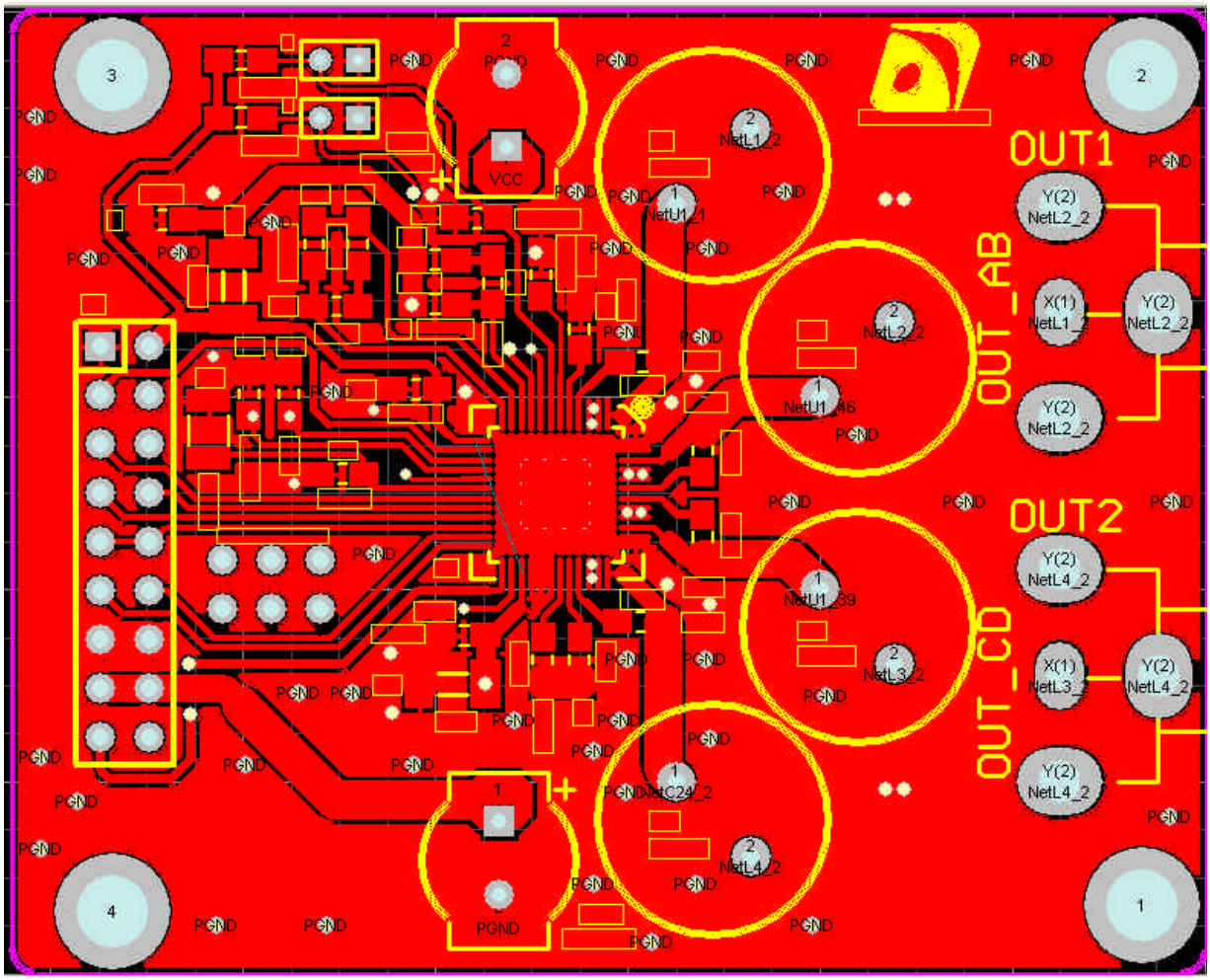
Layout Recommendation



TQFP7X7-48 Land Pattern Recommendation

Application Information(Cont.)

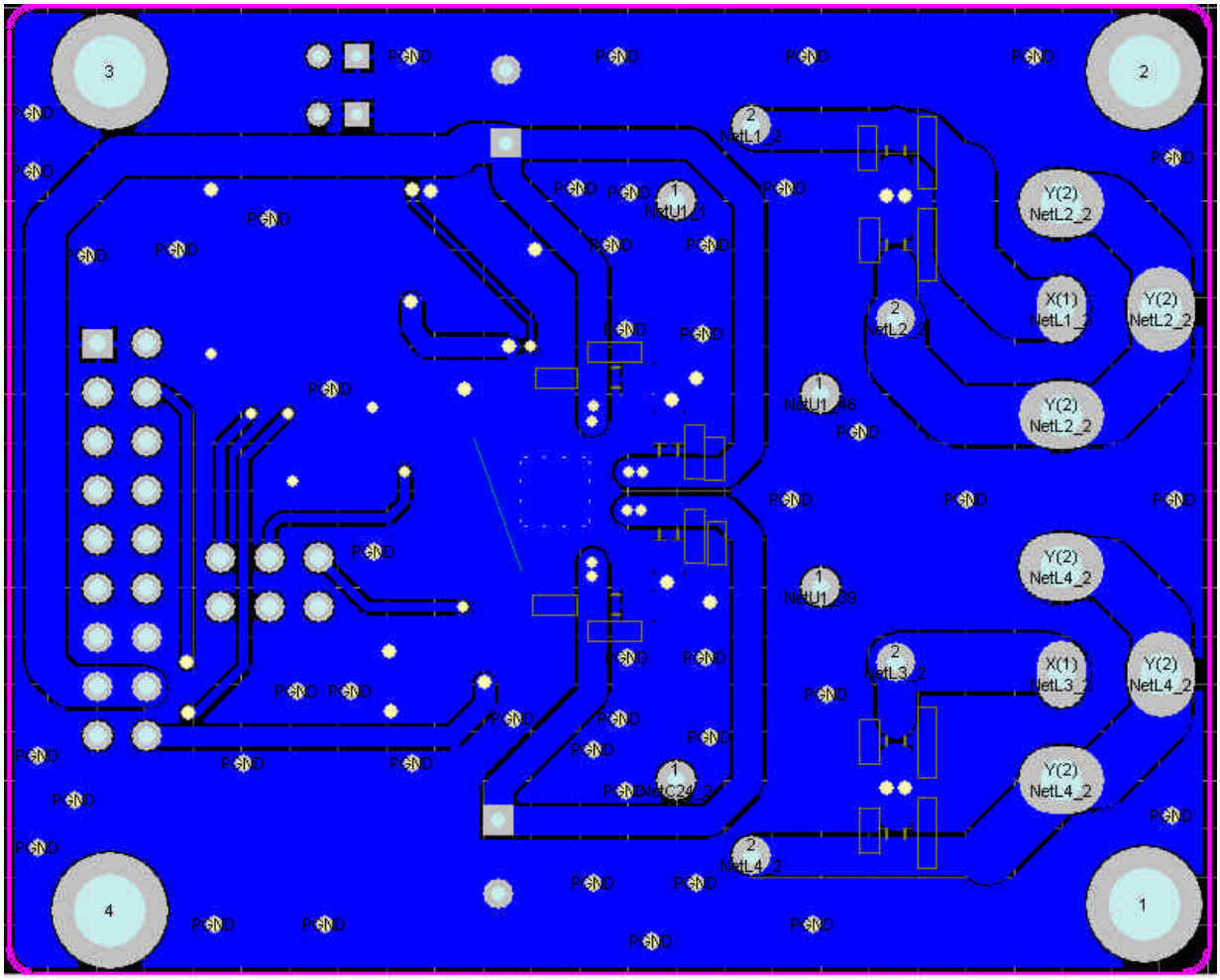
Layout Recommendation



PCB Referance (Top Layer)

Application Information(Cont.)

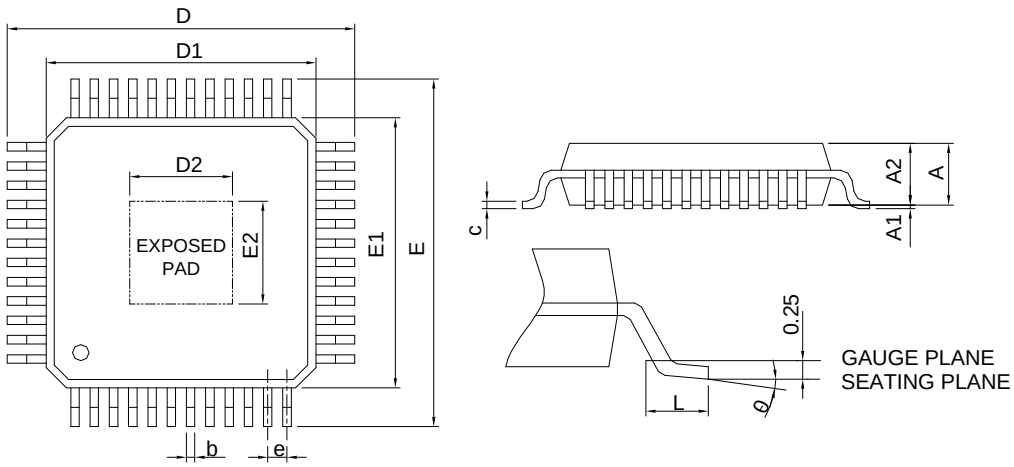
Layout Recommendation



PCB Referance (Bottom Layer)

Package Information

TQFP7x7-48P



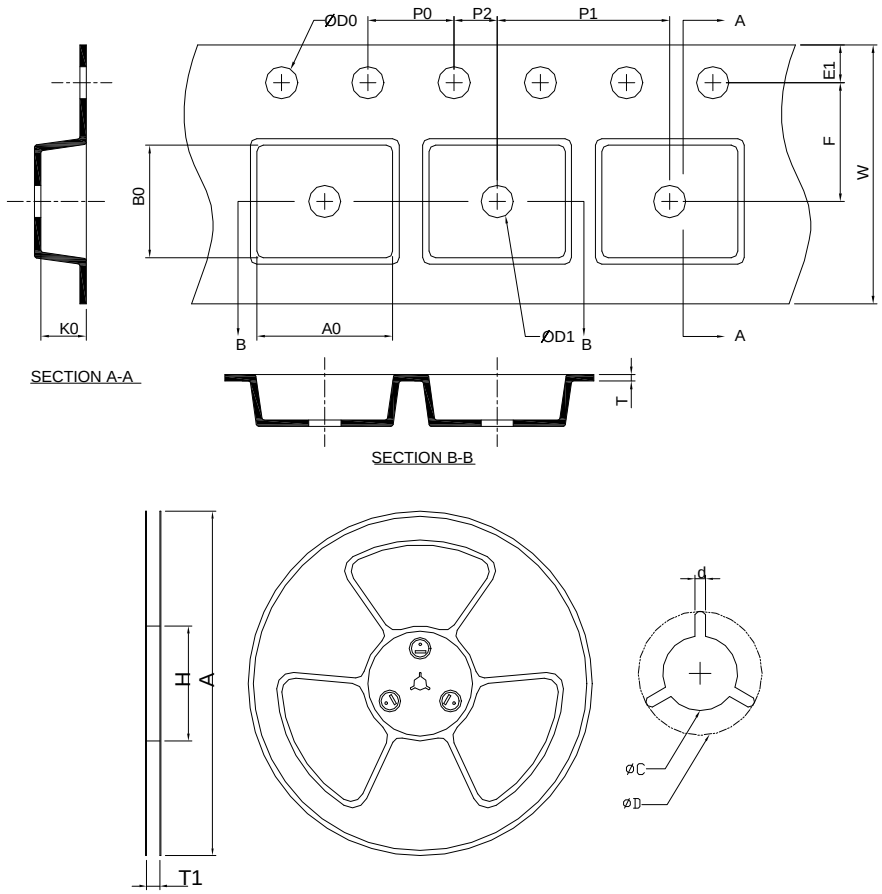
SYMBOL	TQFP7x7-48P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.20		0.047
A1	0.05	0.15	0.002	0.006
A2	0.95	1.05	0.037	0.041
b	0.17	0.27	0.007	0.011
c	0.09	0.20	0.004	0.008
D	8.80	9.20	0.346	0.362
D1	6.90	7.10	0.272	0.280
D2	3.00	5.50	0.118	0.217
E	8.80	9.20	0.346	0.362
E1	6.90	7.10	0.272	0.280
E2	3.00	5.50	0.118	0.217
e	0.50 BSC		0.020 BSC	
L	0.45	0.75	0.018	0.030
	0^o	7^o	0^o	7^o

Note : 1. Followed from JEDEC MS-026 ABC.

2. Dimension "D1" and "E1" do not include mold protrusions. Allowable protrusions is 0.25 mm per side. "D1" and "E1" are maximun plasticbody size dimensions including mold mismatch.

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Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFP7x7-48P	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	12.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	9.4±0.20	9.4±0.20	1.4±0.20

(mm)

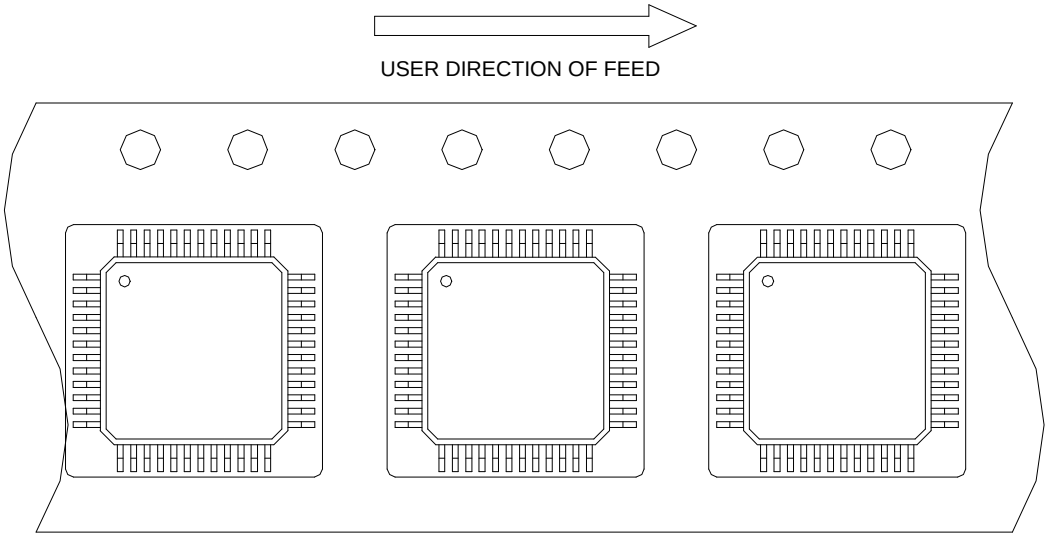
Devices Per Unit

Package Type	Unit	Quantity
TQFP7x7-48P	Tape & Reel	2500

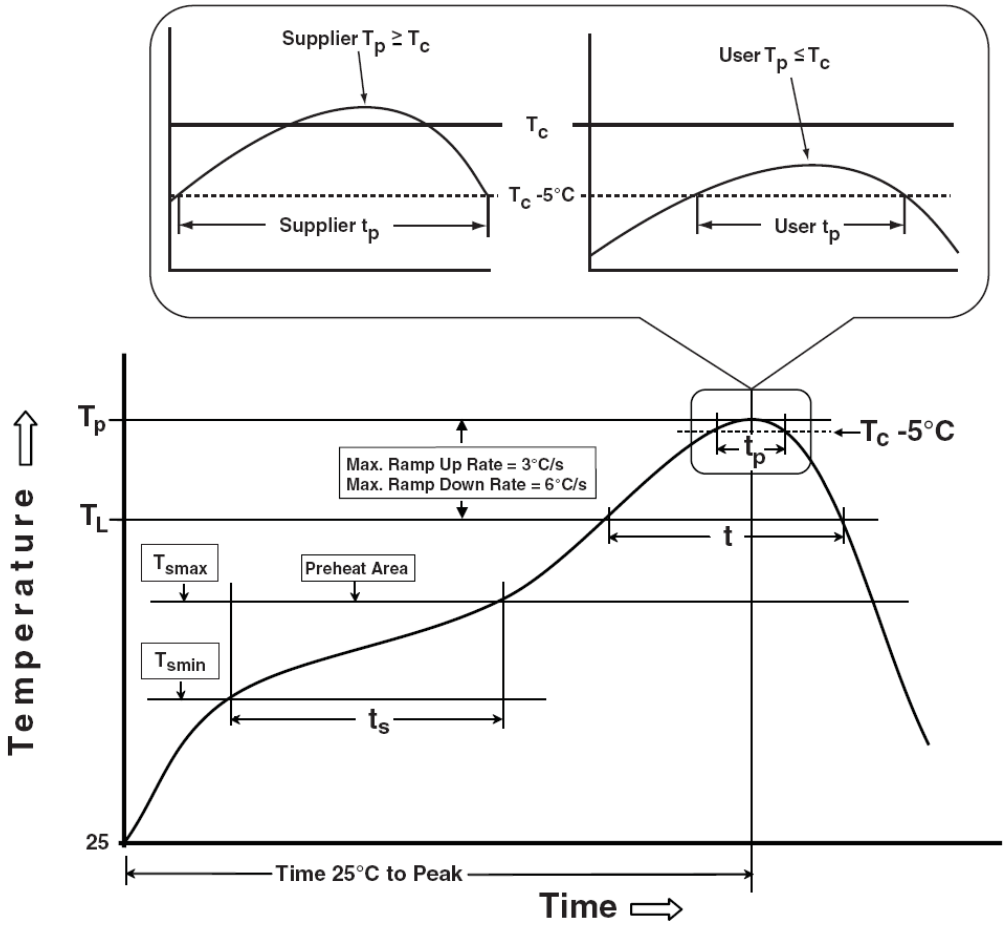
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Taping Direction Information

TQFP7x7-48P



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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Customer Service

Anpec Electronics Corp.
Head Office :
No.6, Dusing 1st Road, SBIP,
Hsin-Chu, Taiwan
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,
Sindian City, Taipei County 23146, Taiwan
Tel : 886-2-2910-3838
Fax : 886-2-2917-3838