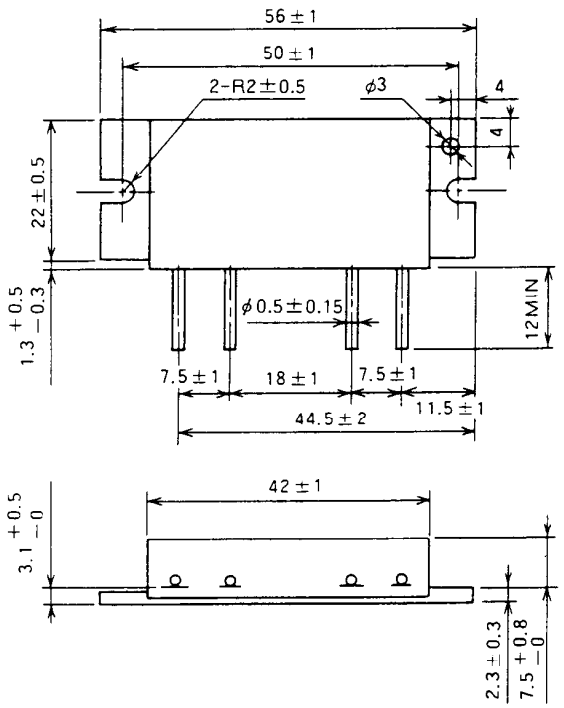
M57747

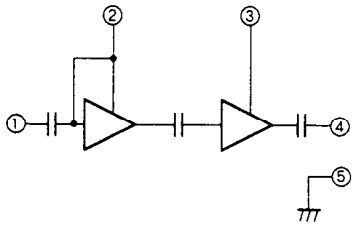
144-148MHz, 12.5V, 13W, FM MOBILE RADIO

OUTLINE DRAWING Dimensions in mm



H6

BLOCK DIAGRAM



PINNING :
①Pin : RF INPUT
②Vcc1 : 1st. DC SUPPLY
③Vcc2 : FINAL DC SUPPLY
④Po : RF OUTPUT
⑤GND : FIN

ABSOLUTE MAXIMUM RATINGS (Tc = 25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		17	V
Icc	Total current		5	A
Pin(max)	Input power	Vcc1 ≦ 12.5V, ZG = ZL = 50 Ω	0.4	W
Po(max)	Output power	Same as above	20	W
Tc(OP)	Operation case temperature	Same as above	− 30 to 110	℃
Tstg	Storage temperature		− 40 to 110	℃

Note. Above parameters are guaranteed independently.

ELECTRICAL CHARACTERISTICS (Tc = 25℃ unless otherwise noted)

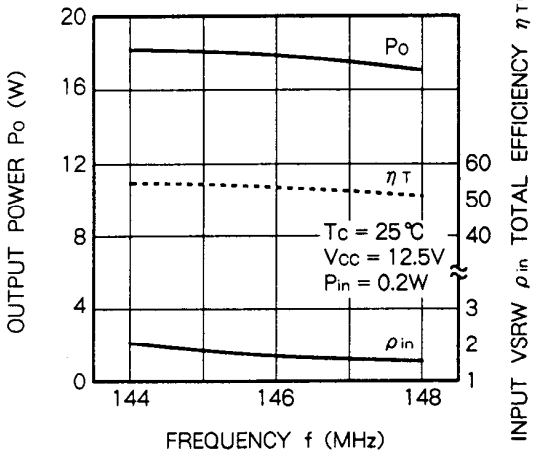
Symbol	Parameter	Test conditions	Limits		Unit
			Min	Max	
f	Frequency range	Pin = 0.2W Vcc = 12.5V ZG = ZL = 50 Ω	144	148	MHz
Po	Output power		13		W
ηT	Total efficiency		48		%
2fo	2nd. harmonic			− 25	dBc
3fo	3rd. harmonic			− 35	dBc
ρin	Input VSWR			2.8	−
−	Load VSWR tolerance	Vcc = 15.2V Po = 14W (Pin : controlled) ρL = 20 : 1 (All phase) ZG = 50 Ω	No degradation or destroy		−

Note. Above parameters, ratings, limits and conditions are subject to change.

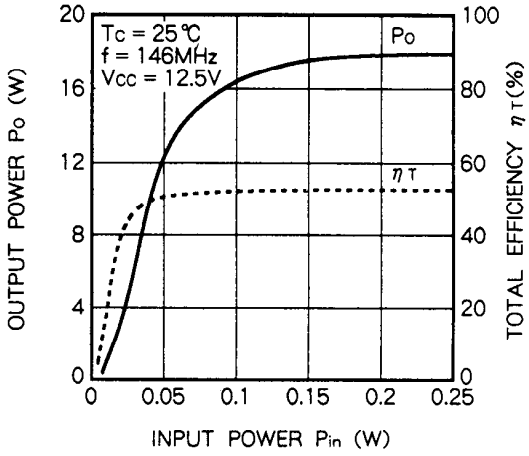
MITSUBISHI ELECTRIC

TYPICAL PERFORMANCE DATA

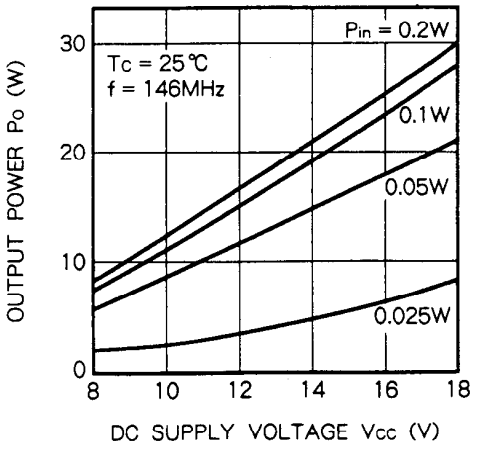
OUTPUT POWER, TOTAL EFFICIENCY, INPUT VSWR VS. FREQUENCY



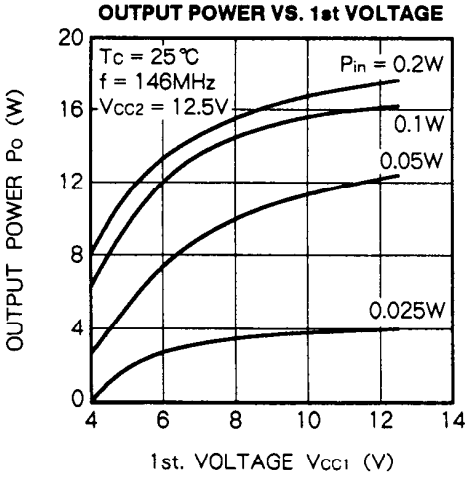
OUTPUT POWER, TOTAL EFFICIENCY, VS. INPUT POWER



OUTPUT POWER VS. DC SUPPLY VOLTAGE



OUTPUT POWER VS. 1st VOLTAGE



DESIGN CONSIDERATION OF HEAT RADIATION

Please refer to following consideration when designing heat sink.

1. Junction temperature of incorporated transistors at standard operation.

(1) Thermal resistance between junction and package of incorporated transistors.

a) First stage transistor

$R_{th(j-c)1}$ = 10℃/W(Typ.)

b) Final stage transistor

$R_{th(j-c)2}$ = 3℃/W(Typ.)

(2) Junction temperature of incorporated transistors at standard operation.

- Conditions for standard operation.

  P_O = 13W, V_{CC} = 12.5V, P_{in} = 0.2W, ηT = 48 % (minimum rating). P_{O1} (Note1) = 2.5W, I_T = 2.2A(I_{T1} (2) = 0.45A, I_{T2} (3) = 1.75A)

  Note1 : Output power of the first stage transistor

  Note2 : Circuit current of the first stage transistor

  Note3 : Circuit current of the first stage transistor

- Junction temperature of the first stage transistor

  $T_{j1} = (V_{CC} \times I_{T1} - P_{O1} + P_{in}) \times R_{th(j-c)1} + T_C$ (4)

  $= (12.5 \times 0.45 - 2.5 + 0.2) \times 10 + T_C$

  $= 33 + T_C$(℃)

  Note4 : Package temperature of device

- Junction temperature of the final stage transistor

  $T_{j2} = (V_{CC} \times I_{T2} - P_O + P_{O1}) \times R_{th(j-c)2} + T_C$

  $= (12.5 \times 1.75 - 13 + 2.5) \times 3 + T_C$

  $= 34 + T_C$(℃)

2. Heat sink design

In thermal design of heat sink, try to keep the package temperature at the upper limit of the operating ambinet temperature (normally Ta = 60℃) and at the output power of 13W below 90℃.

The thermal resistance $R_{th(c-a)}$ (5) of the heat sink to realize this :

$$R_{th(c-a)} = \frac{T_c - T_a}{(P_O/\eta T) - P_O + P_{in}} = \frac{90 - 60}{(13/0.48) - 13 + 0.2}$$

$$= 2.8(℃/W)$$

Note5 : Inclusive of the contact thermal resistance between device and heat sink

Mounting the heat sink of the above thermal resistance on the device,

T_{j1} = 113℃, T_{j2} = 134℃ at T_a = 60℃, T_c = 90℃,

In the annual average of ambient temperature is 30℃,

T_{j1} = 103℃, T_{j2} = 104℃

As the maximum junction temperature of these incorporated transistors T_{jmax} are 175℃, application under fully derated condition is ensured.