Structure Silicon monolithic Integrated circuit
Product Clock Generator

Type **BU3073HFV**

Feature
To generate clocks for digital still camera VIDEO
To generate clocks by connecting reference clock
SELECT pin allowing for the selection of 24.545454MHz or 24.375000MHz
Selection of PD pin enabling Power-Down function

○Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.5 ～ 4.1	V
Input Voltage	VIN	-0.5 ～ VDD+0.5	V
Storage Temperature range	Tstg	-30 ～ 125	℃
Power dissipation	PD	410 ※1	mW

※1 A measure value at mounting on 50×50×1.6mm glass epoxy substrate.
In the case of exceeding Ta=25℃, 4.1mW should be reduced per 1℃.
※ The radiation-resistance design is not carried out.
※ Operation is not guaranteed.

○Operating Conditions (Ta=-5℃~+70℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	VDD	3.0	3.3	3.6	V
Input "H" Voltage	VIH	0.8VDD	-	VDD	V
Input "L" Voltage	VIL	0.0	-	0.2VDD	V
Output load	CL	0	-	15	pF

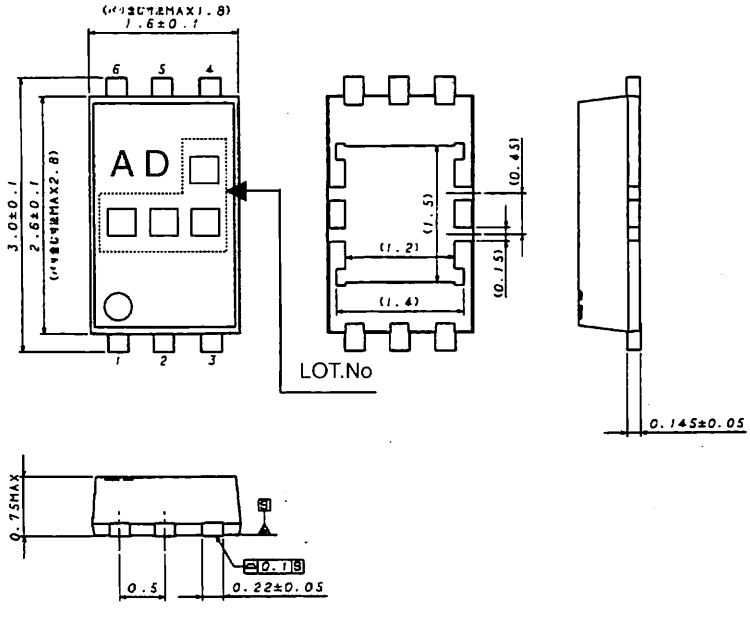
Application example
- ROHM cannot provide adequate confirmation of patents.
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○ Electrical Characteristics

(VDD=3.3V,Ta=25℃,Crystal frequency=48.0000MHz,at No Load ,unless otherwise specified)

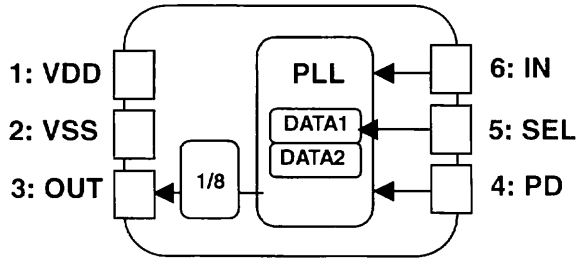
Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Output H voltage	VOH	2.8	–	–	V	IOH=-4.0mA
Output L voltage	VOL	–	–	0.5	V	IOL=4.0mA
Consumption current1	IDD1	–	11	16	mA	OE=H、at No Load
Consumption current2	IDD2	–	–	5	μA	OE=L
Output frequency	CLK_375	–	24.375000	–	MHz	SEL=L、IN*65/16/8
	CLK_545	–	24.545454		MHz	SEL=H、IN*45/11/8
The follow parameters are design guaranteed performance.						
Duty	Duty	45	50	55	%	Measured at a voltage of 1/2VDD
Rise time	tr	–	2.5	–	nsec	Period of transition time required for the output to reach 80% from 20% of VDD.
Fall time	tf	–	2.5	–	nsec	Period of transition time required for the output to reach 20% from 80% of VDD.
Period Jitter 1 σ	PJsSD	–	45	–	psec	1sigma of short Jitter
Long-Term Jitter MIN-MAX	LTJsABS	–	0.9	1.5	nsec	MIN-MAX of long-term jitter (100 μsec from trigger)
Output Lock time	tLOCK	–	–	1	msec	

○Package outline, Appearance of Marker



HVSOF-6 (Unit:mm)

○Block diagram, pin function



PIN No.	PIN NAME	Function
1	VDD	Power supply
2	VSS	GND
3	OUT	Clock output terminal (L : 24.375000MHz, H : 24.545454MHz)
4	PD	power down (L : disable, H : enable) Equipment with pull-down function, output fixed to L at disable
5	SEL	Output selector (L : 24.375000MHz, H : 24.545454MHz)
6	IN	Clock input pin (48.0000MHz input)

●Cautions on use (BU3073HFV)

Basically, mount ICs to the printed circuit board for use. (If the ICs are not mounted to the printed circuit board, the characteristics of ICs may not be fully demonstrated.)

Mount 0.1μF capacitors in the vicinity of the IC PINs between 1PIN (VDD) and 2PIN (VSS), respectively.

Depending on the conditions of the printed circuit board, mount an additional electrolytic capacitor between the power supply and GND terminal.

For EMI protection, it is effective to put ferrite beads in the origin of power supply to be fed to BU3073HFV from the printed circuit board or to insert a capacitor (of 1Ω or less), which bypasses high frequency desired, between the power supply and the GND terminal.

●Cautions on use(common)

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

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