# SENSOR SIGNAL CONDITIONING IC FOR CLOSED-LOOP MAGNETIC CURRENT SENSOR

## FEATURES

- **Designed For Sensors From VACUUMSCHMELZE (VAC)**
- **Single Supply: 5 V**
- **Power Output: H-Bridge**
- **Designed For Driving Inductive Loads**
- **Excellent DC Precision**
- **Wide System Bandwidth**
- **High-Resolution, Low-Temperature Drift**
- **Built-In Degauss System**
- **Extensive Fault Detection**
- **External High-Power Driver Option**

## APPLICATIONS

- **Generator/Alternator Monitoring and Control**
- **Frequency and Voltage Inverters**
- **Motor Drive Controllers**
- **System Power Consumption**
- **Photovoltaic Systems**

## SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(1) Custom temperature ranges available

## DESCRIPTION/ORDERING INFORMATION

The DRV401 is designed to control and process signals from specific magnetic current sensors made by VACUUMSCHMELZE GmbH & Co. KG (VAC). A variety of current ranges and mechanical configurations are available. Combined with a VAC sensor, the DRV401 monitors both ac and dc currents to high accuracy.

Provided functions include: probe excitation, signal conditioning of the probe signal, signal loop amplifier, an H-bridge driver for the compensation coil, and an analog signal output stage that provides an output voltage proportional to the primary current. It offers overload and fault detection, as well as transient noise suppression.

The DRV401 can directly drive the compensation coil or connect to external power drivers. Therefore, the DRV401 combines with sensors to measure small to very large currents.

To maintain the highest accuracy, the DRV401 can demagnetize (degauss) the sensor at power-up and on demand.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

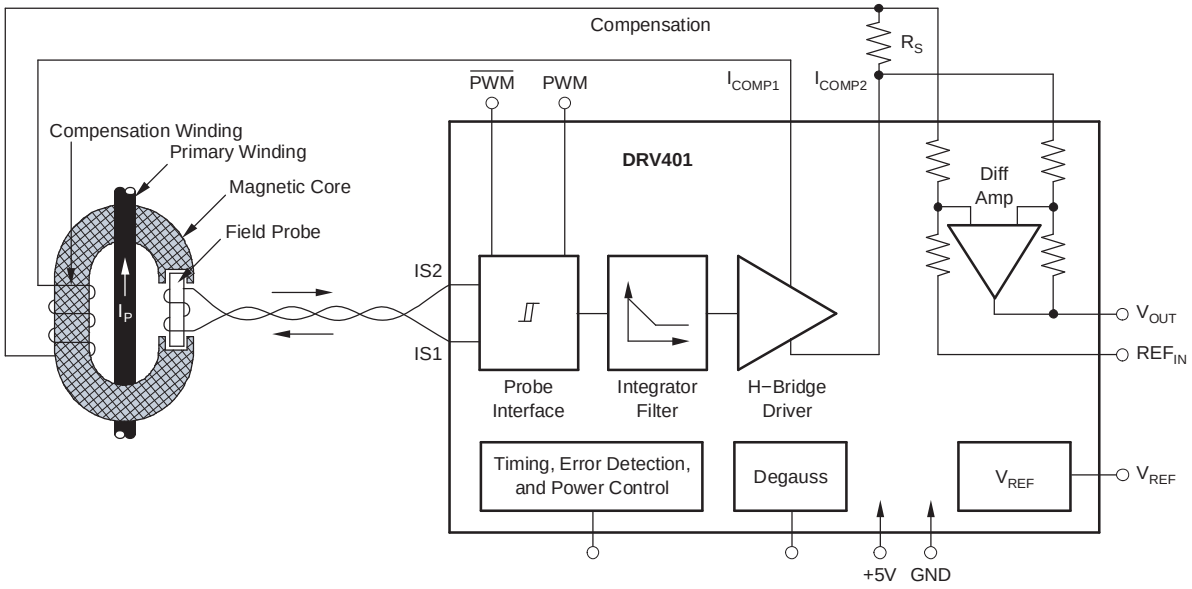
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION(1)

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR(2) | PACKAGE MARKING |
|---|---|---|---|
| DRV401 | SO-20 | DWP | DRV401M |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**Patents Pending.**




## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage | | | | +7 | V |
| Signal Input terminals: | Voltage(2) | | –0.5 | $V_{DD}$ + 0.5 | V |
| | Differential amplifier(3) | | –10 | +10 | V |
| | Current at IS1 and IS2 | | | ±75 | mA |
| | Current (pins other than IS1 and IS2)(2) | | | ±25 | mA |
| $I_{COMP}$ short circuit(4) | | | | +250 | mA |
| Operating junction temperature | | | –55 | +150 | °C |
| Storage temperature | | | –55 | +150 | °C |
| ESD rating | Human body model (HBM) | Pins $IA_{IN1}$ and $IA_{IN2}$ only | | 1 | kV |
| | | All other pins | | 4 | kV |

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited, except for the differential amplifier input pins.
(3) These inputs are not internally protected against over voltage. The differential amplifier input pins must be limited to 5 mA, max or ±10 V, max.
(4) Power-limited; observe maximum junction temperature.


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## ELECTRICAL CHARACTERISTICS[1]

**Boldface** limits apply over the specified temperature range: $T_J$ = –55°C to +125°C.
At $T_A$ = +25°C and $V_{DD1}$ = $V_{DD2}$ = +5 V with external 100 kHz filter BW, and zero output current $I_{COMP}$, unless otherwise noted.

| PARAMETER | | CONDITIONS | DRV401 | | | UNITS |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **DIFFERENTIAL AMPLIFIER** | | $R_L$ = 10 kΩ to 2.5 V, $V_{REFIN}$ = 2.5 V | | | | |
| **OFFSET VOLTAGE** | | | | | | |
| $V_{OS}$ | Offset voltage, RTO[2][3] | Gain 4 V/V | | ±0.01 | ±0.1 | mV |
| **$dV_{OS}/dT$** | **Drift, RTO** [3] | | | **±0.1** | | **µV/°C** |
| **$V_{OS}$** | **Offset voltage, RTO[2][3]** | Gain 4 V/V | | | **±0.17** | **mV** |
| CMRR | vs common-mode, RTO | –1 V to +6 V, $V_{REF}$ = 2.5 V | | ±50 | ±280 | µV/V |
| PSRR | vs power-supply, RTO | $V_{REF}$ not included | | ±4 | ±50 | µV/V |
| **SIGNAL INPUT** | | | | | | |
| | Common-mode voltage range | | –1 | | ($V_{DD}$) + 1 | V |
| **SIGNAL OUTPUT** | | | | | | |
| | **Signal over-range indication (OVER-RANGE), Delay** [3] | **$V_{IN}$ = 1 V step**[3] [4] | | **2.5 to 3.5** | | **µs** |
| | Voltage output swing from negative rail[3], OVER-RANGE trip level | I = +2.5 mA, CMP trip level | | +48 | +85 | mV |
| | Voltage putput swing from positive rail[3], OVER-RANGE trip level | I = –2.5 mA, CMP trip level | $V_{DD}$ – 85 | $V_{DD}$ – 48 | | mV |
| $I_{SC}$ | Short-circuit current[3] | $V_{OUT}$ connected to GND | | –18 | | mA |
| | | $V_{OUT}$ connected to $V_{DD}$ | | +20 | | mA |
| | **Gain, $V_{OUT}/V_{IN_DIFF}$** | | | **4** | | **V/V** |
| | Gain error | | | ±0.02 | = 0.3 | % |
| | **Gain error drift** | | | **±0.1** | | **ppm/°C** |
| | Linearity error | $R_L$ = 1 kΩ | | 10 | | ppm |

(1) For Electromigration derating curves, please refer to http://focus.ti.com/pdfs/hirel/mltry/EP_Reliability_Information.pdf.
(2) Parameter value referred to output (RTO).
(3) See Typical Characteristics curves.
(4) Total input resistance and comparator threshold current are inversely related. See Figure 2a.

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## ELECTRICAL CHARACTERISTICS (continued)

**Boldface** limits apply over the specified temperature range: $T_J$ = –55°C to +125°C.
At $T_A$ = +25°C and $V_{DD1}$ = $V_{DD2}$ = +5 V with external 100 kHz filter BW, and zero output current $I_{COMP}$, unless otherwise noted.

| PARAMETER | | CONDITIONS | DRV401 | | | UNITS |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **FREQUENCY RESPONSE** | | | | | | |
| $BW_{-3dB}$ | Bandwidth(5) | | | 2 | | MHz |
| SR | Slew rate(5) | CMVR = –1 V to = +4 V | | 6.5 | | V/µs |
| | Settling time, large-signal(5) | dV ± 2 V to 1%, No external filter | | 0.9 | | µs |
| | Settling time(5) | dV ± 0.4 V to 0.01% | | 14 | | µs |
| **INPUT RESISTANCE** | | | | | | |
| | Differential | | 16.5 | 20 | 23.5 | kΩ |
| | Common-mode | | 41 | 50 | 59 | kΩ |
| | External reference input | | 41 | 50 | 59 | kΩ |
| **NOISE** | | | | | | |
| $e_n$ | Output voltage noise density, f = 1 kHz, RTO(5) | Compensation loop disabled | | 170 | | nV/√Hz |
| **COMPENSATION LOOP** | | | | | | |
| | **DC STABILITY** | Probe f = 250 kHz, $R_{LOAD}$ = 20 Ω | | | | |
| | Offset error(6) | Deviation from 50% PWM, Pin gain = L | | 0.03 | | % |
| | **Offset error drift(5)** | **Deviation from 50% PWM, Pin gain = L** | | **7.5** | | **ppm/°C** |
| | Gain, pin gain = L(5) | $\lvert V_{ICOMP1}\rvert - \lvert V_{ICOMP2}\rvert$ | –200 | 25 | 200 | ppm/V |
| PSRR | Power-supply rejection ratio | Probe loop f = 250 kHz | | 500 | | ppm/V |
| **FREQUENCY RESPONSE** | | | | | | |
| | Open-loop gain, two modes, 7.8 kHz | Pin gain H/L | | 24/32 | | dB |
| **PROBE COIL LOOP** | | | | | | |
| | Input voltage clamp range | Field probe current < 50 mA | –0.7 | –0.7 to $V_{DD}$ | | V |
| | Internal resistor, IS1 or IS2 to $V_{DD1}$(5) | | 47 | 59 | 71 | Ω |
| $R_{HIGH}$ | Internal resistor, IS1 or IS2 to GND1(5) | | 60 | 75 | 90 | Ω |
| $R_{LOW}$ | Resistance mismatch between IS1 and IS2(5) | ppm of $R_{HIGH}$ + $R_{LOW}$ | | 300 | 1500 | ppm |
| | **Total input resistance(7)** | | | **134** | **200** | **Ω** |
| | Comparator threshold current(7) | | 22 | 28 | 34 | mA |
| | Minimum probe loop half-cycle(5) | | 250 | 280 | 310 | ns |
| | Probe loop minimum frequency | | 250 | | | kHz |
| | No oscillation detect (error) suppression | | | 35 | | µs |
| **COMPENSATION COIL DRIVER, H-BRIDGE** | | | | | | |
| | **Peak current(5)** | **$V_{ICOMP1}$ – $V_{ICOMP2}$ = 4.0$V_{PP}$** | | **250** | | **mA** |
| | Voltage swing | 20 Ω load | 4.2 | | | $V_{PP}$ |
| | Output common-mode voltage | | | $V_{DD2}$/2 | | V |
| | Wire break detect, threshold current(8) | $I_{COMP1}$ and $I_{COMP2}$ railed | | 33 | 57 | mA |
| **VOLTAGE REFERENCE** | | | | | | |
| | Voltage(5) | No load | 2.495 | 2.5 | 2.505 | V |
| | **Drift(5)** | **No load** | | **±5** | | **ppm/°C** |

(5) See Typical Characteristics curves.
(6) For VAC sensors, 0.2% of PWM offset approximately corresponds to 10 mA primary current offset per winding.
(7) Total input resistance and comparator threshold current are inversely related. See Figure 2a.
(8) See *Compensation Driver* section in Applications Information.


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## ELECTRICAL CHARACTERISTICS (continued)

**Boldface** limits apply over the specified temperature range: $T_J$ = –55°C to +125°C.
At $T_A$ = +25°C and $V_{DD1}$ = $V_{DD2}$ = +5 V with external 100 kHz filter BW, and zero output current $I_{COMP}$, unless otherwise noted.

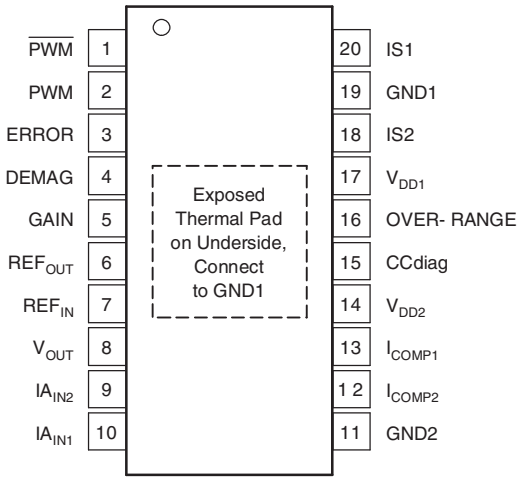
| PARAMETER | | CONDITIONS | DRV401 | | | UNITS |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| | Drift[5] | **No load** | **2.491** | | **2.509** | **V** |
| | PSRR[5] | | | ±15 | ±200 | µV/V |
| | Load regulation[5] | Load to GND/$V_{DD}$, dI = 0 mA to 5 mA | | 0.15 | | mV/mA |
| $I_{SC}$ | Short-circuit current | $REF_{OUT}$ connected to $V_{DD}$ | | +20 | | mA |
| | | $REF_{OUT}$ connected to GND | | –18 | | mA |
| **DEMAGNETIZATION** | | | | | | |
| | **Duration** | **See Timing Diagram** | | **106** | **130[7]** | **ms** |
| **DIGITAL I/O** | | | | | | |
| | **LOGIC INPUTS (DEMAG, GAIN, and CCdiag Pins)** | **CMOS Type Levels** | | | | |
| | Pull-up high current (CCdiag) | $3.5 < V_{IN} < V_{DD}$ | | 160 | | µA |
| | Pull-up low current (CCdiag) | $0 < V_{IN} < 1.5$ | | 5 | | µA |
| | Logic input leakage current | $0 < V_{IN} < V_{DD}$ | | 0.01 | 5 | µA |
| | Logic level, input: L/H | | | 2.1/2.8 | | V |
| | Hysteresis | | | 0.7 | | V |
| | **OUTPUTS (ERROR AND OVER-RANGE Pins)** | | | | | |
| | Logic level, output: L | 4 mA sink | | 0.3 | | V |
| | Logic level, output: H | | | No Internal Pull-Up | | |
| | **OUTPUTS (PWM and $\overline{PWM}$ Pins)** | Push-pull type | | | | |
| | Logic level L | 4 mA sink | | 0.2 | | V |
| | Logic level H | 4 mA source | | ($V_{DD}$) – 0.4 | | V |
| **POWER SUPPLY** | | | | | | |
| **$V_{DD}$** | **Specified voltage range** | | **4.5** | **5** | **5.5** | **V** |
| $V_{RST}$ | Power-on reset threshold | | | 1.8 | | V |
| $I_Q$ | Quiescent current [I($V_{DD1}$) + I($V_{DD2}$)] | $I_{COMP}$ = 0 mA, Sensor not connected | | | 6.8 | mA |
| | Brownout voltage level[9] | | | 5 | | V |
| | Brownout indication delay | | | 135 | | µs |
| **TEMPERATURE RANGE** | | | | | | |
| $T_J$ | Specified range | | –40 | | +125 | °C |
| $T_J$ | Operating range | | –50 | | +150 | °C |
| $\theta_{JA}$ | Package thermal resistance | SO PowerPAD surface-mount[10] | | 27 | | °C/W |

(9) See Typical Characteristics curves.
(10) See *Applications Information* section for information on power dissipation, layout considerations, and proper PCB soldering and heat-sinking technique.

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## PIN CONFIGURATIONS

**Top View** **DWP**




Wide- Body SO- 20

## PIN ASSIGNMENTS

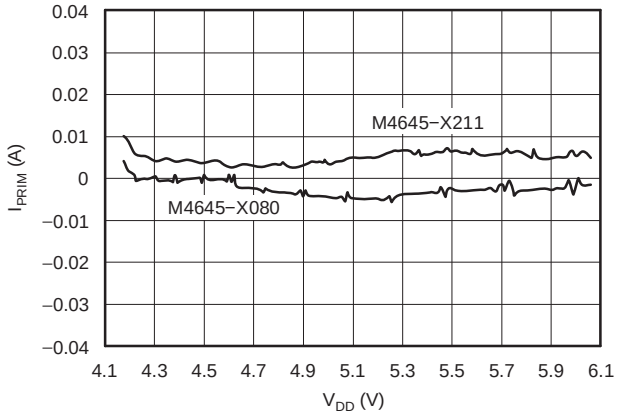
| TERMINAL | | DESCRIPTION |
|---|---|---|
| NAME | NO. | |
| $\overline{PWM}$ | 1 | PWM output from probe circuit (inverted). |
| PWM | 2 | PWM output from probe circuit. |
| ERROR | 3 | Error flag: open-drain output, see the *Error Conditions* section. |
| DEMAG | 4 | Control input, see the *Demagnetization* section. |
| GAIN | 5 | Control input for open-loop gain: low = normal, high = –8 dB. |
| $REF_{OUT}$ | 6 | Output for internal 2.5 V reference voltage. |
| $REF_{IN}$ | 7 | Input for zero reference to differential amplifier. |
| $V_{OUT}$ | 8 | Output for differential amplifier. |
| $IA_{IN2}$ | 9 | Connect to GND1.Noninverting input of differential amplifier. |
| $IA_{IN1}$ | 10 | Inverting input of differential amplifier. |
| GND2 | 11 | Ground connection. |
| $I_{COMP2}$ | 12 | Output 2 of compensation coil driver. |
| $I_{COMP1}$ | 13 | Output 1 of compensation coil driver. |
| $V_{DD2}$ | 14 | Supply voltage. Connect to $V_{DD1}$. |
| CCdiag | 15 | Control input for wire-break detection: high = enable. |
| OVER-RANGE | 16 | Open-drain output for over-range indication: low = over-range. |
| $V_{DD1}$ | 17 | Supply voltage. |
| IS2 | 18 | Probe connection 2. |
| GND1 | 19 | Ground connection. |
| IS1 | 20 | Probe connection 1. |
| Exposed Thermal Pad | – | Connect to GND1. |


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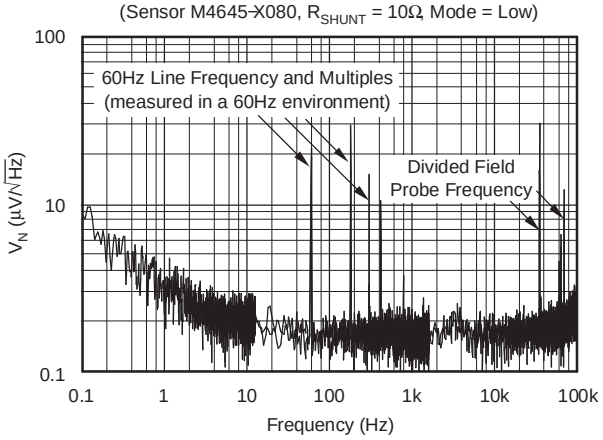
## TYPICAL CHARACTERISTICS

At $T_A$ = +25°C and $V_{DD1}$ = $V_{DD2}$ = +5 V with external 100 kHz filter BW, unless otherwise noted.

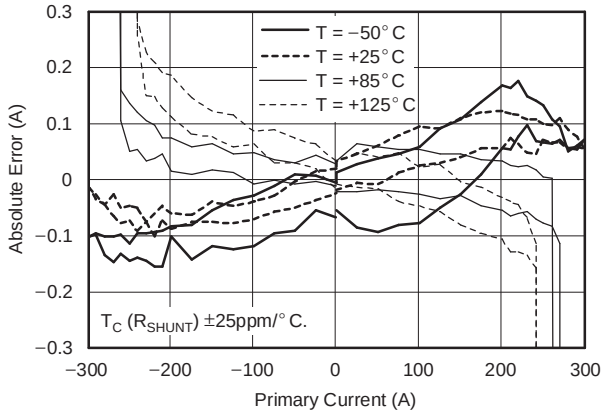
DRV401 AND SENSOR:
OFFSET vs SUPPLY VOLTAGE



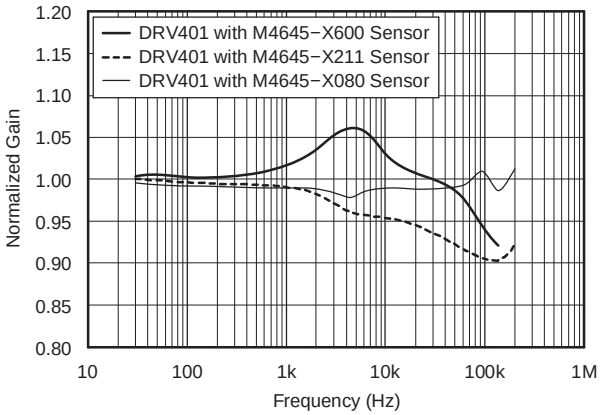

DRV401 AND SENSOR:
OUTPUT VOLTAGE NOISE DENSITY
(Sensor M4645−X080, $R_{SHUNT}$ = 10Ω, Mode = Low)



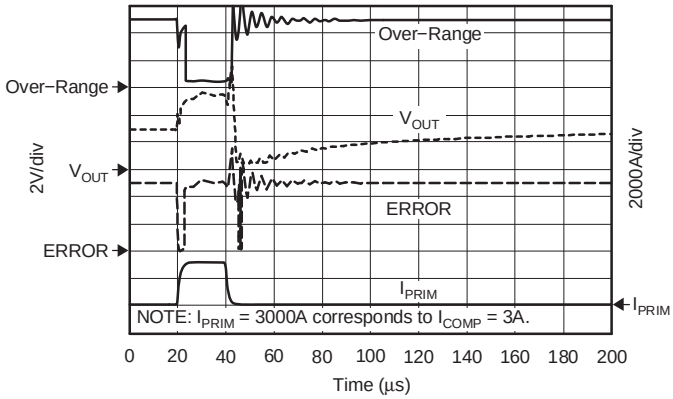

DRV401 AND SENSOR: ABSOLUTE ERROR
(Soldered DWP−20 with 1 Square−Inch Copper Pad)
(Measurements by Vacuumschmelza GmbH)



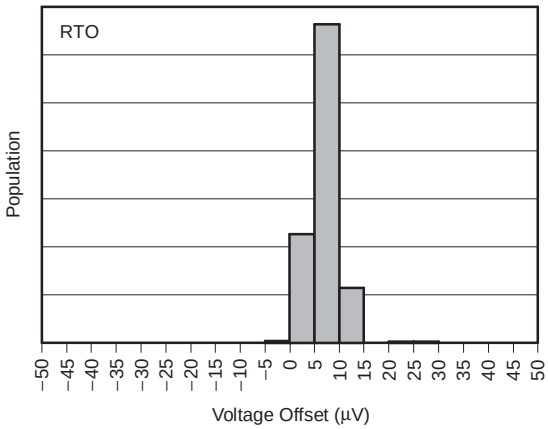

GAIN FLATNESS vs FREQUENCY
(Measurements by Vacuumschmelze GmbH)




3A $I_{COMP}$ OVERLOAD RECOVERY
(Measurements by Vacuumschmelze GmbH)



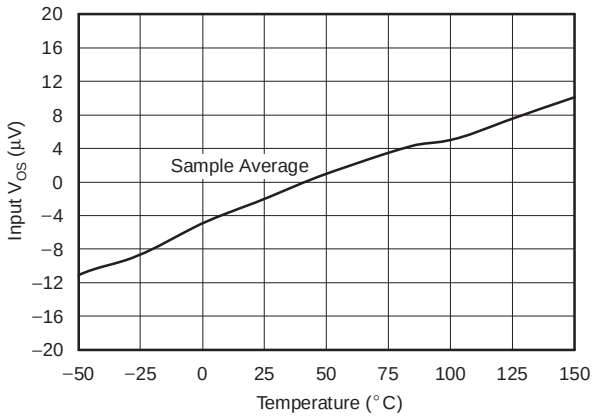

DIFFERENTIAL AMPLIFIER:
VOLTAGE OFFSET PRODUCTION DISTRIBUTION



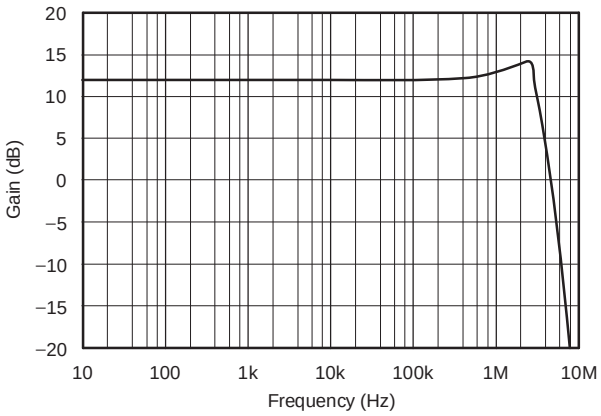
## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C and $V_{DD1}$ = $V_{DD2}$ = +5 V with external 100 kHz filter BW, unless otherwise noted.

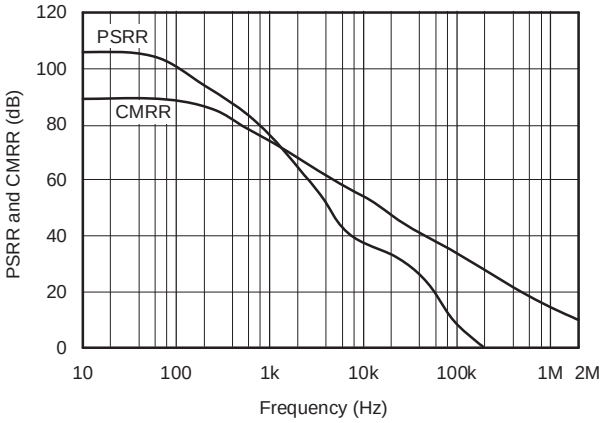
DIFFERENTIAL AMPLIFIER:
OFFSET VOLTAGE vs TEMPERATURE, RTO



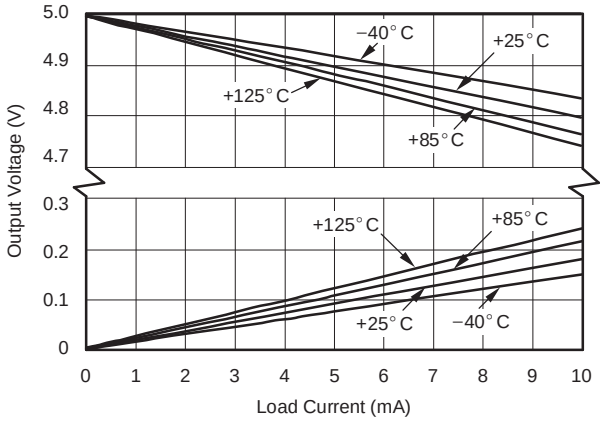

DIFFERENTIAL AMPLIFIER:
GAIN vs FREQUENCY



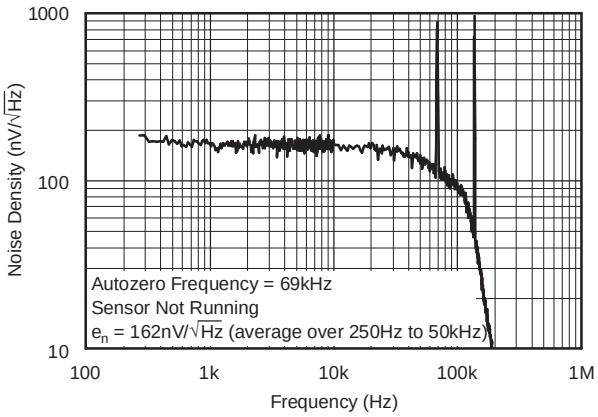

DIFFERENTIAL AMPLIFIER:
PSRR AND CMRR vs FREQUENCY



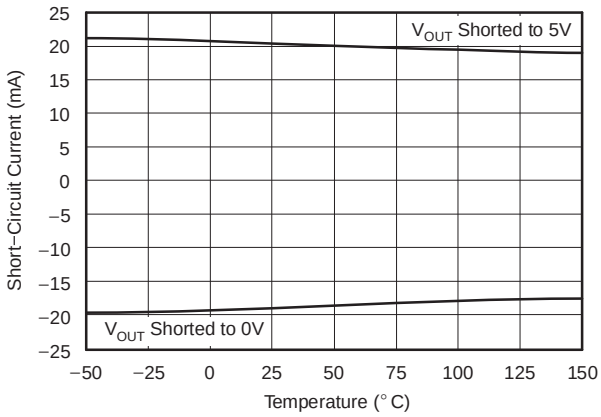

DIFFERENTIAL AMPLIFIER:
OUTPUT VOLTAGE vs OUTPUT CURRENT




DIFFERENTIAL AMPLIFIER:
OUTPUT NOISE DENSITY




DIFFERENTIAL AMPLIFIER:
SHORT−CIRCUIT CURRENT vs TEMPERATURE



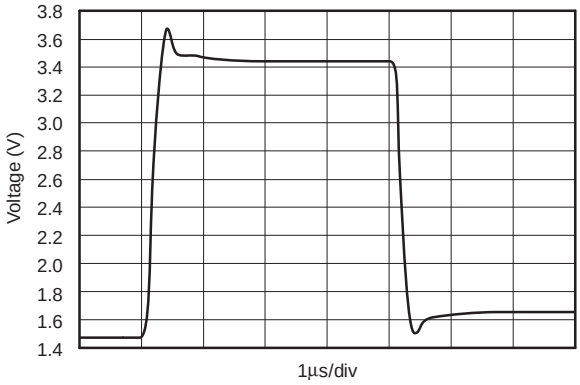


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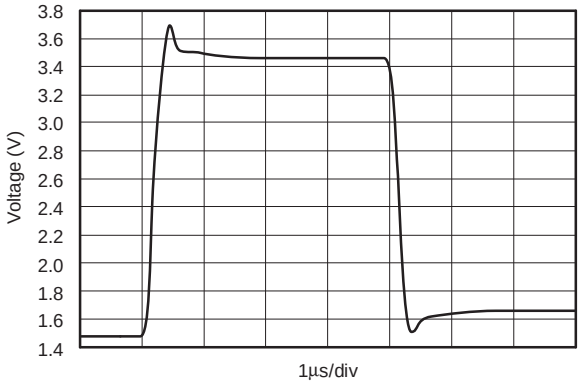
## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C and $V_{DD1}$ = $V_{DD2}$ = +5 V with external 100 kHz filter BW, unless otherwise noted.

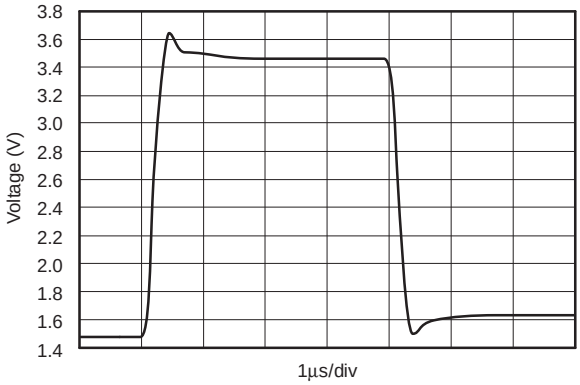
DIFFERENTIAL AMPLIFIER:
$T_A$ = –50°C LARGE–SIGNAL STEP RESPONSE



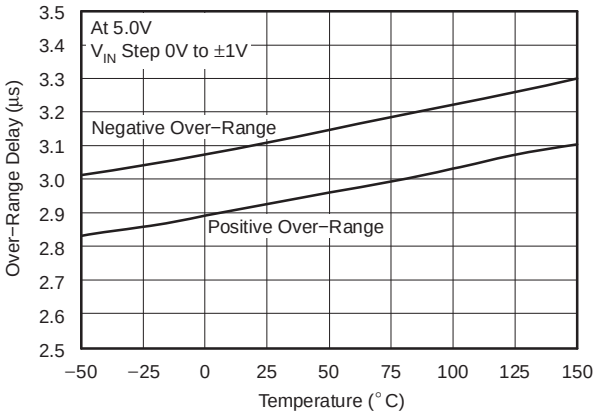

DIFFERENTIAL AMPLIFIER:
$T_A$ = +25°C LARGE–SIGNAL STEP RESPONSE



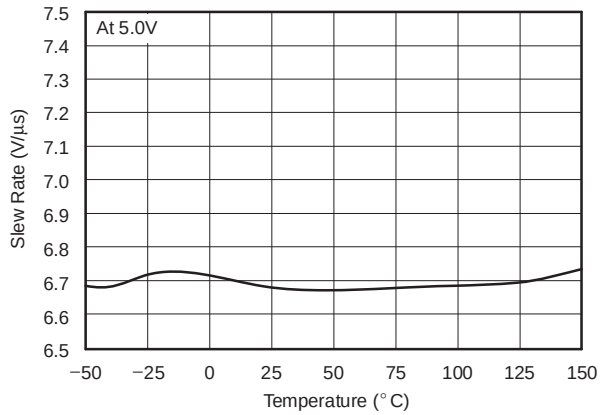

DIFFERENTIAL AMPLIFIER:
$T_A$ = +150°C LARGE–SIGNAL STEP RESPONSE



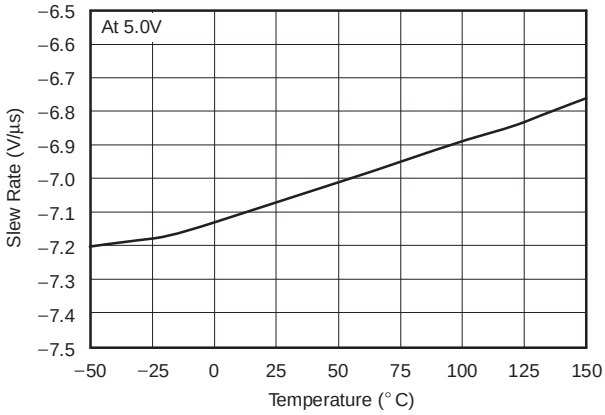

DIFFERENTIAL AMPLIFIER:
OVER–RANGE DELAY vs TEMPERATURE




DIFFERENTIAL AMPLIFIER:
POSITIVE SLEW RATE vs TEMPERATURE




DIFFERENTIAL AMPLIFIER:
NEGATIVE SLEW RATE vs TEMPERATURE

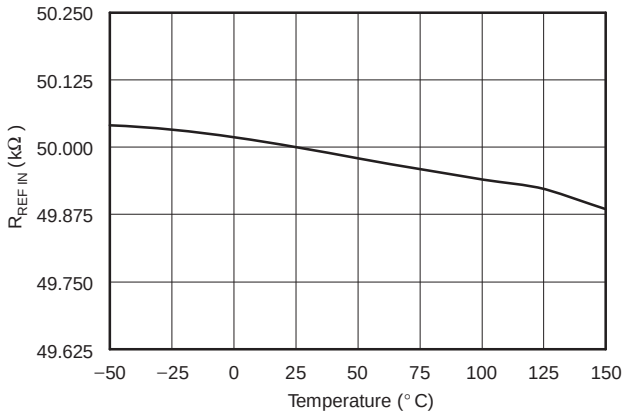



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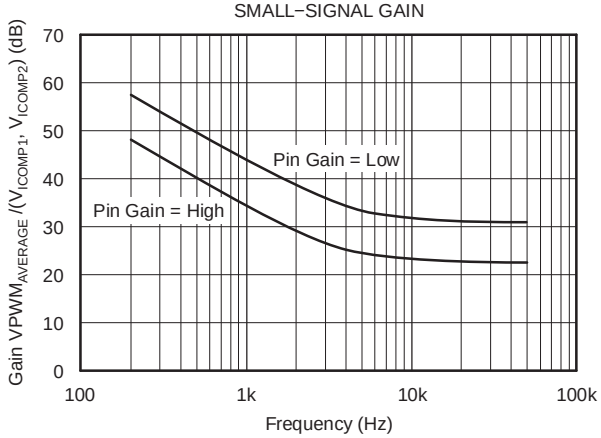
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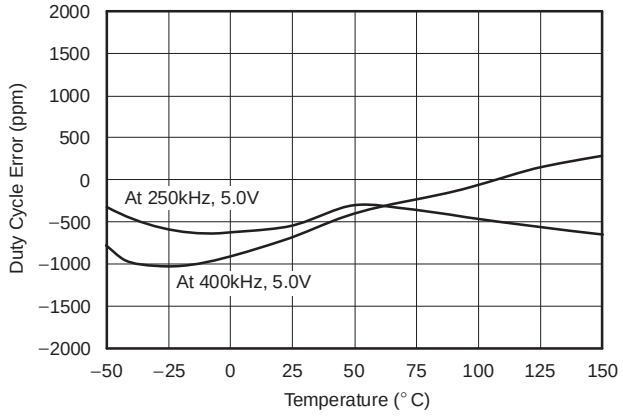
DIFFERENTIAL AMPLIFIER:
$REF_{IN}$ RESISTANCE vs TEMPERATURE



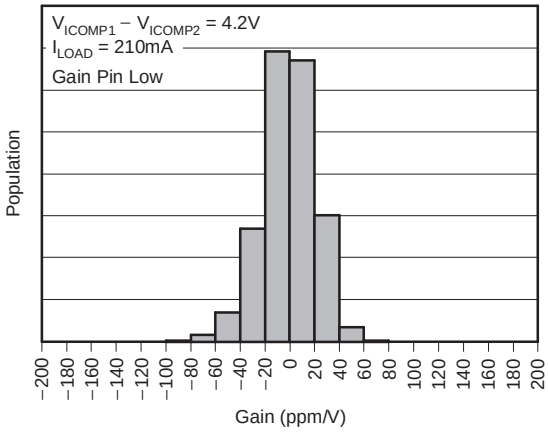

COMPENSATION LOOP:
SMALL−SIGNAL GAIN



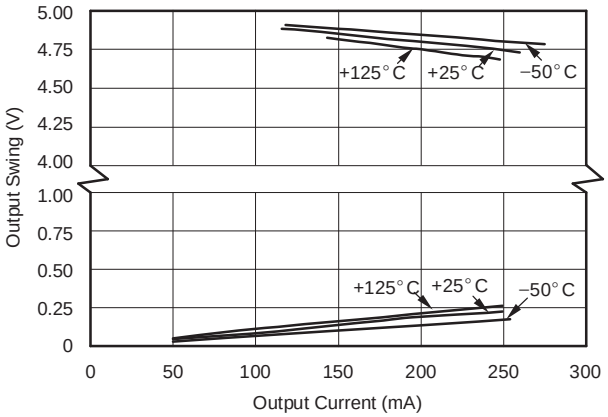

COMPENSATION LOOP:
DUTY CYCLE ERROR vs TEMPERATURE



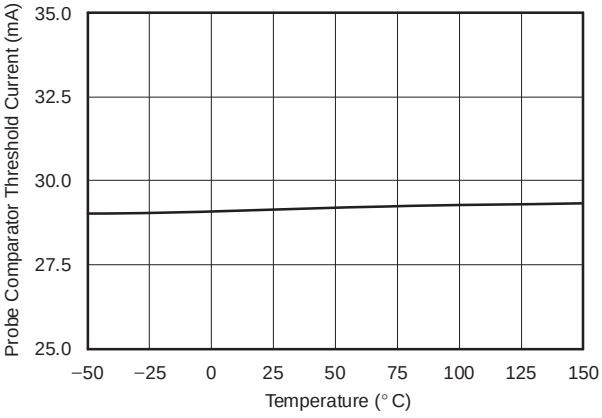

COMPENSATION LOOP:
DC GAIN: DUTY CYCLE ERROR CHANGE




$I_{COMP}$ OUTPUT SWING TO RAIL
vs OUTPUT CURRENT




PROBE COMPARATOR THRESHOLD
CURRENT vs TEMPERATURE



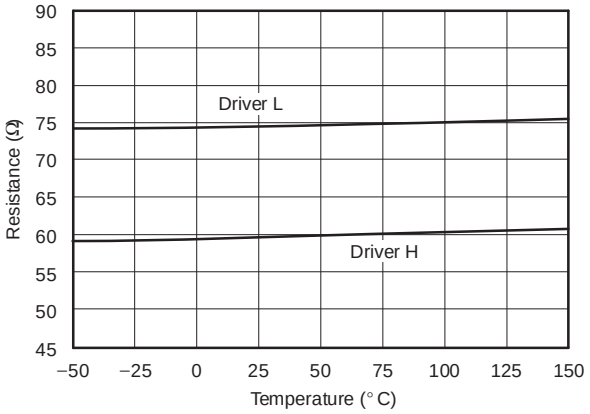


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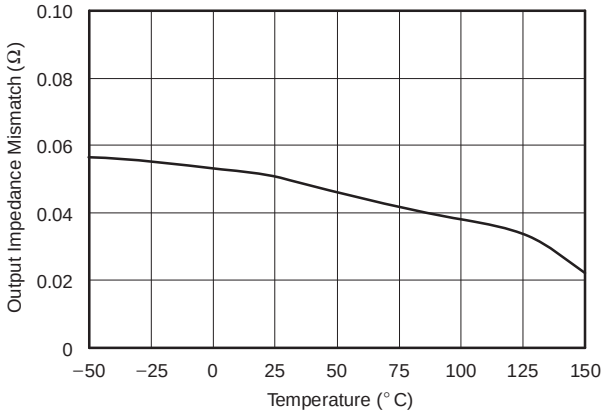
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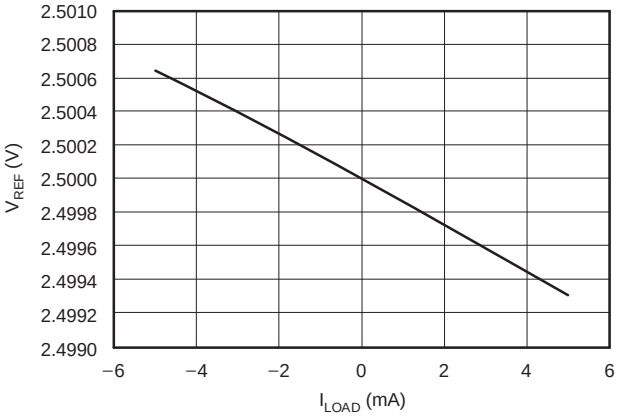
PROBE DRIVER:
INTERNAL RESISTOR vs TEMPERATURE



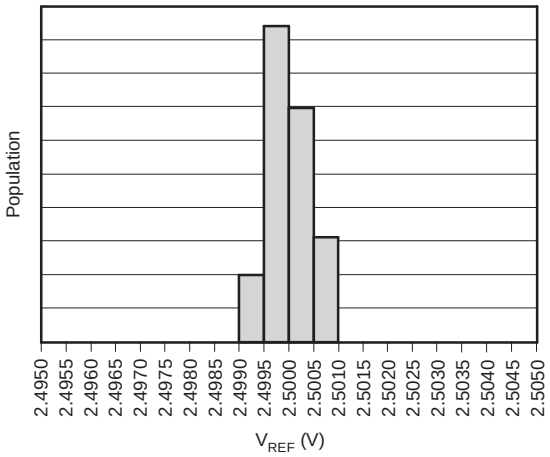

OUTPUT IMPEDANCE MISMATCH OF IS1 AND IS2
vs TEMPERATURE



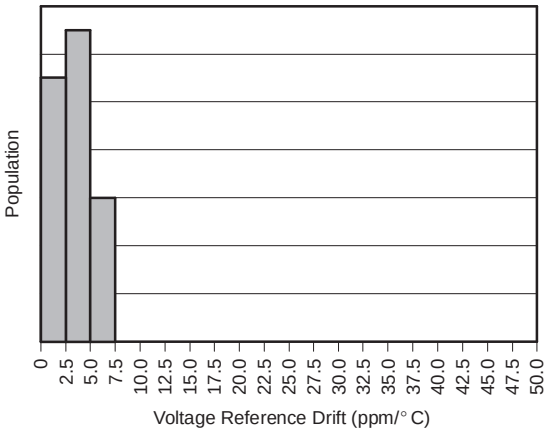

VOLTAGE REFERENCE vs LOAD CURRENT



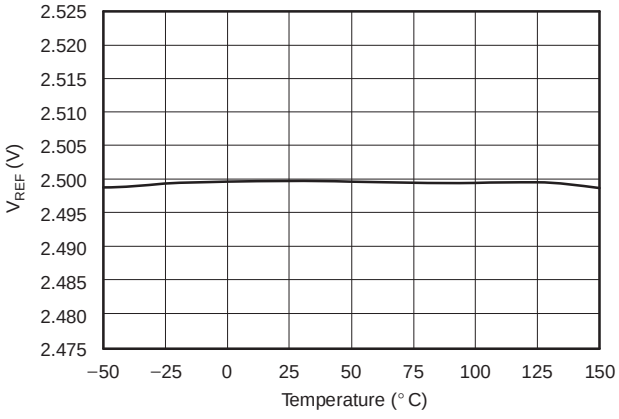

VOLTAGE REFERENCE PRODUCTION DISTRIBUTION




VOLTAGE REFERENCE DRIFT
PRODUCTION DISTRIBUTION



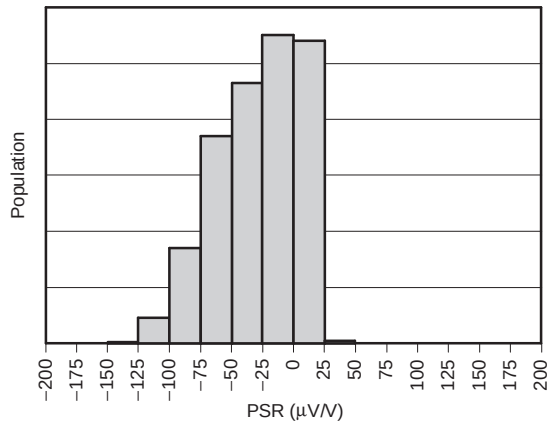

VOLTAGE REFERENCE vs TEMPERATURE



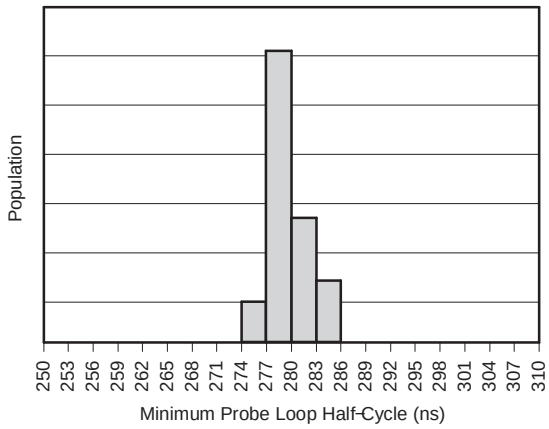
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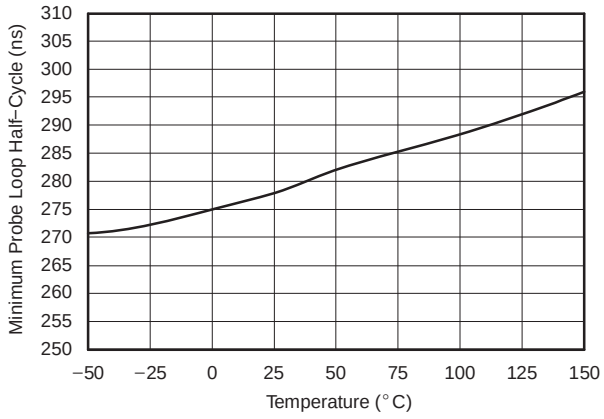
VOLTAGE REFERENCE POWER−SUPPLY REJECTION PRODUCTION DISTRIBUTION



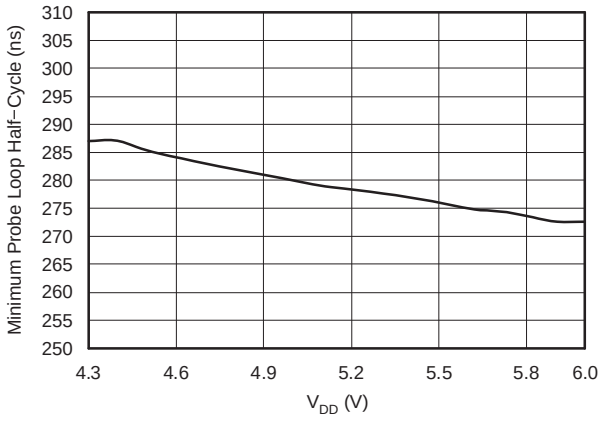

OSCILLATOR PRODUCTION DISTRIBUTION



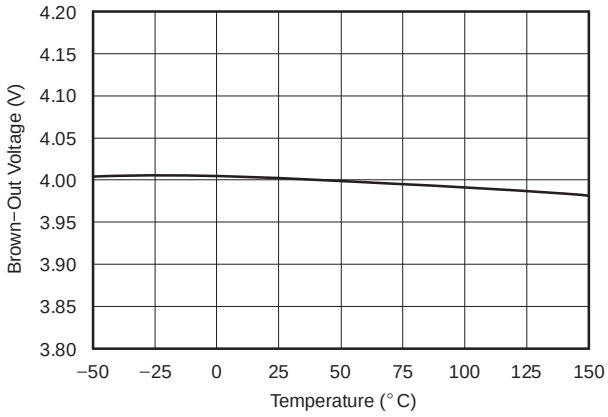

OSCILLATOR vs TEMPERATURE




OSCILLATOR vs SUPPLY VOLTAGE




BROWN−OUT VOLTAGE vs TEMPERATURE





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# APPLICATION INFORMATION

## FUNCTIONAL PRINCIPLE OF CLOSED-LOOP CURRENT SENSORS WITH MAGNETIC PROBE USING THE DRV401

Closed-loop current sensors measure current over wide frequency ranges, including dc. These types of devices offer a contact-free method as well as excellent galvanic isolation performance combined with high resolution, accuracy, and reliability.

At dc and in low-frequency ranges, the magnetic field induced from the current in the primary winding is compensated by a current flowing through a compensation winding. A magnetic field probe, located in the magnetic core loop, detects the magnetic flux. This probe delivers the signal to the amplifier that drives the current through the compensation coil, bringing the magnetic flux back to zero. This compensation current is proportional to the primary current, relative to the winding ratio.

In higher frequency ranges, the compensation winding acts as the secondary winding in the current transformer, while the H-bridge compensation driver is rolled off and provides low output impedance.

A difference amplifier senses the voltage across a small shunt resistor that is connected to the compensation loop. This difference amplifier generates the output voltage that is referenced to REFIN and is proportional to the primary current. Figure 1 shows the DRV401 used as a compensation current sensor.

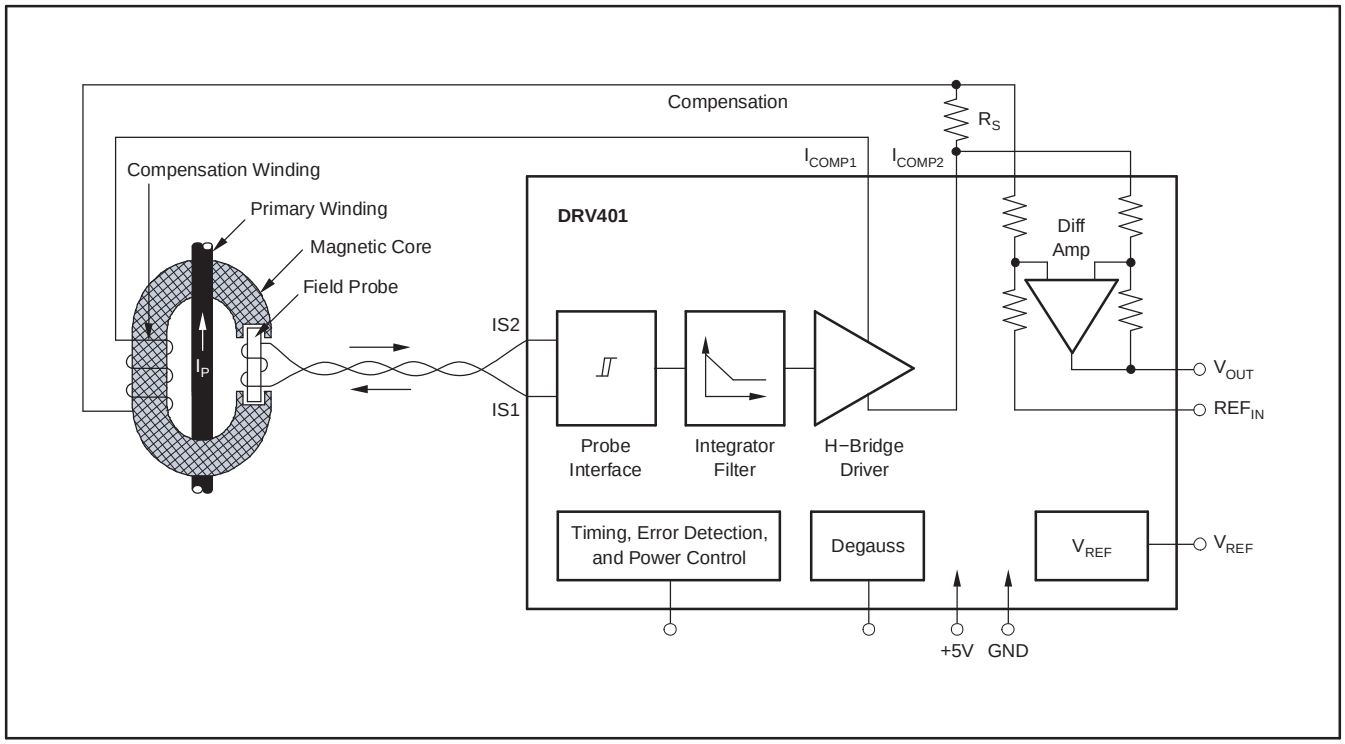



**Figure 1. Principle of Compensation Current Sensor With the DRV401**

## FUNCTIONAL DESCRIPTION

The DRV401 operates from a single +5 V supply. It is a complete sensor signal conditioning circuit that directly connects to the current sensor, providing all necessary functions for the sensor operation. The DRV401 provides magnetic field probe excitation, signal conditioning, and compensation coil driver amplification. In addition, it detects error conditions and handles overload situations. A precise differential amplifier allows translation of the compensation current into an output voltage using a small shunt resistor. A buffered voltage reference can be used for comparator, analog-to-digital converter (ADC), or bipolar zero reference voltages.

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Dynamic error correction ensures high dc precision over temperature and long-term accuracy. The DRV401 uses analog signal conditioning; the internal loop filter and integrator are switched capacitor-based circuits. Therefore, the DRV401 allows combination with high-precision sensors for exceptional accuracy and resolution. The typical characteristic curve, DRV401 and Sensor Linearity, shows an example of the linearity and temperature stability achieved by the device.

A demagnetization cycle can be initiated on demand or on power-up. This cycle reduces offset and restores high performance after a strong overload condition. An internal clock and counter logic generate the degauss function. The same clock controls power-up, overload detection and recovery, error, and time-out conditions.

The DRV401 is built on a highly reliable CMOS process. Unique protection cells at critical connections enable the design to handle inductive energy.

## MAGNETIC PROBE (SENSOR) INTERFACE

The magnetic field probe consists of an inductor wound on a soft magnetic core. The probe is connected between pins IS1 and IS2 of the probe driver that applies approximately +5 V (the supply voltage) through resistors across the probe coil (see Figure 2a).

The probe core reaches saturation at a current of typically 28 mA (see Figure 2a). The comparator is connected to $V_{REF}$ by approximately 0.5 V. A current comparator detects the saturation and inverts the excitation voltage polarity, causing the probe circuit to oscillate in a frequency range of 250 kHz to 550 kHz. The oscillating frequency is a function of the magnetic properties of the probe core and its coil.

The current rise rate is a function of the coil inductance: $dI = V \times dT / L$. However, the inductance of the field probe is low while its core material is in saturation (the horizontal part of the hysteresis curve) and is high at the vertical part of the hysteresis curve. The resulting inductance and the series resistance determine the output voltage and current versus time performance characteristic.

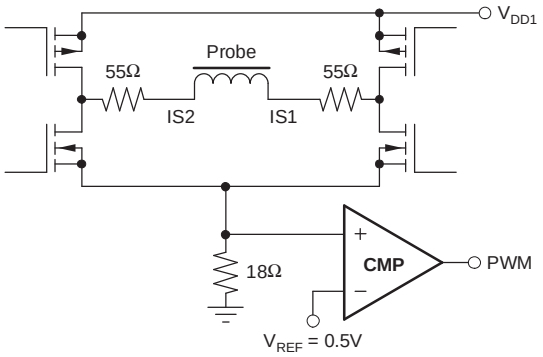
Without external magnetic influence, the duty cycle is exactly 50% because of the inherent symmetry of the magnetic hysteresis; the probe inductor is driven from –B saturation through the high inductance range to +B saturation and back again in a time-symmetric manner (see Figure 2b).

If the core material is magnetized in one direction, a long and a short charge time result because the probe current through the inductors generates a field that either subtracts or adds to the flux in the probe core, either driving the probe core out of saturation or further into saturation (see Figure 2c). The current into the probe is limited by the voltage drops across the probe driver resistors.

The DRV401 continuously monitors the logic magnetic flux polarity state. In the case of distortion noise and excessive overload that could fully saturate the probe, the overload control circuit recovers the probe loop. During an overload condition, the probe oscillation frequency increases to approximately 1.6 MHz until limited by the internal timing control.

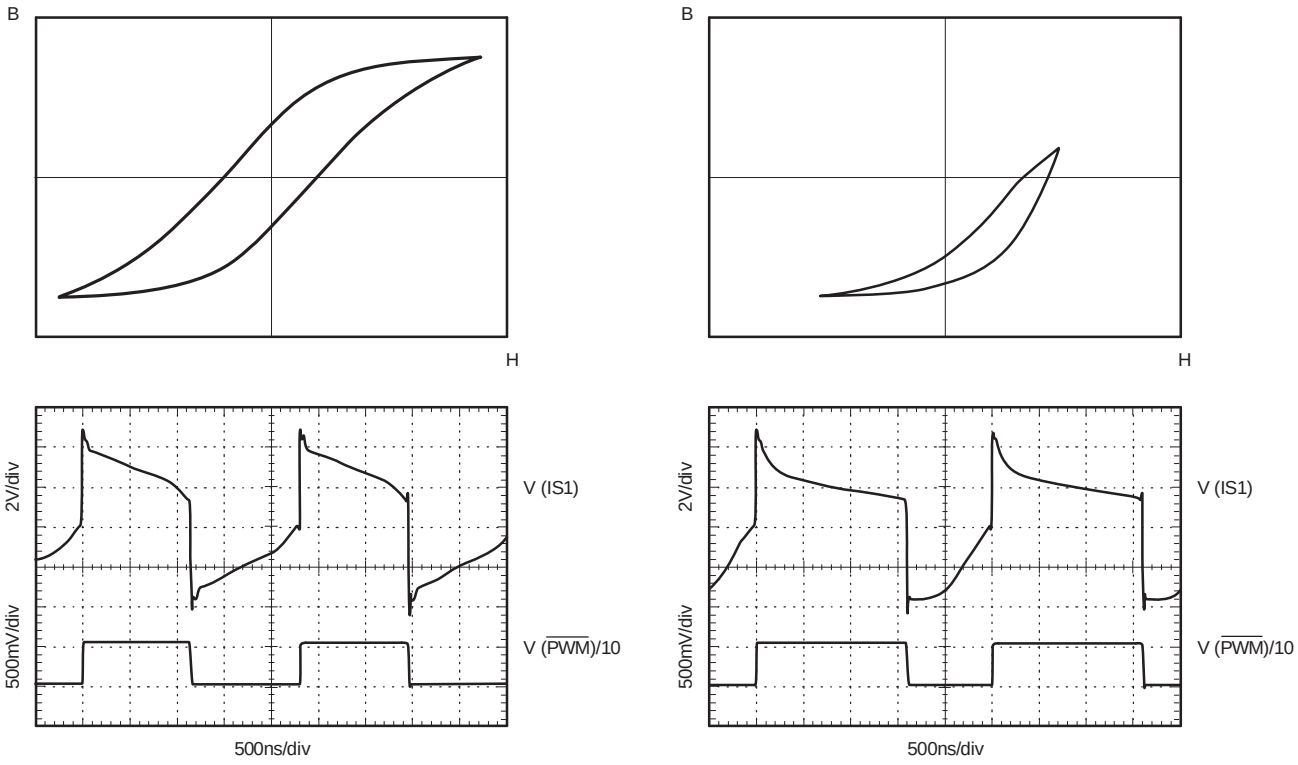
In an overload condition, the compensation current ($I_{COMP}$) driver cannot deliver enough current into the sensor secondary winding, and the magnetic flux in the sensor main core becomes uncompensated.


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NOTE: MOS components function as switches only.

**a)** Simplified probe interface circuit.
The probe is connected between S1 and S2.




**b)** Without an external magnetic field, the hysteresis curve is symmetrical and the probe loop generates 50% duty cycle.

**c)** An external magnetic flux (H) generated from the primary current ($I_{PRIM}$) shifts the hysteresis curve of the magnetic field probe in the H-axis and the probe loop generates a nonsymmetrical duty cycle.

**Figure 2. Magnetic Probe, Hysteresis, and Duty Cycle**

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The transition from normal operation to overload happens relatively slowly, because the inherent sensor transformer characteristics induce the initial primary current step, as shown in Figure 3. As the transformer-induced secondary current starts to decay, the compensation feedback driver increases its output voltage to maintain the sensor core flux compensation at zero.

When the system compensation loop reaches its driving limit, the rising magnetic flux causes one of the probe PWM half-periods to become shorter. The minimum half-period of the probe oscillation is limited by the internal timing to 280 ns, based on the properties of the VAC magnetic sensors. After three consecutive cycles of the same half-period being shorter than 280 ns, the DRV401 goes into overload-latch mode. The device stores the ICOMP driver output signal polarity and continues producing the skewed-duty cycle PWM signal. This action prevents the loss of compensation signal polarity information during very strong overloads. In this case, both PWM half-periods are short and approximately equal, because the field probe stays completely in one of the saturated regions.

The overload-latch condition is removed after the primary current goes low enough for the $I_{COMP}$ driver to compensate, and both half-periods of the probe driver oscillation become longer than 280ns (the field probe comes out of the saturated region).

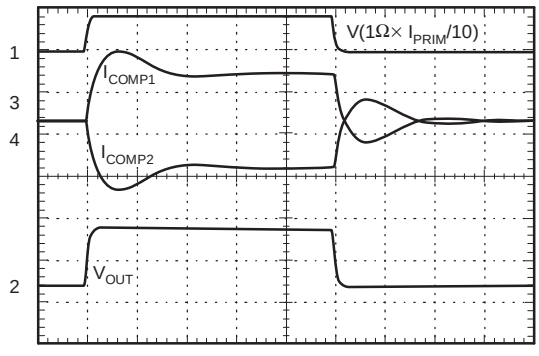
Peak voltages and currents can be generated during normal operations as well as overload conditions. Therefore, both probe connection pins are internally protected against coupled energy from the magnetic core. Wiring between probe and IC inputs should be short and guarded against interference; see *Layout Considerations*.For reliable operation, error detection circuits monitor the probe operation:

1. If the probe driver comparator (CMP) output stays low longer than 32 µs, the ERROR flag asserts active, and the compensation current ($I_{COMP}$) is set to zero.
2. If the probe driver period is less than 275 ns on three consecutive pulses, the ERROR flag asserts active.

See the *Error Conditions* section for more details.

## PWM PROCESSING

The outputs PWM and $\overline{PWM}$ represent the probe output signal as a differential PWM signal. It can drive external circuitry or be used for synchronous ripple reduction. The PWM signal from the probe excitation and sense stage is internally connected to a high-performance, switched-capacitor integrator followed by an integrating-differentiating filter. This filter converts the PWM signal into a filtered delta signal and prepares it for driving the analog compensation coil driver. The gain roll-off frequency of the filter stage is set to provide high dc gain and loop stability. If additional gain is added from external circuitry, the internal gain can be reduced by 8 dB, asserting the GAIN pin high (see the *External Compensation Coil Driver* section).




Sensor: 4 x 100
$R_{SH}$ = 10Ω
Step Response
2kHz In
V(Gain) = Low

Channel 1: 2V/div
Channels 2−4: 500mV/div

A current pulse of 0A to 18A (Ch 1) generates the two $I_{COMP}$ signals (Ch 3 and Ch 4). Ch 2 shows the resulting output signal, $V_{OUT}$. This test uses the M4645-X030 sensor, no bandwidth limitation, but a 20-sample average.

**Figure 3. Primary Current Step Response**


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## COMPENSATION DRIVER

The compensation coil driver provides the driving current for the compensation coil. A fully differential driver stage offers high signal voltages to overcome the wire resistance of the coil with only +5 V supply. The compensation coil is connected between $I_{COMP1}$ and $I_{COMP2}$, both generating an analog voltage across the coil (see Figure 3) that turns into current from the wire resistance (and eventually from the inductance). The compensation current represents the primary current transformed by the turns ratio. A shunt resistor is connected in this loop and the high-precision difference amplifier translates the voltage from this shunt to an output voltage.

Both compensation driver outputs provide low impedance over a wide frequency range to ensure smooth transitions between the closed-loop compensation frequency range and the high-frequency range, where the primary winding directly couples the primary current into the compensation coil at a rate set by the winding ratio.

The two compensation driver outputs are designed with protection circuitry to handle inductive energy. However, additional external protection diodes might be necessary for high current sensors.

For reliable operation, a wire break in the compensation circuit can be detected. If the feedback loop is broken, the integrating filter drives the outputs $I_{COMP1}$ and $I_{COMP2}$ to the opposite rails. With one of these pins coming within 300 mV to ground, a comparator tests for a minimum current flowing between $I_{COMP1}$ and $I_{COMP2}$. If this current stays below the threshold current level for at least 100 µs, the ERROR pin is asserted active (low). The threshold current level for this test is less than 57 mA at 25°C and 65 mA at –40°C, if the $I_{COMP}$ pins are fully railed (see the Typical Characteristics). For sensors with high winding resistance (compensation coil resistance + $R_{SHUNT}$) or connected to an external compensation driver, this function should be disabled by pulling the CCdiag pin low.

$$R_{MAX} = \frac{V_{OUT}}{65mA}$$

Where:

$V_{OUT}$ equals the peak voltage between $I_{COMP1}$ and $I_{COMP2}$ at a 65mA drive current.

$R_{MAX}$ equals the sum of the coil and the shunt resistance.

## EXTERNAL COMPENSATION COIL DRIVER

An external driver for the compensation coil can be connected to the $I_{COMP1}$ and $I_{COMP2}$ outputs. To prevent a wire break indication, CCdiag has to be asserted low.

An external driver can provide both a higher drive voltage and more drive current. It also moves the power dissipation to the external transistors, thereby allowing a higher winding resistance in the compensation coil and more current. Figure 4 shows a block diagram of an external compensation coil driver. To drive the buffer, either one or both $I_{COMP}$ outputs can be used. Note, however, that the additional voltage gain could cause instability of the loop. Therefore, the internal gain can be reduced by approximately 8 dB by asserting the GAIN pin high. $R_{SHUNT}$ is connected to GND to allow for a single-ended external compensation driver. The differential amplifier can continue to sense the voltage, and used for the gain and over-range comparator or ERROR flag.

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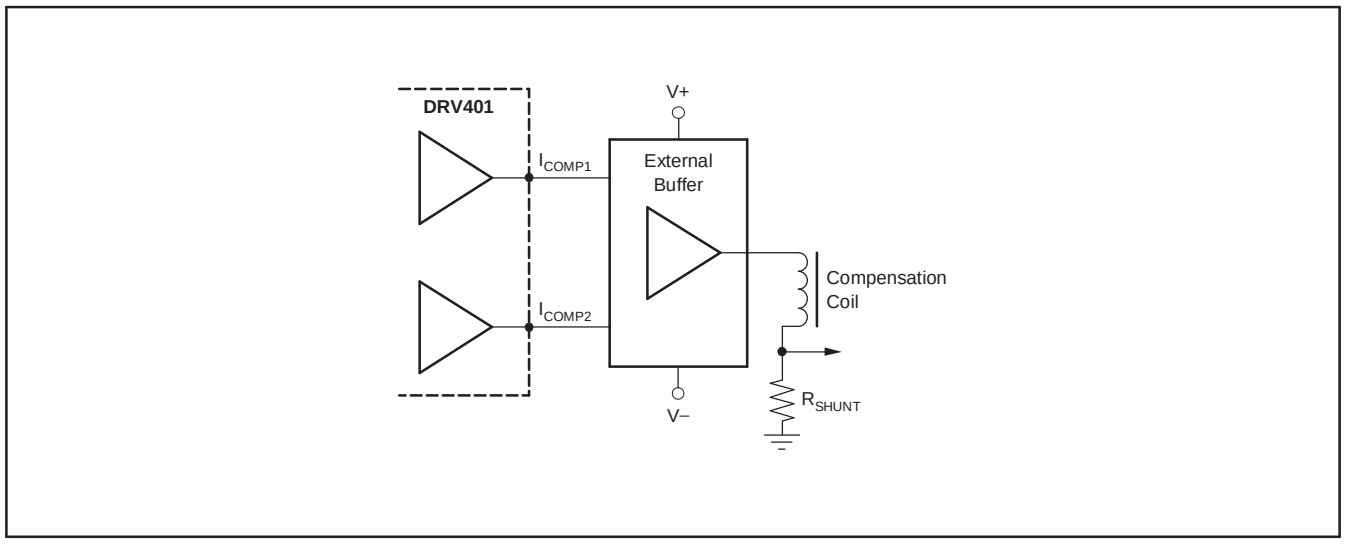



**Figure 4. DRV401 With External Compensation Coil Driver and $R_{SHUNT}$ Connected to GND**

## SHUNT SENSE AMPLIFIER

The differential (H-bridge) driver arrangement for the compensation coil requires a differential sense amplifier for the shunt voltage. This differential amplifier offers wide bandwidth and a high slew rate for fast current sensors. Excellent dc stability and accuracy result from an auto-zero technique. The voltage gain is 4 V/V, set by precisely matched and stable internal SiCr resistors.

Both inputs of the differential amplifier are normally connected to the current shunt resistor. This resistor adds to the internal (10 kΩ) resistor, slightly reducing the gain in this leg. For best common-mode rejection (CMR), a dummy shunt resistor ($R_5$) is placed in series with the $REF_{IN}$ pin to restore matching of both resistor dividers, as shown in Figure 5a.

For gains of 4 V/V:

$$4 = \frac{R_2}{R_1} = \frac{R_4 + R_5}{R_{SHUNT} + R_3}$$

With $R_2/R_1 = R_4/R_3 = 4$; $R_5 = R_{SHUNT} \times 4$

Typically, the gain error resulting from the resistance of $R_{SHUNT}$ is negligible; for 70 dB of common-mode rejection, however, the match of both divider ratios needs to be better than 1/3000.

The amplifier output can drive close to the supply rails, and is designed to drive the input of a SAR-type ADC; adding an RC low-pass filter stage between the DRV401 and the ADC is recommended. This filter not only limits the signal bandwidth but also decouples the high-frequency component of the converter input sampling noise from the amplifier output. For $R_F$ and $C_F$ values, refer to the specific converter recommendations in the specific product data sheet. Empirical evaluation may be necessary to obtain optimum results.

The output can drive 100 pF directly and shows 50% overshoot with approximately 1 nF capacitance. Adding $R_F$ allows much larger capacitive loads, as shown in Figure 5b and Figure 5c. Note that with $R_F$ of only 20 Ω, the load capacitor should be either smaller than 1 nF or larger than 33 nF to avoid overshoot; with $R_F$ of 50 Ω this transient area is avoided.

The reference input ($REF_{IN}$) is the reference node for the exact output signal ($V_{OUT}$). Connecting $REF_{IN}$ to the reference output ($REF_{OUT}$) results in a live zero reference voltage of 2.5 V. Using the same reference for $REF_{IN}$ and the ADC avoids mismatch errors that exist between two reference sources.


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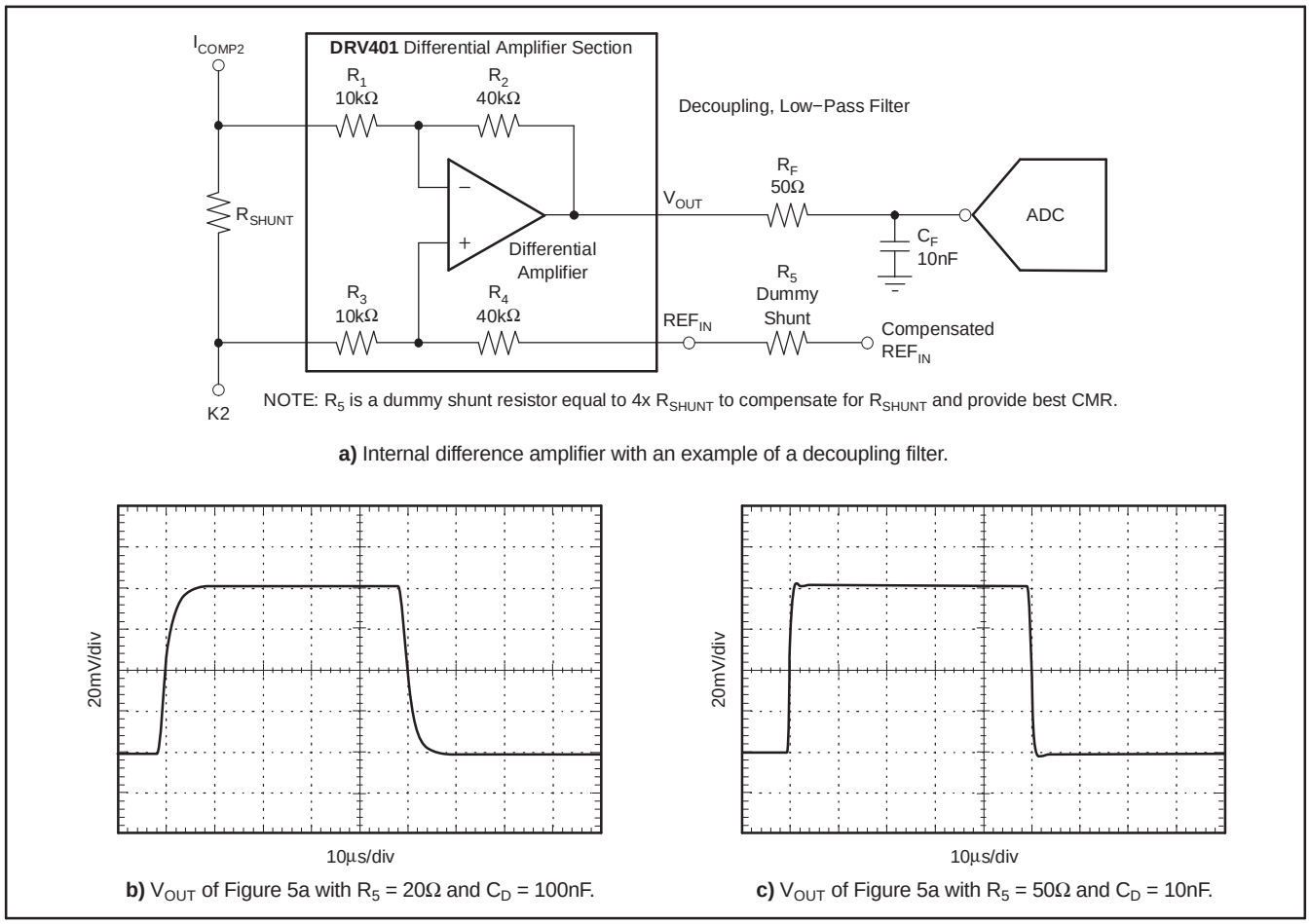



**Figure 5. Internal Difference Amplifier With Example of a Decoupling Filter**

## OVER-RANGE COMPARATOR

High peak current can overload the differential amplifier connected to the shunt. The OVER-RANGE pin, an open-drain output, indicates an over-voltage condition for the differential amplifier by pulling low. The output of this flag is suppressed for 3 µs, preventing unwanted triggering from transients and noise. This pin returns to high as soon as the overload condition is removed (external pull-up required to return the pin high).

This ERROR flag not only provides a warning about a signal clipping condition, but is also a window comparator output for actively shutting off circuits in the system. The value of the shunt resistor defines the operating window for the current. It sets the ratio between the nominal signal and the trip level of the Over-Range flag. The trip current of this window comparator is calculated using the following example:

With a 5 V supply, the output voltage swing is approximately ±2.45 V (load and supply voltage-dependent).

The gain of 4 V/V allows an input swing of ±0.6125 V.

Thus, the clipping current is $I_{MAX}$ = 0.6125 V/$R_{SHUNT}$.

See the differential amplifier curve of the Typical Characteristics, *Output Voltage vs Output Current*.

The over-range condition is internally detected as soon as the amplifier exceeds its linear operating range, not just a set voltage level. Therefore, the error or the over-range comparator level is reliably indicated in fault conditions such as output shorts, low load or low supply conditions. As soon as the output cannot drive the voltage higher, the flag is activated. This configuration is a safety improvement over a voltage level comparator.

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**NOTE:**

The internal resistance of the compensation coil may prevent high compensation current from flowing because of $I_{COMP}$ driver overload. Therefore, the differential amplifier may not overload with this current. However, a fast rate of change of the primary current would be transmitted through transformer action and safely trigger the overload flag.

## VOLTAGE REFERENCE

The precision 2.5 V reference circuit offers low drift (typically 10 ppm/K) and is used for internal biasing; it is also connected to the $REF_{OUT}$ pin. The circuit is intended as the reference point of the output signal to allow a bipolar signal around it. This output is buffered for low impedance and tolerates sink and source currents of ±5 mA. Capacitive loads can be directly connected, but generate ringing on fast load transients. A small series resistor of a few ohms improves the response, especially for a capacitive load in the range of 1 µF. Figure 6 shows the transient load regulation with 1 nF direct load.

The reference source is part of the integrated circuit and referenced to GND2. Large current pulses driving the compensation coil can generate a voltage drop in the GND connection that would add on to the reference voltage. Therefore, a low impedance GND layout is critical to handle the currents and the high bandwidth of this IC.

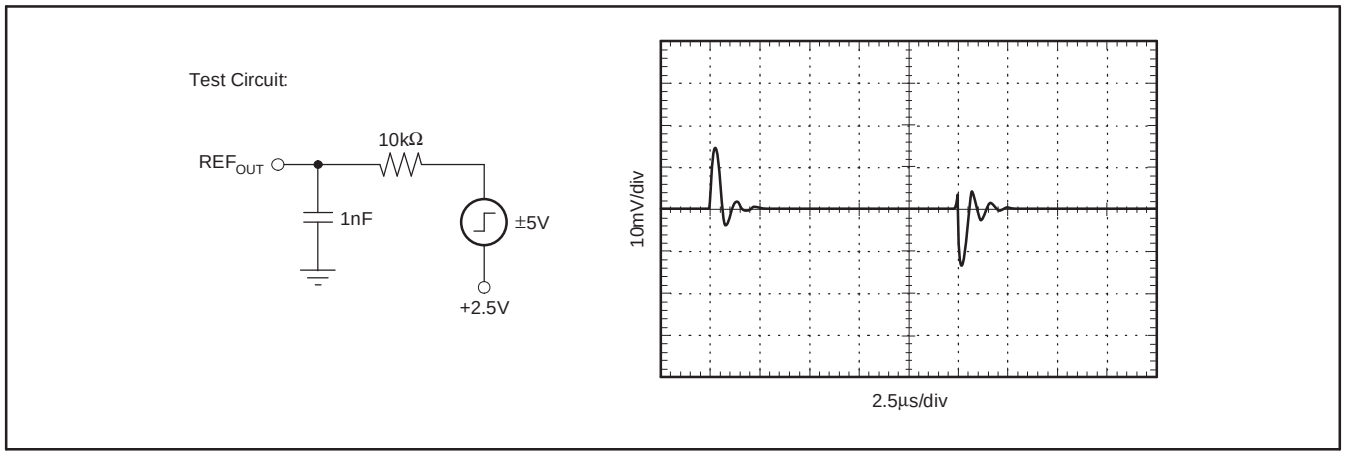



**Figure 6. Pulse Response Test Circuit and Scope Shot of Reference**

## DEMAGNETIZATION

Iron cores are not immune to residual (remanence) magnetism. The residual remanence can produce a signal offset error, especially after strong current overload, which goes along with high magnetic field density. Therefore, the DRV401 includes a signal generator for a demagnetization cycle. The digital control pin, DEMAG, starts this cycle on demand after this pin is held high for at least 25.6 µs. Shorter pulses are ignored. The cycle lasts for approximately 110 ms. During this time, the Error flag is asserted low to indicate that the output is not valid. When DEMAG is high during power-on, a demagnetization cycle immediately initiates (12 µs) after power-on ($V_{DD}$ > 4 V). Holding DEMAG low avoids this cycle at power-up (see the *Power-On and Brownout* section).

The probe circuit is in normal operation and oscillates during the demagnetization cycle. The outputs PWM and PWM are active accordingly.

A demagnetization cycle can be aborted by pulling DEMAG low, filtered by 25 µs to ignore glitches (see Figure 7). In a typical circuit, the DEMAG pin may be connected to the positive supply, which enables a degauss cycle every time the unit is powered on.

The degauss cycle is based on an internal clock and counter logic. The maximum current is limited by the resistance of the connected coil in series with the shunt resistor. The DEMAG logic input requires a +5 V CMOS-compatible signal.


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## POWER-ON AND BROWNOUT

Power-on is detected with the supply voltage going higher than 4 V at $V_{DD1}$. When DEMAG is high, a degauss cycle is started (see Figure 7a). During this time the ERROR flag remains low, indicating the not ready condition. Maintaining DEMAG low prevents this cycle, and the DRV401 starts operation approximately 32 μs after power-up. If no probe error conditions are detected within four full cycles (that is, the probe half-periods are shorter than 32 μs and longer than 280 ns), the compensation driver starts and the ERROR pin indicates the ready condition by going high, typically about 42 μs after power-up.

**NOTE:**

An external pull-up resistor is required to pull the ERROR pin high.

Both supply pins ($V_{DD1}$ and $V_{DD2}$) should not differ by more than 100 mV for proper device operation. They are normally connected together or separately filtered (see *Layout Considerations*).

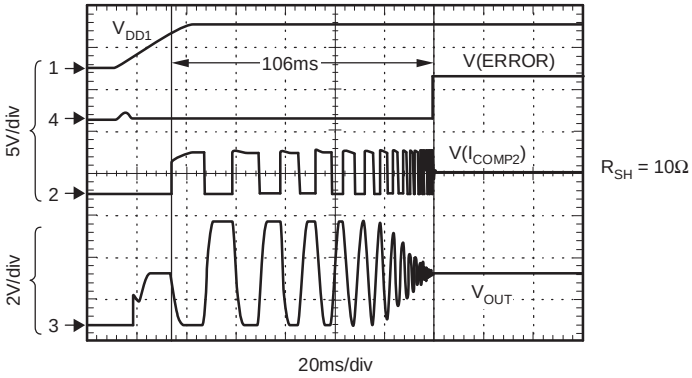
The DRV401 tests for low supply voltage with a brown-out voltage level of +4 V; proper power conditions must be supplied. Good power-supply and low ESR bypass capacitors are required to maintain the supply voltage during the large current pulses that the DRV401 can drive.

A critical voltage level is derived from the proper operation of the probe driver. The probe interface relies on a peak current flowing through the probe to trip the comparator. The probe resistance plus the internal resistance of the driver (see Electrical Characteristics specification, *Probe Coil Loop, Internal Resistor*) sets the lower limit for the acceptable supply voltage. Voltage drops lasting less than 31 ms are ignored. The probe error detection activates the ERROR pin as soon as proper oscillation fails for more than 32 μs.

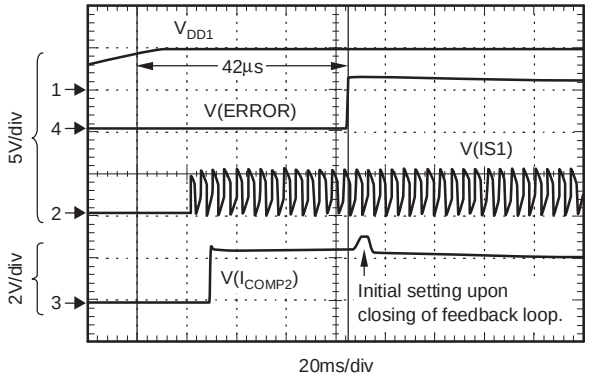
A low supply voltage condition, or brown-out, is detected at +4 V. Short and light voltage drops of less than 100 μs are ignored, provided the probe circuit continues to operate. If the probe no longer operates, the ERROR pin goes active. Signal overload recovery is only provided if the probe loop was not discontinued.

A supply drop lasting longer than 100 μs generates power-on reset. A voltage dip down to +1.8 V (for $V_{DD1}$) also initiates a power-on reset.

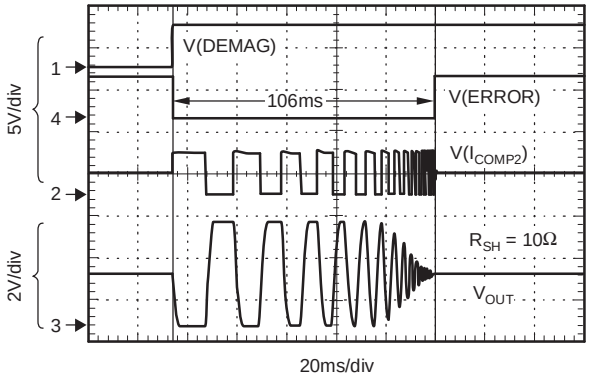
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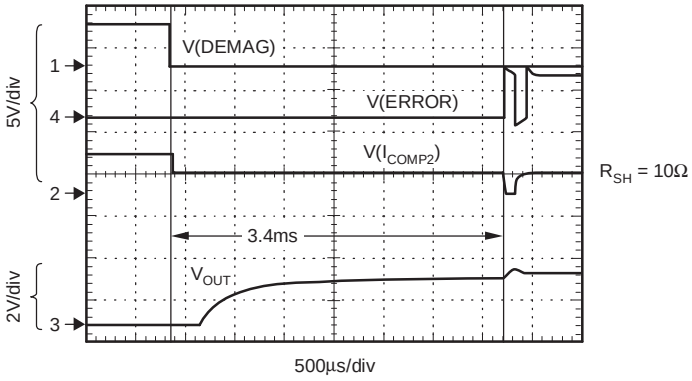

**a)** Demagnetization cycle on power-up. With power-up, the $V_{OUT}$ across the compensation coil centers around half the supply and then starts the cycle after the 4V threshold is exceeded. The ERROR flag resets to H after the cycle is completed.




**b)** Power-up without demagnetization. The probe oscillation V(IS1) starts just before ERROR resets — 15µs after the supply voltage crosses the 4V threshold.




**c)** Demagnetization cycle on command.




**d)** Abort of demagnetization cycle. The ERROR flag resets to H (as shown) and the output settles back to normal operation.

**Figure 7. Demagnetization and Power-On Timing**


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## ERROR CONDITIONS

In addition to the Over-Range flag that indicates signal clipping in the output amplifier (differential amplifier), a system error flag is provided. The ERROR flag indicates conditions when the output voltage does not represent the primary current. It is active during a demagnetization cycle, during a power-fail or brown-out. It also goes active with an open or short-circuit in the probe loop. As soon as the error condition is no longer present and the circuit has returned to normal operation, the flag resets.

Both the ERROR and Over-Range flags are open-drain logic outputs. They can be connected together for a wired-OR and require an external pull-up resistor for proper operation.

The following conditions result in ERROR flag activation (ERROR asserts low):

1. The probe comparator stays low for more than 32 μs. This condition occurs either if the probe coil connection is open or if the supply voltage dips to the level where the required saturation current cannot be reached. During the 32 μs timeout, the $I_{COMP}$ driver remains active but goes inactive thereafter. In case of recovery, ERROR is low and the ICOMP driver remains in reset for another 3.3 ms.
2. The probe driver pulse-width is less than 280 ns for three consecutive periods. This condition indicates either a shorted field probe coil or a fully-saturated sensor at start-up. If this condition persists longer than 25 μs and then recovers, the ERROR flag remains low and ICOMP is in reset for another 3.3 ms. If the condition lasts less than 25 μs, the ERROR flag recovers immediately and the $I_{COMP}$ driver is not interrupted.
3. During demagnetization, if the cycle is aborted early by pulling DEMAG low, the ERROR flag stays low for another 3.3 ms ($I_{COMP}$ is disabled during this time).
4. An open compensation coil is detected (longer than 100 μs). Note: the probe driver, the PWM signal filter and the $I_{COMP}$ driver continue to function in normal mode—only the ERROR flag is asserted in this case. This condition indicates that not enough current is flowing in the $I_{COMP}$ driver output; this condition might be the result of a high-resistance compensation coil or the connection of an external driver. Detection of this condition can be disabled by setting the CCdiag pin low.
5. At power-on after $V_{DD1}$ crosses the +4 V threshold, the ERROR flag is low for approximately 42 μs.
6. A supply voltage low (brown-out) condition lasts longer than 100 μs. Recovery is the same as power-up, either with or without a demag cycle.

## PROTECTION RECOMMENDATIONS

The inputs $IA_{IN1}$ and $IA_{IN2}$ require external protection to limit the voltage swing beyond 10 V of the supply voltage. The driver outputs $I_{COMP1}$ and $I_{COMP2}$ can handle high current pulses protected by internal clamp circuits to the supply voltage. If repeated over-currents of large magnitudes are expected, connect external Schottky diodes to the supply rails. This external protection prevents current flowing into the die.

The probe connections IS1 and IS2 are protected with diode clamps to the supply rails. In normal applications, no external protection is required. The maximum current must be limited to ±75 mA.

All other pins offer standard protection-see the Absolute Maximum Ratings table.

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## BASIC CONNECTION EXAMPLE

The circuit shown in Figure 8 offers an example of a fully-connected current sensor system.

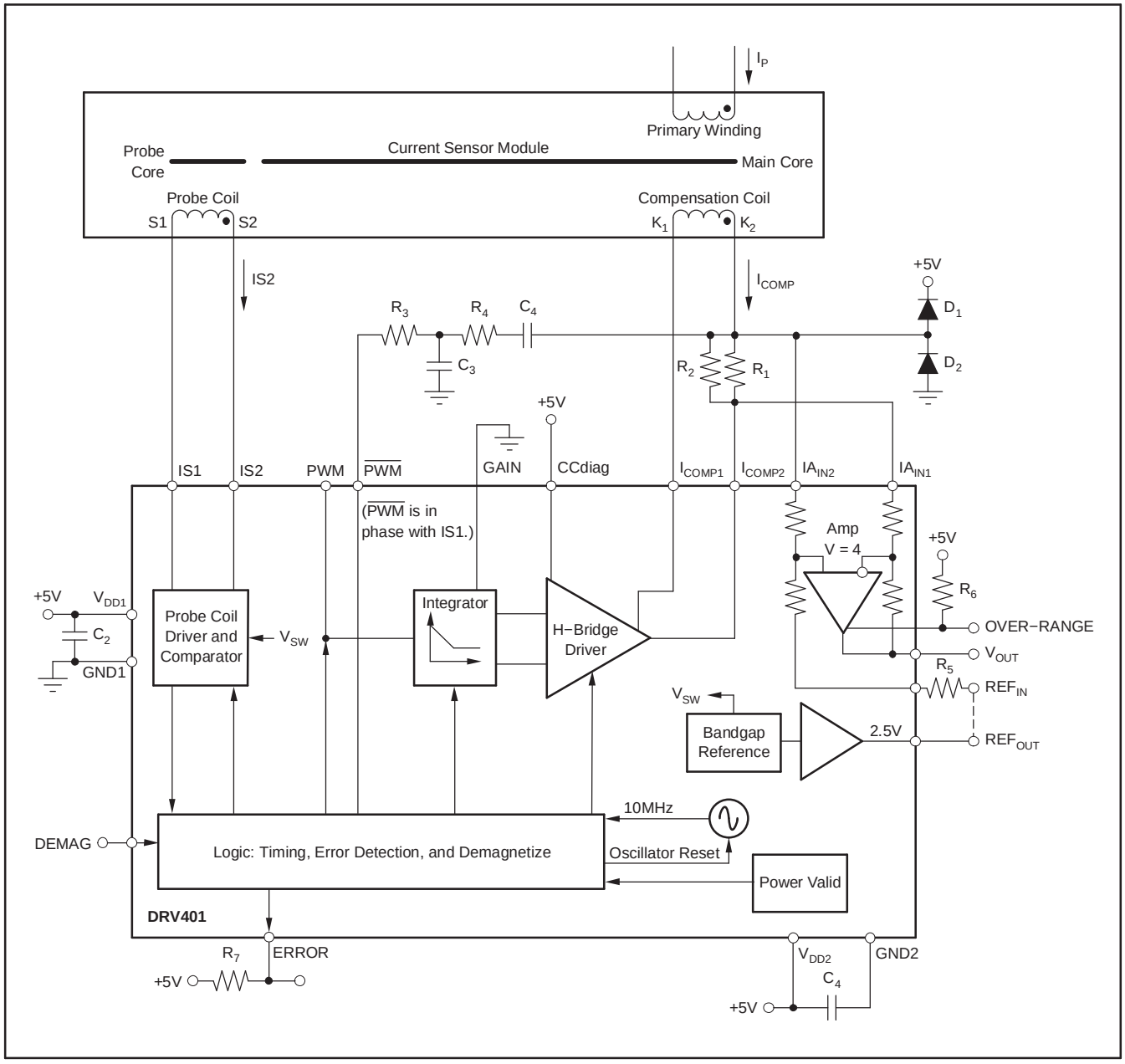



**Figure 8. Basic Connection Circuit**


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The connection example in Figure 8 illustrates the few external components required for optimal performance. Each component is described in the following list:

- **$I_P$** is the primary current to be measured; **$K_1$** and **$K_2$** connect to the compensation coil. **S1** and **S2** connect to the magnetic field probe. The dots indicate the winding direction on the sensor main core.
- **$R_1$** and **$R_2$** form the shunt resistor $R_{SHUNT}$. This resistance is split into two to allow for adjustments to the required $R_{SHUNT}$ value. The accuracy and temperature stability of these resistors are part of the final system performance.
- **$R_3$** and **$R_4$**, together with **$C_3$** and **$C_4$**, form a network that reduces the remaining probe oscillator ripple in the output signal. The component values depend on the sensor type and are tailored for best results. This network is not required for normal operation.
- **$R_5$** is the dummy shunt ($R_D$) resistor used to restore the symmetry of both differential amplifier inputs. $R_5 = 4 \times R_{SHUNT}$, but the accuracy is less important.
- **$R_6$** and **$R_7$** are pull-up resistors connected to the logic outputs.
- **$C_1$** and **$C_2$** are decoupling capacitors. Use low ESR-type capacitors connected close to the pins. Use low impedance printed circuit board (PCB) traces, either avoiding vias (plated-through holes) or using multiple vias. A combination of a large(> 1 μF) and a small (< 4.7 nF) capacitor are suggested. When selecting capacitors, make sure to consider the large pulse currents handled from the DRV401.
- **$D_1$** and **$D_2$** are protection diodes for the differential amplifier input. They are needed only if the voltage drop at $R_{SHUNT}$ exceeds 10 V at the maximum possible peak current.

## LAYOUT CONSIDERATIONS

The DRV401 operates with relatively large currents and fast current pulses, and offers wide-bandwidth performance. It is often exposed to large distortion energy from both the primary signal and the operating environment. Therefore, the wiring layout must provide shielding and low-impedance connections between critical points.

Use low ESR capacitors for power-supply decoupling. Use a combination of a small capacitor and a large capacitor of 1 μF or larger. Use low-impedance tracks to connect the capacitors to the pins.

Both grounds should be connected to a local ground plane. Both supplies can be connected together; however, best results are achieved with separate decoupling (to the local GND plane) and ferrite beads in series with the main supply. The ferrite beads decouple the DRV401, reducing interaction with other circuits powered from the same supply voltage source.

The reference output is referred to GND2. A low-impedance, star-type connection is required to avoid the driver current and the probe current modulating the voltage drop on the ground track.

The connection wires of the difference amplifier to the shunt must be low resistance and of equal length. For best accuracy, avoid current in this connection. Consider using a *Kelvin Contact*-type connection. The required resistance value can be set using two resistors.

Wires and PCB traces for S1 and S2 should be very close or twisted. $I_{COMP1}$ and $I_{COMP2}$ should also be wired close together. To avoid capacitive coupling, run a ground shield between the S1/S2 and ICOMP wire pair or keep them distant from each other.

The compensation driver outputs ($I_{COMP}$) are low frequency only; however, the primary signal (with high-frequency content present) is coupled into the compensation winding, the shunt, and the difference amplifier. Therefore, careful layout is recommended.

The output of $REF_{OUT}$ and $V_{OUT}$ can drive some capacitive loads, but avoid large direct capacitive loads; these loads increase internal pulse currents. Given the wide bandwidth of the differential amplifier, isolate any large capacitive load with a small series resistor. A small capacitor in the pF range can improve the transient response on a high resistive load.

The exposed thermal pad on the bottom of the package must be soldered to GND because it is internally connected to the substrate, which must be connected to the most negative potential. It is also necessary to solder the exposed pad to the PCB to provide structural integrity and long-term reliability.

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## POWER DISSIPATION

Using the thermally-enhanced PowerPAD™ SO package dramatically reduces the thermal impedance from junction to case. This package is constructed using a down-set lead frame upon which the die is mounted, as shown in Figure 9a and Figure 9b. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package. Figure 9 shows the SO-20 package as an example. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The two outputs $I_{COMP1}$ and $I_{COMP2}$ are linear outputs. Therefore, the power dissipation on each output is proportional to the current multiplied by the internal voltage drop on the active transistor. For $I_{COMP1}$ and $I_{COMP2}$, this internal voltage drop is the voltage drop to $V_{DD2}$ or GND, according to the current-conducting side of the output.

Output short-circuits are particularly critical for the driver because the full supply voltage can be seen across the conducting transistor, and the current is not limited by anything other than the current density limitation of the FET. Permanent damage to the device can occur.

The DRV401 does not include temperature protection or thermal shut-down.

## THERMAL PAD

Packages with an exposed thermal pad are specifically designed to provide excellent power dissipation, but board layout greatly influences overall heat dissipation. Table 1 shows the thermal resistance ($T_{JA}$) for the two packages with the exposed thermal pad soldered to a normal PCB, as described in Technical Brief SLMA002, *PowerPAD Thermally-Enhanced Package*. Documents are available for download at www.ti.com.

**Table 1. $\theta_{JA/JP}$ Estimations According to EIA/JED51-7**

| | SO–20 |
|---|---|
| $\theta_{JP}$ (1) | 9 |
| $\theta_{JA}$ (2) Still Air | 35 |
| $\theta_{JA}$ with Forced Airflow (150lfm (3)) | 32 |

(1) $\theta_{JP}$ = junction-to-pad thermal resistance,
(2) $\theta_{JA}$ = junction-to-ambient thermal resistance,
(3) lfm = linear foot per minute.

**NOTE:**

All thermal models have an accuracy 9≈20%.

Measuring the temperature as close as possible to the exposed thermal pad is recommended. The relatively low thermal impedance, $\theta_{JP}$, of less than 10°C/W (with some additional °C/W to the temperature test point on the PCB) allows good estimation of the junction temperature in the application.

The thermal pad on the PCB should contain nine or more vias for the SO package, where the solder pad on the PCB can be larger than the exposed pad (for example, 6.6 mm × 18 mm) as recommended in the application literature noted previously.

Component population, layout of traces, layers, and air flow strongly influence heat dissipation. Worst-case load conditions should be tested in the real environment to ensure proper thermal conditions. Minimize thermal stress for proper long-term operation with a junction temperature well below +125°C.


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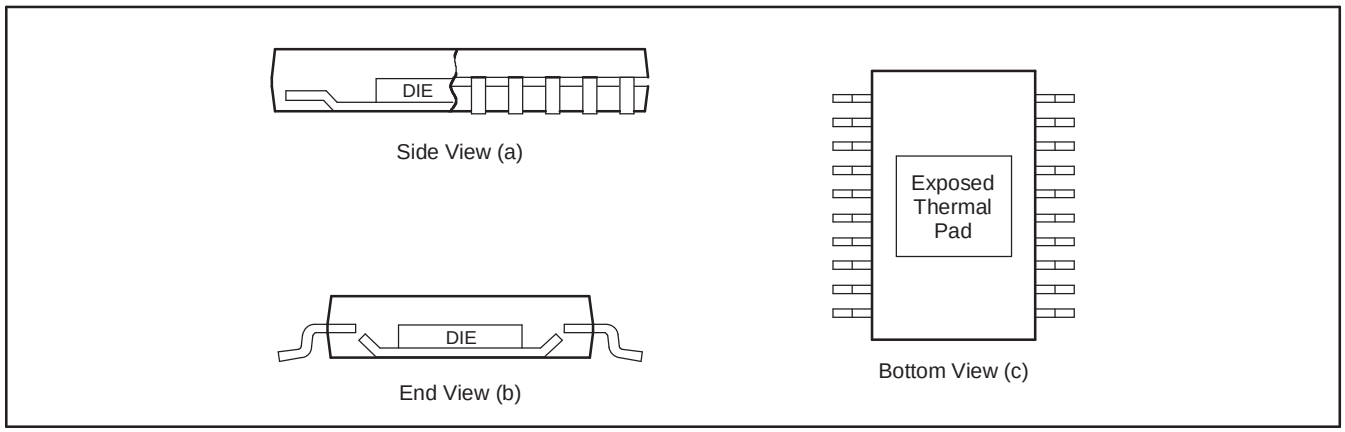



**Figure 9. SO-20 Package Example of Thermally Enhanced PowerPAD**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| DRV401AMDWPREP | ACTIVE | SO Power PAD | DWP | 20 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| V62/08630-01XE | ACTIVE | SO Power PAD | DWP | 20 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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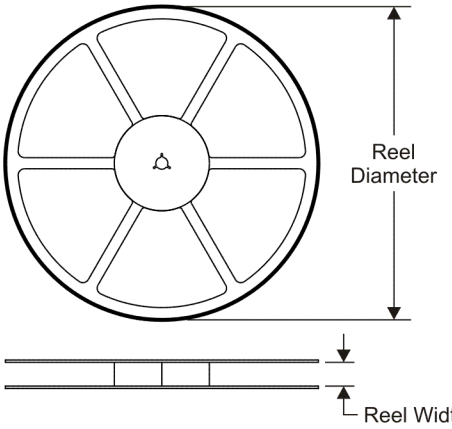
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**OTHER QUALIFIED VERSIONS OF DRV401-EP :**
- Catalog: DRV401

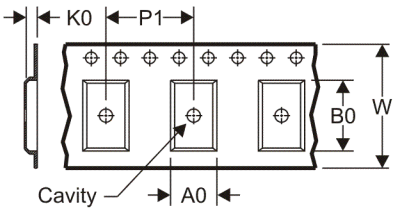
NOTE: Qualified Version Definitions:
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

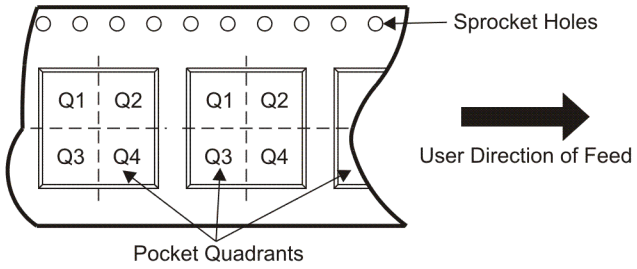



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

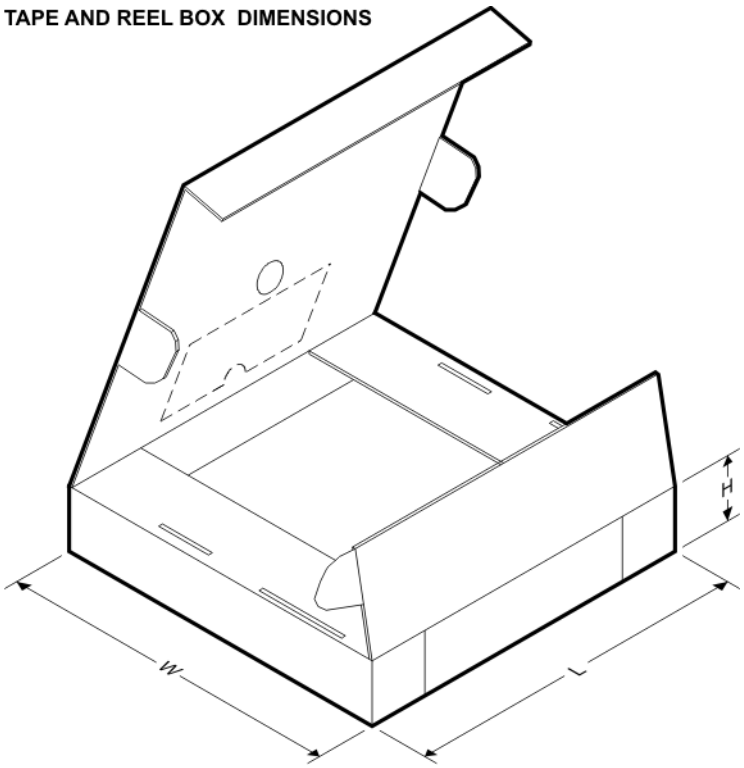
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV401AMDWPREP | SO Power PAD | DWP | 20 | 1000 | 330.0 | 24.4 | 10.8 | 13.0 | 2.7 | 12.0 | 24.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**

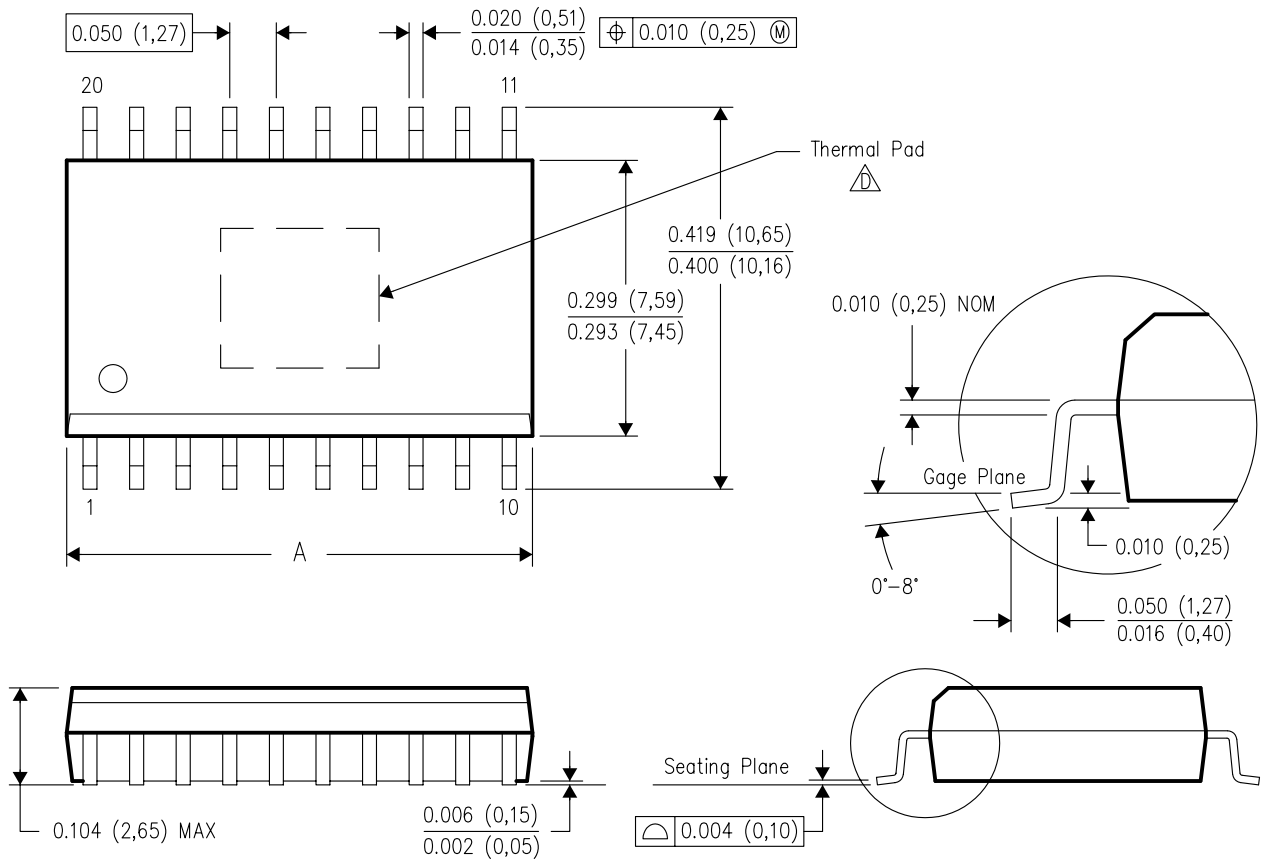



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DRV401AMDWPREP | SO PowerPAD | DWP | 20 | 1000 | 346.0 | 346.0 | 41.0 |

## DWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PINS SHOWN




| DIM \ PINS ** | 16 | 20 | 24 | 28 |
|---|---|---|---|---|
| A MAX | 0.410 (10,41) | 0.510 (12,95) | 0.610 (15,49) | 0.710 (18,03) |
| A MIN | 0.400 (10,16) | 0.500 (12,70) | 0.600 (15,24) | 0.700 (17,78) |

4147575/C 02/05

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.

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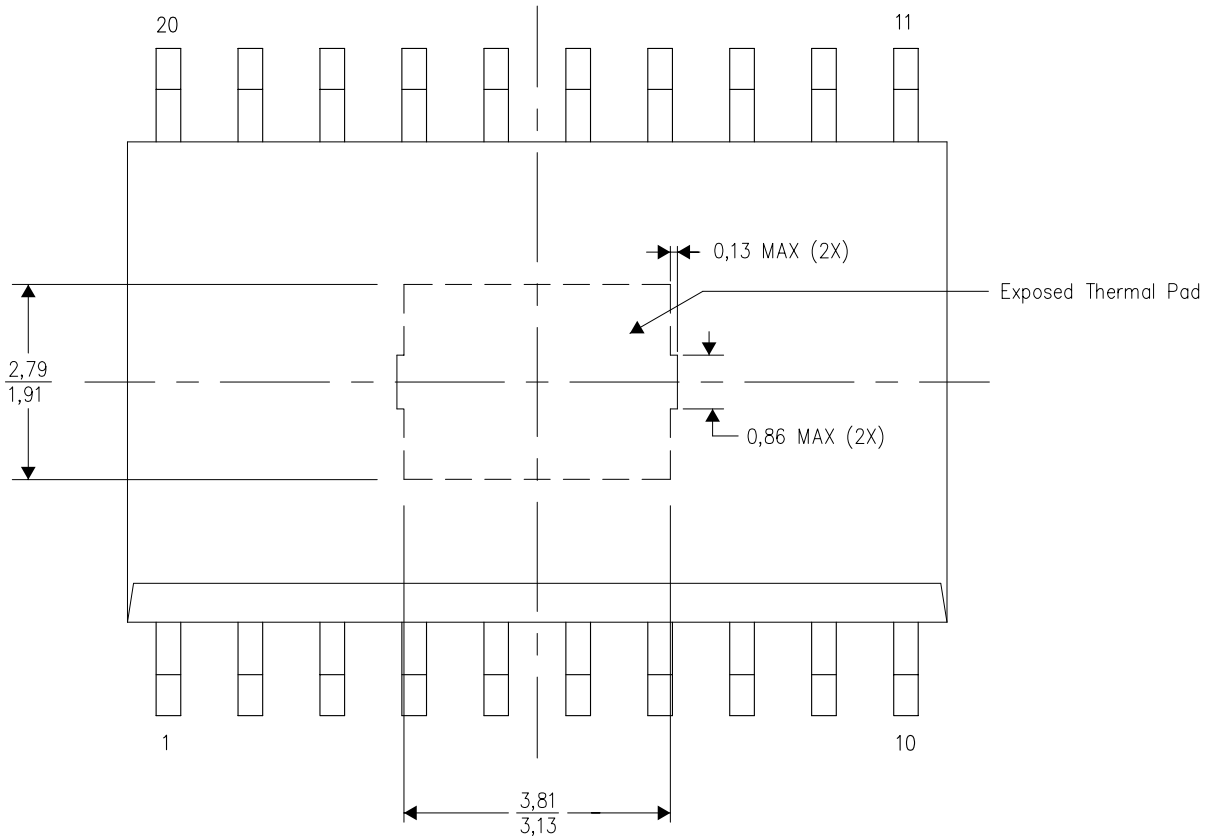
DWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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