SC16C750B

5 V, 3.3 V and 2.5 V UART with 64-byte FIFOs

Rev. 05 — 17 October 2008 Product data sheet

1. General description

The SC16C750B is a Universal Asynchronous Receiver and Transmitter (UART) used for serial data communications. Its principal function is to convert parallel data into serial data, and vice versa. The UART can handle serial data rates up to 3 Mbit/s.

The SC16C750B is pin compatible with the TL16C750 and it will power-up to be functionally equivalent to the 16C450. Programming of control registers enables the added features of the SC16C750B. Some of these added features are the 64-byte receive and transmit FIFOs, automatic hardware flow control. The selectable auto-flow control feature significantly reduces software overload and increases system efficiency while in FIFO mode by automatically controlling serial data flow using $\overline{RTS}$ output and $\overline{CTS}$ input signals. The SC16C750B also provides DMA mode data transfers through FIFO trigger levels and the $\overline{TXRDY}$ and $\overline{RXRDY}$ signals. On-board status registers provide the user with error indications, operational status, and modem interface control. System interrupts may be tailored to meet user requirements. An internal loopback capability allows on-board diagnostics.

The SC16C750B operates at 5 V, 3.3 V and 2.5 V, the industrial temperature range and is available in plastic PLCC44, LQFP64, and HVQFN32 packages.

2. Features

- Single channel
- 5 V, 3.3 V and 2.5 V operation
- 5 V tolerant on input only pins[1]
- Industrial temperature range (−40 °C to +85 °C)
- After reset, all registers are identical to the typical 16C450 register set
- Capable of running with all existing generic 16C450 software
- Pin compatibility with the industry-standard ST16C450/550, TL16C450/550, PC16C450/550. Software compatible with SC16C750 and TL16C750
- Up to 3 Mbit/s transmit/receive operation at 5 V, 2 Mbit/s at 3.3 V, and 1 Mbit/s at 2.5 V
- 64-byte transmit FIFO
- 64-byte receive FIFO with error flags
- Programmable auto-$\overline{RTS}$ and auto-$\overline{CTS}$
  - In auto-$\overline{CTS}$ mode, $\overline{CTS}$ controls transmitter
  - In auto-$\overline{RTS}$ mode, receive FIFO contents and threshold control $\overline{RTS}$
- Automatic hardware flow control
- Software selectable baud rate generator

1. For data bus pins D7 to D0, see Table 24 “Limiting values”.

NXP founded by Philips

- Four selectable Receive interrupt trigger levels
- Standard modem interface
- Sleep mode
- Standard asynchronous error and framing bits (Start, Stop, and Parity Overrun Break)
- Independent receiver clock input
- Transmit, Receive, Line Status, and data set interrupts independently controlled
- Fully programmable character formatting:
  - 5-bit, 6-bit, 7-bit, or 8-bit characters
  - Even, odd, or no-parity formats
  - 1, $1\frac{1}{2}$, or 2-stop bit
  - Baud generation (DC to 3 Mbit/s)
- False start-bit detection
- Complete status reporting capabilities
- 3-state output TTL drive capabilities for bidirectional data bus and control bus
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
- Prioritized interrupt system controls
- Modem control functions ($\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$, $\overline{DCD}$)

3. Ordering information

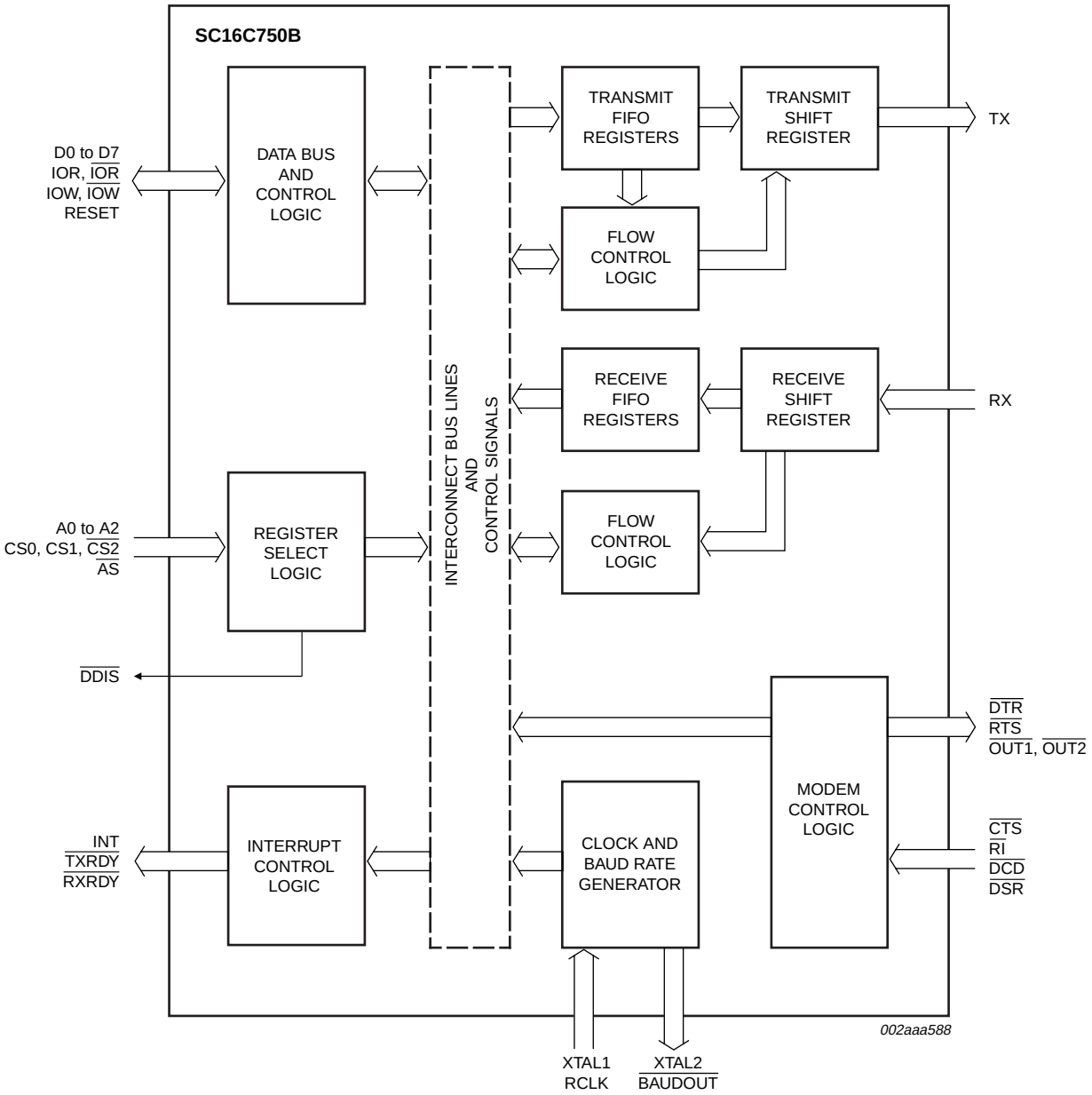
Table 1. Ordering information

Industrial: V_{CC} = 2.5 V, 3.3 V or 5 V ± 10 %; T_{amb} = −40 °C to +85 °C.

Type number	Package		
	Name	Description	Version
SC16C750BIA44	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2
SC16C750BIB64	LQFP64	plastic low profile quad flat package; 64 leads; 10 × 10 × 1.4 mm	SOT314-2
SC16C750BIBS	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-1

© NXP B.V. 2008. All rights reserved.

4. Block diagram



Shown for PLCC44 and LQFP64 pin assignments.

Fig 1. Block diagram of SC16C750B

© NXP B.V. 2008. All rights reserved.

5. Pinning information

5.1 Pinning

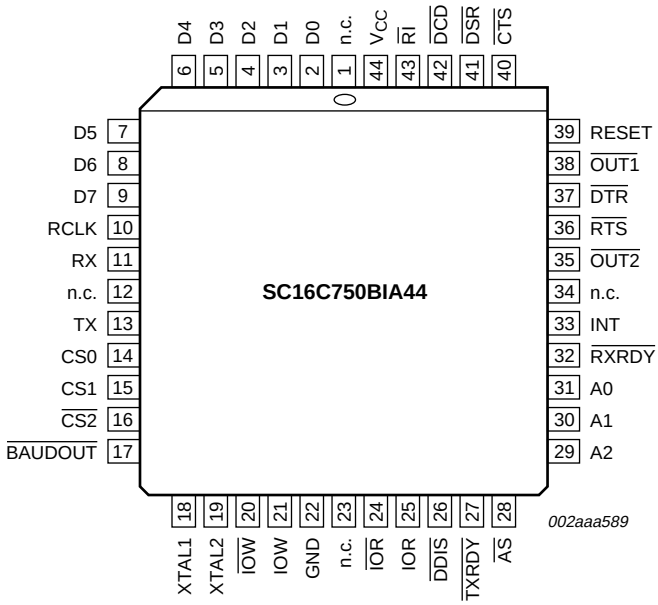


Fig 2. Pin configuration for PLCC44

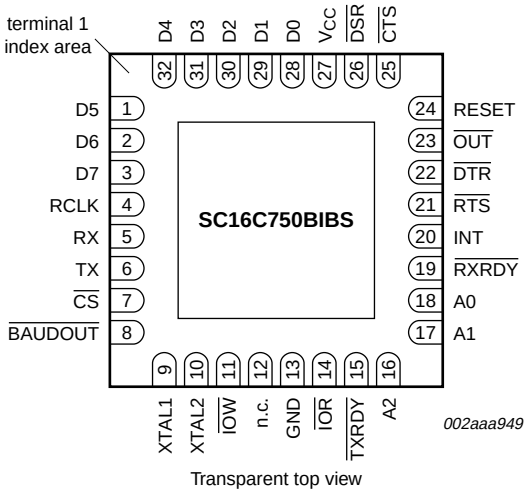


Fig 3. Pin configuration for HVQFN32

© NXP B.V. 2008. All rights reserved.

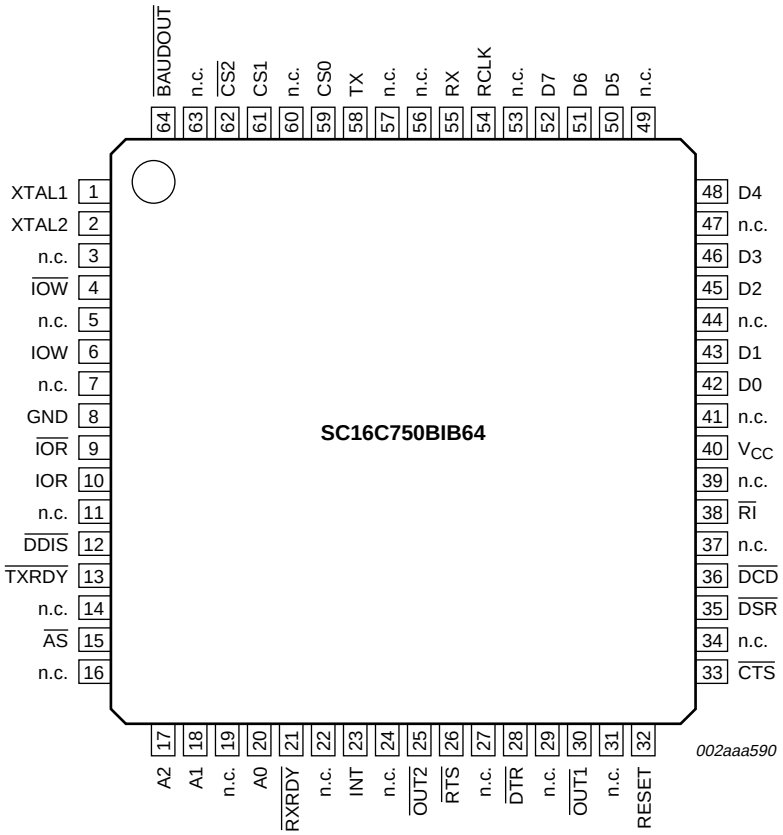


Fig 4. Pin configuration for LQFP64

5.2 Pin description

Table 2. Pin description

Symbol	Pin			Type	Description
	PLCC44	LQFP64	HVQFN32		
A2, A1, A0	29, 30, 31	17, 18, 20	16, 17, 18	I	**Register select.** A0 to A2 are used during read and write operations to select the UART register to read from or write to. Refer to Table 3 for register addresses and refer to $\overline{AS}$ description.
$\overline{AS}$	28	15	-	I	**Address strobe.** When $\overline{AS}$ is active (LOW), A0, A1, and A2 and CS0, CS1, and $\overline{CS2}$ drive the internal select logic directly; when $\overline{AS}$ is HIGH, the register select and chip select signals are held at the logic levels they were in when the LOW-to-HIGH transition of $\overline{AS}$ occurred.
$\overline{BAUDOUT}$	17	64	8	O	**Baud out.** $\overline{BAUDOUT}$ is a 16× clock signal for the transmitter section of the UART. The clock rate is established by the reference oscillator frequency divided by a divisor specified in the baud rate generator divisor latches. $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to RCLK.
CS0, CS1, $\overline{CS2}$	14, 15, 16	59, 61, 62	-	I	**Chip select.** When CS0 and CS1 are HIGH and $\overline{CS2}$ is LOW, these three inputs select the UART. When any of these inputs are inactive, the UART remains inactive (refer to $\overline{AS}$ description).
$\overline{CS}$	-	-	7	I	

© NXP B.V. 2008. All rights reserved.

Table 2. Pin description *...continued*

Symbol	Pin			Type	Description
	PLCC44	LQFP64	HVQFN32		
$\overline{CTS}$	40	33	25	I	**Clear to send.** $\overline{CTS}$ is a modem status signal. Its condition can be checked by reading bit 4 (CTS) of the Modem Status Register (MSR). MSR[3] ($\Delta\overline{CTS}$) indicates that $\overline{CTS}$ has changed states since the last read from the MSR. If the modem status interrupt is enabled when $\overline{CTS}$ changes levels and the auto-$\overline{CTS}$ mode is not enabled, an interrupt is generated. $\overline{CTS}$ is also used in the auto-$\overline{CTS}$ mode to control the transmitter.
D7 to D0	9, 8, 7, 6, 5, 4, 3, 2	52, 51, 50, 48, 46, 45, 43, 42	3, 2, 1, 32, 31, 30, 29, 28	I/O	**Data bus.** Eight data lines with 3-state outputs provide a bidirectional path for data, control and status information between the UART and the CPU.
$\overline{DCD}$	42	36	-	I	**Data carrier detect.** $\overline{DCD}$ is a modem status signal. Its condition can be checked by reading bit 7 (DCD) of the Modem Status Register (MSR). MSR[3] ($\Delta\overline{DCD}$) indicates that $\overline{DCD}$ has changed states since the last read from the MSR. If the modem status interrupt is enabled when $\overline{DCD}$ changes levels, an interrupt is generated.
$\overline{DDIS}$	26	12	-	O	**Driver disable.** $\overline{DDIS}$ is active (LOW) when the CPU is reading data. When inactive (HIGH), $\overline{DDIS}$ can disable an external transceiver.
$\overline{DSR}$	41	35	26	I	**Data set ready.** $\overline{DSR}$ is a modem status signal. Its condition can be checked by reading bit 5 (DSR) of the Modem Status Register. Bit 1 ($D\overline{DSR}$) of the MSR indicates $\overline{DSR}$ has changed levels since the last read from the MSR. If the modem status interrupt is enabled when $\overline{DSR}$ changes levels, an interrupt is generated.
$\overline{DTR}$	37	28	22	O	**Data terminal ready.** When active (LOW), $\overline{DTR}$ informs a modem or data set that the UART is ready to establish communication. $\overline{DTR}$ is placed in the active level by setting the $\overline{DTR}$ bit of the Modem Control Register. $\overline{DTR}$ is placed in the inactive level either as a result of a Master Reset, during Loopback mode operation, or clearing the $\overline{DTR}$ bit.
INT	33	23	20	O	**Interrupt.** When active (HIGH), INT informs the CPU that the UART has an interrupt to be serviced. Four conditions that cause an interrupt to be issued are: a receiver error, received data that is available or timed out (FIFO mode only), an empty transmitter holding register or an enabled modem status interrupt. INT is reset (deactivated) either when the interrupt is serviced or as a result of a Master Reset.
n.c.	34	3, 5, 7, 11, 14, 16, 19, 22, 24, 27, 29, 31, 34, 37, 39, 41, 44, 47, 49, 53, 56, 57, 60, 63	12	-	not connected
$\overline{OUT1}$, $\overline{OUT2}$	38, 35	30, 25	-	O	**Outputs 1 and 2.** These are user-designated output terminals that are set to the active (LOW) level by setting respective Modem Control Register (MCR) bits ($\overline{OUT1}$ and $\overline{OUT2}$). $\overline{OUT1}$ and $\overline{OUT2}$ are set to inactive the (HIGH) level as a result of Master Reset, during Loopback mode operations, or by clearing bit 2 ($\overline{OUT1}$) or bit 3 ($\overline{OUT2}$) of the MCR.
$\overline{OUT}$	-	-	23	O	

© NXP B.V. 2008. All rights reserved.

Table 2. Pin description *...continued*

Symbol	Pin			Type	Description
	PLCC44	LQFP64	HVQFN32		
RCLK	10	54	4	I	**Receiver clock.** RCLK is the 16× baud rate clock for the receiver section of the UART.
RESET	39	32	24	I	**Master Reset.** When active (HIGH), RESET clears most UART registers and sets the levels of various output signals.
IOR	25	10	-	I	**Read inputs.** When either $\overline{IOR}$ or IOR is active (LOW or HIGH, respectively) while the UART is selected, the CPU is allowed to read status information or data from a selected UART register. Only one of these inputs is required for the transfer of data during a read operation; the other input should be tied to its inactive level (that is, IOR tied LOW or $\overline{IOR}$ tied HIGH).
$\overline{IOR}$	24	9	14	I	
$\overline{RI}$	43	38	-	I	**Ring indicator.** $\overline{RI}$ is a modem status signal. Its condition can be checked by reading bit 6 (RI) of the Modem Status Register. Bit 2 ($\Delta\overline{RI}$) of the MSR indicates that $\overline{RI}$ has changed from a LOW to a HIGH level since the last read from the MSR. If the modem status interrupt is enabled when this transition occurs, an interrupt is generated.
$\overline{RTS}$	36	26	21	O	**Request to send.** When active, $\overline{RTS}$ informs the modem or data set that the UART is ready to receive data. $\overline{RTS}$ is set to the active level by setting the $\overline{RTS}$ Modem Control Register bit and is set to the inactive (HIGH) level either as a result of a Master Reset or during Loopback mode operations or by clearing bit 1 ($\overline{RTS}$) of the MCR. In the auto-$\overline{RTS}$ mode, $\overline{RTS}$ is set to the inactive level by the receiver threshold control logic.
$\overline{RXRDY}$	32	21	19	O	**Receiver ready.** Receiver Direct Memory Access (DMA) signaling is available with $\overline{RXRDY}$. When operating in the FIFO mode, one of two types of DMA signaling can be selected using the FIFO Control Register bit 3 (FCR[3]). When operating in the 16C450 mode, only DMA mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multi-transfer DMA in which multiple transfers are made continuously until the receiver FIFO has been emptied. In DMA mode 0 (FCR[0] = 0 or FCR[0] = 1, FCR[3] = 0), when there is at least one character in the receiver FIFO or receiver holding register, $\overline{RXRDY}$ is active (LOW). When $\overline{RXRDY}$ has been active but there are no characters in the FIFO or holding register, $\overline{RXRDY}$ goes inactive (HIGH). In DMA mode 1 (FCR[0] = 1, FCR[3] = 1), when the trigger level or the time-out has been reached, $\overline{RXRDY}$ goes active (LOW); when it has been active but there are no more characters in the FIFO or holding register, it goes inactive (HIGH).
RX	11	55	5	I	**Serial data input.** RX is serial data input from a connected communications device.
TX	13	58	6	O	**Serial data output.** TX is composite serial data output to a connected communication device. TX is set to the marking (HIGH) level as a result of Master Reset.

© NXP B.V. 2008. All rights reserved.

Table 2. Pin description *...continued*

Symbol	Pin			Type	Description
	PLCC44	LQFP64	HVQFN32		
$\overline{TXRDY}$	27	13	15	O	**Transmitter ready.** Transmitter DMA signaling is available with $\overline{TXRDY}$. When operating in the FIFO mode, one of two types of DMA signaling can be selected using FCR[3]. When operating in the 16C450 mode, only DMA mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multi-transfer DMA in which multiple transfers are made continuously until the transmit FIFO has been filled.
V_{CC}	44	40	27	Power	**2.5 V, 3 V or 5 V supply voltage.**
GND	22	8	13	Power	**Ground voltage.**
IOW	21	6	-	I	**Write inputs.** When either $\overline{IOW}$ or IOW is active (LOW or HIGH, respectively) and while the UART is selected, the CPU is allowed to write control words or data into a selected UART register. Only one of these inputs is required to transfer data during a write operation; the other input should be tied to its inactive level (that is, IOW tied LOW or $\overline{IOW}$ tied HIGH).
$\overline{IOW}$	20	4	11	I	
XTAL1	18	1	9	I	**Crystal connection or External clock input.**
XTAL2[1]	19	2	10	O	**Crystal connection or the inversion of XTAL1 if XTAL1 is driven.**

[1] In Sleep mode, XTAL2 is left floating.

6. Functional description

The SC16C750B provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stop bits to the transmit data to form a data character (character orientated protocol). Data integrity is insured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The SC16C750B is fabricated with an advanced CMOS process to achieve low drain power and high speed requirements.

The SC16C750B is an upward solution that provides 64 bytes of transmit and receive FIFO memory, instead of none in the 16C450, or 16 bytes in the 16C550. The SC16C750B is designed to work with high speed modems and shared network environments that require fast data processing time. Increased performance is realized in the SC16C750B by the larger transmit and receive FIFOs. This allows the external processor to handle more networking tasks within a given time. In addition, the four selectable levels of FIFO trigger interrupt and automatic hardware flow control is uniquely provided for maximum data throughput performance, especially when operating in a multi-channel environment. The combination of the above greatly reduces the bandwidth requirement of the external controlling CPU, increases performance, and reduces power consumption.

The SC16C750B is capable of operation up to 3 Mbit/s with a 48 MHz external clock input (at 5 V).

© NXP B.V. 2008. All rights reserved.

The rich feature set of the SC16C750B is available through internal registers. Automatic hardware flow control, selectable transmit and receive FIFO trigger level, selectable TX and RX baud rates, modem interface controls, and a sleep mode are some of these features.

6.1 Internal registers

The SC16C750B provides 12 internal registers for monitoring and control. These registers are shown in Table 3. These twelve registers are similar to those already available in the standard 16C550. These registers function as data holding registers (THR/RHR), interrupt status and control registers (IER/ISR), a FIFO Control Register (FCR), line status and control registers (LCR/LSR), modem status and control registers (MCR/MSR), programmable data rate (clock) control registers (DLL/DLM), and a user accessible Scratchpad Register (SPR). Register functions are more fully described in the following paragraphs.

Table 3. Internal registers decoding

A2	A1	A0	READ mode	WRITE mode
General register set (THR/RHR, IER/ISR, MCR/MSR, FCR, LSR, SPR)[1]				
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1	Interrupt Enable Register	Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1	Line Control Register	Line Control Register
1	0	0	Modem Control Register	Modem Control Register
1	0	1	Line Status Register	n/a
1	1	0	Modem Status Register	n/a
1	1	1	Scratchpad Register	Scratchpad Register
Baud rate register set (DLL/DLM)[2]				
0	0	0	LSB of Divisor Latch	LSB of Divisor Latch
0	0	1	MSB of Divisor Latch	MSB of Divisor Latch

[1] These registers are accessible only when LCR[7] is a logic 0.

[2] These registers are accessible only when LCR[7] is a logic 1.

© NXP B.V. 2008. All rights reserved.

6.2 FIFO operation

The 64-byte transmit and receive data FIFOs are enabled by the FIFO Control Register bit 0 (FCR[0]). The receiver FIFO section includes a time-out function to ensure data is delivered to the external CPU. An interrupt is generated whenever the Receive Holding Register (RHR) has not been read following the loading of a character or the receive trigger level has not been reached.

Table 4. Flow control mechanism

Selected trigger level (characters)	INT pin activation	Negate $\overline{RTS}$	Assert $\overline{RTS}$
16-byte FIFO			
1	1	1	0
4	4	4	0
8	8	8	0
14	14	14	0
64-byte FIFO			
1	1	1	0
16	16	16	0
32	32	32	0
56	56	56	0

6.3 Hardware flow control

When automatic hardware flow control is enabled, the SC16C750B monitors the $\overline{CTS}$ pin for a remote buffer overflow indication and controls the $\overline{RTS}$ pin for local buffer overflows. Automatic hardware flow control is selected by setting MCR[5] (RTS) and MCR[1] (CTS) to a logic 1. If $\overline{CTS}$ transitions from a logic 0 to a logic 1 indicating a flow control request, the SC16C750B will suspend TX transmissions as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the $\overline{CTS}$ input returns to a logic 0, indicating more data may be sent.

With the auto-$\overline{RTS}$ function enabled, an interrupt is generated when the receive FIFO reaches the programmed trigger level. The $\overline{RTS}$ pin will not be forced to a logic 1 (RTS off), until the receive FIFO reaches the next trigger level. However, the $\overline{RTS}$ pin will return to a logic 0 after the data buffer (FIFO) is emptied. However, under the above described conditions, the SC16C750B will continue to accept data until the receive FIFO is full.

6.4 Time-out interrupts

When two interrupt conditions have the same priority, it is important to service these interrupts correctly. Receive Data Ready and Receive Time-Out have the same interrupt priority (when enabled by IER[0]). The receiver issues an interrupt after the number of characters have reached the programmed trigger level. In this case, the SC16C750B FIFO may hold more characters than the programmed trigger level. Following the removal of a data byte, the user should re-check LSR[0] for additional characters. A Receive Time-Out will not occur if the receive FIFO is empty. The time-out counter is reset at the center of each stop bit received or each time the receive holding register (RHR) is read. The actual time-out value is 4 character time.

© NXP B.V. 2008. All rights reserved.

6.5 Programmable baud rate generator

The SC16C750B supports high speed modem technologies that have increased input data rates by employing data compression schemes. For example, a 33.6 kbit/s modem that employs data compression may require a 115.2 kbit/s input data rate. A 128.0 kbit/s ISDN modem that supports data compression may need an input data rate of 460.8 kbit/s.

A single baud rate generator is provided for the transmitter and receiver, allowing independent TX/RX channel control. The programmable baud rate generator is capable of accepting an input clock up to 48 MHz, as required for supporting a 3 Mbit/s data rate. The SC16C750B can be configured for internal or external clock operation. For internal clock oscillator operation, an industry standard microprocessor crystal (parallel resonant, 22 pF to 33 pF load) is connected externally between the XTAL1 and XTAL2 pins (see Figure 5). Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates (see Table 5).

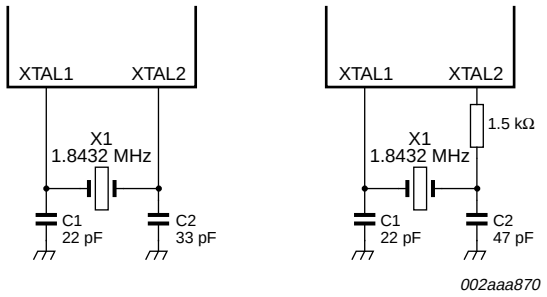


Fig 5. Crystal oscillator connection

The generator divides the input 16× clock by any divisor from 1 to ($2^{16} - 1$). The SC16C750B divides the basic crystal or external clock by 16. The frequency of the $\overline{\text{BAUDOUT}}$ output pin is exactly 16× (16 times) of the selected baud rate (BAUDOUT = 16 Baud Rate). Customized baud rates can be achieved by selecting the proper divisor values for the MSB and LSB sections of baud rate generator.

Programming the baud rate generator registers DLM (MSB) and DLL (LSB) provides a user capability for selecting the desired final baud rate. The example in Table 5 shows selectable baud rates when using a 1.8432 MHz crystal.

For custom baud rates, the divisor value can be calculated using Equation 1:

$$divisor\ (in\ decimal) = \frac{XTAL1\ clock\ frequency}{serial\ data\ rate \times 16} \quad (1)$$

© NXP B.V. 2008. All rights reserved.

Table 5. Baud rates using 1.8432 MHz or 3.072 MHz crystal

Using 1.8432 MHz crystal			Using 3.072 MHz crystal		
Desired baud rate	Divisor for 16× clock	Baud rate error	Desired baud rate	Divisor for 16× clock	Baud rate error
50	2304		50	3840	
75	1536		75	2560	
110	1047	0.026	110	1745	0.026
134.5	857	0.058	134.5	1428	0.034
150	768		150	1280	
300	384		300	640	
600	192		600	320	
1200	96		1200	160	
1800	64		1800	107	0.312
2000	58	0.69	2000	96	
2400	48		2400	80	
3600	32		3600	53	0.628
4800	24		4800	40	
7200	16		7200	27	1.23
9600	12		9600	20	
19200	6		19200	10	
38400	3		38400	5	
56000	2	2.86			

6.6 DMA operation

The SC16C750B FIFO trigger level provides additional flexibility to the user for block mode operation. The user can optionally operate the transmit and receive FIFOs in the DMA mode (FCR[3]). The DMA mode affects the state of the $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ output pins. Table 6 and Table 7 show this.

Table 6. Effect of DMA mode on state of $\overline{\text{RXRDY}}$ pin

Non-DMA mode	DMA mode
1 = FIFO empty	0-to-1 transition when FIFO empties
0 = at least 1 byte in FIFO	1-to-0 transition when FIFO reaches trigger level, or time-out occurs

Table 7. Effect of DMA mode on state of $\overline{\text{TXRDY}}$ pin

Non-DMA mode	DMA mode
1 = at least 1 byte in FIFO	0-to-1 transition when FIFO becomes full
0 = FIFO empty	1-to-0 transition when FIFO becomes empty

© NXP B.V. 2008. All rights reserved.

6.7 Sleep mode

The SC16C750B is designed to operate with low power consumption. A special Sleep mode is included to further reduce power consumption (the internal oscillator driver is disabled) when the chip is not being used. With IER[4] enabled (set to a logic 1), the SC16C750B enters the Sleep mode, but resumes normal operation when a start bit is detected, a change of state of RX or on any of the modem input pins $\overline{RI}$, $\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, or a transmit data is provided by the user. If the Sleep mode is enabled and the SC16C750B is awakened by one of the conditions described above, it will return to the Sleep mode automatically after the last character is transmitted or read by the user. In any case, the Sleep mode will not be entered while an interrupt(s) is pending. The SC16C750B will stay in the Sleep mode of operation until it is disabled by setting IER[4] to a logic 0.

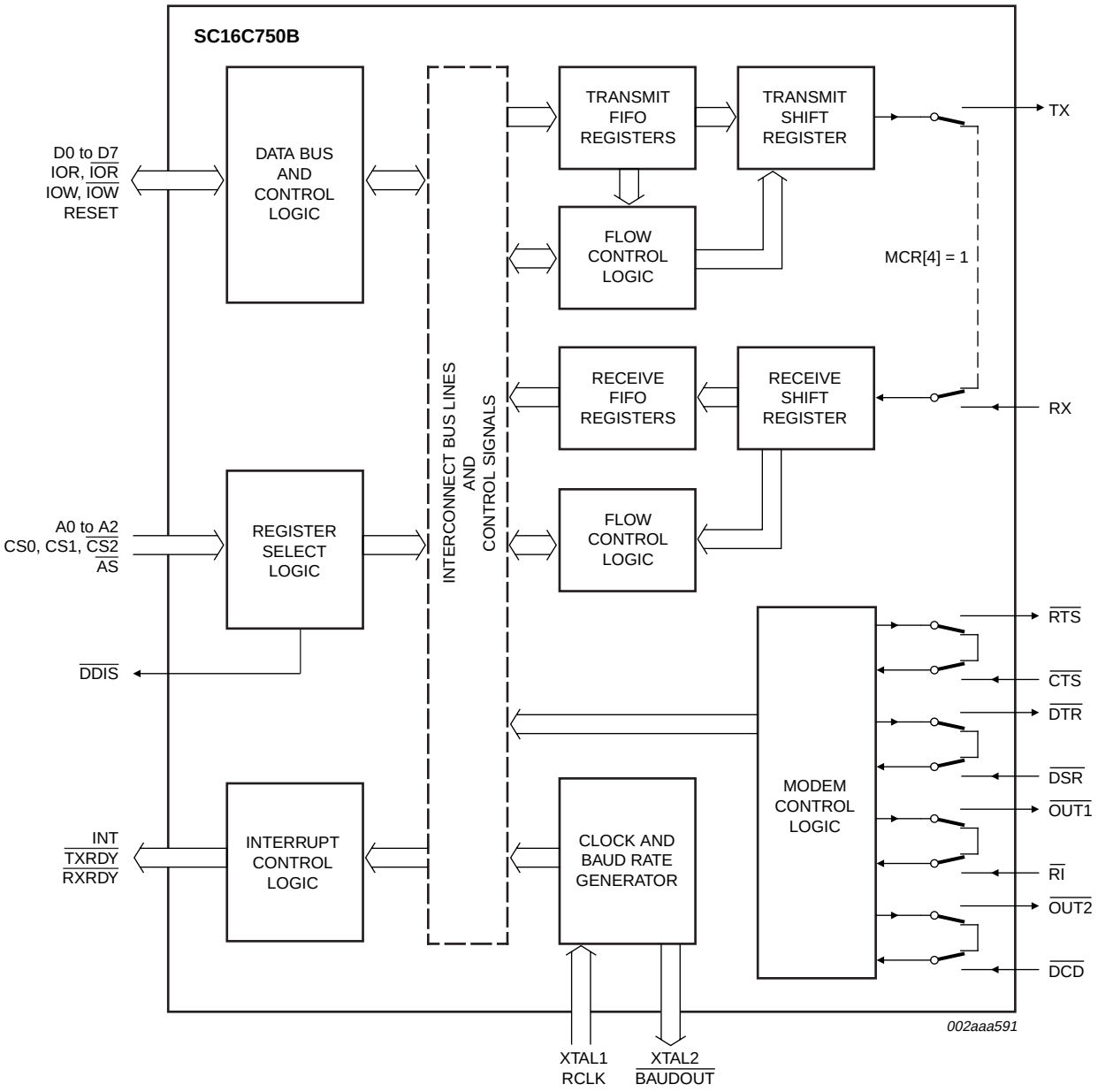
6.8 Low power mode

In Low power mode the oscillator is still running and only the clock to the UART core is cut off. This helps to reduce the operating current to about $\frac{1}{3}$. The UART wakes up under the same conditions as in Sleep mode.

6.9 Loopback mode

The internal loopback capability allows on-board diagnostics. In the Loopback mode, the normal modem interface pins are disconnected and reconfigured for loopback internally. MCR[3:0] register bits are used for controlling loopback diagnostic testing. In the Loopback mode, OUT1 and OUT2 in the MCR register (bit 2 and bit 3) control the modem $\overline{RI}$ and $\overline{DCD}$ inputs, respectively. MCR signals $\overline{DTR}$ and $\overline{RTS}$ (bit 0 and bit 1) are used to control the modem $\overline{DSR}$ and $\overline{CTS}$ inputs, respectively. The transmitter output (TX) and the receiver input (RX) are disconnected from their associated interface pins, and instead are connected together internally (see Figure 6). The $\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$ are disconnected from their normal modem control input pins, and instead are connected internally to $\overline{RTS}$, $\overline{DTR}$, $\overline{OUT2}$ and $\overline{OUT1}$. Loopback test data is entered into the Transmit Holding Register via the user data bus interface, D0 to D7. The transmit UART serializes the data and passes the serial data to the receive UART via the internal loopback connection. The receive UART converts the serial data back into parallel data that is then made available at the user data interface D0 to D7. The user optionally compares the received data to the initial transmitted data for verifying error-free operation of the UART TX/RX circuits.

© NXP B.V. 2008. All rights reserved.



Shown for PLCC44 and LQFP64 pin assignments.

Fig 6. Internal Loopback mode diagram

© NXP B.V. 2008. All rights reserved.

7. Register descriptions

Table 8 details the assigned bit functions for the fifteen SC16C750B internal registers. The assigned bit functions are more fully defined in Section 7.1 through Section 7.10.

Table 8. SC16C750B internal registers

A2	A1	A0	Register	Default[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
General Register Set[2]												
0	0	0	RHR	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	0	THR	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	1	IER	00	0	0	Low power mode	Sleep mode	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0	1	0	FCR	00	RCVR trigger (MSB)	RCVR trigger (LSB)	64-byte FIFO enable	reserved	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0	1	0	ISR	01	FIFOs enabled	FIFOs enabled	64-byte FIFO enable	0	INT priority bit 2	INT priority bit 1	INT priority bit 0	INT status
0	1	1	LCR	00	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit 1	word length bit 0
1	0	0	MCR	00	0	0	flow control enable	loopback	$\overline{OUT2}$	$\overline{OUT1}$	$\overline{RTS}$	$\overline{DTR}$
1	0	1	LSR	60	FIFO data error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1	1	0	MSR	X0	DCD	RI	DSR	CTS	$\Delta\overline{DCD}$	$\Delta\overline{RI}$	$\Delta\overline{DSR}$	$\Delta\overline{CTS}$
1	1	1	SPR	FF	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Special Register Set[3]												
0	0	0	DLL	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	1	DLM	XX	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8

[1] The value shown represents the register's initialized HEX value; X = n/a.

[2] These registers are accessible only when LCR[7] = 0.

[3] The Special Register set is accessible only when LCR[7] is set to a logic 1.

© NXP B.V. 2008. All rights reserved.

7.1 Transmit Holding Register (THR) and Receive Holding Register (RHR)

The serial transmitter section consists of an 8-bit Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the THR is provided in the Line Status Register (LSR). Writing to the THR transfers the contents of the data bus (D7 to D0) to the THR, providing that the THR or TSR is empty. The THR empty flag in the LSR register will be set to a logic 1 when the transmitter is empty or when data is transferred to the TSR. Note that a write operation can be performed when the THR empty flag is set (logic 0 = FIFO full; logic 1 = at least one FIFO location available).

The serial receive section also contains an 8-bit Receive Holding Register (RHR). Receive data is removed from the SC16C750B and receive FIFO by reading the RHR register. The receive section provides a mechanism to prevent false starts. On the falling edge of a start or false start bit, an internal receiver counter starts counting clocks at the 16× clock rate. After $7\frac{1}{2}$ clocks, the start bit time should be shifted to the center of the start bit. At this time the start bit is sampled, and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. Receiver status codes will be posted in the LSR.

7.2 Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) masks the interrupts from receiver ready, transmitter empty, line status and modem status registers. These interrupts would normally be seen on the INT output pin.

Table 9. Interrupt Enable Register bits description

Bit	Symbol	Description
7:6	IER[7:6]	Not used.
5	IER[5]	Low power mode. logic 0 = disable Low power mode (normal default condition) logic 1 = enable Low power mode
4	IER[4]	Sleep mode. logic 0 = disable Sleep mode (normal default condition) logic 1 = enable Sleep mode. See Section 6.7 “Sleep mode” for details.
3	IER[3]	Modem Status Interrupt. logic 0 = disable the modem status register interrupt (normal default condition) logic 1 = enable the modem status register interrupt
2	IER[2]	Receive Line Status interrupt. This interrupt will be issued whenever a fully assembled receive character is transferred from RSR to the RHR/FIFO, i.e., data ready, LSR[0]. logic 0 = disable the receiver line status interrupt (normal default condition) logic 1 = enable the receiver line status interrupt

© NXP B.V. 2008. All rights reserved.

Table 9. Interrupt Enable Register bits description *…continued*

Bit	Symbol	Description
1	IER[1]	Transmit Holding Register interrupt. This interrupt will be issued whenever the THR is empty, and is associated with LSR[1]. logic 0 = disable the transmitter empty interrupt (normal default condition) logic 1 = enable the transmitter empty interrupt
0	IER[0]	Receive Holding Register interrupt. This interrupt will be issued when the FIFO has reached the programmed trigger level, or is cleared when the FIFO drops below the trigger level in the FIFO mode of operation. logic 0 = disable the receiver ready interrupt (normal default condition) logic 1 = enable the receiver ready interrupt

7.2.1 IER versus Receive FIFO interrupt mode operation

When the receive FIFO (FCR[0] = logic 1), and receive interrupts (IER[0] = logic 1) are enabled, the receive interrupts and register status will reflect the following:

- The receive data available interrupts are issued to the external CPU when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.
- FIFO status will also be reflected in the user accessible ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.
- The data ready bit (LSR[0]) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

7.2.2 IER versus Receive/Transmit FIFO polled mode operation

When FCR[0] = logic 1, resetting IER[3:0] enables the SC16C750B in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR, either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

- LSR[0] will be a logic 1 as long as there is one byte in the receive FIFO.
- LSR[4:1] will provide the type of errors encountered, if any.
- LSR[5] will indicate when the transmit FIFO is empty.
- LSR[6] will indicate when both the transmit FIFO and transmit shift register are empty.
- LSR[7] will indicate any FIFO data errors.

© NXP B.V. 2008. All rights reserved.

7.3 FIFO Control Register (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receive FIFO trigger levels, and select the DMA mode.

7.3.1 DMA mode

7.3.1.1 Mode 0 (FCR bit 3 = 0)

Set and enable the interrupt for each single transmit or receive operation, and is similar to the 16C450 mode. Transmit Ready ($\overline{\text{TXRDY}}$) will go to a logic 0 whenever an empty transmit space is available in the Transmit Holding Register (THR). Receive Ready ($\overline{\text{RXRDY}}$) will go to a logic 0 whenever the Receive Holding Register (RHR) is loaded with a character.

7.3.1.2 Mode 1 (FCR bit 3 = 1)

Set and enable the interrupt in a block mode operation. The transmit interrupt is set when the transmit FIFO is below the programmed trigger level. The receive interrupt is set when the receive FIFO fills to the programmed trigger level. However, the FIFO continues to fill regardless of the programmed level until the FIFO is full. $\overline{\text{RXRDY}}$ remains a logic 0 as long as the FIFO fill level is above the programmed trigger level.

7.3.2 FIFO mode

Table 10. FIFO Control Register bits description

Bit	Symbol	Description
7:6	FCR[7] (MSB), FCR[6] (LSB)	RCVR trigger. These bits are used to set the trigger level for the receive FIFO interrupt. An interrupt is generated when the number of characters in the FIFO equals the programmed trigger level. However, the FIFO will continue to be loaded until it is full. Refer to Table 11.
5	FCR[5]	64-byte FIFO enable. logic 0 = 16-byte mode (normal default condition) logic 1 = 64-byte mode
4	FCR[4]	reserved
3	FCR[3]	DMA mode select. logic 0 = set DMA mode ‘0’ (normal default condition). logic 1 = set DMA mode ‘1’ **Transmit operation in mode ‘0’:** When the SC16C750B is in the 16C450 mode (FIFOs disabled; FCR[0] = logic 0) or in the FIFO mode (FIFOs enabled; FCR[0] = logic 1; FCR[3] = logic 0), and when there are no characters in the transmit FIFO or transmit holding register, the $\overline{\text{TXRDY}}$ pin will be a logic 0. Once active, the $\overline{\text{TXRDY}}$ pin will go to a logic 1 after the first character is loaded into the transmit holding register. **Receive operation in mode ‘0’:** When the SC16C750B is in 16C450 mode, or in the FIFO mode (FCR[0] = logic 1; FCR[3] = logic 0) and there is at least one character in the receive FIFO, the $\overline{\text{RXRDY}}$ pin will be a logic 0. Once active, the $\overline{\text{RXRDY}}$ pin will go to a logic 1 when there are no more characters in the receiver.

© NXP B.V. 2008. All rights reserved.

Table 10. FIFO Control Register bits description *…continued*

Bit	Symbol	Description
	FCR[3] (continued)	**Transmit operation in mode '1':** When the SC16C750B is in FIFO mode (FCR[0] = logic 1; FCR[3] = logic 1), the $\overline{\text{TXRDY}}$ pin will be a logic 1 when the transmit FIFO is completely full. It will be a logic 0 when the FIFO is emptied. **Receive operation in mode '1':** When the SC16C750B is in FIFO mode (FCR[0] = logic 1; FCR[3] = logic 1) and the trigger level has been reached, or a Receive Time-Out has occurred, the $\overline{\text{RXRDY}}$ pin will go to a logic 0. Once activated, it will go to a logic 1 after there are no more characters in the FIFO.
2	FCR[2]	XMIT FIFO reset. logic 0 = no FIFO transmit reset (normal default condition) logic 1 = clears the contents of the transmit FIFO and resets the FIFO counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.
1	FCR[1]	RCVR FIFO reset. logic 0 = no FIFO receive reset (normal default condition) logic 1 = clears the contents of the receive FIFO and resets the FIFO counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.
0	FCR[0]	FIFO enable. logic 0 = disable the transmit and receive FIFO (normal default condition) logic 1 = enable the transmit and receive FIFO

Table 11. RCVR trigger levels

FCR[7]	FCR[6]	RX FIFO trigger level (bytes)	
		16-byte operation	64-byte operation
0	0	1	1
0	1	4	16
1	0	8	32
1	1	14	56

© NXP B.V. 2008. All rights reserved.

7.4 Interrupt Status Register (ISR)

The SC16C750B provides four levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with four interrupt status bits. Performing a read cycle on the ISR will provide the user with the highest pending interrupt level to be serviced. No other interrupts are acknowledged until the pending interrupt is serviced. Whenever the interrupt status register is read, the interrupt status is cleared. However, it should be noted that only the current pending interrupt is cleared by the read. A lower level interrupt may be seen after re-reading the interrupt status bits. Table 12 “Interrupt source” shows the data values (bit 0 to bit 4) for the four prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels.

Table 12. Interrupt source

Priority level	ISR[3]	ISR[2]	ISR[1]	ISR[0]	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2	1	1	0	0	RXRDY (Receive Data time-out)
3	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

Table 13. Interrupt Status Register bits description

Bit	Symbol	Description
7:6	ISR[7:6]	FIFOs enabled. These bits are set to a logic 0 when the FIFO is not being used. They are set to a logic 1 when the FIFOs are enabled. logic 0 or cleared = default condition
5	ISR[5]	64-byte FIFO enable. logic 0 = 16-byte operation logic 1 = 64-byte operation
4	ISR[4]	not used
3:1	ISR[3:1]	INT priority bit 2 to bit 0. These bits indicate the source for a pending interrupt at interrupt priority levels 1, 2, and 3 (see Table 12). logic 0 or cleared = default condition
0	ISR[0]	INT status. logic 0 = an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine logic 1 = no interrupt pending (normal default condition)

© NXP B.V. 2008. All rights reserved.

7.5 Line Control Register (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The word length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

Table 14. Line Control Register bits description

Bit	Symbol	Description
7	LCR[7]	Divisor latch enable. The internal baud rate counter latch and Enhanced Feature mode enable. logic 0 = divisor latch disabled (normal default condition) logic 1 = divisor latch and enhanced feature register enabled
6	LCR[6]	Set break. When enabled, the Break control bit causes a break condition to be transmitted (the TX output is forced to a logic 0 state). This condition exists until disabled by setting LCR[6] to a logic 0. logic 0 = no TX break condition (normal default condition) logic 1 = forces the transmitter output (TX) to a logic 0 for alerting the remote receiver to a line break condition
5	LCR[5]	Set parity. If the parity bit is enabled, LCR[5] selects the forced parity format. Programs the parity conditions (see Table 15). logic 0 = parity is not forced (normal default condition) LCR[5] = logic 1 and LCR[4] = logic 0: parity bit is forced to a logic 1 for the transmit and receive data LCR[5] = logic 1 and LCR[4] = logic 1: parity bit is forced to a logic 0 for the transmit and receive data
4	LCR[4]	Even parity. If the parity bit is enabled with LCR[3] set to a logic 1, LCR[4] selects the even or odd parity format. logic 0 = odd parity is generated by forcing an odd number of logic 1s in the transmitted data. The receiver must be programmed to check the same format (normal default condition). logic 1 = even parity is generated by forcing an even number of logic 1s in the transmitted data. The receiver must be programmed to check the same format.
3	LCR[3]	Parity enable. Parity or no parity can be selected via this bit. logic 0 = no parity (normal default condition) logic 1 = a parity bit is generated during the transmission, receiver checks the data and parity for transmission errors
2	LCR[2]	Stop bits. The length of stop bit is specified by this bit in conjunction with the programmed word length (see Table 16). logic 0 or cleared = default condition
1:0	LCR[1:0]	Word length bit 1, bit 0. These two bits specify the word length to be transmitted or received (see Table 17). logic 0 or cleared = default condition

© NXP B.V. 2008. All rights reserved.

Table 15. LCR[5] parity selection

LCR[5]	LCR[4]	LCR[3]	Parity selection
X	X	0	no parity
0	0	1	odd parity
0	1	1	even parity
1	0	1	force parity ‘1’
1	1	1	forced parity ‘0’

Table 16. LCR[2] stop bit length

LCR[2]	Word length (bits)	Stop bit length (bit times)
0	5, 6, 7, 8	1
1	5	$1\frac{1}{2}$
1	6, 7, 8	2

Table 17. LCR[1:0] word length

LCR[1]	LCR[0]	Word length (bits)
0	0	5
0	1	6
1	0	7
1	1	8

© NXP B.V. 2008. All rights reserved.

7.6 Modem Control Register (MCR)

This register controls the interface with the modem or a peripheral device.

Table 18. Modem Control Register bits description

Bit	Symbol	Description
7	MCR[7]	reserved; set to 0
6	MCR[6]	reserved; set to 0
5	MCR[5]	AFE. This bit is the auto flow control enable. When this bit is set, the auto flow control is enabled.
4	MCR[4]	Loopback. Enable the local Loopback mode (diagnostics). In this mode the transmitter output ($\overline{TX}$) and the receiver input ($\overline{RX}$), $\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$ are disconnected from the SC16C750B I/O pins. Internally the modem data and control pins are connected into a loopback data configuration (see Figure 6). In this mode, the receiver and transmitter interrupts remain fully operational. The Modem Control Interrupts are also operational, but the interrupts' sources are switched to the lower four bits of the Modem Control. Interrupts continue to be controlled by the IER register. logic 0 = disable Loopback mode (normal default condition) logic 1 = enable local Loopback mode (diagnostics)
3	MCR[3]	$\overline{OUT2}$, INT enable. Used to control the modem $\overline{DCD}$ signal in the Loopback mode. logic 0 = set $\overline{OUT2}$ to HIGH. In the Loopback mode, sets $\overline{OUT2}$ ($\overline{DCD}$) internally to a logic 1. logic 1 = set $\overline{OUT2}$ to LOW. In the Loopback mode, sets $\overline{OUT2}$ ($\overline{DCD}$) internally to a logic 0.
2	MCR[2]	$\overline{OUT1}$. This bit is used in the Loopback mode only. In the Loopback mode, this bit is used to write the state of the modem $\overline{RI}$ interface signal via $\overline{OUT1}$.
1	MCR[1]	$\overline{RTS}$ logic 0 = force $\overline{RTS}$ output to a logic 1 (normal default condition) logic 1 = force $\overline{RTS}$ output to a logic 0
0	MCR[0]	$\overline{DTR}$ logic 0 = force $\overline{DTR}$ output to a logic 1 (normal default condition) logic 1 = force $\overline{DTR}$ output to a logic 0

The flow control can be configured by programming MCR[1] and MCR[5] as shown in Table 19.

Table 19. Flow control configuration

MCR[5] (AFE)	MCR[1] ($\overline{RTS}$)	Flow configuration
1	1	auto $\overline{RTS}$ and $\overline{CTS}$ enabled
1	0	auto $\overline{CTS}$ only enabled
0	X	auto $\overline{RTS}$ and $\overline{CTS}$ disabled

© NXP B.V. 2008. All rights reserved.

7.7 Line Status Register (LSR)

This register provides the status of data transfers between the SC16C750B and the CPU.

Table 20. Line Status Register bits description

Bit	Symbol	Description
7	LSR[7]	FIFO data error. logic 0 = no error (normal default condition) logic 1 = at least one parity error, framing error or break indication is in the current FIFO data. This bit is cleared when LSR register is read.
6	LSR[6]	THR and TSR empty. This bit is the Transmit Empty indicator. This bit is set to a logic 1 whenever the transmit holding register and the transmit shift register are both empty. It is reset to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode, this bit is set to logic 1 whenever the transmit FIFO and transmit shift register are both empty.
5	LSR[5]	THR empty. This bit is the Transmit Holding Register Empty indicator. This bit indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to CPU when the THR interrupt enable is set. The THR bit is set to a logic 1 when a character is transferred from the transmit holding register into the transmitter shift register. The bit is reset to a logic 0 concurrently with the loading of the transmitter holding register by the CPU. In the FIFO mode, this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO.
4	LSR[4]	Break interrupt. logic 0 = no break condition (normal default condition) logic 1 = the receiver received a break signal (RX was a logic 0 for one character frame time). In the FIFO mode, only one break character is loaded into the FIFO.
3	LSR[3]	Framing error. logic 0 = no framing error (normal default condition) logic 1 = framing error. The receive character did not have a valid stop bit(s). In the FIFO mode, this error is associated with the character at the top of the FIFO.
2	LSR[2]	Parity error. logic 0 = no parity error (normal default condition) logic 1 = parity error. The receive character does not have correct parity information and is suspect. In the FIFO mode, this error is associated with the character at the top of the FIFO.
1	LSR[1]	Overrun error. logic 0 = no overrun error (normal default condition) logic 1 = overrun error. A data overrun error occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case, the previous data in the shift register is overwritten. Note that under this condition, the data byte in the receive shift register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error.
0	LSR[0]	Receive data ready. logic 0 = no data in receive holding register or FIFO (normal default condition) logic 1 = data has been received and is saved in the receive holding register or FIFO

© NXP B.V. 2008. All rights reserved.

7.8 Modem Status Register (MSR)

This register provides the current state of the control interface signals from the modem, or other peripheral device to which the SC16C750B is connected. Four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a control input from the modem changes state. These bits are set to a logic 0 whenever the CPU reads this register.

Table 21. Modem Status Register bits description

Bit	Symbol	Description
7	MSR[7]	Data Carrier Detect. DCD (active HIGH, logic 1). Normally this bit is the complement of the $\overline{DCD}$ input. In the Loopback mode this bit is equivalent to the OUT2 bit in the MCR register.
6	MSR[6]	Ring Indicator. RI (active HIGH, logic 1). Normally this bit is the complement of the $\overline{RI}$ input. In the Loopback mode this bit is equivalent to the OUT1 bit in the MCR register.
5	MSR[5]	Data Set Ready. DSR (active HIGH, logic 1). Normally this bit is the complement of the $\overline{DSR}$ input. In Loopback mode this bit is equivalent to the DTR bit in the MCR register.
4	MSR[4]	Clear To Send. CTS. $\overline{CTS}$ functions as hardware flow control signal input if it is enabled via MCR[5]. Flow control (when enabled) allows starting and stopping the transmissions based on the external modem $\overline{CTS}$ signal. A logic 1 at the $\overline{CTS}$ pin will stop SC16C750B transmissions as soon as current character has finished transmission. Normally MSR[4] is the complement of the $\overline{CTS}$ input. However, in the Loopback mode, this bit is equivalent to the RTS bit in the MCR register.
3	MSR[3]	$\Delta\overline{DCD}$ [1] logic 0 = no $\overline{DCD}$ change (normal default condition) logic 1 = the $\overline{DCD}$ input to the SC16C750B has changed state since the last time it was read. A modem Status Interrupt will be generated.
2	MSR[2]	$\Delta\overline{RI}$ [1] logic 0 = no $\overline{RI}$ change (normal default condition) logic 1 = the $\overline{RI}$ input to the SC16C750B has changed from a logic 0 to a logic 1. A modem Status Interrupt will be generated.
1	MSR[1]	$\Delta\overline{DSR}$ [1] logic 0 = no $\overline{DSR}$ change (normal default condition) logic 1 = the $\overline{DSR}$ input to the SC16C750B has changed state since the last time it was read. A modem Status Interrupt will be generated.
0	MSR[0]	$\Delta\overline{CTS}$ [1] logic 0 = no $\overline{CTS}$ change (normal default condition) logic 1 = the $\overline{CTS}$ input to the SC16C750B has changed state since the last time it was read. A modem Status Interrupt will be generated.

[1] Whenever any MSR[0:3] is set to logic 1, a Modem Status Interrupt will be generated.

© NXP B.V. 2008. All rights reserved.

7.9 Scratchpad Register (SPR)

The SC16C750B provides a temporary data register to store 8 bits of user information.

7.10 SC16C750B external reset conditions

Table 22. Reset state for registers

Register	Reset state
IER	IER[7:0] = 0
ISR	ISR[7:1] = 0; ISR[0] = 1
LCR	LCR[7:0] = 0
MCR	MCR[7:0] = 0
LSR	LSR[7] = 0; LSR[6:5] = 1; LSR[4:0] = 0
MSR	MSR[7:4] = input signals; MSR[3:0] = 0
FCR	FCR[7:0] = 0

Table 23. Reset state for outputs

Output	Reset state
TX	HIGH
$\overline{RTS}$	HIGH
$\overline{DTR}$	HIGH
$\overline{RXRDY}$	HIGH (STD mode)
$\overline{TXRDY}$	LOW (STD mode)
INT	LOW (STD mode)

8. Limiting values

Table 24. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-	7	V
V_n	voltage on any other pin	at D7 to D0 pins	GND – 0.3	V_{CC} + 0.3	V
		at input only pins	GND – 0.3	5.3	V
T_{amb}	ambient temperature	operating	–40	+85	°C
T_{stg}	storage temperature		–65	+150	°C
P_{tot}/pack	total power dissipation per package		-	500	mW

© NXP B.V. 2008. All rights reserved.

9. Static characteristics

Table 25. Static characteristics

T_{amb} = −40 °C to +85 °C; tolerance of V_{CC} = ± 10 %, unless otherwise specified.

Symbol	Parameter	Conditions		V_{CC} = 2.5 V		V_{CC} = 3.3 V		V_{CC} = 5.0 V		Unit
				Min	Max	Min	Max	Min	Max	
$V_{IL(clk)}$	clock LOW-level input voltage			−0.3	0.45	−0.3	0.6	−0.5	0.6	V
$V_{IH(clk)}$	clock HIGH-level input voltage			1.8	V_{CC}	2.4	V_{CC}	3.0	V_{CC}	V
V_{IL}	LOW-level input voltage			−0.3	0.65	−0.3	0.8	−0.5	0.8	V
V_{IH}	HIGH-level input voltage			1.6	-	2.0	-	2.2	V_{CC}	V
V_{OL}	LOW-level output voltage	on all outputs	[1]							
		I_{OL} = 5 mA (data bus)		-	-	-	-	-	0.4	V
		I_{OL} = 4 mA (other outputs)		-	-	-	0.4	-	-	V
		I_{OL} = 2 mA (data bus)		-	0.4	-	-	-	-	V
		I_{OL} = 1.6 mA (other outputs)		-	0.4	-	-	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −5 mA (data bus)		-	-	-	-	2.4	-	V
		I_{OH} = −1 mA (other outputs)		-	-	2.0	-	-	-	V
		I_{OH} = −800 µA (data bus)		1.85	-	-	-	-	-	V
		I_{OH} = −400 µA (other outputs)		1.85	-	-	-	-	-	V
I_{LIL}	LOW-level input leakage current			-	±10	-	±10	-	±10	µA
$I_{L(clk)}$	clock leakage current			-	±30	-	±30	-	±30	µA
$I_{CC(AV)}$	average supply current			-	3.5	-	4.5	-	4.5	mA
$I_{CC(sleep)}$	sleep mode supply current		[2]	-	50	-	50	-	50	µA
$I_{CC(lp)}$	low-power mode supply current			-	1.0	-	1.5	-	1.5	mA
C_i	input capacitance			-	5	-	5	-	5	pF
$R_{pu(int)}$	internal pull-up resistance			500	-	500	-	500	-	kΩ

[1] Except for XTAL2, V_{OL} = 1 V typically.

[2] Sleep current might be higher if there is activity on the UART data bus during Sleep mode.

© NXP B.V. 2008. All rights reserved.

10. Dynamic characteristics

Table 26. Dynamic characteristics

T_{amb} = −40 °C to +85 °C; tolerance of V_{CC} = ± 10 %, unless otherwise specified.

Symbol	Parameter	Conditions		V_{CC} = 2.5 V		V_{CC} = 3.3 V		V_{CC} = 5.0 V		Unit
				Min	Max	Min	Max	Min	Max	
t_{w1}	clock pulse duration			15	-	13	-	10	-	ns
t_{w2}	clock pulse duration			15	-	13	-	10	-	ns
f_{XTAL1}	frequency on pin XTAL1		[1]	-	16	-	32	-	48	MHz
t_{4w}	address strobe width			45	-	35	-	25	-	ns
t_{5s}	address set-up time			5	-	5	-	1	-	ns
t_{5h}	address hold time			5	-	5	-	5	-	ns
t_{6s}	chip select set-up time to $\overline{AS}$			10	-	5	-	0	-	ns
t_{6h}	address hold time			0	-	0	-	0	-	ns
$t_{6s'}$	address set-up time		[2]	10	-	10	-	5	-	ns
t_{6h}	chip select hold time			0	-	0	-	0	-	ns
t_{7d}	$\overline{IOR}$ delay from chip select			10	-	10	-	10	-	ns
t_{7w}	$\overline{IOR}$ strobe width	25 pF load		77	-	26	-	23	-	ns
t_{7h}	chip select hold time from $\overline{IOR}$			0	-	0	-	0	-	ns
$t_{7h'}$	address hold time		[2]	5	-	5	-	5	-	ns
t_{8d}	$\overline{IOR}$ delay from address			10	-	10	-	10	-	ns
t_{9d}	read cycle delay	25 pF load		20	-	20	-	20	-	ns
t_{11d}	$\overline{IOR}$ to $\overline{DDIS}$ delay	25 pF load		-	100	-	35	-	30	ns
t_{12d}	delay from $\overline{IOR}$ to data	25 pF load		-	77	-	26	-	23	ns
t_{12h}	data disable time	25 pF load		-	15	-	15	-	15	ns
t_{13d}	$\overline{IOW}$ delay from chip select			10	-	10	-	10	-	ns
t_{13w}	$\overline{IOW}$ strobe width			20	-	20	-	15	-	ns
t_{13h}	chip select hold time from $\overline{IOW}$			0	-	0	-	0	-	ns
t_{14d}	$\overline{IOW}$ delay from address			10	-	10	-	10	-	ns
t_{15d}	write cycle delay			25	-	25	-	20	-	ns
t_{16s}	data set-up time			20	-	20	-	15	-	ns
t_{16h}	data hold time			15	-	5	-	5	-	ns
t_{17d}	delay from $\overline{IOW}$ to output	25 pF load		-	100	-	33	-	29	ns
t_{18d}	delay to set interrupt from Modem input	25 pF load		-	100	-	24	-	23	ns
t_{19d}	delay to reset interrupt from $\overline{IOR}$	25 pF load		-	100	-	24	-	23	ns
t_{20d}	delay from stop to set interrupt		[3]	-	$1T_{RCLK}$	-	$1T_{RCLK}$	-	$1T_{RCLK}$	s
t_{21d}	delay from $\overline{IOR}$ to reset interrupt	25 pF load		-	100	-	29	-	28	ns
t_{22d}	delay from start to set interrupt			-	100	-	45	-	40	ns
t_{23d}	delay from $\overline{IOW}$ to transmit start		[3]	$8T_{RCLK}$	$24T_{RCLK}$	$8T_{RCLK}$	$24T_{RCLK}$	$8T_{RCLK}$	$24T_{RCLK}$	s

© NXP B.V. 2008. All rights reserved.

Table 26. Dynamic characteristics *...continued*

T_{amb} = −40 °C to +85 °C; tolerance of V_{CC} = ± 10 %, unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} = 2.5 V		V_{CC} = 3.3 V		V_{CC} = 5.0 V		Unit
			Min	Max	Min	Max	Min	Max	
t_{24d}	delay from $\overline{IOW}$ to reset interrupt		-	100	-	45	-	40	ns
t_{25d}	delay from stop to set $\overline{RXRDY}$	[3]	-	$1T_{RCLK}$	-	$1T_{RCLK}$	-	$1T_{RCLK}$	s
t_{26d}	delay from $\overline{IOR}$ to reset $\overline{RXRDY}$		-	100	-	45	-	40	ns
t_{27d}	delay from $\overline{IOW}$ to set $\overline{TXRDY}$		-	100	-	45	-	40	ns
t_{28d}	delay from start to reset $\overline{TXRDY}$	[3]	-	$8T_{RCLK}$	-	$8T_{RCLK}$	-	$8T_{RCLK}$	s
t_{RESET}	Reset pulse width	[4]	100	-	40	-	40	-	ns
N	baud rate divisor		1	$2^{16} - 1$	1	$2^{16} - 1$	1	$2^{16} - 1$	

[1] Applies to external clock, crystal oscillator max 24 MHz.

[2] Applicable only when $\overline{AS}$ is tied LOW.

[3] RCLK is an internal signal derived from Divisor Latch LSB (DLL) and Divisor Latch MSB (DLM) divisor latches.

[4] Reset pulse must happen when these signals are inactive: $\overline{CS}$, $\overline{CS2}$, CS1, CS0, IOR, $\overline{IOR}$, IOW, $\overline{IOW}$.

10.1 Timing diagrams

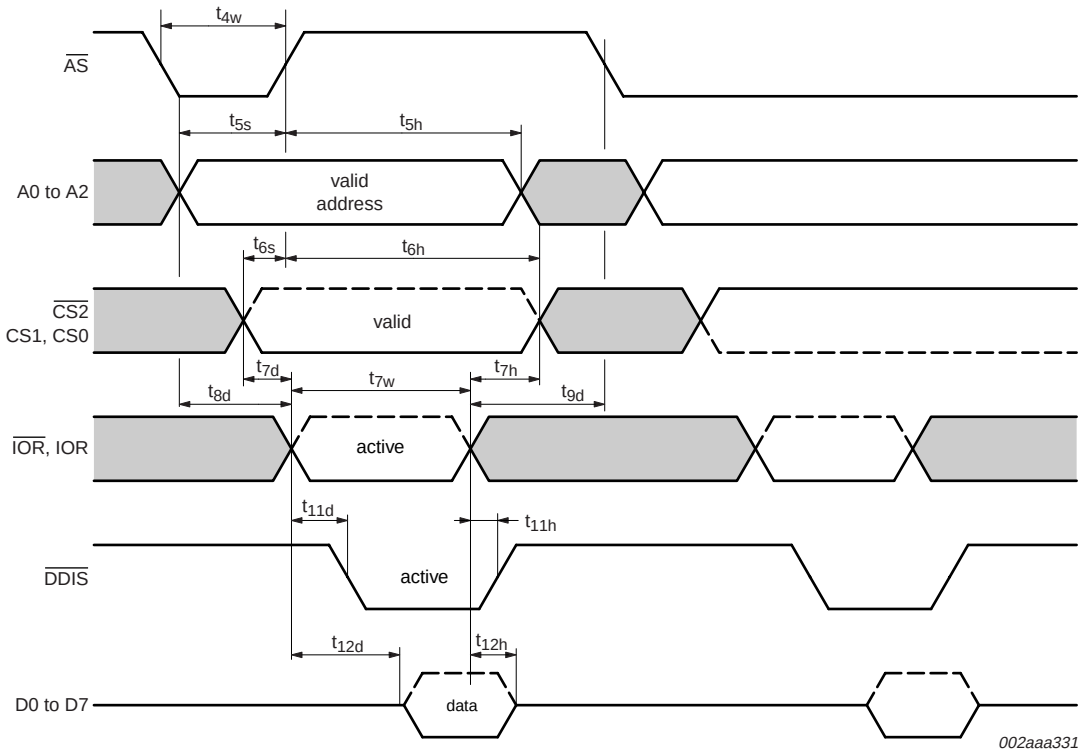


Fig 7. General read timing when using $\overline{AS}$ signal

© NXP B.V. 2008. All rights reserved.

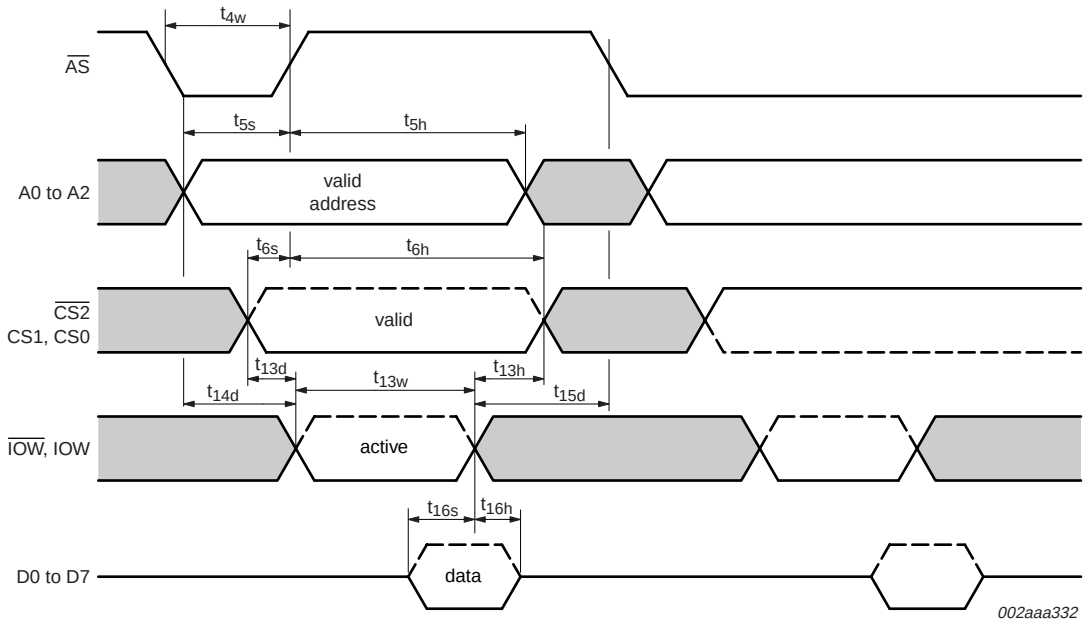


Fig 8. General write timing when using $\overline{AS}$ signal

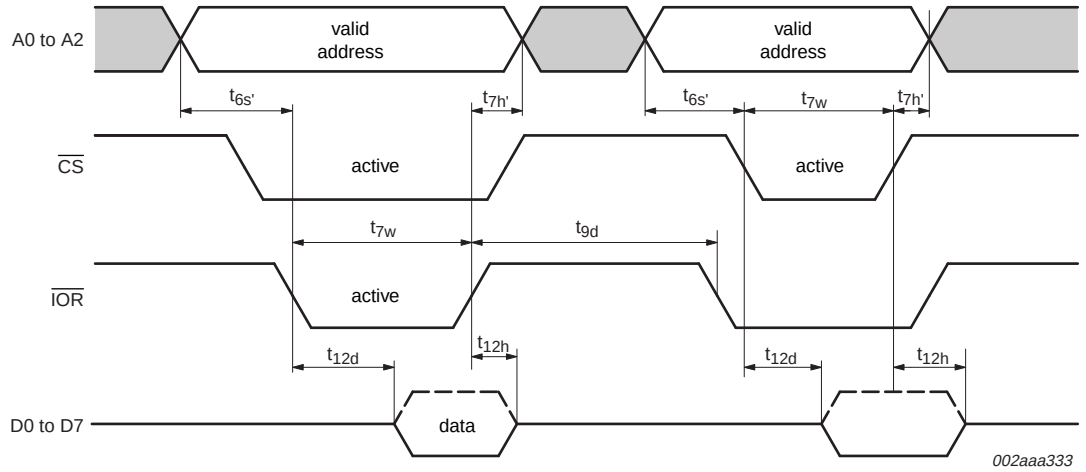


Fig 9. General read timing when $\overline{AS}$ is tied to GND

© NXP B.V. 2008. All rights reserved.

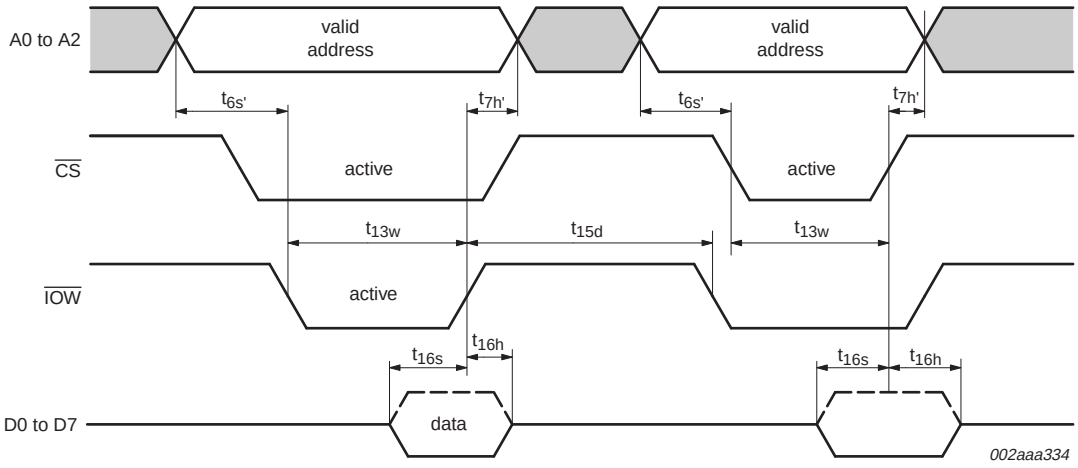


Fig 10. General write timing when $\overline{AS}$ is tied to GND

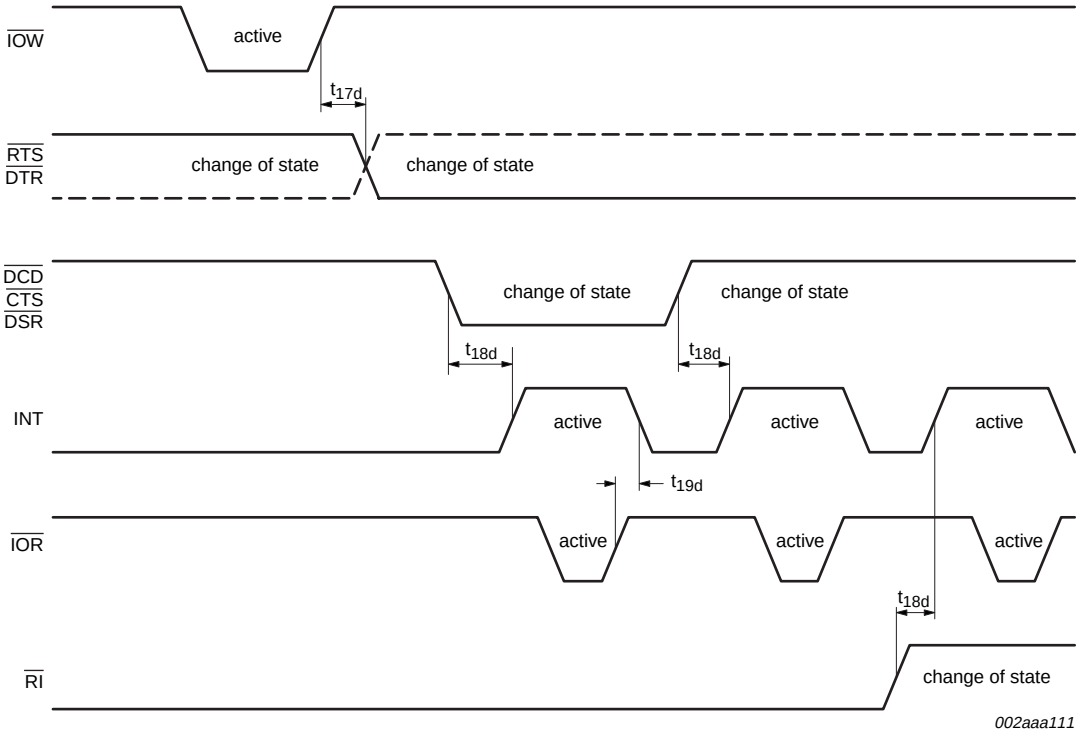
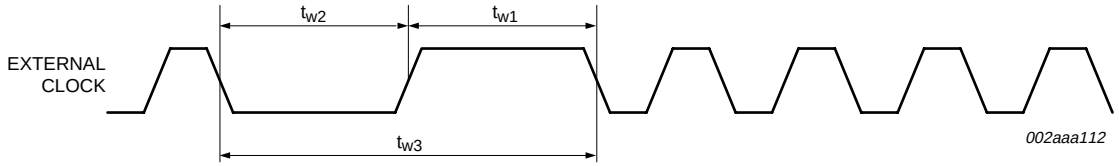


Fig 11. Modem input/output timing

© NXP B.V. 2008. All rights reserved.



$$f_{XTAL1} = \frac{1}{t_{w3}}$$

Fig 12. External clock timing

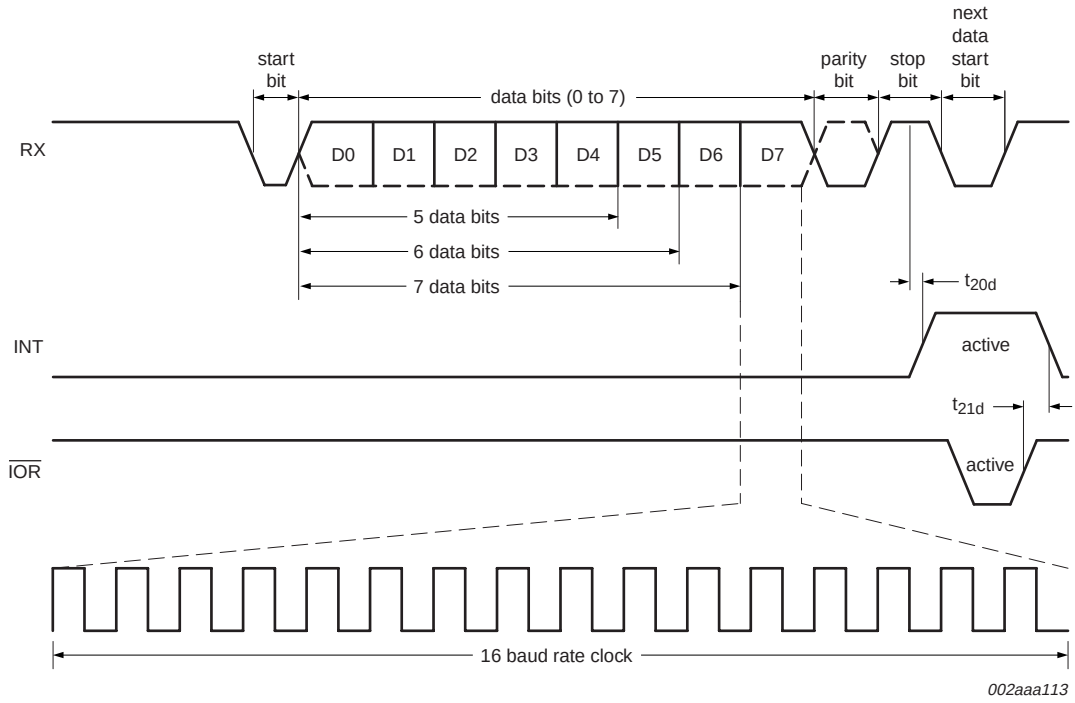


Fig 13. Receive timing

© NXP B.V. 2008. All rights reserved.

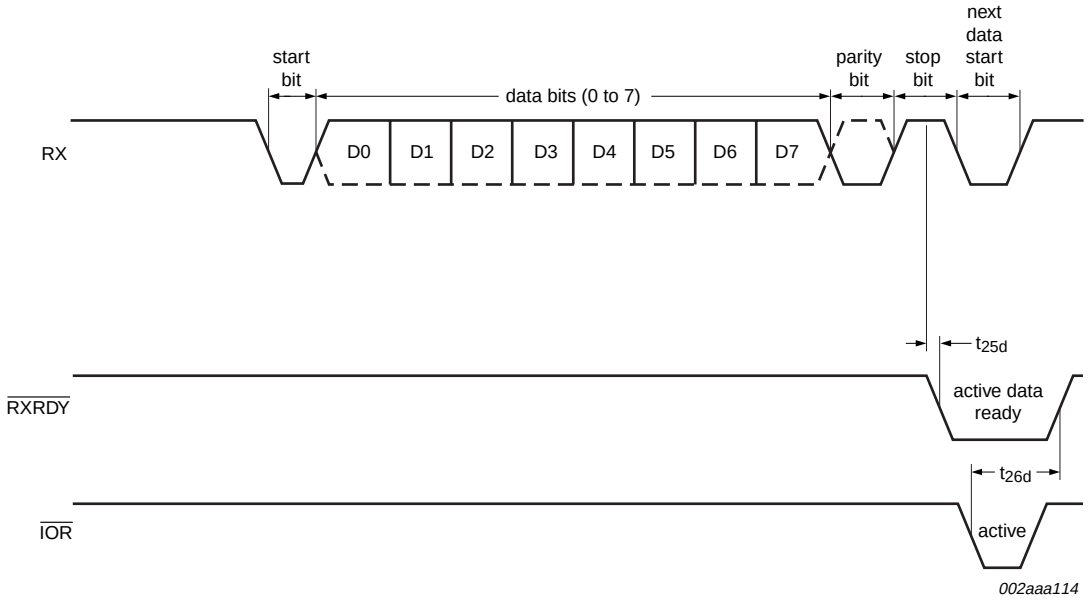


Fig 14. Receive ready timing in non-FIFO mode

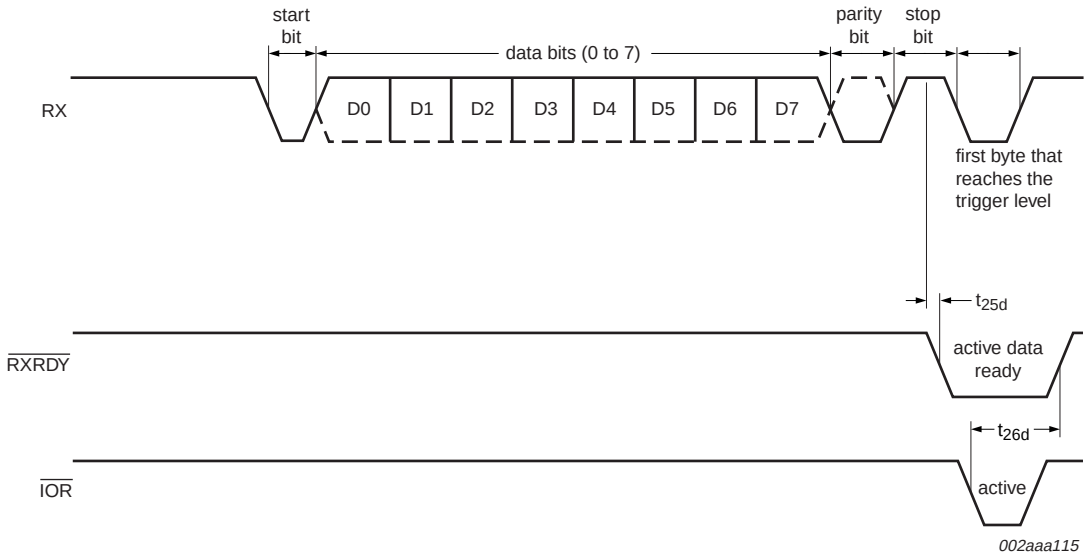


Fig 15. Receive ready timing in FIFO mode

© NXP B.V. 2008. All rights reserved.

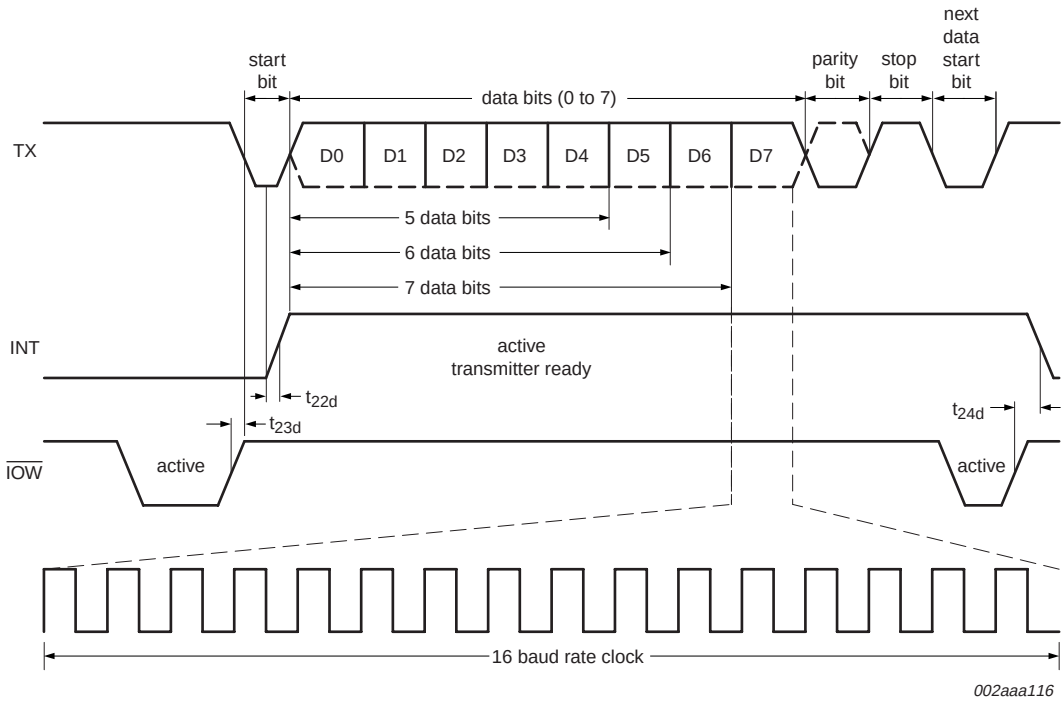


Fig 16. Transmit timing

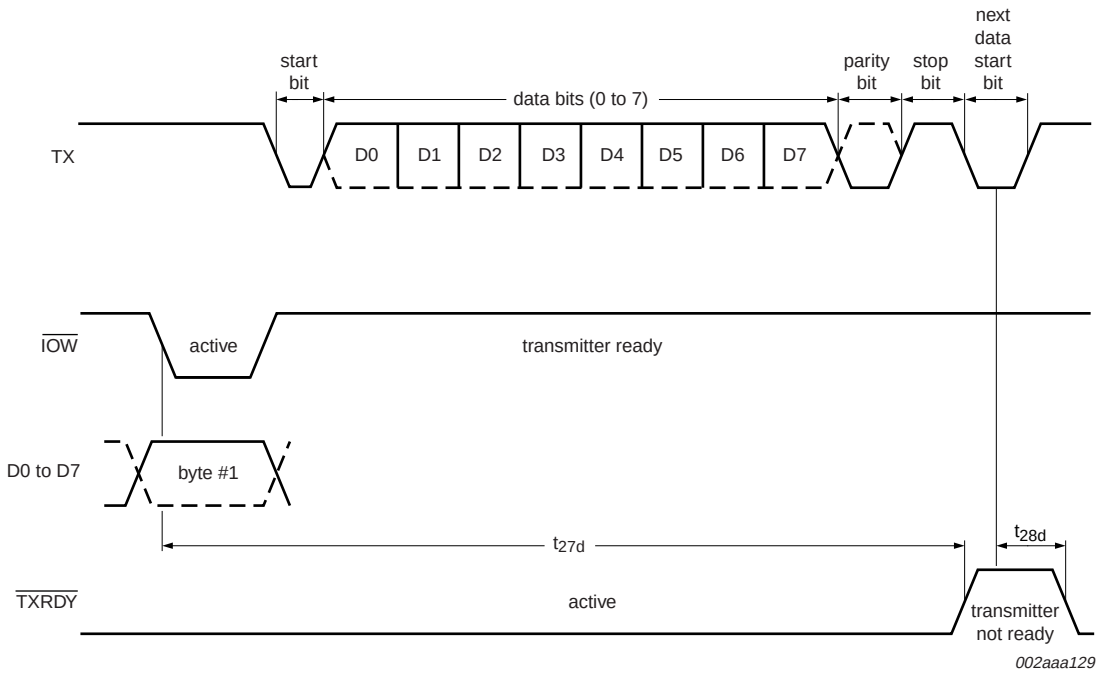


Fig 17. Transmit ready timing in non-FIFO mode

© NXP B.V. 2008. All rights reserved.

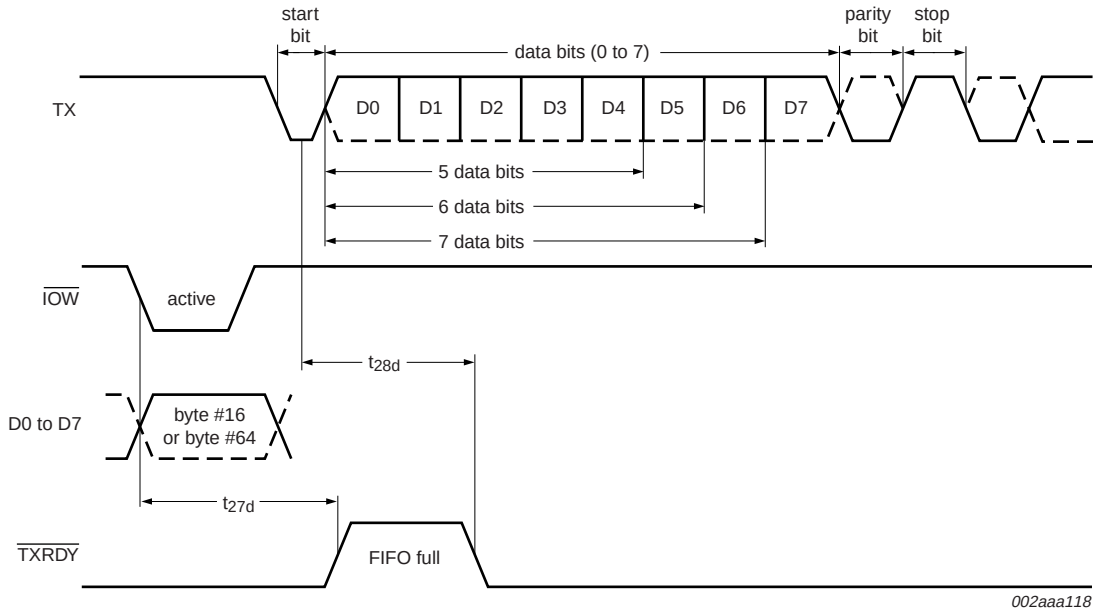
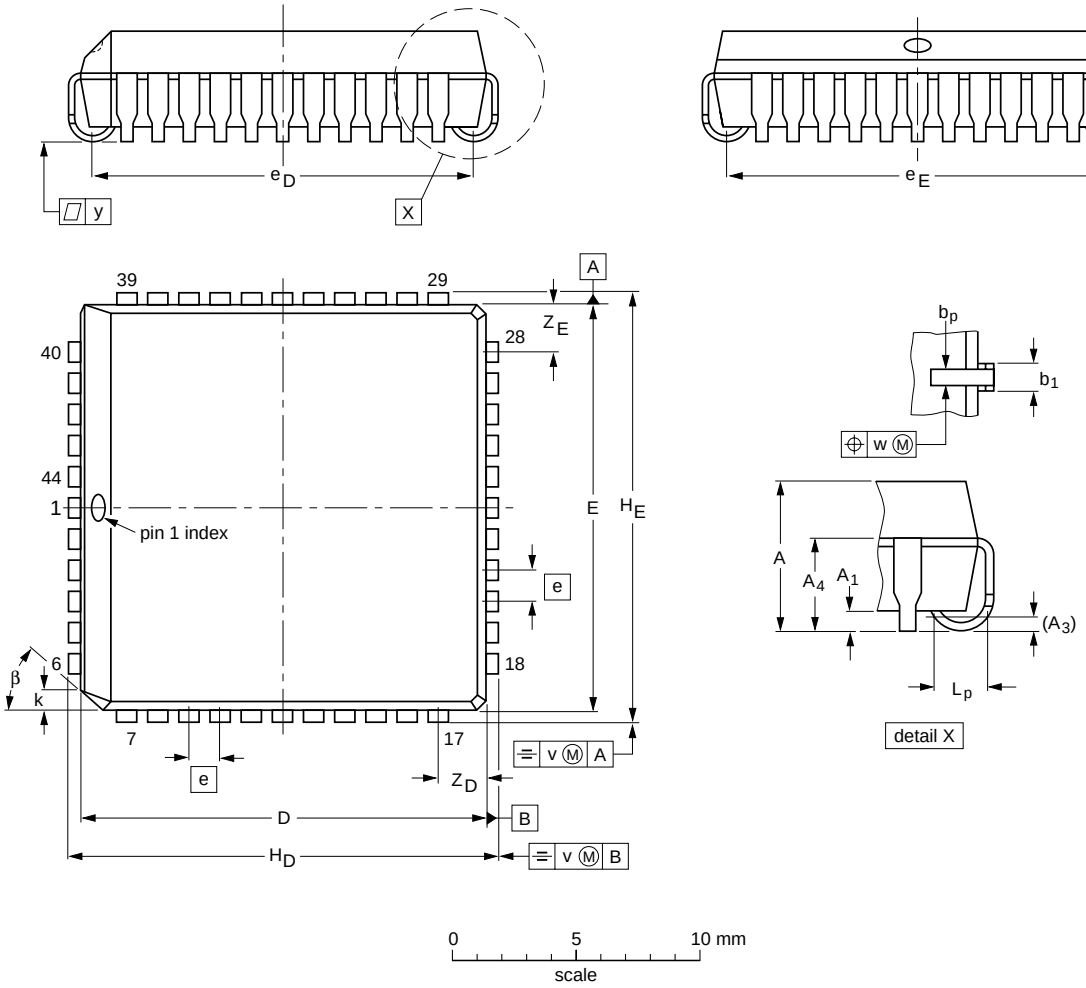


Fig 18. Transmit ready timing in FIFO mode (DMA mode '1')

© NXP B.V. 2008. All rights reserved.

11. Package outline

PLCC44: plastic leaded chip carrier; 44 leads **SOT187-2**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.63 0.59	0.63 0.59	0.695 0.685	0.695 0.685	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

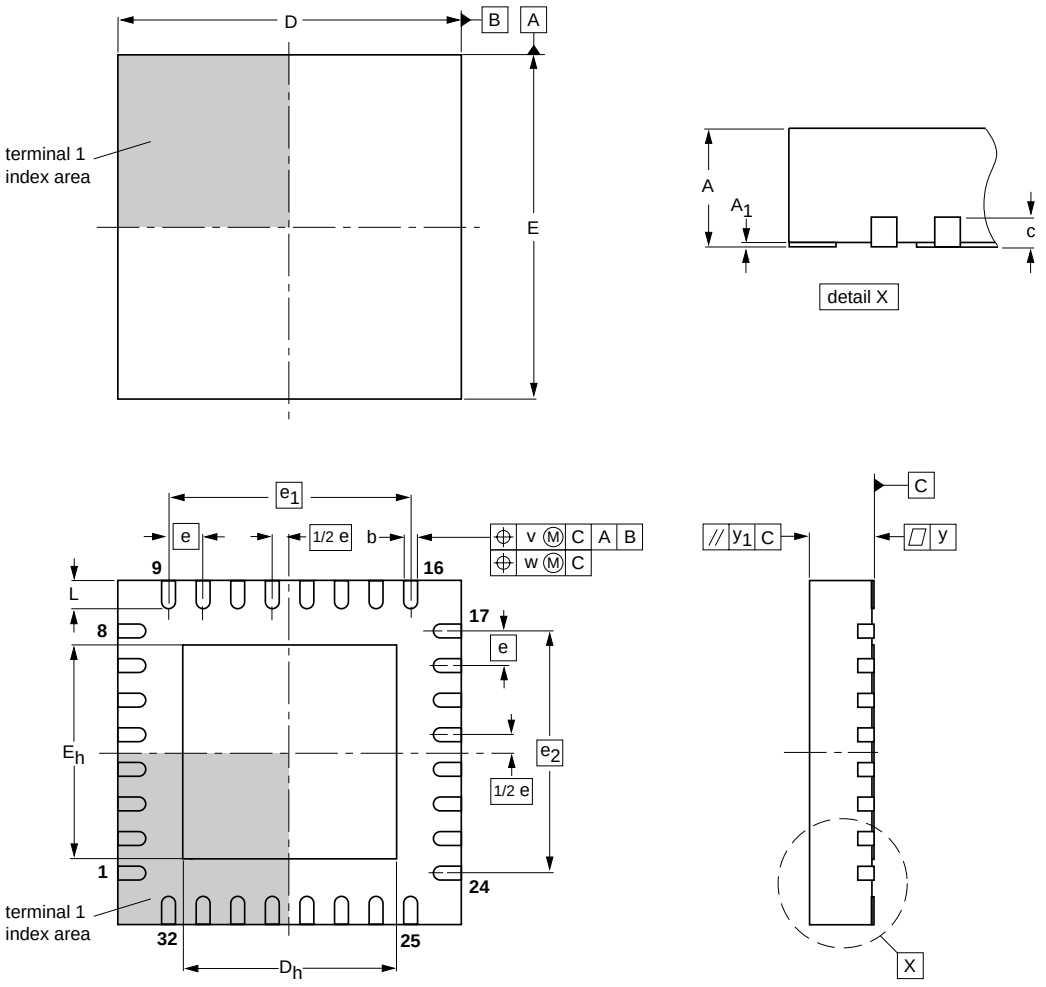
1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT187-2	112E10	MS-018	EDR-7319			~~99-12-27~~ 01-11-14

Fig 19. Package outline SOT187-2 (PLCC44)

© NXP B.V. 2008. All rights reserved.

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

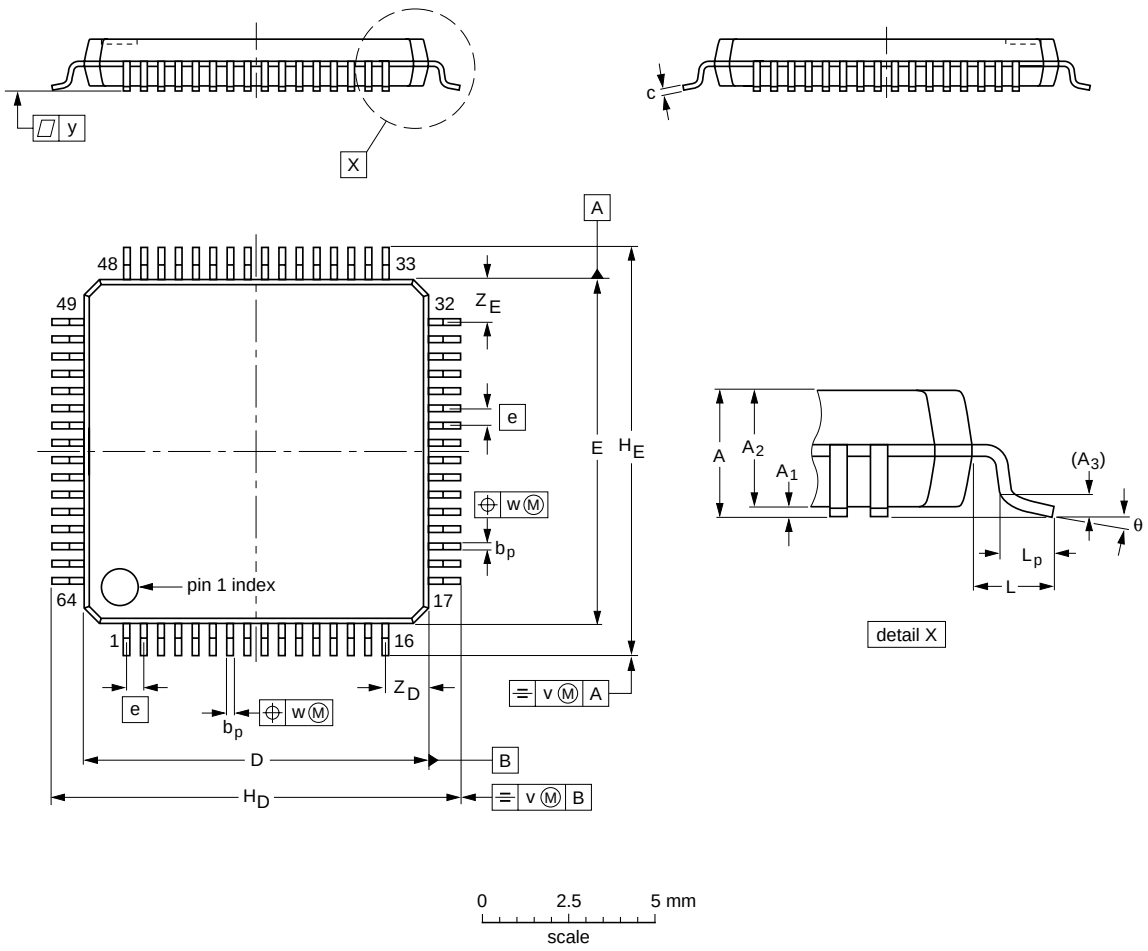
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT617-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-18

Fig 20. Package outline SOT617-1 (HVQFN32)

© NXP B.V. 2008. All rights reserved.

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 21. Package outline SOT314-2 (LQFP64)

© NXP B.V. 2008. All rights reserved.

12. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

12.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

12.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

12.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

© NXP B.V. 2008. All rights reserved.

12.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 22) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 27 and 28

Table 27. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

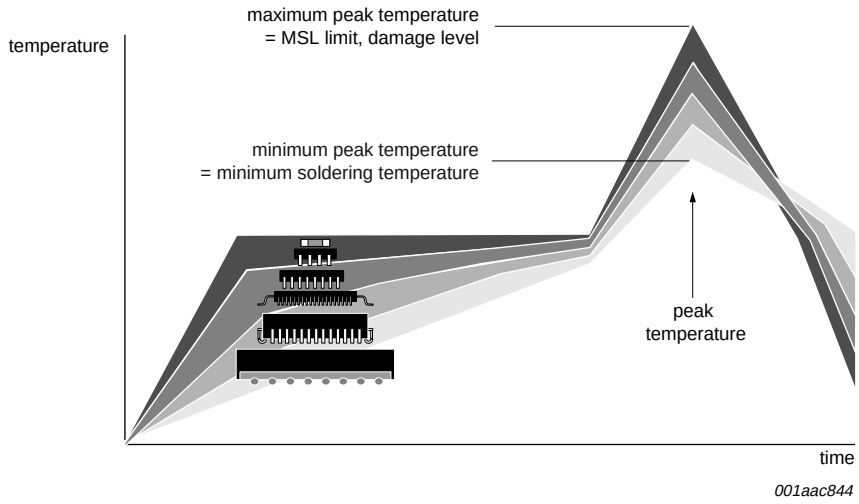
Table 28. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 22.

© NXP B.V. 2008. All rights reserved.



MSL: Moisture Sensitivity Level

Fig 22. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

13. Abbreviations

Table 29. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
DLL	Divisor Latch LSB
DLM	Divisor Latch MSB
DMA	Direct Memory Access
FIFO	First In, First Out
ISDN	Integrated Service Digital Network
LSB	Least Significant Bit
MSB	Most Significant Bit
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver and Transmitter

© NXP B.V. 2008. All rights reserved.

14. Revision history

Table 30. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SC16C750B_5	20081017	Product data sheet	-	SC16C750B_4
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 2 “Features”, 3rd bullet item re-written; added Footnote 1 • Figure 3 “Pin configuration for HVQFN32”: corrected pin 7 signal name from “$\overline{CS2}$” to “$\overline{CS}$” • Table 2 “Pin description”, description of $\overline{RI}$: changed from “... has transitioned from a LOW to a HIGH ...” to “... has changed from a LOW to a HIGH ...” • Table 24 “Limiting values”: – symbol V_n split to show 2 separate conditions: “at D7 to D0 pins” and “at input only pins” • Table 25 “Static characteristics”: – Symbol/parameter changed from “$V_{IL(CK)}$, LOW-level clock input voltage” to “$V_{IL(clk)}$, clock LOW-level input voltage” – Symbol/parameter changed from “$V_{IH(CK)}$, HIGH-level clock input voltage” to “$V_{IH(clk)}$, clock HIGH-level input voltage” – Symbol changed from “I_{CL}” to “$I_{L(clk)}$” – Table note [1]: changed from “Except for x_2, ...” to “Except for XTAL2, ...” • Table 26 “Dynamic characteristics”: – Symbol “t_{w2}, t_{2w}” changed to 2 separate symbols, “t_{w1}” and “t_{w2}” – Table note [4]: added “$\overline{CS}$” to list of signals which must be inactive when reset pulse happens • Updated soldering information		
SC16C750B_4	20060825	Product data sheet	-	SC16C750B-03
SC16C750B-03 (9397 750 14453)	20041213	Product data	-	SC16C750B-02
SC16C750B-02 (9397 750 13318)	20040527	Product data	-	SC16C750B-01
SC16C750B-01 (9397 750 11969)	20040329	Product data	-	-

© NXP B.V. 2008. All rights reserved.

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

15.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

© NXP B.V. 2008. All rights reserved.

17. Contents

1 General description 1
2 Features 1
3 Ordering information 2
4 Block diagram 3
5 Pinning information 4
5.1 Pinning 4
5.2 Pin description 5
6 Functional description 8
6.1 Internal registers 9
6.2 FIFO operation 10
6.3 Hardware flow control 10
6.4 Time-out interrupts 10
6.5 Programmable baud rate generator 11
6.6 DMA operation 12
6.7 Sleep mode 13
6.8 Low power mode 13
6.9 Loopback mode 13
7 Register descriptions 15
7.1 Transmit Holding Register (THR) and Receive Holding Register (RHR) 16
7.2 Interrupt Enable Register (IER) 16
7.2.1 IER versus Receive FIFO interrupt mode operation 17
7.2.2 IER versus Receive/Transmit FIFO polled mode operation 17
7.3 FIFO Control Register (FCR) 18
7.3.1 DMA mode 18
7.3.1.1 Mode 0 (FCR bit 3 = 0) 18
7.3.1.2 Mode 1 (FCR bit 3 = 1) 18
7.3.2 FIFO mode 18
7.4 Interrupt Status Register (ISR) 20
7.5 Line Control Register (LCR) 21
7.6 Modem Control Register (MCR) 23
7.7 Line Status Register (LSR) 24
7.8 Modem Status Register (MSR) 25
7.9 Scratchpad Register (SPR) 26
7.10 SC16C750B external reset conditions 26
8 Limiting values 26
9 Static characteristics 27
10 Dynamic characteristics 28
10.1 Timing diagrams 29
11 Package outline 36
12 Soldering of SMD packages 39
12.1 Introduction to soldering 39
12.2 Wave and reflow soldering 39
12.3 Wave soldering 39
12.4 Reflow soldering 40
13 Abbreviations 41
14 Revision history 42
15 Legal information 43
15.1 Data sheet status 43
15.2 Definitions 43
15.3 Disclaimers 43
15.4 Trademarks 43
16 Contact information 43
17 Contents 44

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2008. **All rights reserved.**

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 17 October 2008
Document identifier: SC16C750B_5

founded by

PHILIPS