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National Semiconductor

LM2460
Monolithic Triple Channel High Swing CRT Driver

General Description

The LM2460 is an integrated high voltage CRT driver circuit designed for use in high brightness monitor applications. The IC contains three high input impedance, wide band amplifiers which directly drive the RGB cathodes of a CRT. Each channel has its gain internally set to –30 and can drive CRT capacitive loads as well as resistive loads present in other application, limited only by the package's power dissipation.

The IC is packaged in an industry standard 9 lead TO-220 molded plastic package.

Features

- 0V to 5V input range
- Capable of up to a 70 V_{p-p} output swing
- Stable with 0–20 pF capacitive loads and inductive peaking networks
- Convenient TO-220 staggered lead package style
- Matched to LM126X/3X/4X pre-amplifier families

Applications

- High brightness CRT monitors

Schematic and Connection Diagrams

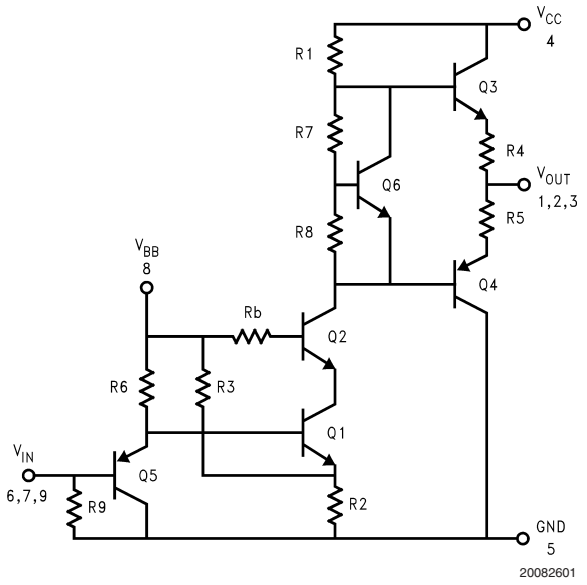
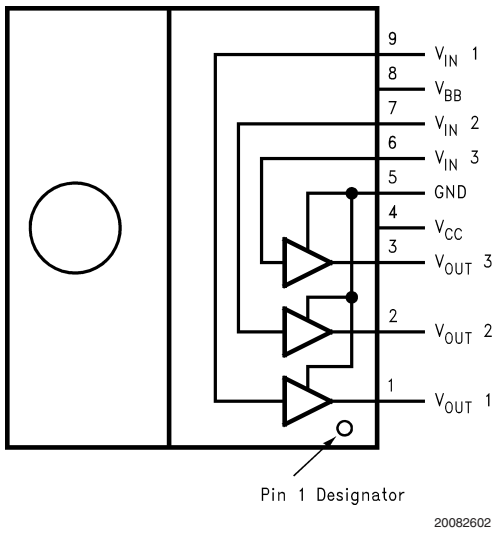


FIGURE 1. Simplified Schematic Diagram (One Channel)



Top View

Order Number LM2460TA
See NS Package Number TA09A

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Absolute Maximum Ratings (Notes 1, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	+136V
Bias Voltage (V_{BB})	+16V
Input Voltage (V_{IN})	$-0.5 > V_{IN} > 4.25V$
Storage Temperature	−40˚C to +150˚C
Lead Temperature	
(Soldering, <10 sec.)	265˚C
ESD Tolerance,	
Human Body Model	2 kV
Machine Model	200V
Junction Temperature (T_J)	150˚C

Operating Ratings (Note 2)

V_{CC}	+80V to +125V
V_{BB}	+6V to +10V
V_{IN}	+1V to +5V
V_{OUT}	+25V to +115V
Case Temperature	100˚C

Do not operate the part without a heatsink

Electrical Characteristics

(See *Figure 2* for Test Circuit) Unless otherwise noted: V_{CC} = +120V, V_{BB} = +8V, C_L = 8 pF, T_C = 50˚C

DC Tests: V_{IN} = +2.2 V_{DC}

AC Tests: Output = 60 V_{P-P} (45V – 105V) at 1 MHz

Symbol	Parameter	Conditions	LM2460			Units
			Min	Typ	Max	
I_{CC}	Supply Current	All Three Channels, No Video Input, No Output Load		35	45	mA
I_{BB}	Bias Current	All Three Channels		15	25	mA
$V_{OUT, 1}$	DC Output Voltage	No AC Input Signal, V_{IN} = 2.2 V_{DC}	73	78	83	V_{DC}
$V_{OUT, 2}$	DC Output Voltage	No AC Input Signal, V_{IN} = 1.2 V_{DC}	104	109	114	V_{DC}
A_V	DC Voltage Gain	No AC Input Signal	−28	−32	−34	V/V
ΔA_V	Gain Matching	(Note 4), No AC Input Signal		1.0		dB
LE	Linearity Error	(Note 4), (Note 5), No AC Input Signal		10		%
t_r (60 V_{P-P})	Rise Time, 45V to 105V	(Note 6), 10% to 90%		8.0		ns
t_f (60 V_{P-P})	Fall Time, 45V to 105V	(Note 6), 90% to 10%		11.5		ns
t_r (40 V_{P-P})	Rise Time, 65V to 105V	(Note 6), 10% to 90%		7.7		ns
t_f (40 V_{P-P})	Fall Time, 65V to 105V	(Note 6), 90% to 10%		9.5		ns
OS	Overshoot	(Note 6)		5		%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may change when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to GND, unless otherwise specified.

Note 4: Calculated value from Voltage Gain test on each channel.

Note 5: Linearity Error is the variation in dc gain from V_{IN} = 1.1V to V_{IN} = 3.8V.

Note 6: Input from signal generator: t_r, t_f < 1 ns.

AC Test Circuit

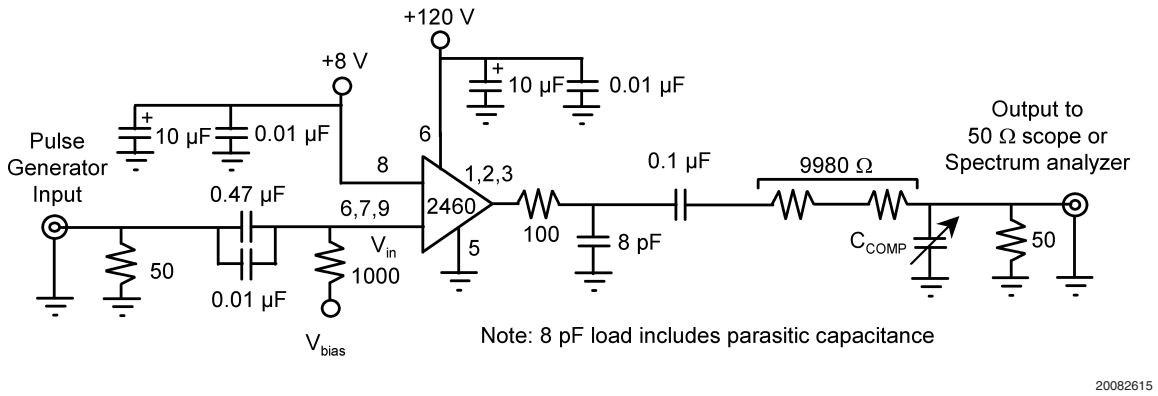


FIGURE 2. Test Circuit (One Channel)

Figure 2 shows a typical test circuit for evaluation of the LM2460. This circuit is designed to allow testing of the LM2460 in a 50Ω environment without the use of an expensive FET probe. The two 4990Ω resistors form a 200:1 divider with the 50Ω resistor and the oscilloscope. A test point is included for easy use of an oscilloscope probe. The compensation capacitor is used to compensate the stray capacitance of the two 4990Ω resistors to achieve flat frequency response.

Typical Performance Characteristics

(V_{CC} = +120 V_{DC}, V_{BB} = +8 V_{DC}, C_L = 8 pF, V_{OUT} = 60 V_{PP} (45–105V), Test Circuit — *Figure 2* unless otherwise specified.

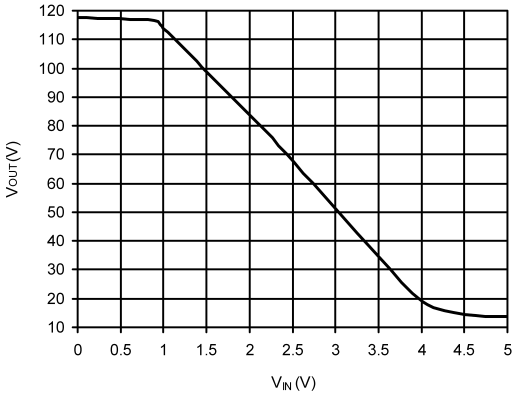


FIGURE 3. V_{IN} vs V_{OUT}

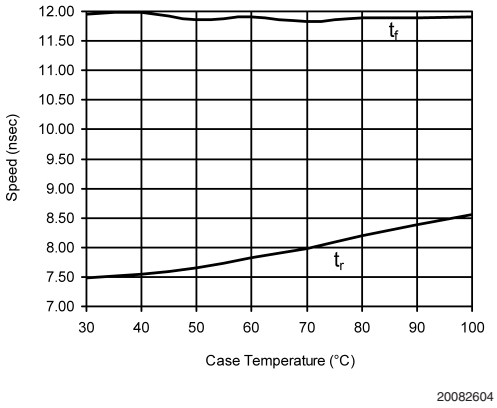


FIGURE 4. Speed vs Case Temperature

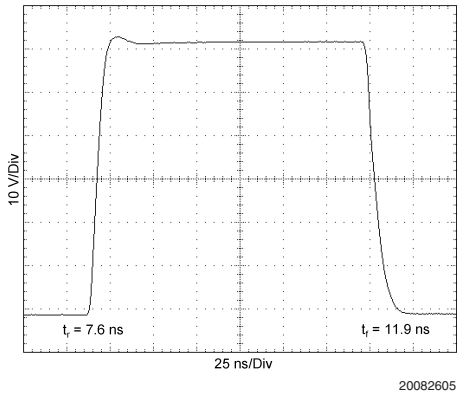


FIGURE 5. LM2460 Pulse Response

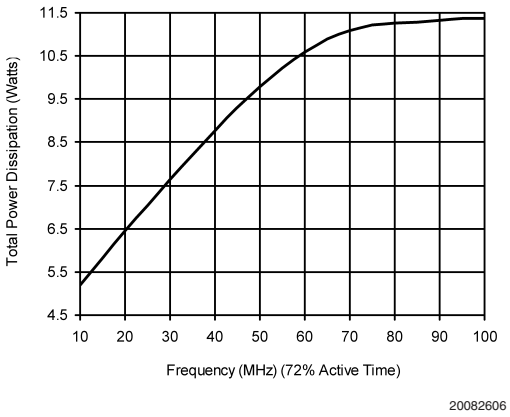


FIGURE 6. Power Dissipation vs Frequency

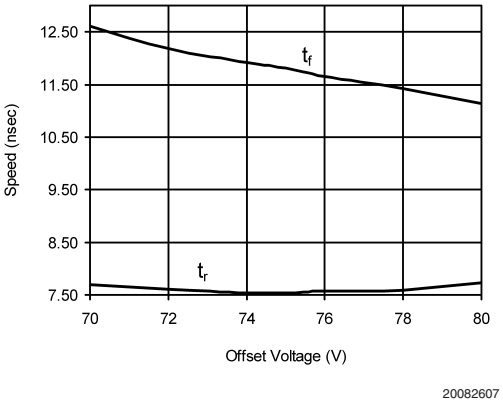


FIGURE 7. Speed vs Offset Voltage

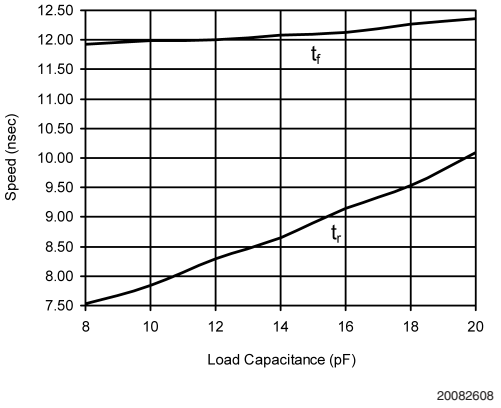


FIGURE 8. Speed vs Load Capacitance

Theory of Operation

The LM2460 is a high voltage monolithic three channel CRT driver with a higher output swing suitable for driving the new high brightness CRTs. The LM2460 operates with 120V and 8V power supplies. The part is housed in the industry standard 9-lead TO-220 molded plastic power package.

The circuit diagram of the LM2460 is shown in *Figure 1*. The PNP emitter follower, Q5, provides input buffering. Q1 and Q2 form a fixed gain cascode amplifier with resistors R1 and R2 setting the gain at −32. Emitter followers Q3 and Q4 isolate the high output impedance of the amplifier from the capacitive load on the output of the amplifier, decreasing the sensitivity of the device to changes in load capacitance. Q6 provides biasing to the output emitter follower stage to reduce crossover distortion at low signal levels.

Figure 2 shows a typical test circuit for evaluation of the LM2460. This circuit is designed to allow testing of the LM2460 in a 50Ω environment without the use of an expensive FET probe. In this test circuit, two low inductance resistors in series totaling 4.95 kΩ form a 200:1 wideband, low capacitance probe when connected to a 50Ω coaxial cable and a 50Ω load (such as a 50Ω oscilloscope input). The input signal from the generator is AC coupled to the base of Q5. V_{BIAS} is used to adjust the DC level of the output.

Application Hints

INTRODUCTION

National Semiconductor (NSC) is committed to provide application information that assists our customers in obtaining the best performance possible from our products. The following information is provided in order to support this commitment. The reader should be aware that the optimization of performance was done using a specific printed circuit board designed at NSC. Variations in performance can be realized due to physical changes in the printed circuit board and the application. Therefore, the designer should know that component value changes may be required in order to optimize performance in a given application. The values shown in this document can be used as a starting point for evaluation purposes. When working with high bandwidth circuits, good layout practices are also critical to achieving maximum performance.

IMPORTANT INFORMATION

The LM2460 performance is targeted for the 15" and 17" market with resolutions up to 1024 x 7684 and 75 Hz refresh rate. It is designed to be a replacement for discrete CRT drivers. The application circuits shown in this document to optimize performance and to protect against damage from CRT arc-over are designed specifically for the LM2460. If another member of the LM246X family is used, please refer to its datasheet.

POWER SUPPLY BYPASS

Since the LM2460 is a wide bandwidth amplifier, proper power supply bypassing is critical for optimum performance. Improper power supply bypassing can result in large overshoot, ringing or oscillation. A 0.1 µF capacitor should be connected from the supply pin, V_{CC}, to ground, as close to the supply and ground pins as is practical. Additionally, a 22 µF to 100 µF electrolytic capacitor should be connected from the supply pin to ground. The electrolytic capacitor should also be placed reasonably close to the LM2460's supply and ground pins. A 0.1 µF capacitor should be connected from the bias pin (V_{BB}) to ground, as close as is practical to the part.

ARC PROTECTION

During normal CRT operation, internal arcing may occasionally occur. Spark gaps, in the range of 200V, connected from the CRT cathodes to CRT ground will limit the maximum voltage, but to a value that is much higher than allowable on the LM2460. This fast, high voltage, high energy pulse can damage the LM2460 output stage. The application circuit shown in *Figure 9* is designed to help clamp the voltage at the output of the LM2460 to a safe level. The clamp diodes, D1 and D2, should have a fast transient response, high peak current rating, low series impedance and low shunt capacitance. FDH400 or equivalent diodes are recommended. Do not use 1N4148 diodes for the clamp diodes. D1 and D2 should have short, low impedance connections to V_{CC} and ground respectively. The cathode of D1 should be located very close to a separately decoupled bypass capacitor (C3 in *Figure 9*). The ground connection of D2 and the decoupling capacitor should be very close to the LM2460 ground. This will significantly reduce the high frequency voltage transients that the LM2460 would be subjected to during an arcover condition. Resistor R2 limits the arcover current that is seen by the diodes while R1 limits the current into the LM2460 as well as the voltage stress at the outputs of the device. R2 should be a 1/2W solid carbon type resistor. R1 can be a 1/4W metal or carbon film type resistor. Having large value resistors for R1 and R2 would be desirable, but this has the effect of increasing rise and fall times. Inductor L1 is critical to reduce the initial high frequency voltage levels that the LM2460 would be subjected to. The inductor will not only help protect the device but it will also help optimize rise and fall times as well as minimize EMI. For proper arc protection, it is important to not omit any of the arc protection components shown in *Figure 9*.

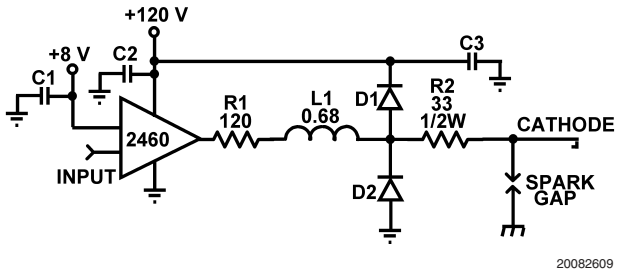


FIGURE 9. One Channel of the LM2460 with the Recommended Application Circuit

OPTIMIZING TRANSIENT RESPONSE

Referring to *Figure 9*, there are three components, (R1, R2 and L1) that can be adjusted to optimize the transient response of the application circuit. Increasing the values of R1 and R2 will slow the circuit down while decreasing overshoot. Increasing the value of L1 will speed up the circuit as well as increase overshoot. It is very important to use inductors with very high self-resonant frequencies, perferably above 300 MHz. Ferrite core inductors from J.W. Miller Magnetics (part # 78FR--K) were used for optimizing the performance of the device in the NSC application board. The values shown in *Figure 9* can be used as a good starting point for the evaluation of the LM2460. Using a variable

Application Hints (Continued)

resistor for R1 will simplify finding the value needed for optimum performance in a given application. Once the optimum value is determined the variable resistor can be replaced with a fixed value.

Effect of Load Capacitance

Figure 8 shows the effect of increased load capacitance on the speed of the device. This demonstrates the importance of knowing the load capacitance in the application. The rise time increased about 0.8 ns for an increase of 1 pF in the load capacitance. The fall time does remain almost the same as the load capacitance is increased.

Effect of Offset

Figure 7 shows the variation in rise and fall times when the output offset of the device is varied from 70 to 80 V_{DC}. The rise time has very little increase over its fastest point near 75V. The fall time becomes a little faster as the offset voltage increases.

THERMAL CONSIDERATIONS

Figure 4 shows the performance of the LM2460 in the test circuit shown in *Figure 2* as a function of case temperature. The figure shows that the rise time of the LM2460 increases by approximately 13% as the case temperature increases from 30˚C to 100˚C. This corresponds to a speed degradation of 2.0% for every 10˚C rise in case of temperature. The fall time has almost no change as the case temperature increases.

Figure 6 shows the maximum power dissipation of the LM2460 vs Frequency when all three channels of the device are driving an 8 pF load with a 60 V_{p-p} alternating one pixel on, one pixel off. The graph assumes a 72% active time (device operating at the specified frequency) which is typical in a monitor application. The other 28% of the time the device is assumed to be sitting at the black level (105V in this case). This graph gives the designer the information needed to determine the heat sink requirement for his application. The designer should note that if the load capacitance is increased the AC component of the total power dissipation would also increase.

The LM2460 case temperature must be maintained below 100˚C. If the maximum expected ambient temperature is 70˚C and the maximum power dissipation is 11W (from *Figure 6*, 70 MHz bandwidth) then a maximum heat sink thermal resistance can be calculated:

$$R_{TH} = \frac{100°C - 70°C}{11W} = 2.7°C/W$$

This example assumes a capacitive load of 8 pF and no resistive load.

TYPICAL APPLICATION

A typical application of the LM2460 is shown in *Figure 10* and *Figure 11*. Used in conjunction with a LM1267 pre-amp and a LM2479 bias clamp, a complete video channel from monitor input to CRT cathode can be achieved. Performance is ideal for 1024 x 768 resolution displays with pixel clock frequencies up to 80 MHz. *Figure 10* and *Figure 11* are the schematic for the NSC demonstration board that can be used to evaluate the LM1267/2460/2479 combination in a monitor.

PC Board Layout Considerations

For optimum performance, an adequate ground plane, isolation between channels, good supply bypassing and minimizing unwanted feedback are necessary. Also, the length of the signal traces from the preamplifier to the LM2460 and from the LM2460 to the CRT cathode should be as short as possible. The following references are recommended:

Ott, Henry W., “Noise Reduction Techniques in Electronic Systems”, John Wiley & Sons, New York, 1976.

“Video Amplifier Design for Computer Monitors”, National Semiconductor Application Note 1013.

Pease, Robert A., “Troubleshooting Analog Circuits”, Butterworth-Heinemann, 1991.

Because of its high small signal bandwidth, the part may oscillate in a monitor if feedback occurs around the video channel through the chassis wiring. To prevent this, leads to the video amplifier input circuit should be shielded, and input circuit wiring should be spaced as far as possible from output circuit wiring.

NSC Demonstration Board

Figure 12 shows the routing and component placement on the NSC LM126X/246X/LM2479/80 demonstration board. The schematic of the board is shown in *Figure 10* and *Figure 11*. This board provides a good example of a layout that can be used as a guide for future layouts. Note the location of the following components:

- *C16, C19* — V_{CC} bypass capacitor, located very close to pin 4 and ground pins
- *C17, C20* — V_{BB} bypass capacitors, located close to pin 8 and ground
- *C46, C47, C48* — V_{CC} bypass capacitors, near LM2460 and V_{CC} clamp diodes. Very important for arc protection.

The routing of the LM2460 outputs to the CRT is very critical to achieving optimum performance. *Figure 13* shows the routing and component placement from pin 3 of the LM2460 to the blue cathode. The blue video path from the LM2460 output is shown by the darker traces. Note that the components are placed so that they almost line up from the output pin of the LM2460 to the blue cathode pin of the CRT connector. This is done to minimize the length of the video path between these two components. Note also that D8, D9, R24 and D6 are placed to minimize the size of the video nodes that they are attached to. This minimizes parasitic capacitance in the video path and also enhances the effectiveness of the protection diodes. The anode of protection diode D8 is connected directly to a section of the ground plane that has a short and direct path to the LM2460 ground pins. The cathode of D9 is connected to V_{CC} very close to decoupling capacitor C48 (see *Figure 13*) which is connected to the same section of the ground plane as D8. The diode placement and routing is very important for minimizing the voltage stress on the LM2460 during an arc over event. Lastly, notice that S3 is placed very close to the blue cathode and is tied directly to CRT ground.

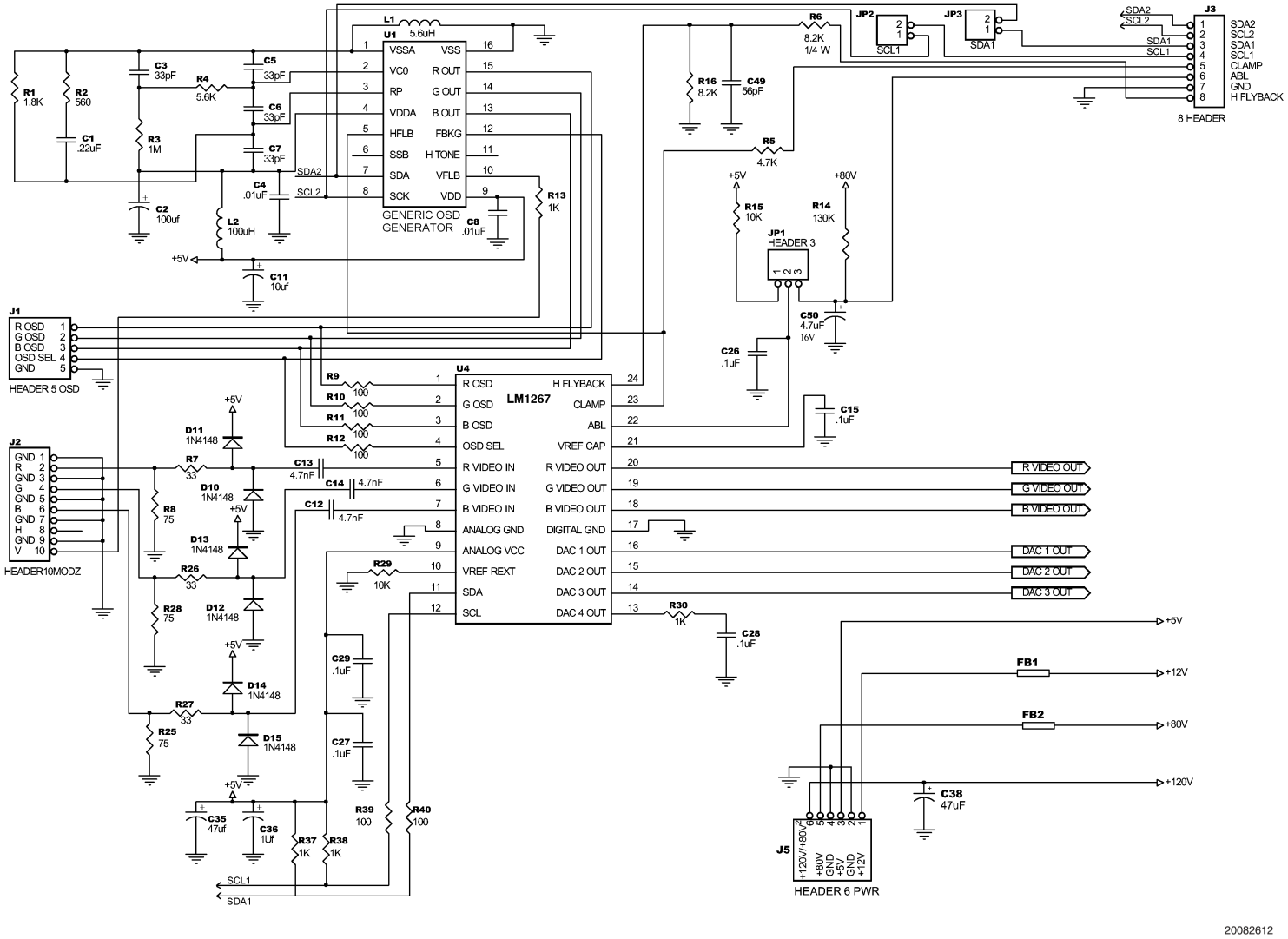


FIGURE 10. LM1267/2460 Demonstration Board Schematic

Application Hints (Continued)

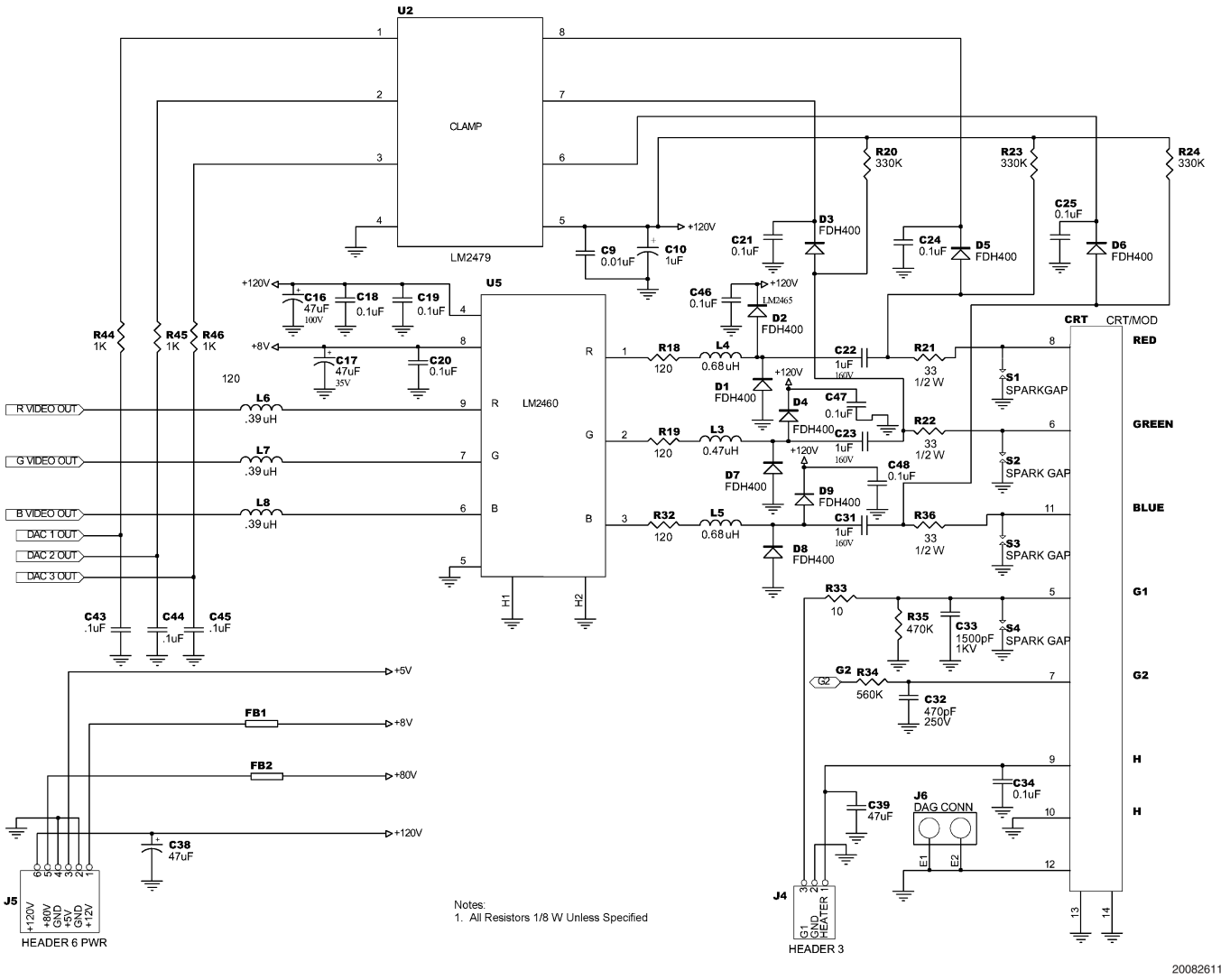
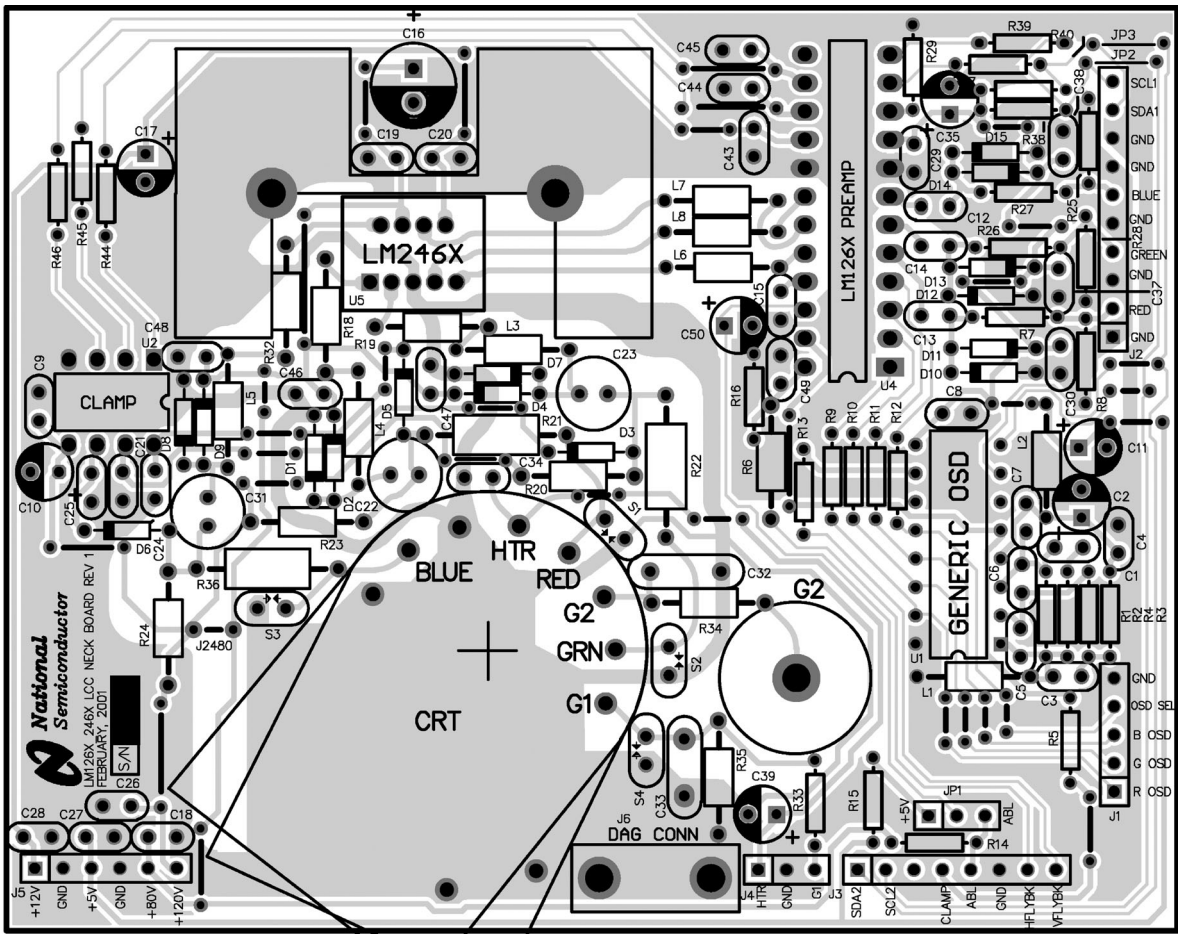


FIGURE 11. LM1267/2460 Demonstration Board Schematic (continued)

Application Hints (Continued)



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FIGURE 12. LM126X/246X Demo Board Layout

Application Hints (Continued)

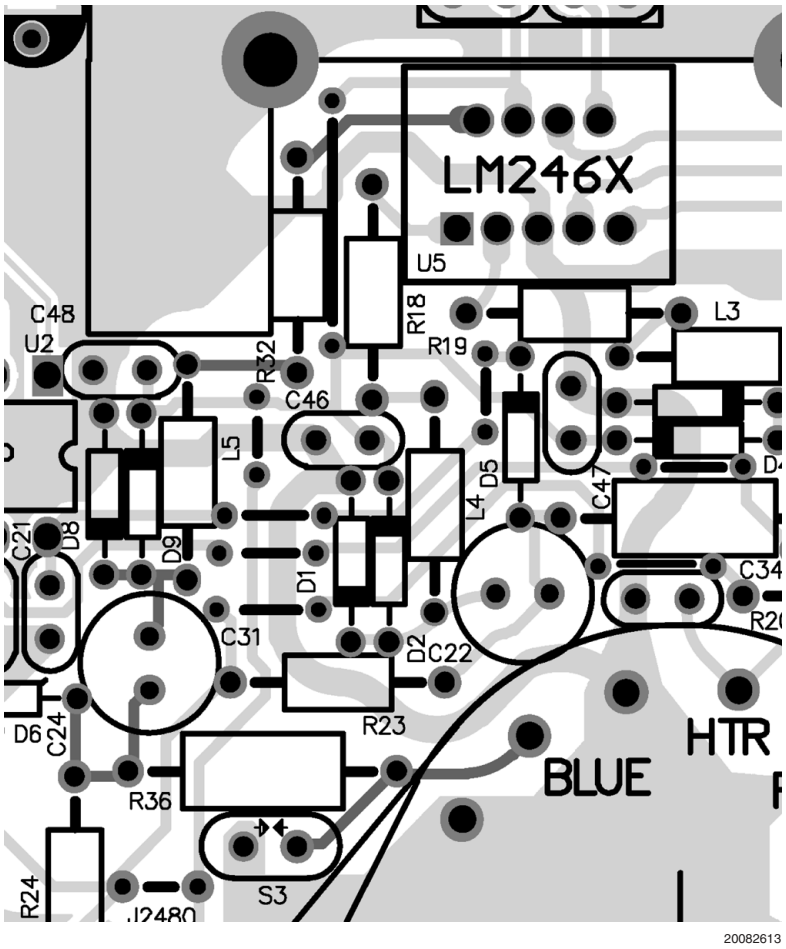
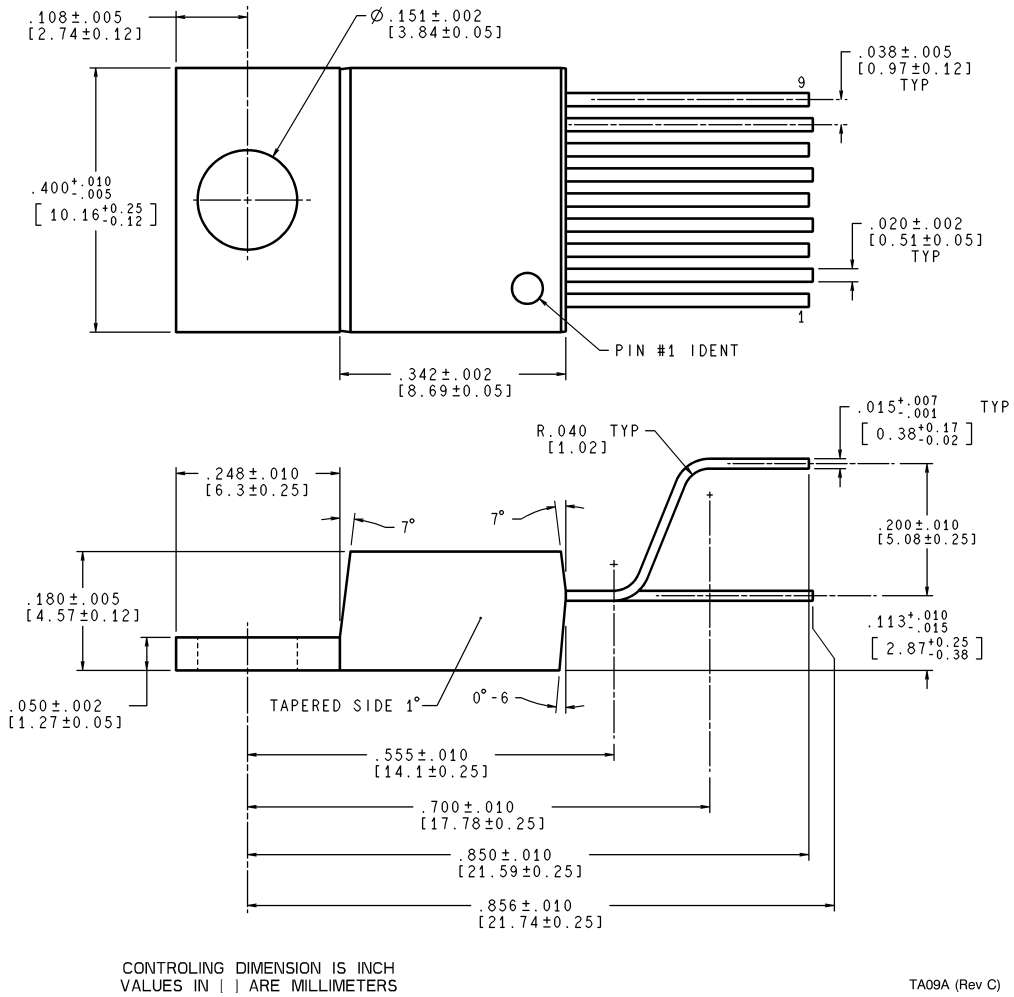


FIGURE 13. Trace Routing and Component Placement for Blue Channel Output

Physical Dimensions inches (millimeters) unless otherwise noted



CONTROLING DIMENSION IS INCH
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TA09A (Rev C)

NS Package Number TA09A
Order Number LM2460TA

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