ELPIDA

DATA SHEET

128M bits SDRAM

EDS1232CATA (4M words × 32 bits)

Description

The EDS1232CA is a 128M bits SDRAM organized as 1,048,576 words × 32 bits × 4 banks. All inputs and outputs are synchronized with the positive edge of the clock.

It is packaged in 86-pin plastic TSOP (II).

Features

- 2.5V power supply
- Clock frequency: 100MHz (max.)
- Single pulsed /RAS
- ×32 organization
- 4 banks can operate simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length (BL): 1, 2, 4, 8 and full page
- 2 variations of burst sequence
  - — Sequential (BL = 1, 2, 4, 8, full page)
  - — Interleave (BL = 1, 2, 4, 8)
- Programmable /CAS latency (CL): 2, 3
- Byte control by DQM
- Refresh cycles: 4096 refresh cycles/64ms
- 2 variations of refresh
  - — Auto refresh
  - — Self refresh

Pin Configurations

/xxx indicate active low signal.

86-pin Plastic TSOP(II)

VDD	1	86	VSS
DQ0	2	85	DQ15
VDDQ	3	84	VSSQ
DQ1	4	83	DQ14
DQ2	5	82	DQ13
VSSQ	6	81	VDDQ
DQ3	7	80	DQ12
DQ4	8	79	DQ11
VDDQ	9	78	VSSQ
DQ5	10	77	DQ10
DQ6	11	76	DQ9
VSSQ	12	75	VDDQ
DQ7	13	74	DQ8
NC	14	73	NC
VDD	15	72	VSS
DQM0	16	71	DQM1
/WE	17	70	NC
/CAS	18	69	NC
/RAS	19	68	CLK
/CS	20	67	CKE
A11	21	66	A9
BA0	22	65	A8
BA1	23	64	A7
A10(AP)	24	63	A6
A0	25	62	A5
A1	26	61	A4
A2	27	60	A3
DQM2	28	59	DQM3
VDD	29	58	VSS
NC	30	57	NC
DQ16	31	56	DQ31
VSSQ	32	55	VDDQ
DQ17	33	54	DQ30
DQ18	34	53	DQ29
VDDQ	35	52	VSSQ
DQ19	36	51	DQ28
DQ20	37	50	DQ27
VSSQ	38	49	VDDQ
DQ21	39	48	DQ26
DQ22	40	47	DQ25
VDDQ	41	46	VSSQ
DQ23	42	45	DQ24
VDD	43	44	VSS

(Top view)

A0 to A11,	Address inputs	DQM0 to DQM3	DQ mask enable
BA0, BA1	Bank select	CKE	Clock enable
DQ0 to DQ31	Data input/output	CLK	Clock input
/CS	Chip select	VDD	Supply voltage
/RAS	Row address strobe	VSS	Ground
/CAS	Column address strobe	VDDQ	Supply voltage for DQ
/WE	Write enable	VSSQ	Ground for DQ
		NC	No connection

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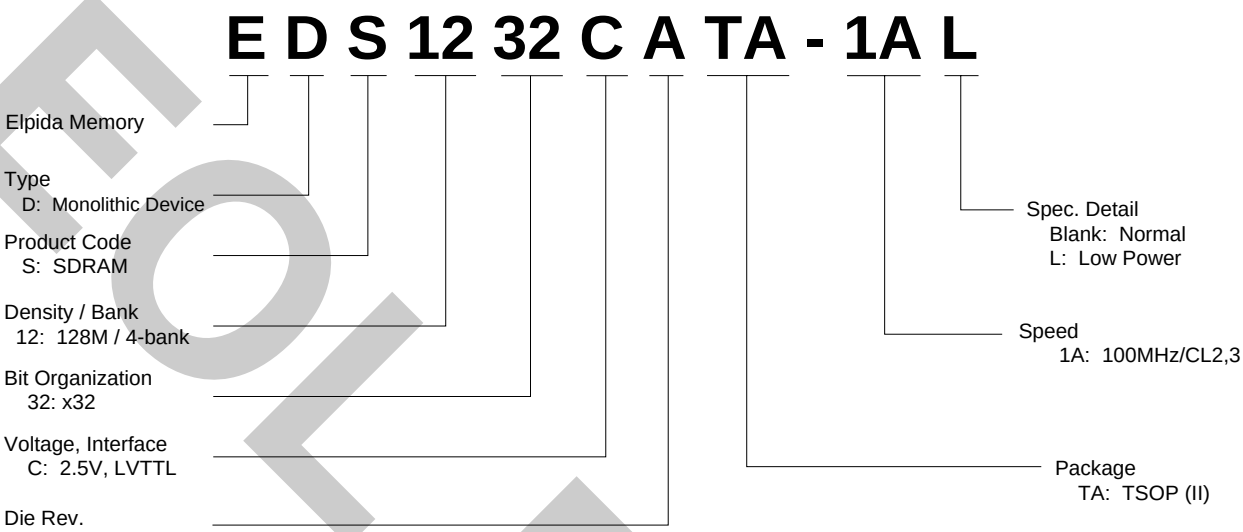
This product became EOL in March, 2007.

Ordering Information

Part number	Supply voltage	Organization (words × bits)	Internal Banks	Clock frequency MHz (max.)	/CAS latency	Package
EDS1232CATA-1A	2.5V	4M × 32	4	100	2, 3	86-pin plastic
EDS1232CATA-1AL						TSOP (II)

Part Number



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Electrical Specifications

- All voltages are referenced to VSS (GND).
- After power up, execute power up sequence and initialization sequence before proper device operation is achieved (refer to the Power up sequence).

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Voltage on any pin relative to VSS	VT	–0.5 to +3.6	V	
Supply voltage relative to VSS	VDD, VDDQ	–0.5 to +3.6	V	
Short circuit output current	IOS	50	mA	
Power dissipation	PD	1.0	W	
Operating ambient temperature	TA	0 to +70	°C	
Storage temperature	Tstg	–55 to +125	°C	

Caution

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (TA = 0 to +70°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply voltage	VDD, VDDQ	2.3	2.5	2.7	V	
	VSS	0	0	0	V	
Input high voltage	VIH	1.7	—	VDD + 0.3*[1]	V	
Input low voltage	VIL	–0.3	—	0.7	V	

Notes: 1. VIH (max.) = VDDQ + 1.5V (pulse width ≤ 5ns).
2. VIL (min.) = –1.5V (pulse width ≤ 5ns).

DC Characteristics 1 (TA = 0 to +70°C, VDD, VDDQ = 2.5V±0.2V, VSS, VSSQ = 0V)

Parameter /CAS latency	Symbol	Grade	max.	Unit	Test condition	Notes
Operating current (CL = 2)	IDD1		100	mA	Burst length = 1 tRC ≥ tRC (min.) IO = 0mA One bank active	1
(CL = 3)	IDD1		100	mA		
Standby current in power down	IDD2P		1	mA	CKE ≤ VIL (max.) tCK = 15ns	
Standby current in power down (input signal stable)	IDD2PS		1	mA	CKE ≤ VIL (max.) tCK = ∞	
Standby current in non power down	IDD2N		20	mA	CKE ≥ VIH (min.) tCK = 15ns CS ≥ VIH (min.) Input signals are changed one time during 30ns	
Standby current in non power down (input signal stable)	IDD2NS		8	mA	CKE ≥ VIH (min.) tCK = ∞	
Active standby current in power down	IDD3P		5	mA	CKE ≤ VIL (max.) tCK = 15ns	
Active standby current in power down (input signal stable)	IDD3PS		4	mA	CKE ≤ VIL (max.), tCK = ∞	
Active standby current in non power down	IDD3N		25	mA	CKE ≥ VIH (min.), tCK = 15 ns, /CS ≥ VIH (min.), Input signals are changed one time during 30ns.	
Active standby current in non power down (input signal stable)	IDD3NS		15	mA	CKE ≥ VIH (min.), tCK = ∞,	
Burst operating current	IDD4		130	mA	tCK ≥ tCK (min.), IO = 0mA, All banks active	2
Refresh current	IDD5		200	mA	tRC ≥ tRC (min.)	3
Self refresh current	IDD6		2.0	mA	VIH ≥ VDD − 0.2V, VIL ≤ GND + 0.2V	
Self refresh current (L-version)	IDD6	-xxL	0.6	mA		

Notes: 1. IDD1 depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, IDD1 is measured condition that addresses are changed only one time during tCK (min.).

2. IDD4 depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, IDD4 is measured condition that addresses are changed only one time during tCK (min.).

3. IDD5 is measured on condition that addresses are changed only one time during tCK (min.).

DC Characteristics 2 (TA = 0 to +70°C, VDD, VDDQ = 2.5V±0.2V, VSS, VSSQ = 0V)

Parameter	Symbol	min.	max.	Unit	Test condition	Notes
Input leakage current	ILI	–1.0	1.0	µA	0 = VIN = VDDQ, VDDQ = VDD, All other pins not under test = 0V	
Output leakage current	ILO	–1.5	1.5	µA	0 = VIN = VDDQ DOUT is disabled	
Output high voltage	VOH	2.0	—	V	IOH = –1mA	
Output low voltage	VOL	—	0.4	V	IOL = 1mA	

Pin Capacitance (TA = 25°C, f = 1MHz)

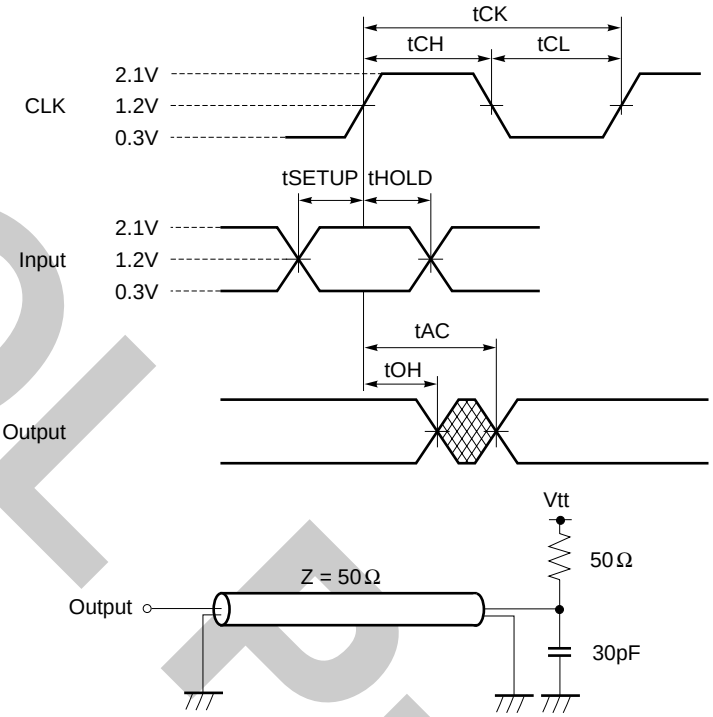
Parameter	Symbol	Pins	min.	Typ	max.	Unit	Notes
Input capacitance	CI1	Address	2.5	—	4.0	pF	
	CI2	CLK, CKE, /CS, /RAS, /CAS, /WE, DQM	2.5	—	4.0	pF	
Data input/output capacitance	CI/O	DQ	4.0	—	6.5	pF	

AC Characteristics (TA = 0 to +70°C, VDD, VDDQ = 2.5V±0.2V, VSS, VSSQ = 0V)

		-1A			
Parameter	Symbol	min.	max.	Unit	Notes
System clock cycle time (CL = 2)	tCK	10	—	ns	
(CL = 3)	tCK	10	—	ns	
CLK high pulse width	tCH	3	—	ns	
CLK low pulse width	tCL	3	—	ns	
Access time from CLK	tAC	—	6	ns	
Data-out hold time	tOH	2	—	ns	
CLK to Data-out low impedance	tLZ	0	—	ns	
CLK to Data-out high impedance	tHZ	2	6	ns	
Input setup time	tSI	2	—	ns	
Input hold time	tHI	1	—	ns	
CKE setup time (Power down exit)	tCKSP	2	—	ns	
ACT to REF/ACT command period (operation)	tRC	70	—	ns	
(refresh)	tRC	70	—	ns	
Active to Precharge command period	tRAS	50	120000	ns	
Active command to column command (same bank)	tRCD	20	—	ns	
Precharge to active command period	tRP	20	—	ns	
Write recovery or data-in to precharge lead time	tDPL	20	—	ns	
Last data into active latency	tDAL	2CLK + 20ns	—		
Active (a) to Active (b) command period	tRRD	20	—	ns	
Mode register set cycle time	tRSC	2	—	CLK	
Transition time (rise and fall)	tT	0.5	30	ns	
Refresh period (4096 refresh cycles)	tREF	—	64	ms	

Test Conditions

- AC high level input voltage / low level input voltage: 2.1V / 0.3V
- Input timing measurement reference level: 1.2V
- Transition time (Input rise and fall time): 1ns
- Output timing measurement reference level: 1.2V
- Termination voltage (Vtt): 1.2V



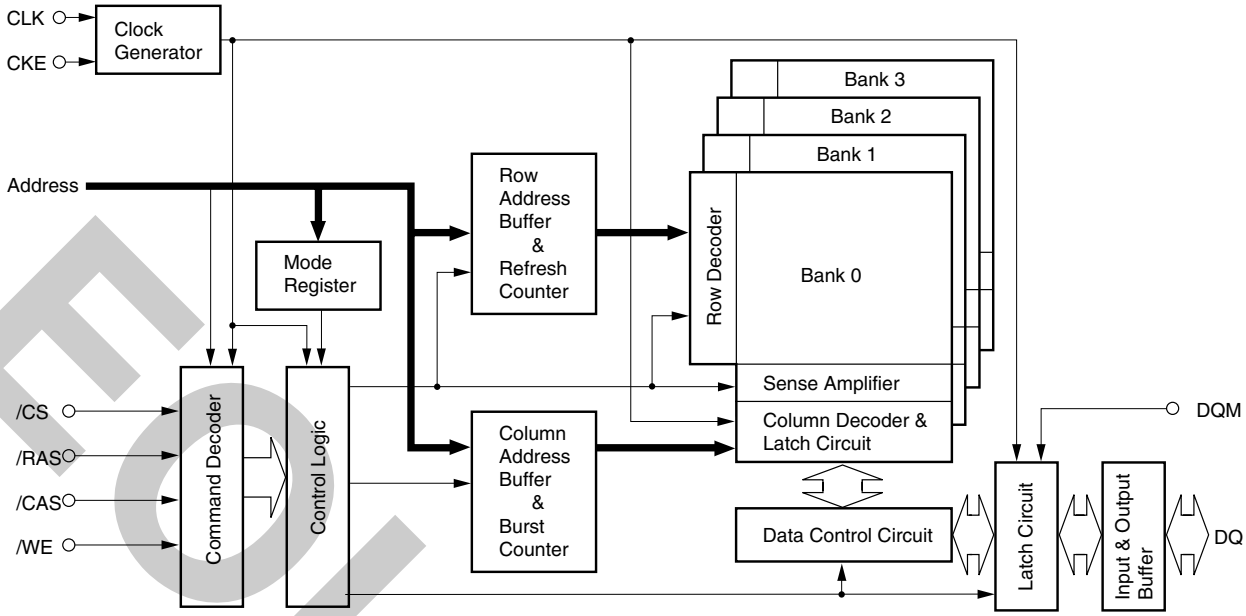
Input Waveforms and Output Load

Relationship Between Frequency and Minimum Latency

Parameter		-1A			
Frequency (MHz)		100	77		
tCK (ns)	Symbol	10	13	Unit	Notes
Active command to column command (same bank)	*I*RCD	2	2	tCK	1
Active command to active command (same bank)	*I*RC	7	6	tCK	1
Active command to precharge command (same bank)	*I*RAS	5	4	tCK	1
Precharge command to active command (same bank)	*I*RP	2	2	tCK	1
Write recovery or data-in to precharge command (same bank)	*I*DPL	2	2	tCK	1
Active command to active command (different bank)	*I*RRD	2	2	tCK	1
Self refresh exit time	*I*SREX	1	1	tCK	2
Last data in to active command (Auto precharge, same bank)	*I*DAL	4	4	tCK	= [*I*DPL + *I*RP]
Self refresh exit to command input	*I*SEC	7	6	tCK	= [*I*RC] 3
Precharge command to high impedance (CL = 2)	*I*HZP	2	2	tCK	
(CL = 3)	*I*HZP	3	3	tCK	
Last data out to active command (Auto precharge, same bank)	*I*APR	1	1	tCK	
Last data out to precharge (early precharge) (CL = 2)	*I*EP	–1	–1	tCK	
(CL = 3)	*I*EP	–2	–2	tCK	
Column command to column command	*I*CCD	1	1	tCK	
Write command to data in latency	*I*WCD	0	0	tCK	
DQM to data in	*I*DID	0	0	tCK	
DQM to data out	*I*DOD	2	2	tCK	
CKE to CLK disable	*I*CLE	1	1	tCK	
Register set to active command	*I*MRD	2	2	tCK	
/CS to command disable	*I*CDD	0	0	tCK	
Power down exit to command input	*I*PEC	1	1	tCK	

Notes: 1. *I*RCD to *I*RRD are recommended value.
2. Be valid [DESL] or [NOP] at next command of self refresh exit.
3. Except [DESL] and [NOP]

Block Diagram



Pin Function

CLK (input pin)

CLK is the master clock input. Other inputs signals are referenced to the CLK rising edge.

CKE (input pins)

CKE determine validity of the next CLK (clock). If CKE is high, the next CLK rising edge is valid; otherwise it is invalid. If the CLK rising edge is invalid, the internal clock is not issued and the Synchronous DRAM suspends operation.

When the Synchronous DRAM is not in burst mode and CKE is negated, the device enters power down mode. During power down mode, CKE must remain low.

/CS (input pins)

/CS low starts the command input cycle. When /CS is high, commands are ignored but operations continue.

/RAS, /CAS, and /WE (input pins)

/RAS, /CAS and /WE have the same symbols on conventional DRAM but different functions. For details, refer to the command table.

A0 to A11 (input pins)

Row Address is determined by A0 to A11 at the CLK (clock) rising edge in the active command cycle.

Column Address is determined by A0 to 7 at the CLK rising edge in the read or write command cycle.

A10 defines the precharge mode. When A10 is high in the precharge command cycle, all banks are precharged; when A10 is low, only the bank selected by BA0 and BA1 is precharged.

When A10 is high in read or write command cycle, the precharge starts automatically after the burst access.

BA0 and BA1 (input pin)

BA0 and BA1 are bank select signal. (See Bank Select Signal Table)

[Bank Select Signal Table]

	BA0	BA1
Bank 0	L	L
Bank 1	H	L
Bank 2	L	H
Bank 3	H	H

Remark: H: VIH. L: VIL.

DQM (input pins)

DQM controls I/O buffers. DQM0 controls DQ0 to 7, DQM1 controls DQ8 to DQ15, DQM2 controls DQ16 to DQ23, DQM3 controls DQ24 to DQ31. In read mode, DQM controls the output buffers like a conventional /OE pin. DQM high and DQM low turn the output buffers off and on, respectively. The DQM latency for the read is two clocks. In write mode, DQM controls the word mask. Input data is written to the memory cell if DQM is low but not if DQM is high. The DQM latency for the write is zero.

DQ0 to DQ31 (input/output pins)

DQ pins have the same function as I/O pins on a conventional DRAM.

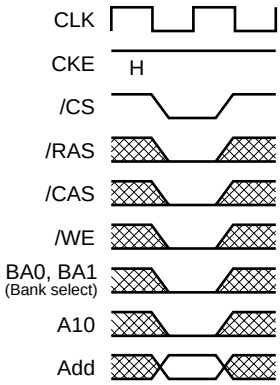
VDD, VSS, VDDQ, VSSQ (Power supply)

VDD and VSS are power supply pins for internal circuits. VDDQ and VSSQ are power supply pins for the output buffers.

Command Operation

Mode register set command (/CS, /RAS, /CAS, /WE)

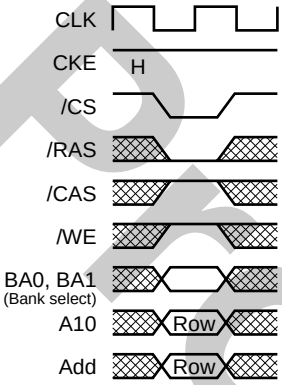
The Synchronous DRAM has a mode register that defines how the device operates. In this command, A0 through A11 are the data input pins. After power on, the mode register set command must be executed to initialize the device. The mode register can be set only when all banks are in idle state. During 2CLK (tRSC) following this command, the Synchronous DRAM cannot accept any other commands.



Mode Register Set Command

Activate command (/CS, /RAS = Low, /CAS, /WE = High)

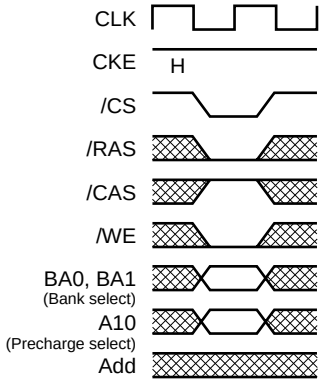
The Synchronous DRAM has four banks, each with 4,096 rows. This command activates the bank selected by BA0 and BA1 and a row address selected by A0 through A11. This command corresponds to a conventional DRAM's /RAS falling.



Row Address Strobe and Bank Activate Command

Precharge command (/CS, /RAS, /WE = Low, /CAS = High)

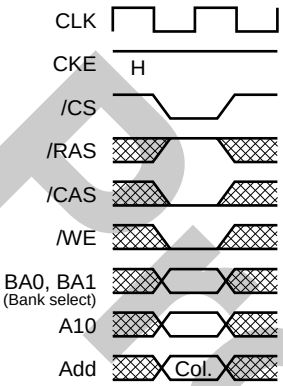
This command begins precharge operation of the bank selected by BA0 and BA1. When A10 is High, all banks are precharged, regardless of BA0 and BA1. When A10 is Low, only the bank selected by BA0 and BA1 is precharged. After this command, the Synchronous DRAM can't accept the activate command to the precharging bank during tRP (precharge to activate command period). This command corresponds to a conventional DRAM's /RAS rising.



Precharge Command

Write command (/CS, /CAS, /WE = Low, /RAS = High)

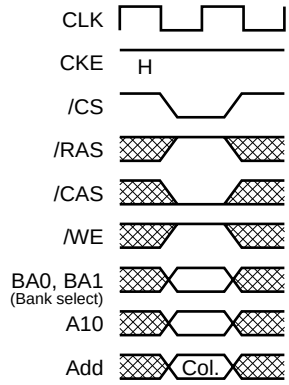
If the mode register is in the burst write mode, this command sets the burst start address given by the column address to begin the burst write operation. The first write data in burst mode can input with this command with subsequent data on following clocks.



Column Address and Write Command

Read command (/CS, /CAS = Low, /RAS, /WE = High)

Read data is available after /CAS latency requirements have been met. This command sets the burst start address given by the column address.

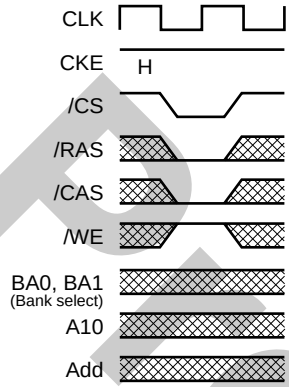


Column Address and and Read Command

CBR (auto) refresh command (/CS, /RAS, /CAS = Low, /WE, CKE = High)

This command is a request to begin the CBR (auto) refresh operation. The refresh address is generated internally.

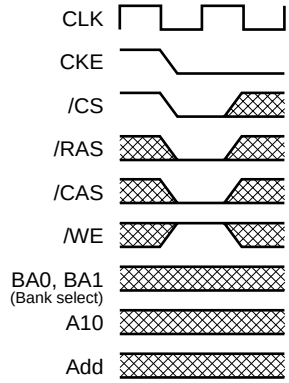
Before executing CBR (auto) refresh, all banks must be precharged. After this cycle, all banks will be in the idle (precharged) state and ready for a row activate command. During tRC period (from refresh command to refresh or activate command), the Synchronous DRAM cannot accept any other command



CBR (auto) Refresh Command

Self refresh entry command (/CS, /RAS, /CAS, CKE = Low, /WE = High)

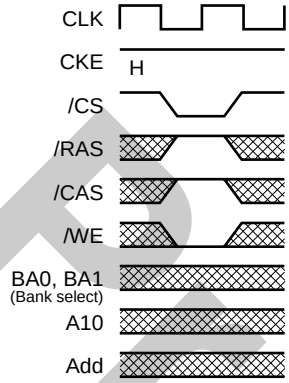
After the command execution, self refresh operation continues while CKE remains low. When CKE goes high, the Synchronous DRAM exits the self refresh mode. During self refresh mode, refresh interval and refresh operation are performed internally, so there is no need for external control. Before executing self refresh, all banks must be precharged.



Self Refresh Entry Command

Burst stop command (/CS = /WE = Low, /RAS, /CAS = High)

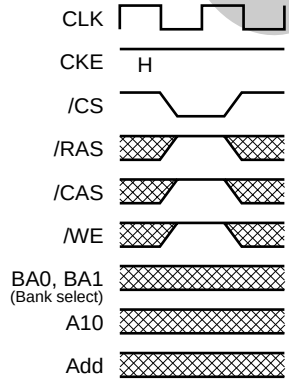
This command can stop the current burst operation.



Burst Stop Command in Full Page Mode

No operation (/CS = Low, /RAS, /CAS, /WE = High)

This command is not an execution command. No operations begin or terminate by this command.



No Operation

Truth Table

Command Truth Table

Function	Symbol	CKE n – 1	CKE n	/CS	/RAS	/CAS	/WE	BA0, BA1	A10	A9 - A0, A11
Device deselect	DESL	H	×	H	×	×	×	×	×	×
No operation	NOP	H	×	L	H	H	H	×	×	×
Burst stop	BST	H	×	L	H	H	L	×	×	×
Read	READ	H	×	L	H	L	H	V	L	V
Read with auto precharge	READA	H	×	L	H	L	H	V	H	V
Write	WRIT	H	×	L	H	L	L	V	L	V
Write with auto precharge	WRITA	H	×	L	H	L	L	V	H	V
Bank activate	ACT	H	×	L	L	H	H	V	V	V
Precharge select bank	PRE	H	×	L	L	H	L	V	L	×
Precharge all banks	PALL	H	×	L	L	H	L	×	H	×
Mode register set	MRS	H	×	L	L	L	L	L	L	V

Remark: H: VIH. L: VIL. ×: VIH or VIL, V = Valid data

DQM Truth Table

Function	Symbol	CKE n – 1	CKE n	DQM 0	DQM 1	DQM 2	DQM 3
Data write / output enable	ENB	H	×	L	L	L	L
Data mask / output disable	MASK	H	×	H	H	H	H
DQ0 to DQ7 write enable/output enable	ENB0	H	×	L	×	×	×
DQ8 to DQ15 write enable/output enable	ENB1	H	×	×	L	×	×
DQ16 to DQ23 write enable/output enable	ENB2	H	×	×	×	L	×
DQ24 to DQ31 write enable/output enable	ENB3	H	×	×	×	×	L
DQ0 to DQ7 write inhibit/output disable	MASK0	H	×	H	×	×	×
DQ8 to DQ15 write inhibit/output disable	MASK 1	H	×	×	H	×	×
DQ16 to DQ23 write inhibit/output disable	MASK 2	H	×	×	×	H	×
DQ24 to DQ31 write inhibit/output disable	MASK 3	H	×	×	×	×	H

Remark: H: VIH. L: VIL. ×: VIH or VIL

CKE Truth Table

Current state	Function	Symbol	CKE n – 1	CKE n	/CS	/RAS	/CAS	/WE	Address
Activating	Clock suspend mode entry		H	L	×	×	×	×	×
Any	Clock suspend mode		L	L	×	×	×	×	×
Clock suspend	Clock suspend mode exit		L	H	×	×	×	×	×
Idle	CBR (auto) refresh command	REF	H	H	L	L	L	H	×
Idle	Self refresh entry	SELF	H	L	L	L	L	H	×
Self refresh	Self refresh exit		L	H	L	H	H	H	×
			L	H	H	×	×	×	×
Idle	Power down entry		H	L	L	H	H	H	×
			H	L	H	×	×	×	×
Power down	Power down exit		L	H	H	×	×	×	×
			L	H	L	H	H	H	×

Remark: H: VIH. L: VIL. ×: VIH or VIL

Function Truth Table*[1]

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Notes
Idle	H	×	×	×	×	DESL	Nop or power down	2
	L	H	H	×	×	NOP or BST	Nop or power down	2
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	Row activating	
	L	L	H	L	BA, A10	PRE/PALL	Nop	
	L	L	L	H	×	REF/SELF	CBR (auto) refresh or self refresh	4
	L	L	L	L	OPCODE	MRS	Mode register accessing	
Row active	H	×	×	×	×	DESL	Nop	
	L	H	H	×	×	NOP or BST	Nop	
	L	H	L	H	BA, CA, A10	READ/READA	Begin read: Determine AP	5
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	Begin write: Determine AP	5
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Precharge	6
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	OPCODE	MRS	ILLEGAL	
Read	H	×	×	×	×	DESL	Continue burst to end → Row active	
	L	H	H	H	×	NOP	Continue burst to end → Row active	
	L	H	H	L	×	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ/READA	Terminate burst, new read: Determine AP	7
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Terminate burst, begin write: Determine AP	7, 8
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst, Precharging	
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	OPCODE	MRS	ILLEGAL	
Write	H	×	×	×	×	DESL	Continue burst to end → Write recovering	
	L	H	H	H	×	NOP	Continue burst to end → Write recovering	
	L	H	H	L	×	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ/READA	Terminate burst, start read : Determine AP	7, 8
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Terminate burst, new write : Determine AP	7
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst, Precharging	9
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	OPCODE	MRS	ILLEGAL	

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Notes
Read with auto precharge	H	×	×	×	×	DESL	Continue burst to end → Precharging	
	L	H	H	H	×	NOP	Continue burst to end → Precharging	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	OPCODE	MRS	ILLEGAL	
Write with auto precharge	H	×	×	×	×	DESL	Continue burst to end → Write recovering with auto precharge	
	L	H	H	H	×	NOP	Continue burst to end → Write recovering with auto precharge	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	OPCODE	MRS	ILLEGAL	
Precharging	H	×	×	×	×	DESL	Nop → Enter idle after tRP	
	L	H	H	H	×	NOP	Nop → Enter idle after tRP	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Nop → Enter idle after tRP	
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	OPCODE	MRS	ILLEGAL	
Row activating	H	×	×	×	×	DESL	Nop → Enter bank active after tRCD	
	L	H	H	H	×	NOP	Nop → Enter bank active after tRCD	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3, 10
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	OPCODE	MRS	ILLEGAL	

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Notes
Write recovering	H	×	×	×	×	DESL	Nop → Enter row active after tDPL	
	L	H	H	H	×	NOP	Nop → Enter row active after tDPL	
	L	H	H	L	×	BST	Nop → Enter row active after tDPL	
	L	H	L	H	BA, CA, A10	READ/READA	Start read, Determine AP	8
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	New write, Determine AP	
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	OPCODE	MRS	ILLEGAL	
Write recovering with auto precharge	H	×	×	×	×	DESL	Nop → Enter precharge after tDPL	
	L	H	H	H	×	NOP	Nop → Enter precharge after tDPL	
	L	H	H	L	×	BST	Nop → Enter row active after tDPL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3, 8
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	OPCODE	MRS	ILLEGAL	
Refresh	H	×	×	×	×	DESL	Nop → Enter idle after tRC	
	L	H	H	H	×	NOP/BST	Nop → Enter idle after tRC	
	L	H	H	L	×	READ/READA	ILLEGAL	
	L	H	L	H	×	ACT/PRE/PALL	ILLEGAL	
	L	H	L	L	×	REF/SELF/MRS	ILLEGAL	
Mode register accessing	H	×	×	×	×	DESL	Nop → Enter idle after tRSC	
	L	H	H	H	×	NOP	Nop → Enter idle after tRSC	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	×	READ/READA	ILLEGAL	
	L	L	L	L	×	ACT/PRE/PLL/ REF/SELF/MRS	ILLEGAL	

Remark: H: VIH. L: VIL. ×: VIH or VIL, V = Valid data
BA: Bank Address, CA: Column Address, RA: Row Address

Notes: 1. All entries assume that CKE was active (High level) during the preceding clock cycle.
2. If all banks are idle, and CKE is inactive (Low level), the Synchronous DRAM will enter Power down mode.
3. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
4. If all banks are idle, and CKE is inactive (Low level), the Synchronous DRAM will enter Self refresh mode. All input buffers except CKE will be disabled.
5. Illegal if tRCD is not satisfied.
6. Illegal if tRAS is not satisfied.
7. Must satisfy burst interrupt condition.
8. Must satisfy bus contention, bus trun around, and/or write recovery requirements.
9. Must mask preceding data which don't satisfy tDPL.
10. Illegal if tRRD is not satisfied.

Command Truth Table for CKE

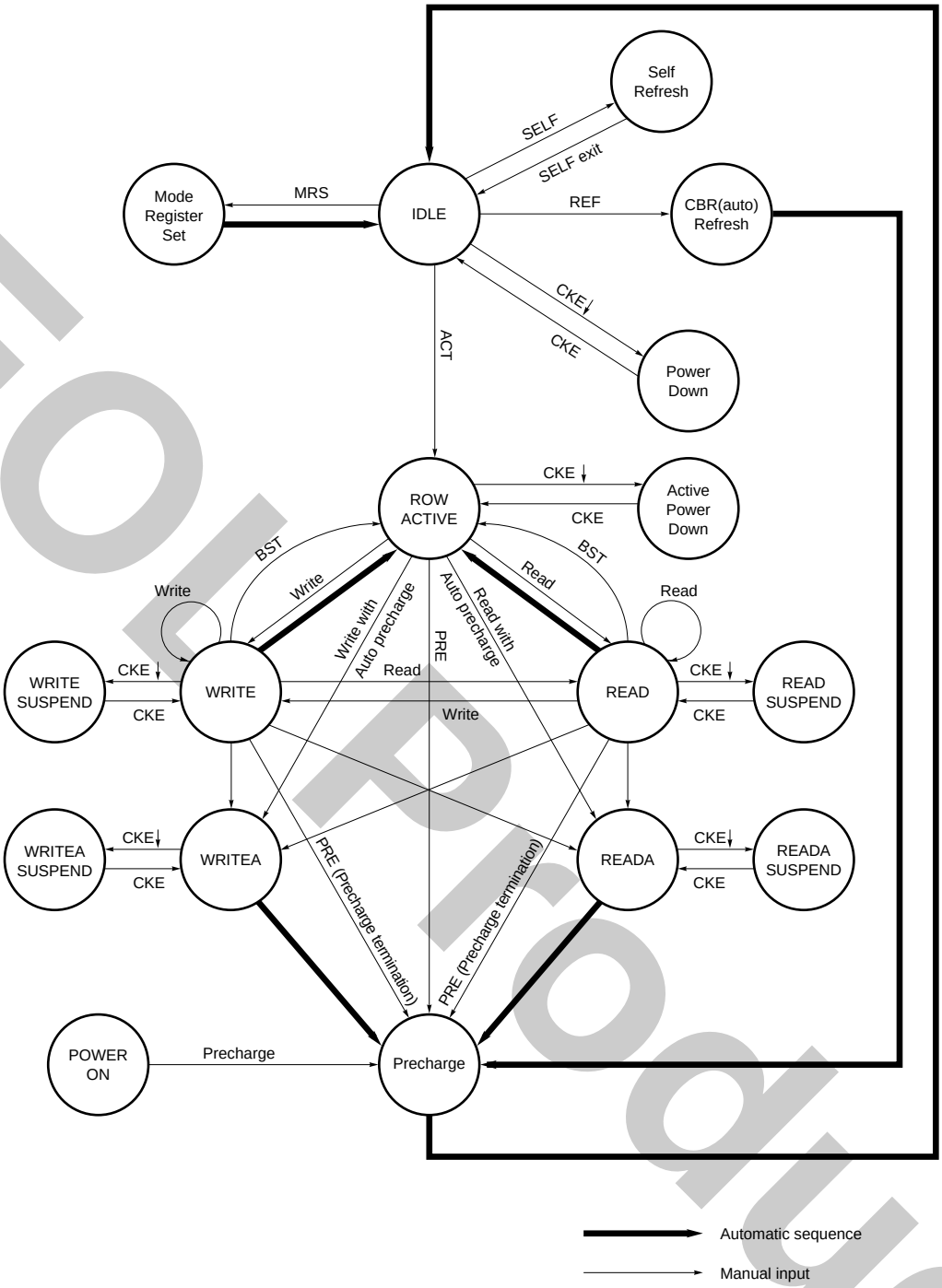
Current State	CKE n – 1	CKE n	/CS	/RAS	/CAS	/WE	Address	Operation	Notes
Self refresh	H	×	×	×	×	×	×	INVALID, CLK (n – 1) would exit self refresh	
	L	H	H	×	×	×	×	Self refresh recovery	
	L	H	L	H	H	×	×	Self refresh recovery	
	L	H	L	H	L	×	×	ILLEGAL	
	L	H	L	L	×	×	×	ILLEGAL	
	L	L	×	×	×	×	×	Continue self refresh	
Self refresh recovery	H	H	H	×	×	×	×	Idle after tRC	
	H	H	L	H	H	×	×	Idle after tRC	
	H	H	L	H	L	×	×	ILLEGAL	
	H	H	L	L	×	×	×	ILLEGAL	
	H	L	H	×	×	×	×	ILLEGAL	
	H	L	L	H	H	×	×	ILLEGAL	
	H	L	L	H	L	×	×	ILLEGAL	
	H	L	L	L	×	×	×	ILLEGAL	
Power down	H	×	×	×	×	×		INVALID, CLK (n – 1) would exit power down	
	L	H	H	×	×	×	×	EXIT power down	
	L	H	L	H	H	H	×	EXIT power down	
	L	L	×	×	×	×	×	Continue power down mode	
All banks idle	H	H	H	×	×	×		Refer to operations in Function Truth Table	
	H	H	L	H	×	×		Refer to operations in Function Truth Table	
	H	H	L	L	H	×		Refer to operations in Function Truth Table	
	H	H	L	L	L	H	×	CBR (auto) Refresh	
	H	H	L	L	L	L	OPCODE	Refer to operations in Function Truth Table	
	H	L	H	×	×	×		Begin power down next cycle	
	H	L	L	H	×	×		Refer to operations in Function Truth Table	
	H	L	L	L	H	×		Refer to operations in Function Truth Table	
	H	L	L	L	L	H	×	Self refresh	1
	H	L	L	L	L	L	OPCODE	Refer to operations in Function Truth Table	
	L	H	×	×	×	×	×	Exit power down next cycle	
	L	L	×	×	×	×	×	Power down	1
Row active	H	×	×	×	×	×	×	Refer to operations in Function Truth Table	
	L	×	×	×	×	×	×	Clock suspend	1
Any state other than	H	H	×	×	×	×		Refer to operations in Function Truth Table	
listed above	H	L	×	×	×	×	×	Begin clock suspend next cycle	2
	L	H	×	×	×	×	×	Exit clock suspend next cycle	
	L	L	×	×	×	×	×	Maintain clock suspend	

Remark**:** H = VIH, L = VIL, × = VIH or VIL

Notes: 1. Self refresh can be entered only from the all banks idle state. Power down can be entered only from all banks idle or row active state.

2. Must be legal command as defined in Function Truth Table.

Simplified State Diagram



Programming Mode Registers

The mode register is programmed by the Mode register set command using address bits A11 through A0, BA0 and BA1 as data inputs. The registers retain data until it is re-programmed, or the device loses power.

The mode register has three fields;

Options	:	A11 through A7, BA0, BA1
/CAS latency	:	A6 through A4
Wrap type	:	A3
Burst length	:	A2 through A0

Following mode register programming, no command can be issued before at least 2 CLK have elapsed.

/CAS Latency

/CAS latency is the most critical of the parameters being set. It tells the device how many clocks must elapse before the data will be available. The value is determined by the frequency of the clock and the speed grade of the device. ”Relationship between Frequency and Latency” shows the relationship of /CAS latency to the clock period and the speed grade of the device.

Burst Length

Burst Length is the number of words that will be output or input in a read or write cycle. After a read burst is completed, the output bus will become High-Z. The burst length is programmable as 1, 2, 4, 8 or full page.

Wrap Type (Burst Sequence)

The wrap type specifies the order in which the burst data will be addressed. This order is programmable as either “Sequential” or “Interleave”. The method chosen will depend on the type of CPU in the system.

Some microprocessor cache systems are optimized for sequential addressing and others for interleaved addressing. “Burst Length Sequence” shows the addressing sequence for each burst length using them. Both sequences support bursts of 1, 2, 4 and 8. Additionally, sequence supports the full page length.

Mode Register

BA0	BA1	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	1								JEDEC Standard Test Set (refresh counter test)
x	x	x	x	1	0	0	LTMODE			WT	BL			Burst Read and Single Write (for Write Through Cache)
					1	0								Use in future
x	x	x	x	x	1	1	V	V	V	V	V	V	V	Vender Specific
0	0	0	0	0	0	0	LTMODE			WT	BL			Mode Register Set

V = Valid
x = Don't care

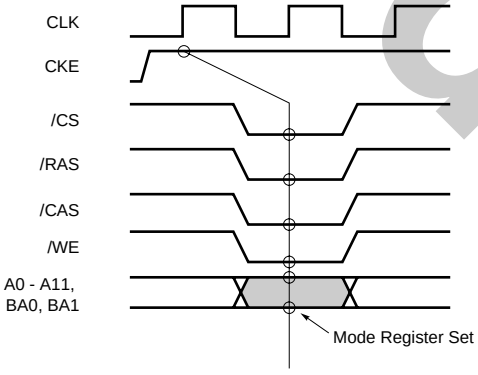
Burst length	Bits2-0	WT = 0	WT = 1
	000	1	1
	001	2	2
	010	4	4
	011	8	8
	100	R	R
	101	R	R
	110	R	R
	111	Full page	R

Wrap type		
	0	Sequential
	1	Interleave

Latency mode	Bits6-4	/CAS latency
	000	R
	001	R
	010	2
	011	3
	100	R
	101	R
	110	R
	111	R

Remark R : Reserved

Mode Register Set Timing



Burst Length and Sequence

[Burst of Two]

Starting address (column address A0, binary)	Sequential addressing sequence (decimal)	Interleave addressing sequence (decimal)
0	0, 1	0, 1
1	1, 0	1, 0

[Burst of Four]

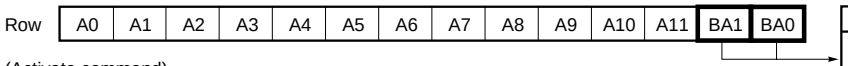
Starting address (column address A1 to A0, binary)	Sequential addressing sequence (decimal)	Interleave addressing sequence (decimal)
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 2, 3, 0	1, 0, 3, 2
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 0, 1, 2	3, 2, 1, 0

[Burst of Eight]

Starting address (column address A2 to A0, binary)	Sequential addressing sequence (decimal)	Interleave addressing sequence (decimal)
000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

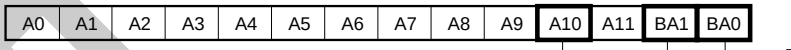
Full page burst is an extension of the above tables of sequential addressing, with the length being 256.

Address Bits of Bank-Select and Precharge



(Activate command)

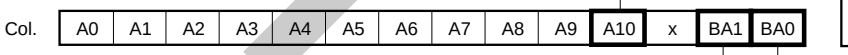
BA1	BA0	Result
0	0	**Select Bank 0 “Activate” command**
0	1	**Select Bank 1 “Activate” command**
1	0	**Select Bank 2 “Activate” command**
1	1	**Select Bank 3 “Activate” command**



(Precharge command)

A10	BA1	BA0	Result
0	0	0	**Precharge Bank 0**
0	0	1	**Precharge Bank 1**
0	1	0	**Precharge Bank 2**
0	1	1	**Precharge Bank 3**
1	x	x	**Precharge All Banks**

x : Don’t care



(/CAS strobes)

0	**disables Auto-Precharge (End of Burst)**
1	**enables Auto-Precharge (End of Burst)**

BA1	BA0	Result
0	0	**enables Read/Write commands for Bank 0**
0	1	**enables Read/Write commands for Bank 1**
1	0	**enables Read/Write commands for Bank 2**
1	1	**enables Read/Write commands for Bank 3**

Power-up sequence

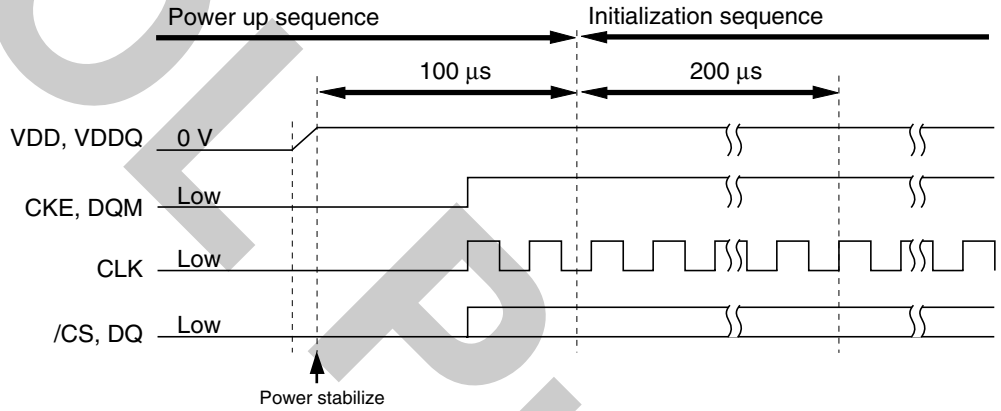
Power-up sequence

The SDRAM should be goes on the following sequence with power up.

The CLK, CKE, /CS, DQM and DQ pins keep low till power stabilizes.
The CLK pin is stabilized within 100 µs after power stabilizes before the following initialization sequence.
The CKE and DQM is driven to high between power stabilizes and the initialization sequence.
This SDRAM has VDD clamp diodes for CLK, CKE, /CS DQM and DQ pins. If these pins go high before power up, the large current flows from these pins to VDD through the diodes.

Initialization sequence

When 200 µs or more has past after the above power-up sequence, all banks must be precharged using the precharge command (PALL). After tRP delay, set 8 or more auto refresh commands (REF). Set the mode register set command (MRS) to initialize the mode register. We recommend that by keeping DQM and CKE to High, the output buffer becomes High-Z during Initialization sequence, to avoid DQ bus contention on memory system formed with a number of device.



Power-up sequence and Initialization sequence

Operation of the SDRAM

Read/Write Operations

Bank active

Before executing a read or write operation, the corresponding bank and the row address must be activated by the bank active (ACT) command. An interval of tRCD is required between the bank active command input and the following read/write command input.

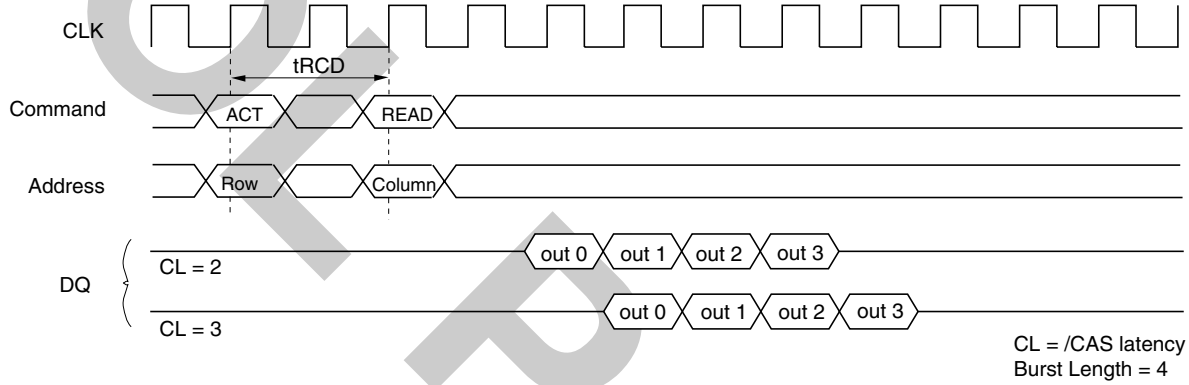
Read operation

A read operation starts when a read command is input. Output buffer becomes Low-Z in the (/CAS Latency - 1) cycle after read command set. The SDRAM can perform a burst read operation.

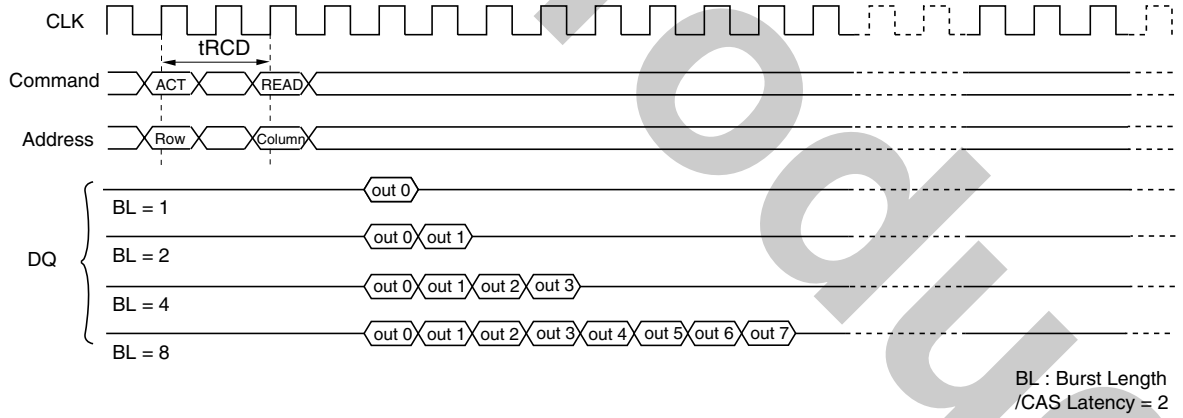
The burst length can be set to 1, 2, 4 and 8. The start address for a burst read is specified by the column address and the bank select address at the read command set cycle. In a read operation, data output starts after the number of clocks specified by the /CAS Latency. The /CAS Latency can be set to 2 or 3.

When the burst length is 1, 2, 4 and 8 the DOUT buffer automatically becomes High-Z at the next clock after the successive burst-length data has been output.

The /CAS latency and burst length must be specified at the mode register.



/CAS Latency

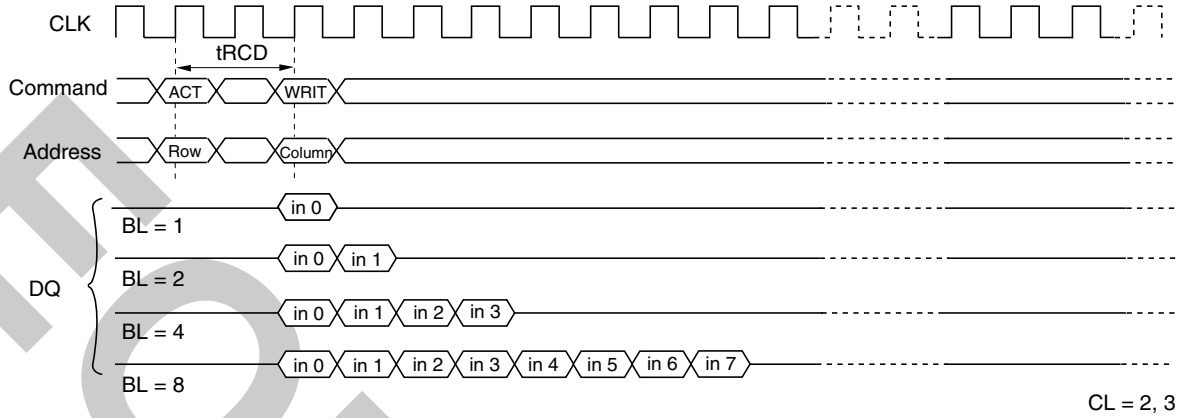


Burst Length

Write operation

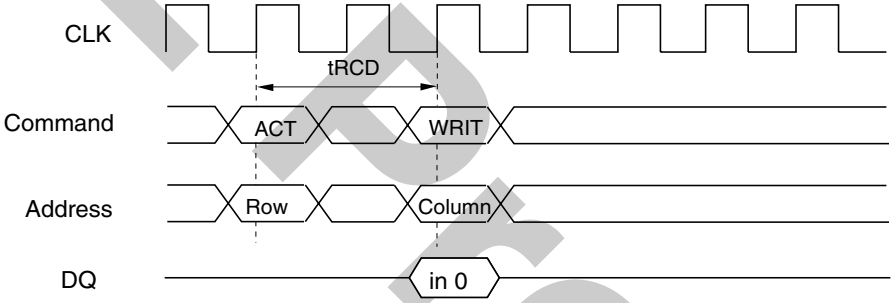
Burst write or single write mode is selected by the OPCODE of the mode register.

1. Burst write: A burst write operation is enabled by setting OPCODE (A9, A8) to (0, 0). A burst write starts in the same clock as a write command set. (The latency of data input is 0 clock.) The burst length can be set to 1, 2, 4 and 8, like burst read operations. The write start address is specified by the column address and the bank select address at the write command set cycle.



Burst write

2. Single write: A single write operation is enabled by setting OPCODE (A9, A8) to (1, 0). In a single write operation, data is only written to the column address and the bank select address specified by the write command set cycle without regard to the burst length setting. (The latency of data input is 0 clock).



Single write

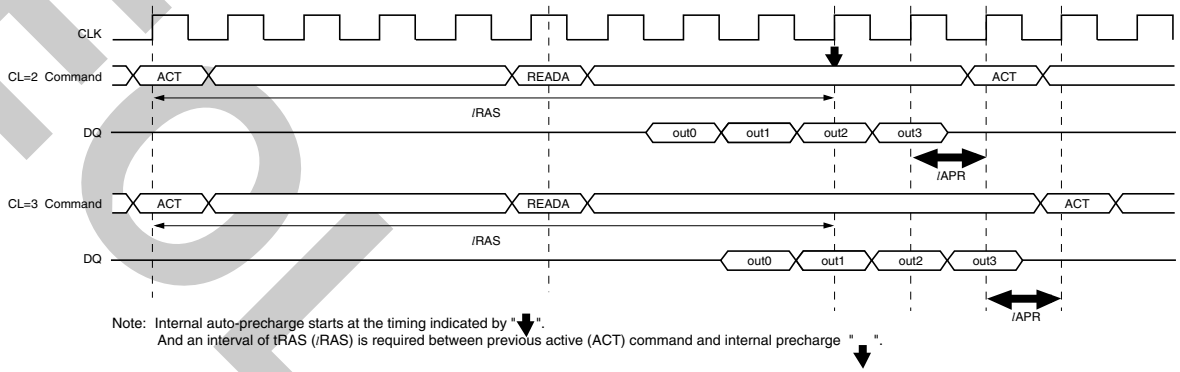
Auto Precharge

Read with auto-precharge

In this operation, since precharge is automatically performed after completing a read operation, a precharge command need not be executed after each read operation. The command executed for the same bank after the execution of this command must be the bank active (ACT) command. In addition, an interval defined by *l*APR is required before execution of the next command.

[Clock cycle time]

/CAS latency	Precharge start cycle
3	2 cycle before the final data is output
2	1 cycle before the final data is output

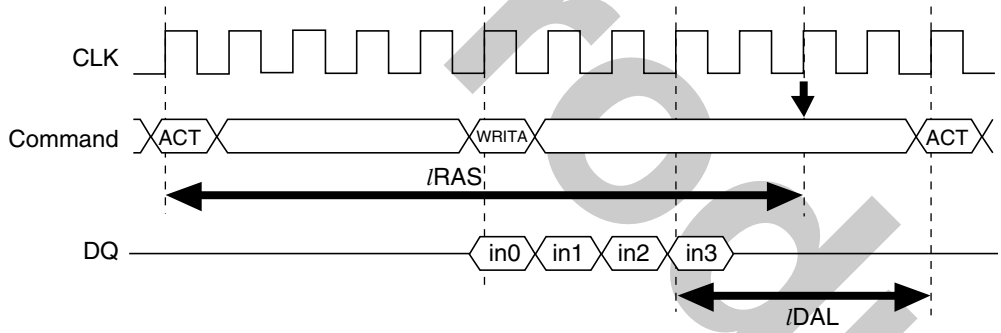


Note: Internal auto-precharge starts at the timing indicated by "↓".
And an interval of tRAS (/RAS) is required between previous active (ACT) command and internal precharge "↓".

Burst Read (BL = 4)

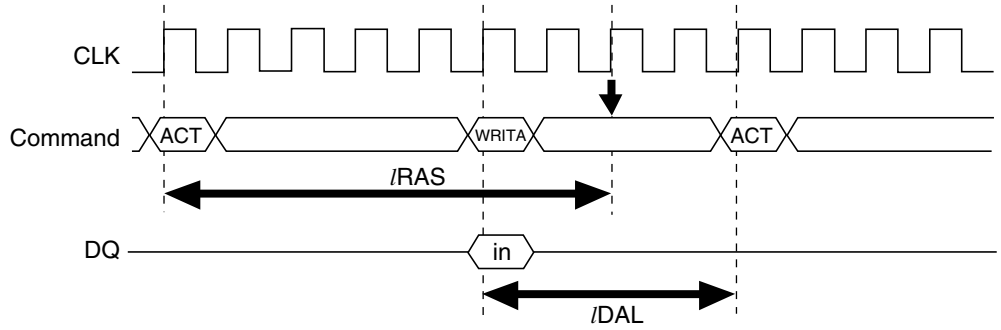
Write with auto-precharge

In this operation, since precharge is automatically performed after completing a burst write or single write operation, a precharge command need not be executed after each write operation. The command executed for the same bank after the execution of this command must be the bank active (ACT) command. In addition, an interval of *l*DAL is required between the final valid data input and input of next command.



Note: Internal auto-precharge starts at the timing indicated by "↓".
and an interval of tRAS (/RAS) is required between previous active (ACT) command and internal precharge "↓".

Burst Write (BL = 4)

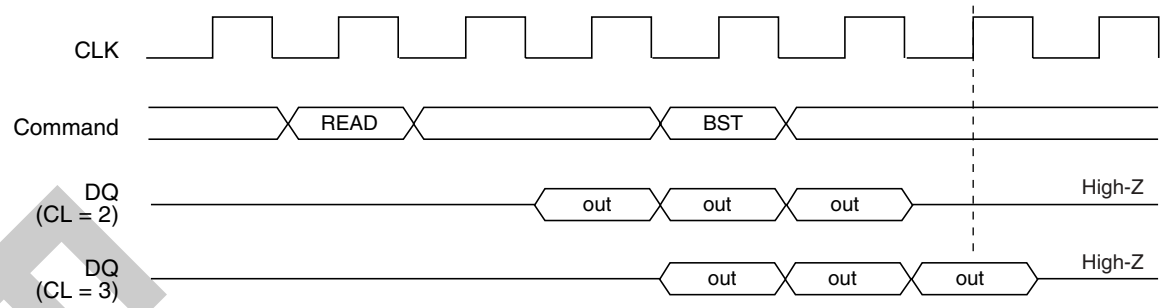


Note: Internal auto-precharge starts at the timing indicated by "↓".
and an interval of tRAS (/RAS) is required between previous active (ACT) command and internal precharge "↓".

Single Write

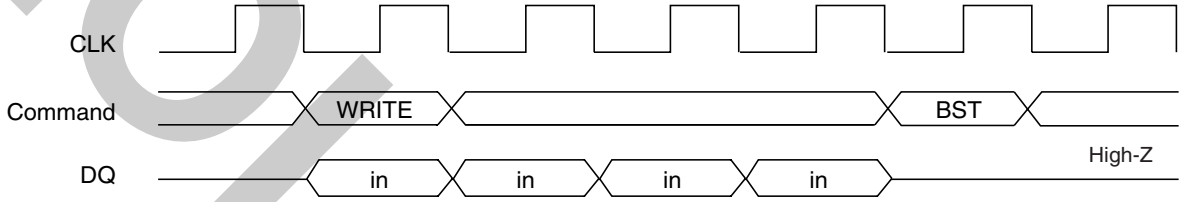
Burst Stop Command

During a read cycle, when the burst stop command is issued, the burst read data are terminated and the data bus goes to High-Z after the /CAS latency from the burst stop command.



Burst Stop at Read

During a write cycle, when the burst stop command is issued, the burst write data are terminated and data bus goes to High-Z at the same clock with the burst stop command.

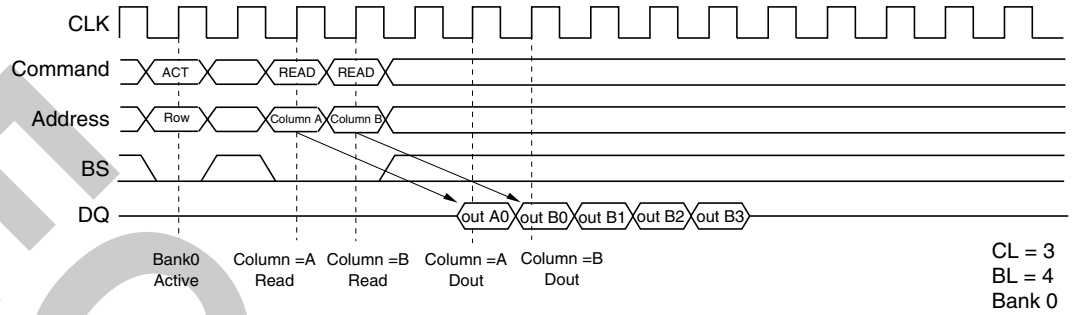


Burst Stop at Write

Command Intervals

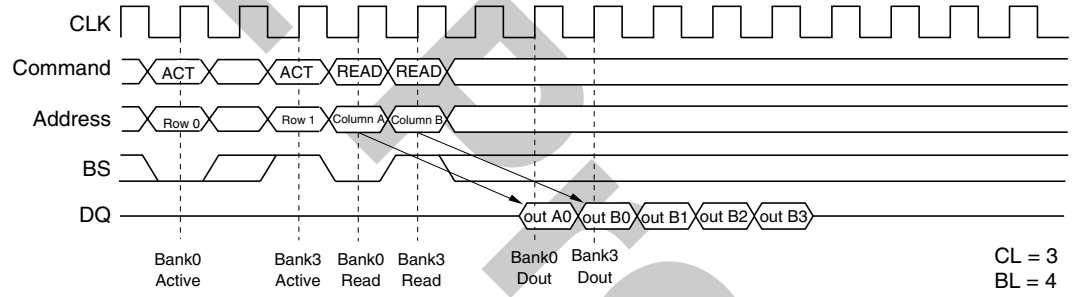
Read command to Read command interval

1. Same bank, same ROW address: When another read command is executed at the same ROW address of the same bank as the preceding read command execution, the second read can be performed after an interval of no less than 1 clock. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.



READ to READ Command Interval (same ROW address in same bank)

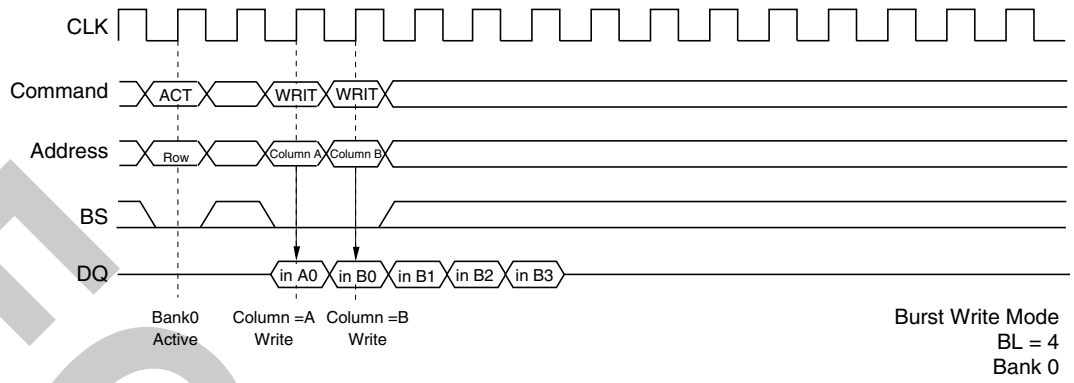
2. Same bank, different ROW address: When the ROW address changes on same bank, consecutive read commands cannot be executed; it is necessary to separate the two read commands with a precharge command and a bank active command.
3. Different bank: When the bank changes, the second read can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank active state. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.



READ to READ Command Interval (different bank)

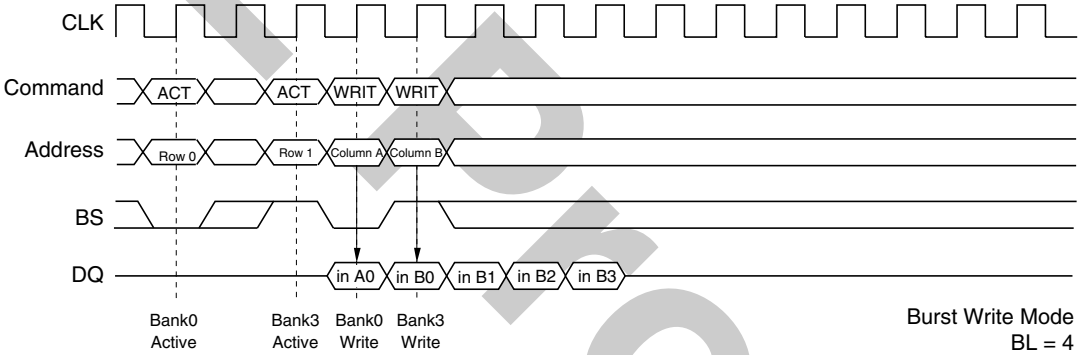
Write command to Write command interval

1. Same bank, same ROW address: When another write command is executed at the same ROW address of the same bank as the preceding write command, the second write can be performed after an interval of no less than 1 clock. In the case of burst writes, the second write command has priority.



WRITE to WRITE Command Interval (same ROW address in same bank)

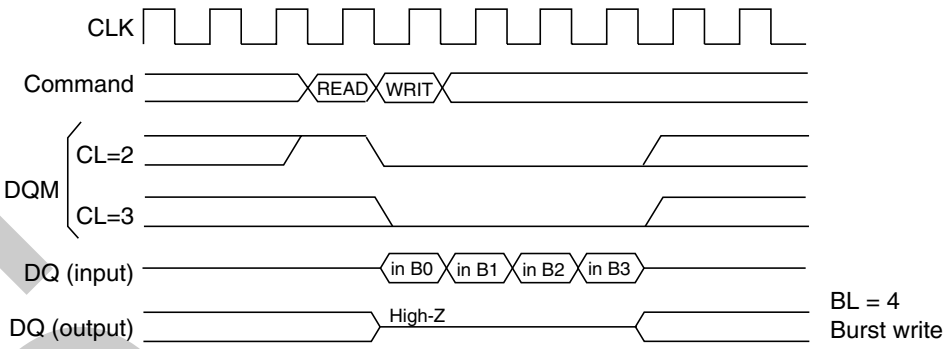
2. Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a precharge command and a bank active command.
3. Different bank: When the bank changes, the second write can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank active state. In the case of burst write, the second write command has priority.



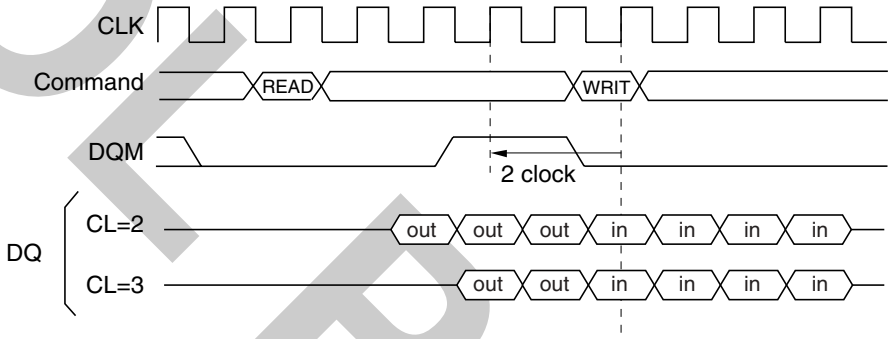
WRITE to WRITE Command Interval (different bank)

Read command to Write command interval

1. Same bank, same ROW address: When the write command is executed at the same ROW address of the same bank as the preceding read command, the write command can be performed after an interval of no less than 1 clock. However, DQM must be set High so that the output buffer becomes High-Z before data input.



READ to WRITE Command Interval (1)

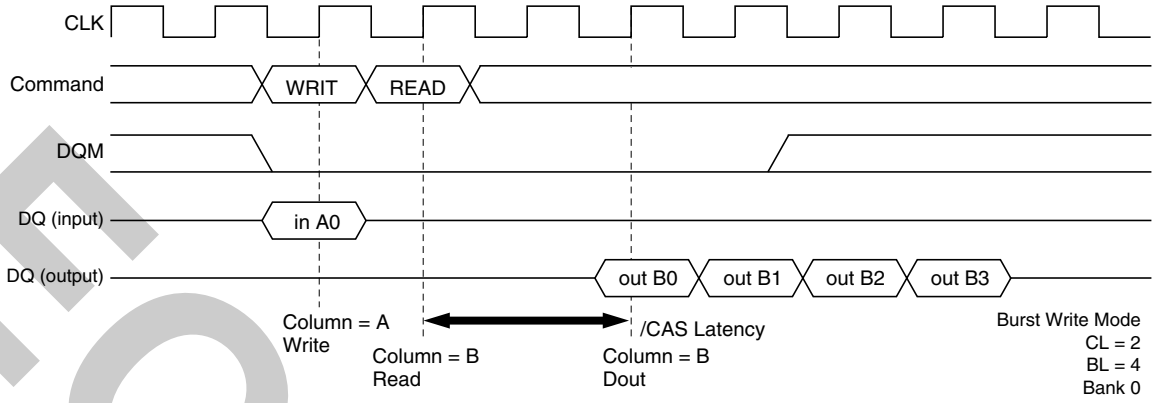


READ to WRITE Command Interval (2)

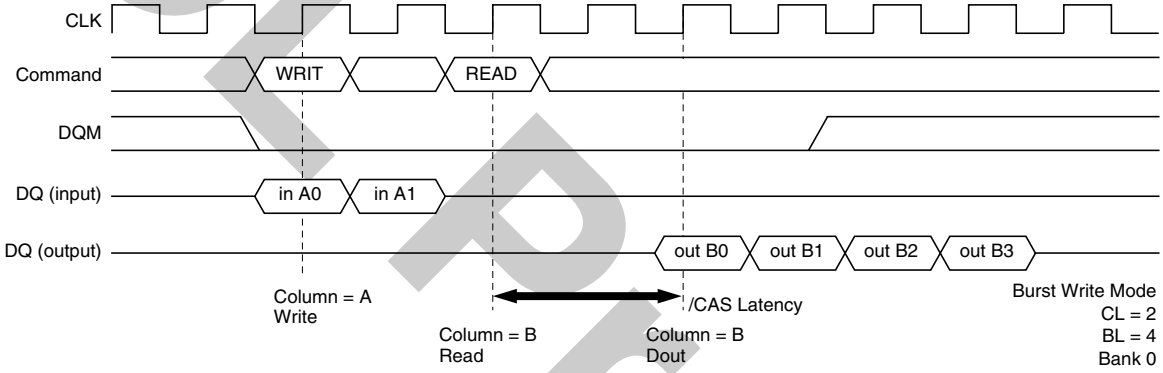
2. Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank active command.
3. Different bank: When the bank changes, the write command can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank active state. However, DQM must be set High so that the output buffer becomes High-Z before data input.

Write command to Read command interval:

1. Same bank, same ROW address: When the read command is executed at the same ROW address of the same bank as the preceding write command, the read command can be performed after an interval of no less than 1 clock. However, in the case of a burst write, data will continue to be written until one clock before the read command is executed.



WRITE to READ Command Interval (1)

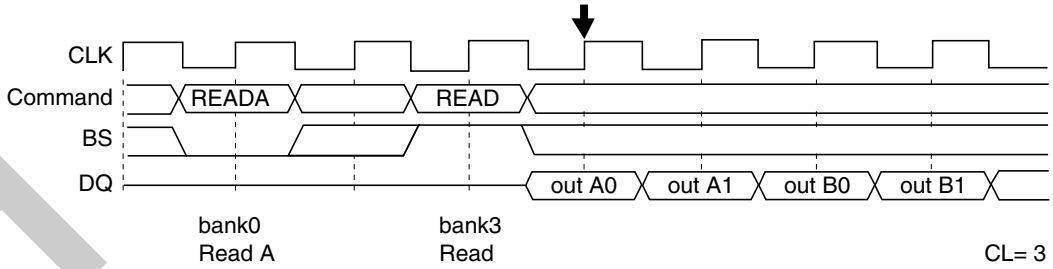


WRITE to READ Command Interval (2)

2. Same bank, different ROW address: When the ROW address changes, consecutive read commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank active command.
3. Different bank: When the bank changes, the read command can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank active state. However, in the case of a burst write, data will continue to be written until one clock before the read command is executed (as in the case of the same bank and the same address).

Read with auto precharge to Read command interval

1. Different bank: When some banks are in the active state, the second read command (another bank) is executed. Even when the first read with auto-precharge is a burst read that is not yet finished, the data read by the second command is valid. The internal auto-precharge of one bank starts at the next clock of the second command.



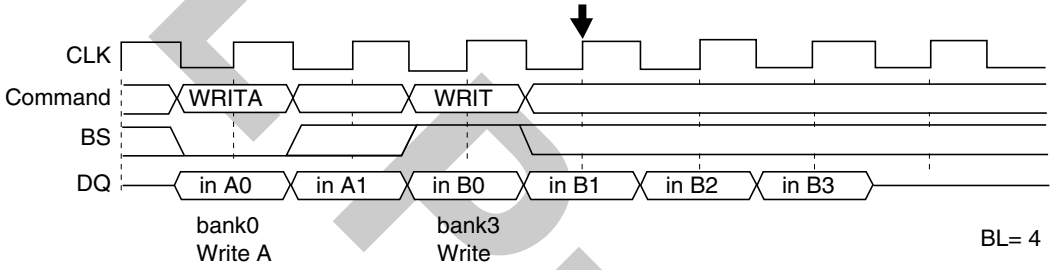
Note: Internal auto-precharge starts at the timing indicated by " ↓ ".

Read with Auto Precharge to Read Command Interval (Different bank)

2. Same bank: The consecutive read command (the same bank) is illegal.

Write with auto precharge to Write command interval

1. Different bank: When some banks are in the active state, the second write command (another bank) is executed. In the case of burst writes, the second write command has priority. The internal auto-precharge of one bank starts 2 clocks later from the second command.



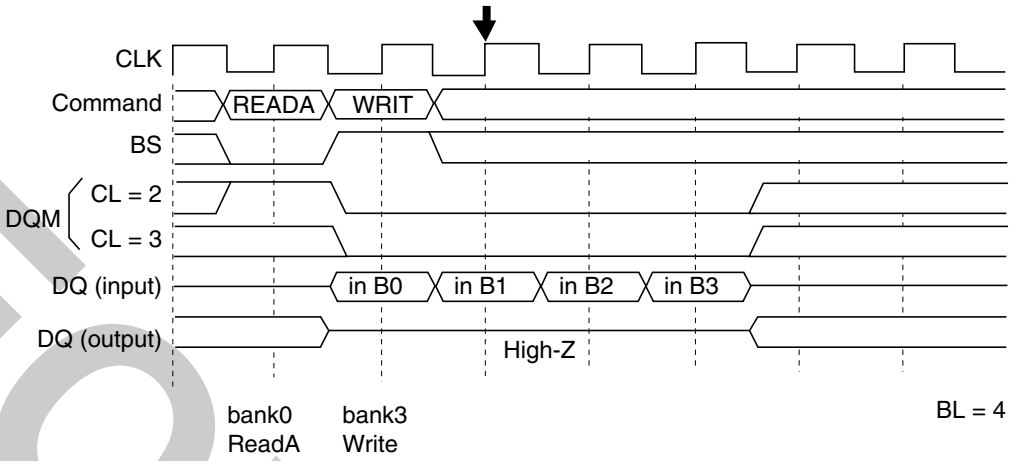
Note: Internal auto-precharge starts at the timing indicated by " ↓ ".

Write with Auto Precharge to Write Command Interval (Different bank)

2. Same bank: The consecutive write command (the same bank) is illegal.

Read with auto precharge to Write command interval

1. Different bank: When some banks are in the active state, the second write command (another bank) is executed. However, DQM must be set High so that the output buffer becomes High-Z before data input. The internal auto-precharge of one bank starts at the next clock of the second command.



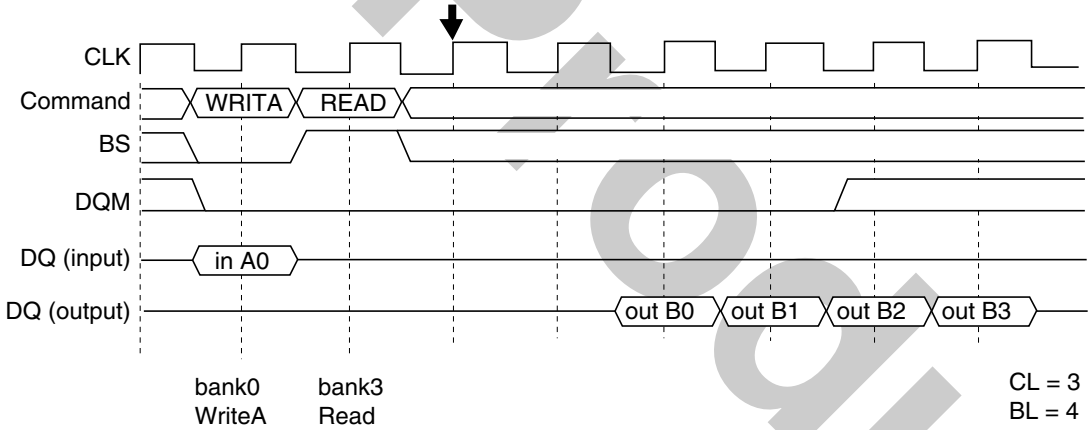
Note: Internal auto-precharge starts at the timing indicated by " ↓ ".

Read with Auto Precharge to Write Command Interval (Different bank)

2. Same bank: The consecutive write command from read with auto precharge (the same bank) is illegal. It is necessary to separate the two commands with a bank active command.

Write with auto precharge to Read command interval

1. Different bank: When some banks are in the active state, the second read command (another bank) is executed. However, in case of a burst write, data will continue to be written until one clock before the read command is executed. The internal auto-precharge of one bank starts at 2 clocks later from the second command.



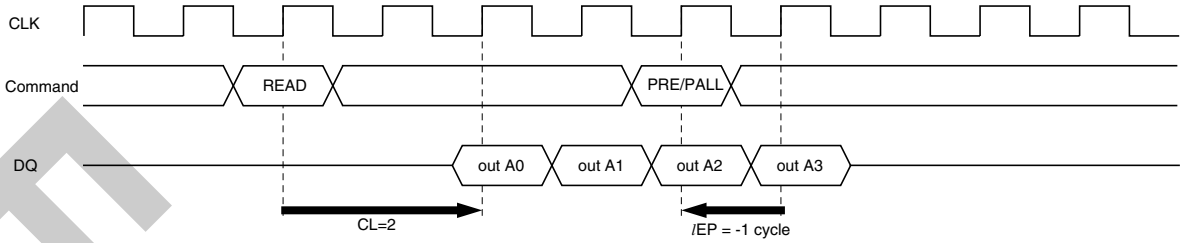
Note: Internal auto-precharge starts at the timing indicated by " ↓ ".

Write with Auto Precharge to Read Command Interval (Different bank)

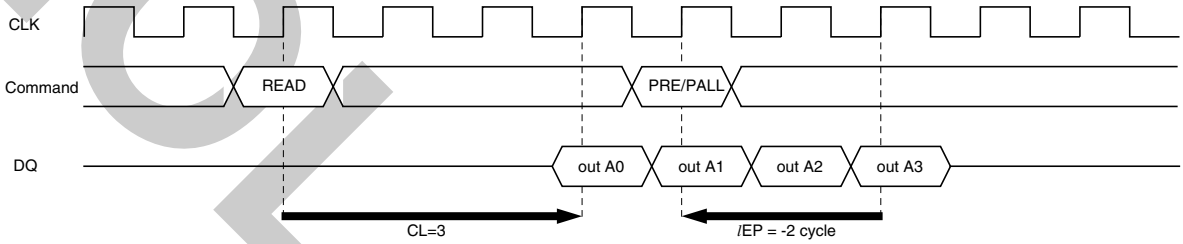
2. Same bank: The consecutive read command from write with auto precharge (the same bank) is illegal. It is necessary to separate the two commands with a bank active command.

Read command to Precharge command interval (same bank)

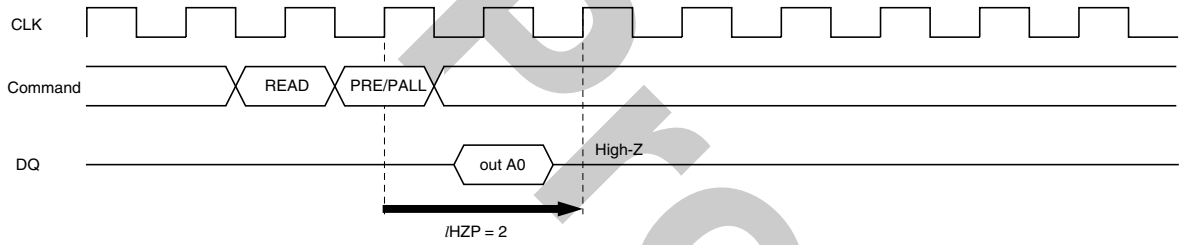
When the precharge command is executed for the same bank as the read command that preceded it, the minimum interval between the two commands is one clock. However, since the output buffer then becomes High-Z after the clocks defined by *l*HZP, there is a case of interruption to burst read data output will be interrupted, if the precharge command is input during burst read. To read all data by burst read, the clocks defined by *l*EP must be assured as an interval from the final data output to precharge command execution.



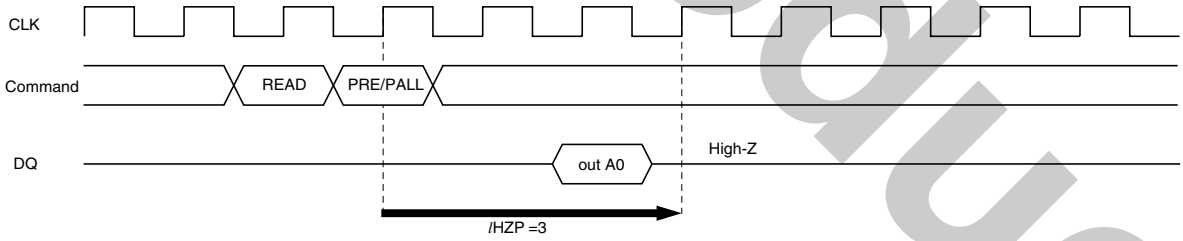
READ to PRECHARGE Command Interval (same bank): To output all data (CL = 2, BL = 4)



READ to PRECHARGE Command Interval (same bank): To output all data (CL = 3, BL = 4)



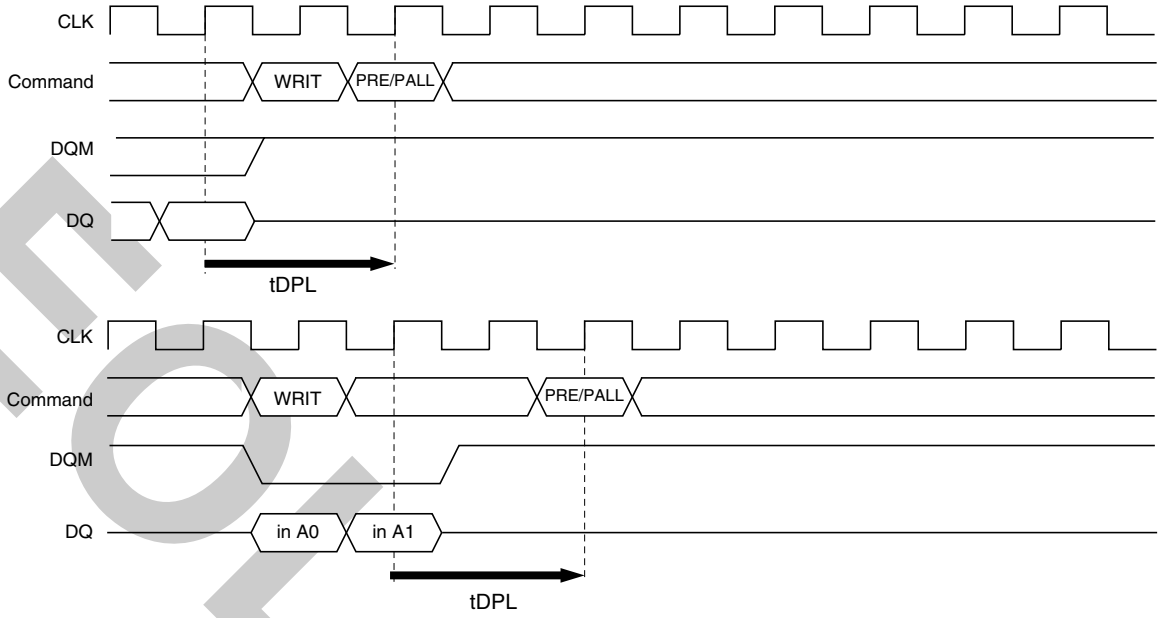
READ to PRECHARGE Command Interval (same bank): To stop output data (CL = 2, BL = 1, 2, 4, 8)



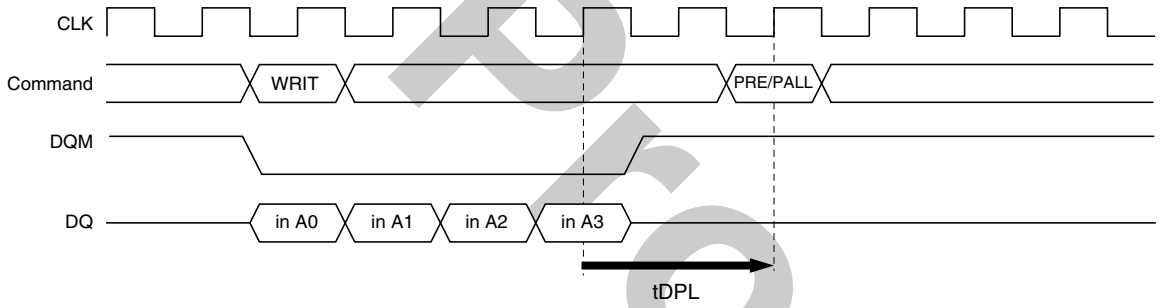
READ to PRECHARGE Command Interval (same bank): To stop output data (CL = 3, BL = 1, 2, 4, 8)

Write command to Precharge command interval (same bank)

When the precharge command is executed for the same bank as the write command that preceded it, the minimum interval between the two commands is 1 clock. However, if the burst write operation is unfinished, the input data must be masked by means of DQM for assurance of the clock defined by tDPL.



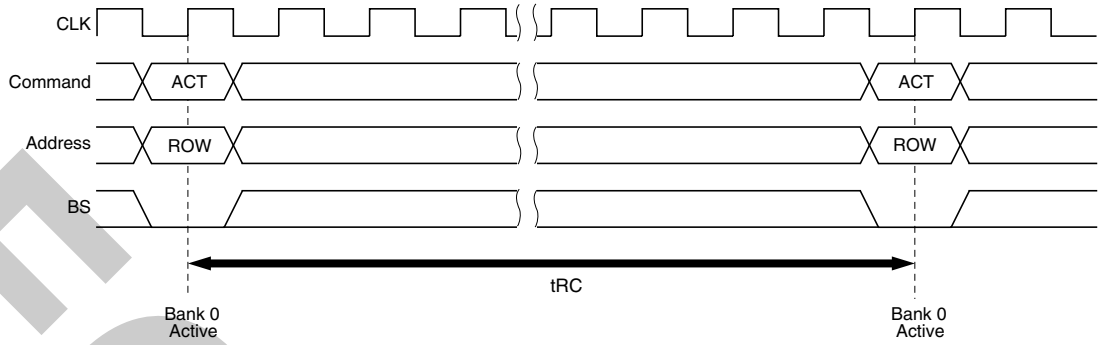
WRITE to PRECHARGE Command Interval (same bank) (BL = 4 (To stop write operation))



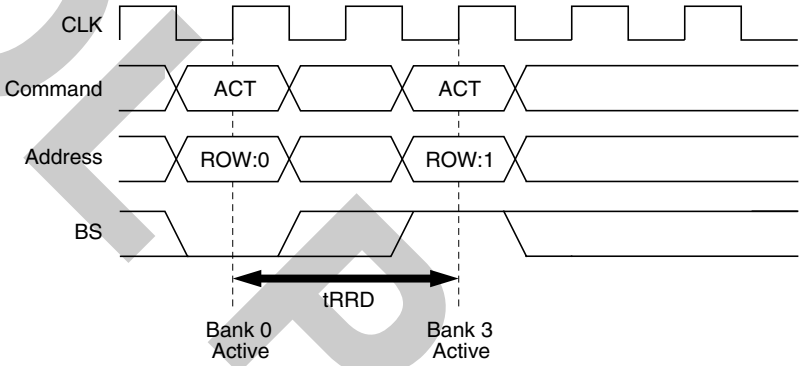
WRITE to PRECHARGE Command Interval (same bank) (BL = 4 (To write all data))

Bank active command interval

1. Same bank: The interval between the two bank active commands must be no less than tRC.
2. In the case of different bank active commands: The interval between the two bank active commands must be no less than tRRD.



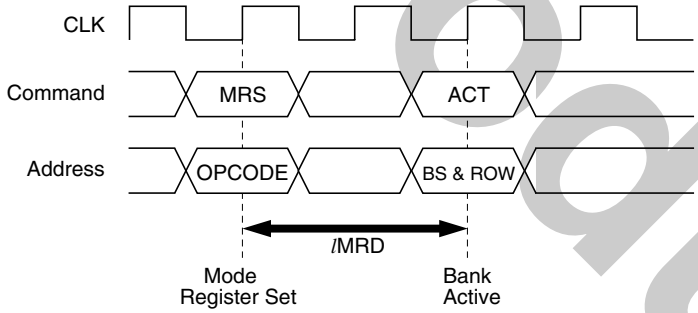
Bank Active to Bank Active for Same Bank



Bank Active to Bank Active for Different Bank

Mode register set to Bank active command interval

The interval between setting the mode register and executing a bank active command must be no less than *t*MRD.



Mode register set to Bank active command interval

DQM Control

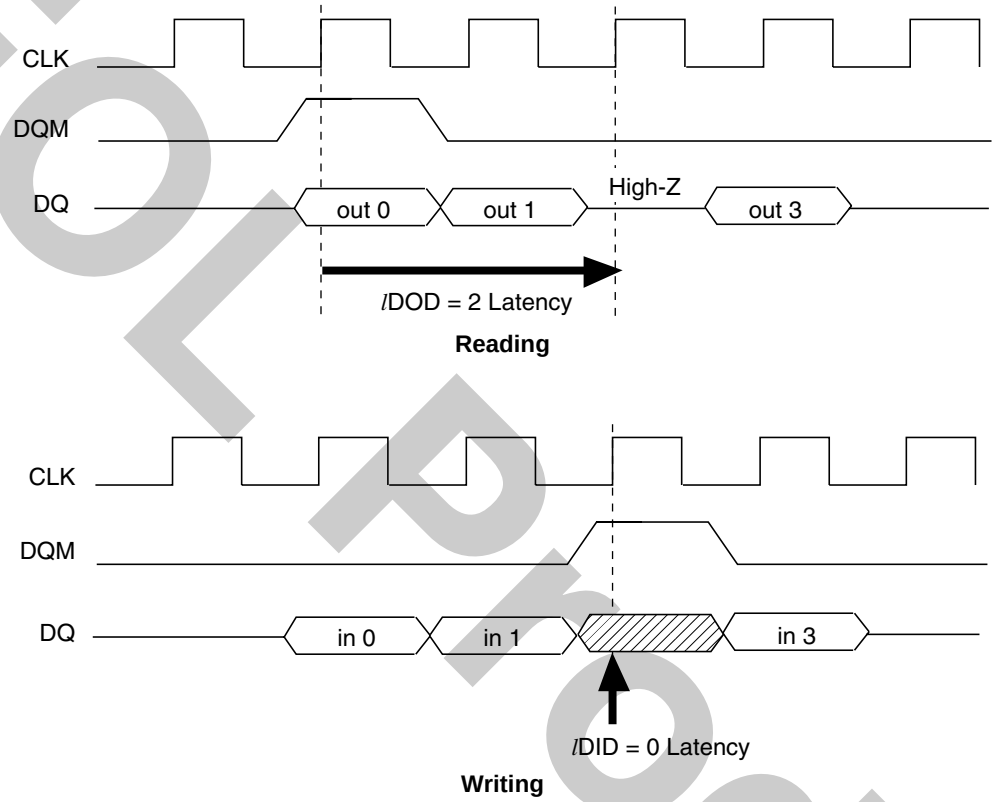
The DQM mask the DQ data. The UDQM and LDQM mask the upper and lower bytes of the DQ data, respectively. The timing of UDQM/LDQM is different during reading and writing.

Reading

When data is read, the output buffer can be controlled by DQM. By setting DQM to Low, the output buffer becomes Low-Z, enabling data output. By setting DQM to High, the output buffer becomes High-Z, and the corresponding data is not output. However, internal reading operations continue. The latency of DQM during reading is 2 clocks.

Writing

Input data can be masked by DQM. By setting DQM to Low, data can be written. In addition, when DQM is set to High, the corresponding data is not written, and the previous data is held. The latency of DQM during writing is 0 clock.



Refresh

Auto-refresh

All the banks must be precharged before executing an auto-refresh command. Since the auto-refresh command updates the internal counter every time it is executed and determines the banks and the ROW addresses to be refreshed, external address specification is not required. The refresh cycles are required to refresh all the ROW addresses within tREF (max.). The output buffer becomes High-Z after auto-refresh start. In addition, since a precharge has been completed by an internal operation after the auto-refresh, an additional precharge operation by the precharge command is not required.

Self-refresh

After executing a self-refresh command, the self-refresh operation continues while CKE is held Low. During self-refresh operation, all ROW addresses are refreshed by the internal refresh timer. A self-refresh is terminated by a self-refresh exit command. Before and after self-refresh mode, execute auto-refresh to all refresh addresses in or within tREF (max.) period on the condition 1 and 2 below.

1. Enter self-refresh mode within time as below* after either burst refresh or distributed refresh at equal interval to all refresh addresses are completed.
2. Start burst refresh or distributed refresh at equal interval to all refresh addresses within time as below*after exiting from self-refresh mode.

Note: tREF (max.) / refresh cycles.

Others

Power-down mode

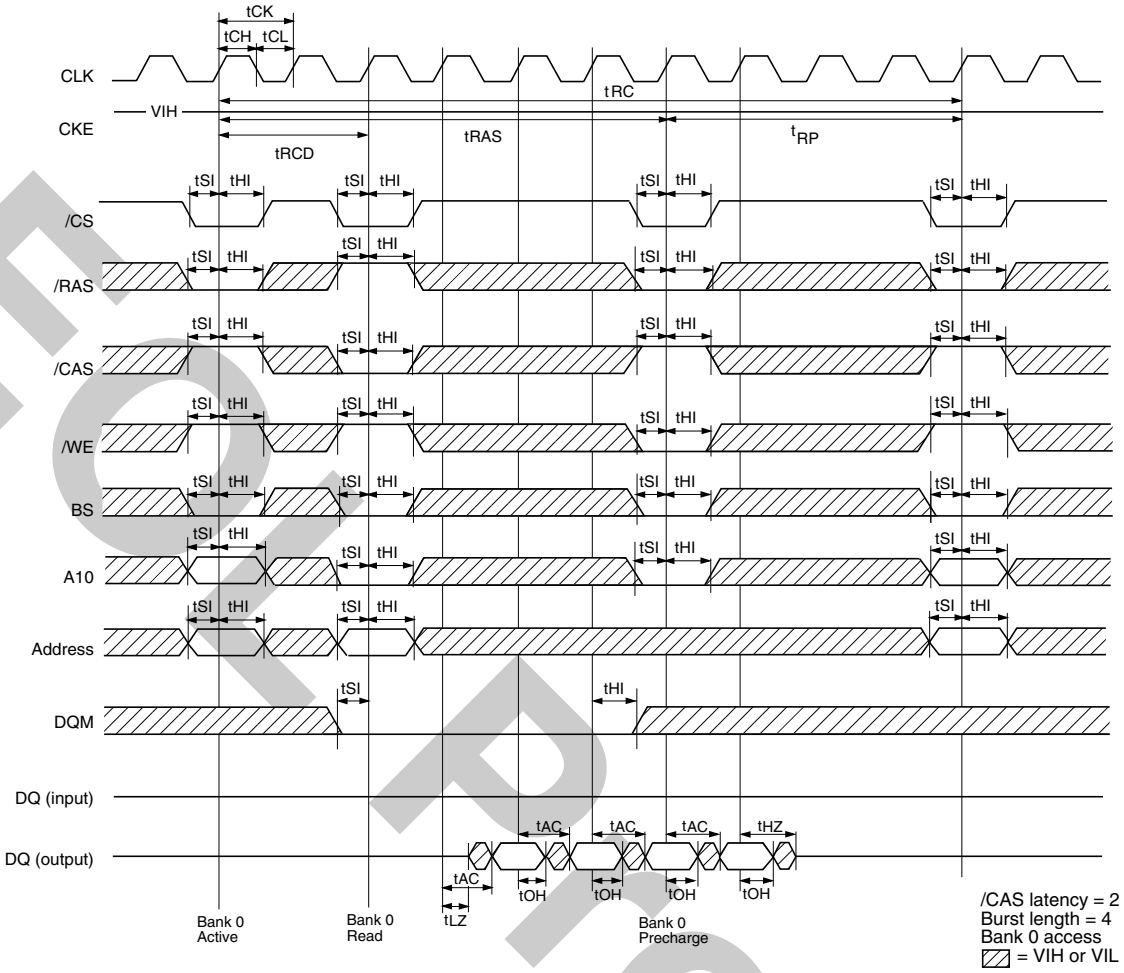
The SDRAM enters power-down mode when CKE goes Low in the IDLE state. In power down mode, power consumption is suppressed by deactivating the input initial circuit. Power down mode continues while CKE is held Low. In addition, by setting CKE to High, the SDRAM exits from the power down mode, and command input is enabled from the next clock. In this mode, internal refresh is not performed.

Clock suspend mode

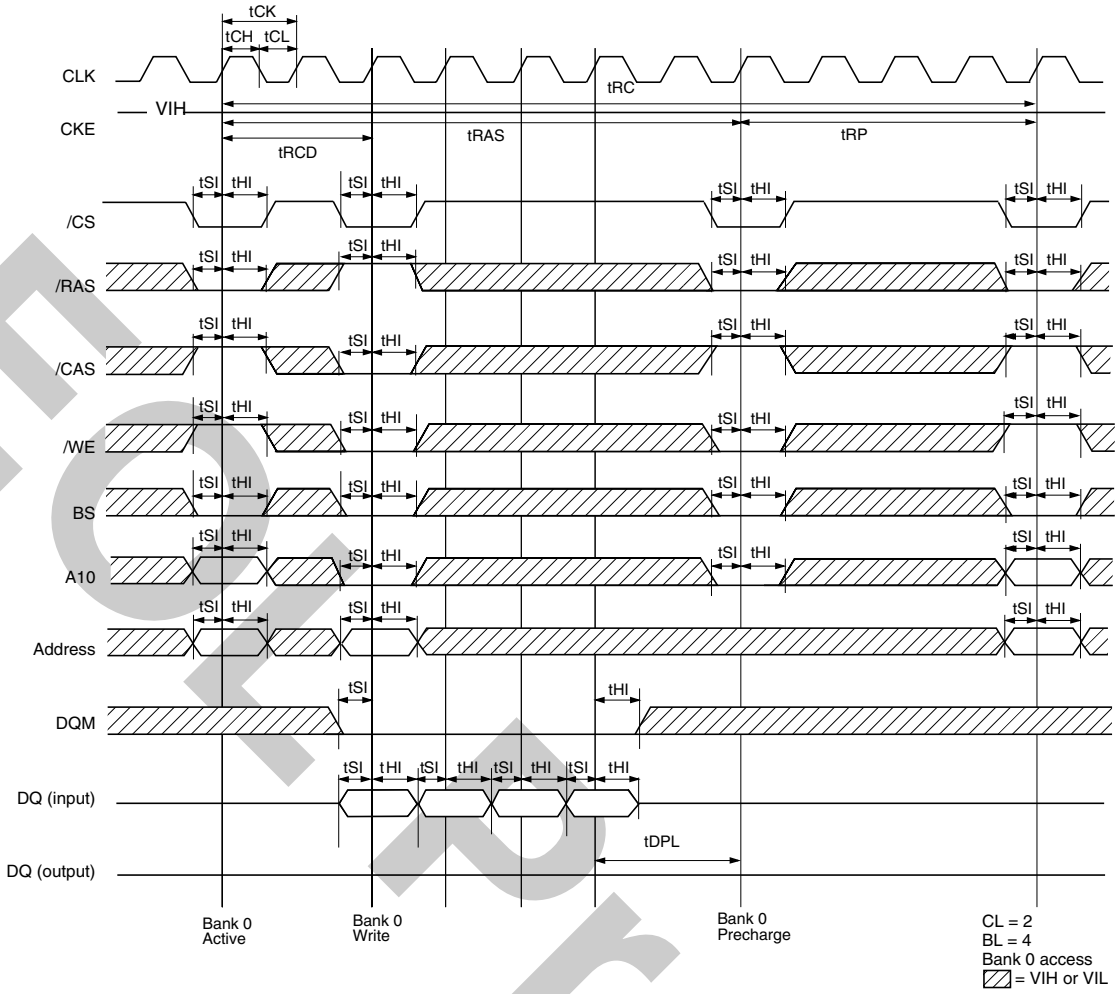
By driving CKE to Low during a bank active or read/write operation, the SDRAM enters clock suspend mode. During clock suspend mode, external input signals are ignored and the internal state is maintained. When CKE is driven High, the SDRAM terminates clock suspend mode, and command input is enabled from the next clock. For details, refer to the "CKE Truth Table".

Timing Waveforms

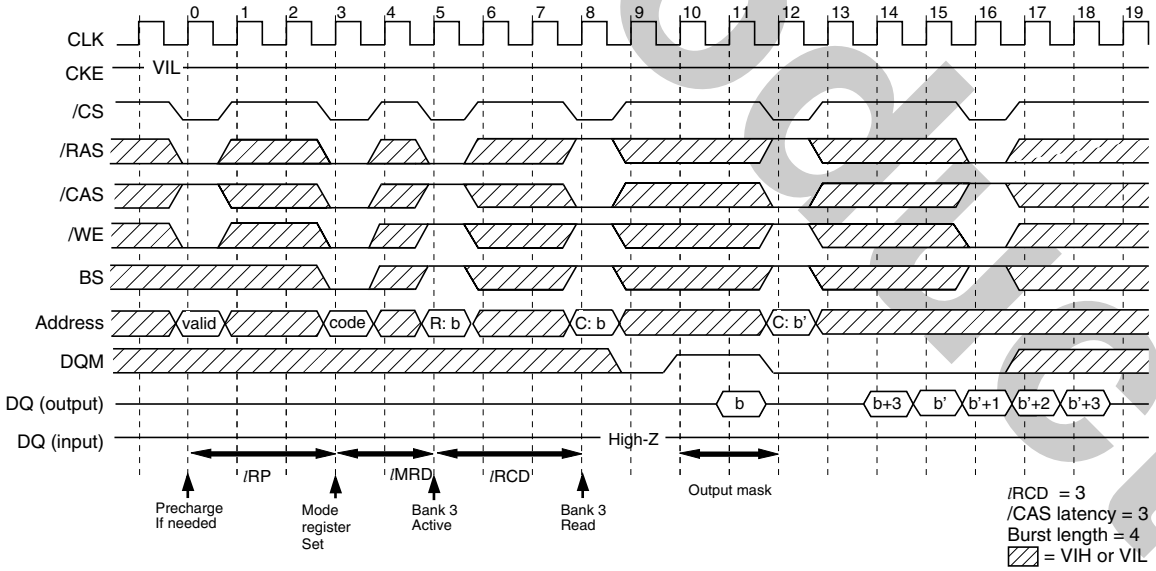
Read Cycle



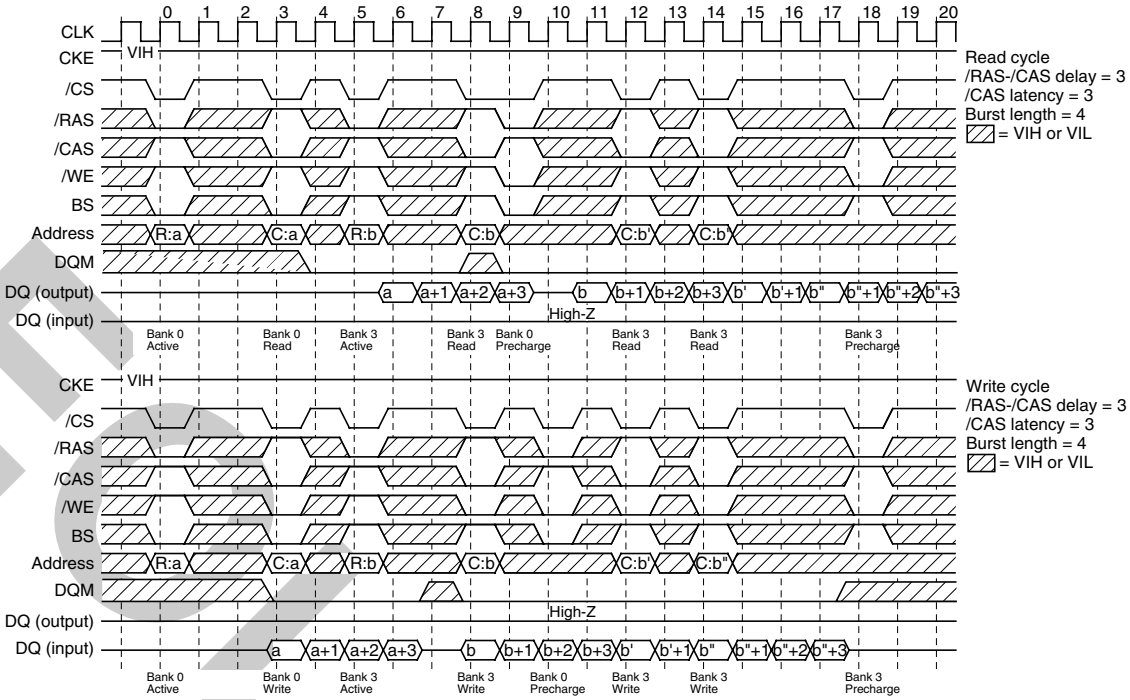
Write Cycle



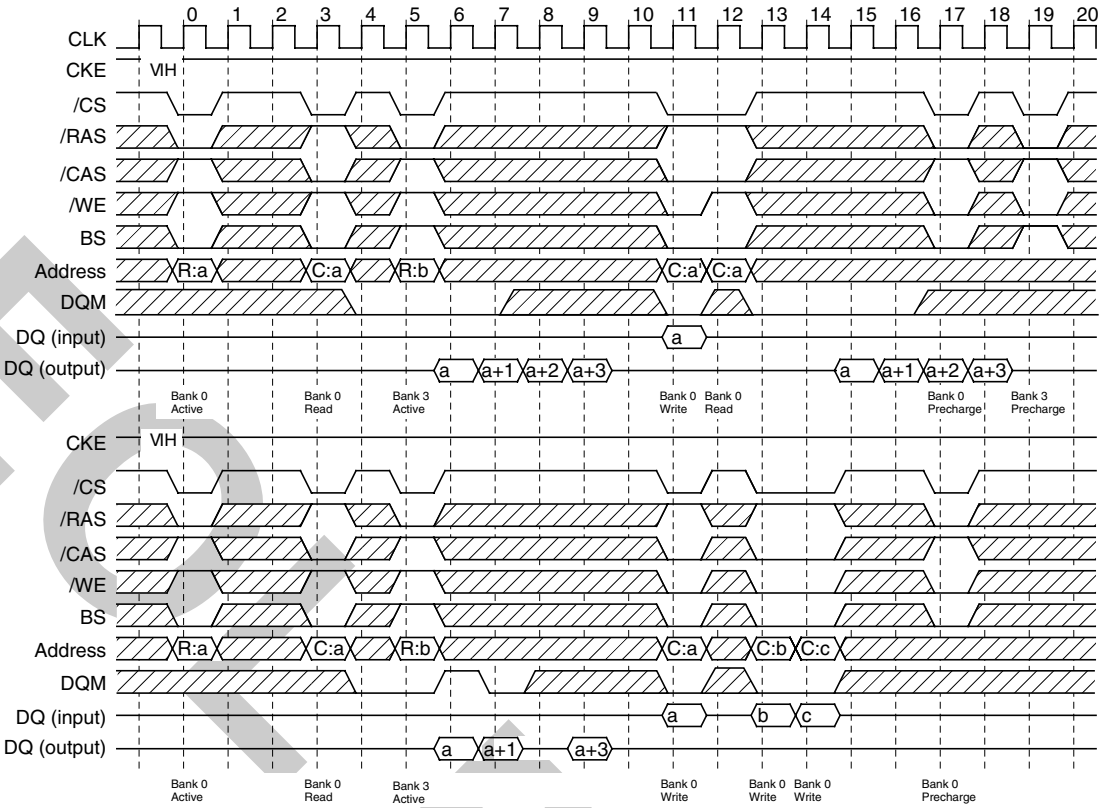
Mode Register Set Cycle



Read Cycle/Write Cycle

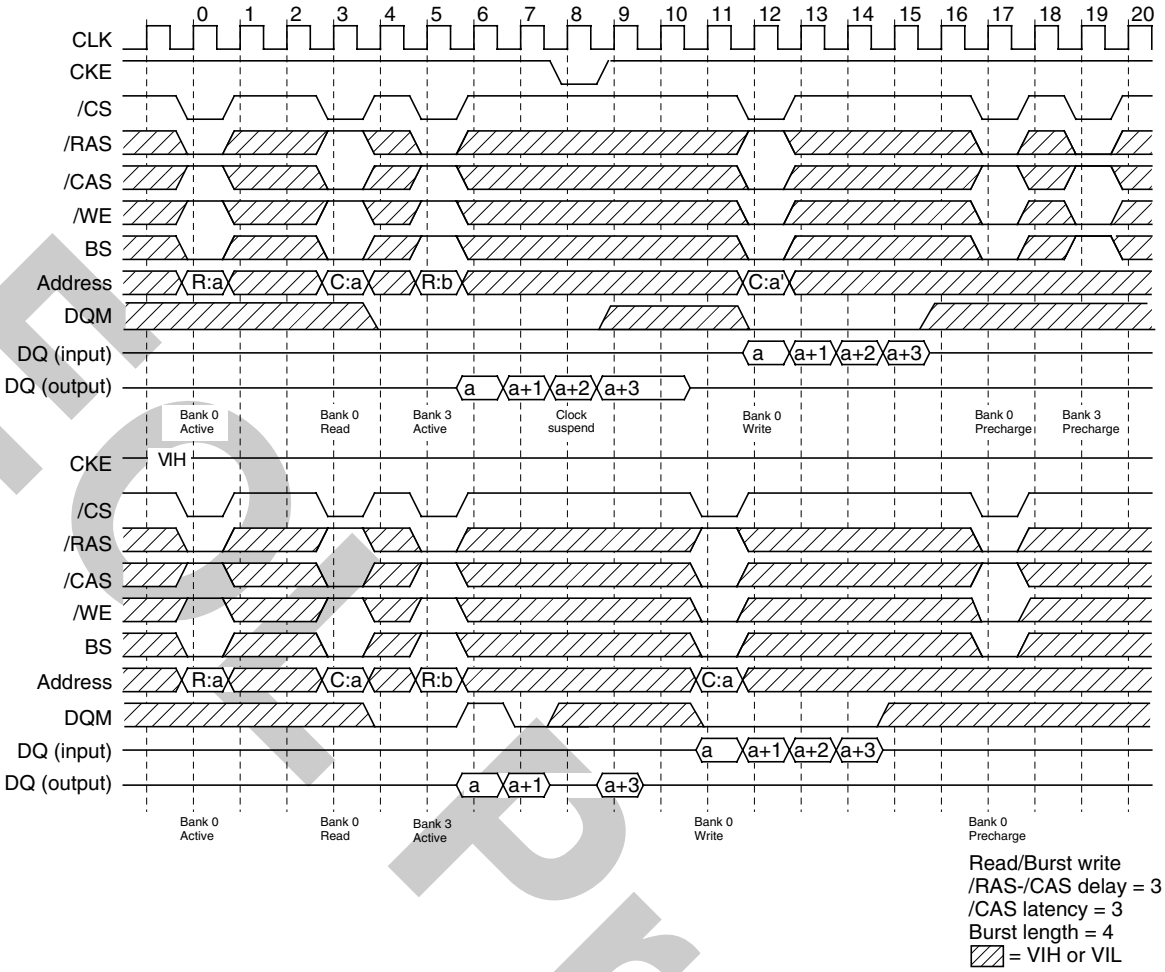


Read/Single Write Cycle

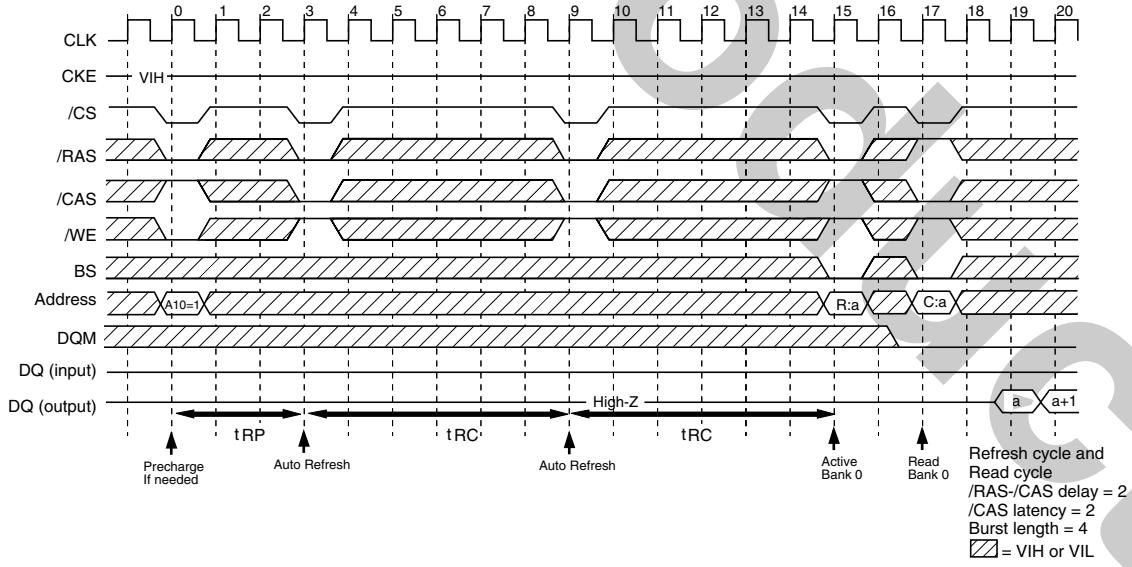


Read/Single write
/RAS-/CAS delay = 3
/CAS latency = 3
Burst length = 4
▨ = VIH or VIL

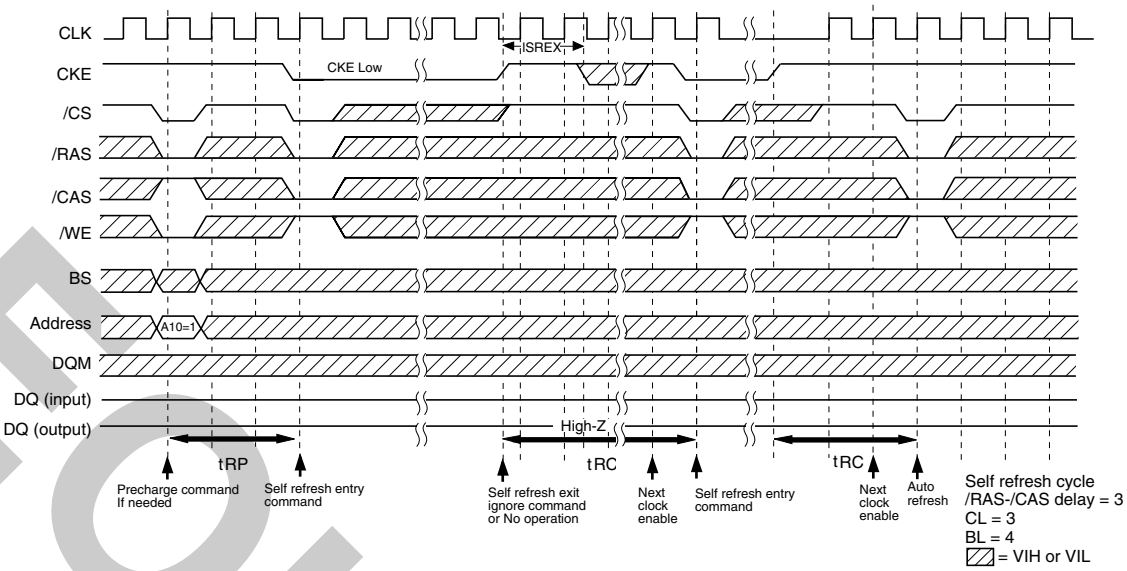
Read/Burst Write Cycle



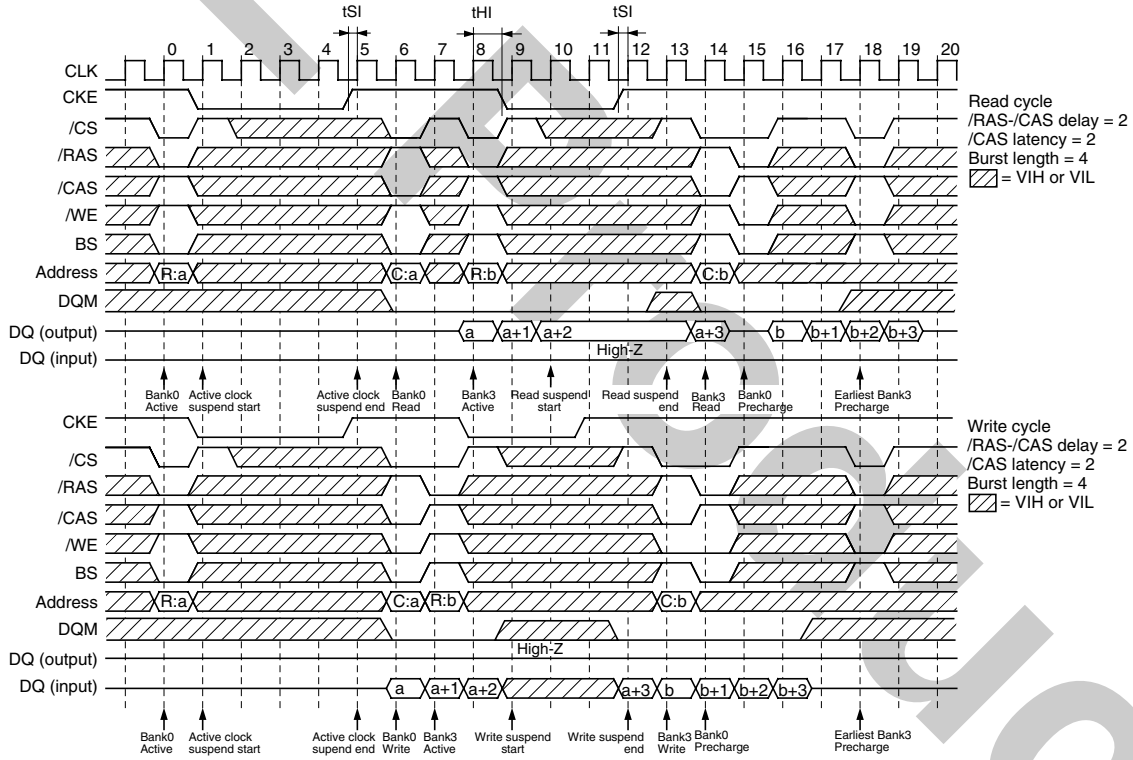
Auto Refresh Cycle



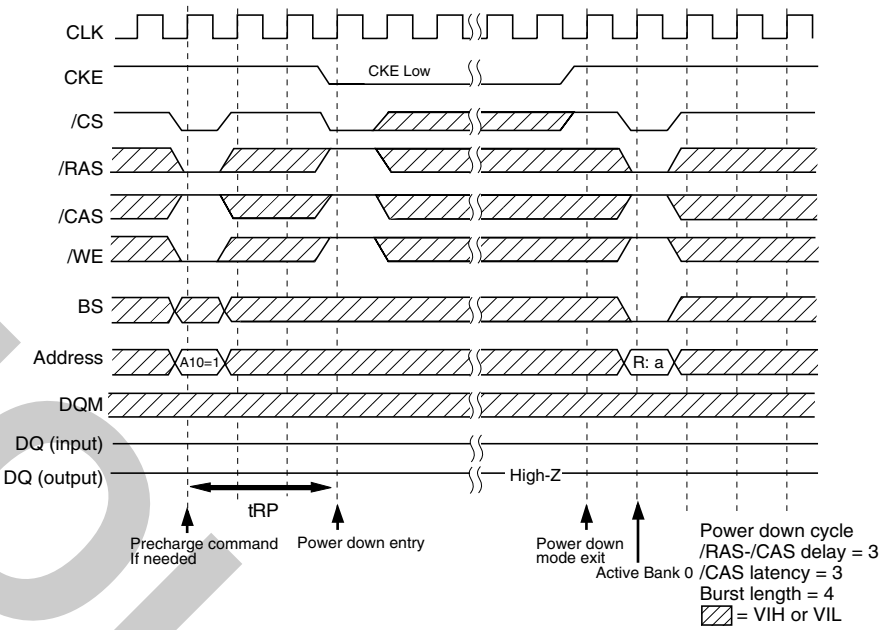
Self Refresh Cycle



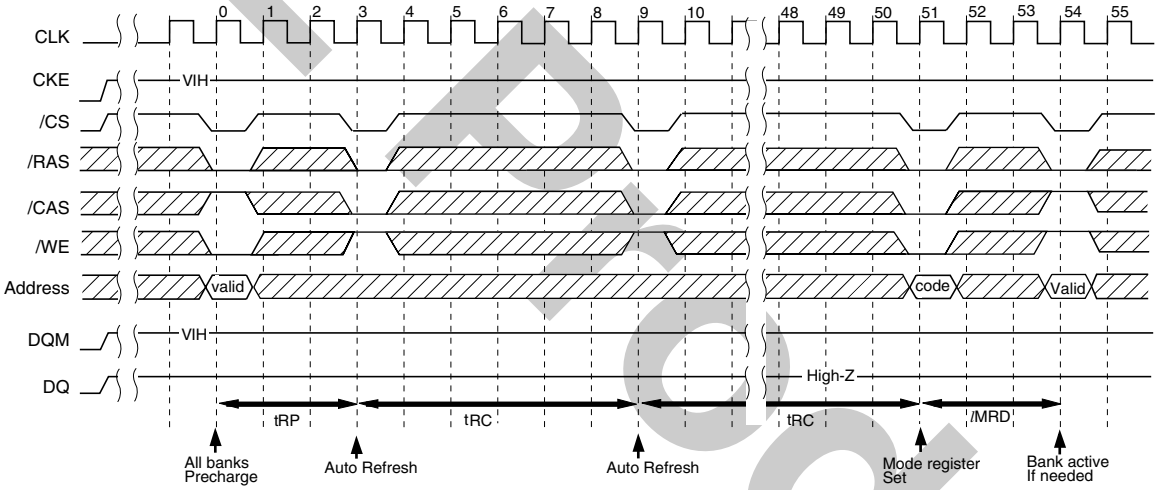
Clock Suspend Mode



Power Down Mode



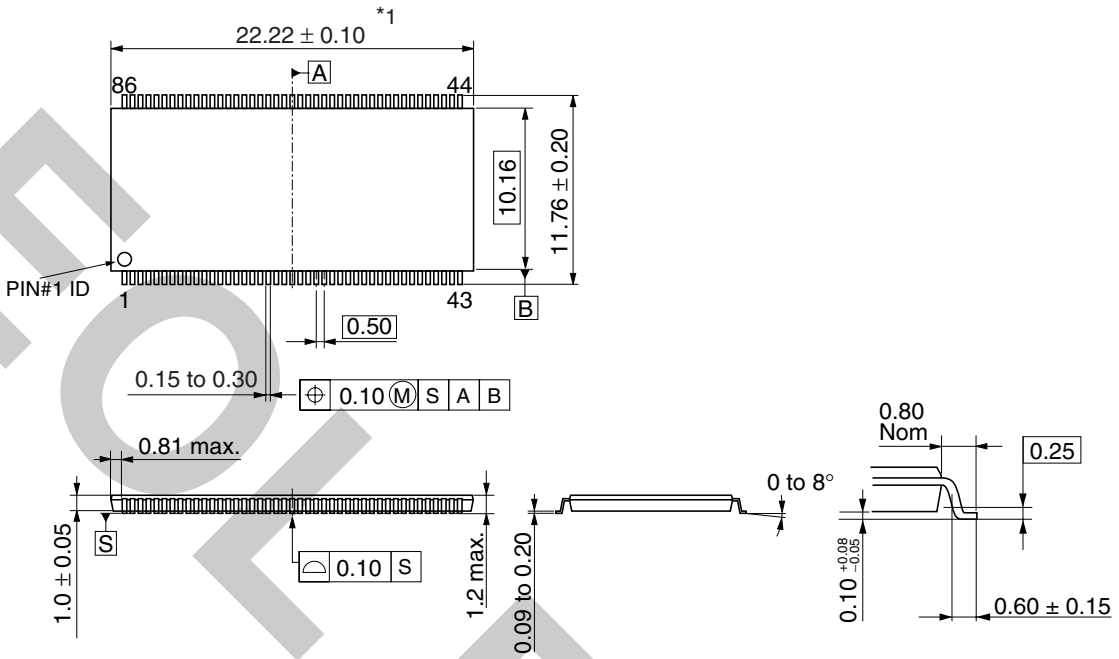
Initialization Sequence



Package Drawing

86-pin Plastic TSOP (II)

Unit: mm



Note: 1. This dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.20mm per side.

ECA-TS2-0030-01

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the EDS1232CA.

Type of Surface Mount Device
EDS1232CATA: 86-pin Plastic TSOP (II)

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107