Fully Integrated Switch-Mode One-Cell Li-Ion Charger with Full USB Compliance and USB-OTG Support

FEATURES

- Charge Faster than Linear Chargers
- High-Accuracy Voltage and Current Regulation
  - Input Current Regulation Accuracy: ±5% (100 mA and 500 mA)
  - Charge Voltage Regulation Accuracy: ±0.5% (25°C), ±1% (0°C-125°C)
  - Charge Current Regulation Accuracy: ±5%
- High-Efficiency Mini-USB/AC Battery Charger for Single-Cell Li-Ion and Li-Polymer Battery Packs
- 20-V Absolute Maximum Input Voltage Rating
- 6-V Maximum Operating Input Voltage
- Built-In Input Current Sensing and Limiting
- Integrated Power FETs for Up To 1.25-A Charge Rate
- Programmable Charge Parameters through I²C™ Interface (up to 3.4 Mbps):
  - Input Current
  - Fast-Charge/Termination Current
  - Charge Voltage (3.5 V to 4.44 V)
  - Safety Timer
  - Termination Enable
- Synchronous Fixed-Frequency PWM Controller Operating at 3 MHz with 0% to 99.5% Duty Cycle
- Automatic High Impedance Mode for Low Power Consumption
- Safety Timer with Reset Control
- Reverse Leakage Protection Prevents Battery Drainage
- Thermal Regulation and Protection
- Input/Output Overvoltage Protection
- Status Output for Charging and Faults
- USB Friendly Boot-Up Sequence
- Automatic Charging
- Power up System without Battery
- Boost Mode Operation for USB OTG:
  - Input Voltage Range (from Battery): 2.5 V to 4.5 V
  - Output Voltage for VBUS: 5.05 V
- 1.976 x 1.924mm 20-Pin WCSP Package

APPLICATIONS

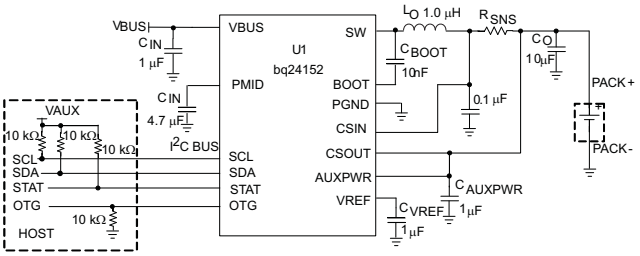
- Mobile and Smart Phones
- MP3 Players
- Handheld Devices

DESCRIPTION

The bq24152 is a compact, flexible, high-efficiency, USB-friendly switch-mode charge management device for single-cell Li-ion and Li-polymer batteries used in a wide range of portable applications. The charge parameters can be programmed through an I²C interface. The bq24152 integrates a synchronous PWM controller, power MOSFETs, input current sensing, high-accuracy current and voltage regulation, and charge termination, into a small WCSP package.

The bq24152 charges the battery in three phases: conditioning, constant current and constant voltage. The input current is automatically limited to the value set by the host. Charge is terminated based on user-selectable minimum current level. A safety timer with reset control provides a safety backup for I²C interface. During normal operation, bq24152 automatically restarts the charge cycle if the battery voltage falls below an internal threshold and automatically enters sleep mode or high impedance mode when the input supply is removed. The charge status is reported to the host using the I²C interface.

Typical Application Circuit



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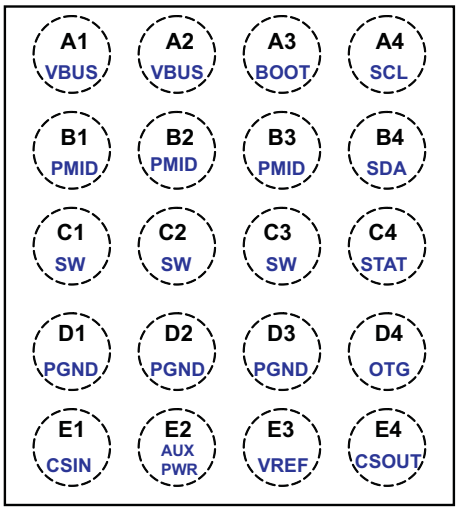
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION CONTINUED

During the charging process, the bq24152 monitors its junction temperature (T_J) and reduces the charge current once T_J increases to approximately 125°C. To support USB OTG device, bq24152 provides VBUS (approximately 5.05V) by boosting the battery voltage. The bq24152 is available in 20-pin WCSP package.

WCSP PACKAGE
(Top View)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
CSOUT	E4	I	Battery voltage and current sense input. Bypass it with a ceramic capacitor (minimum 0.1 µF) to PGND if there are long inductive leads to battery.
VBUS	A1, A2	I	Charger input voltage. Bypass it with a 1-µF ceramic capacitor from VBUS to PGND.
PMID	B1, B2, B3	O	Connection point between reverse blocking MOSFET and high-side switching MOSFET. Bypass it with a minimum of 3.3-µF capacitor from PMID to PGND.
SW	C1, C2, C3	O	Internal switch to output inductor connection.
BOOT	A3	O	Boot-strapped capacitor for the high-side MOSFET gate driver. Connect a 10-nF ceramic capacitor (voltage rating above 10 V) from BOOT pin to SW pin.
PGND	D1, D2, D3		Power ground
CSIN	E1	I	Charge current-sense input. Battery current is sensed via the voltage drop across an external sense resistor. A 0.1-µF ceramic capacitor to PGND is required.
SCL	A4	I	I^2C interface clock. Open drain output, connect a 10-kΩ pullup resistor
SDA	B4	I/O	I^2C interface data. Open drain output, connect a 10-kΩ pullup resistor
STAT	C4	O	Charge status pin. Pull low when charge in progress. Open drain for other conditions. During faults, a 128µS pulse is sent out. STAT pin can be disabled by the EN_STAT bit in control register. STAT can be used to drive a LED or communicate with a host processor.
VREF	E3	O	Internal bias regulator voltage. Connect a 1-µF ceramic capacitor from this output to PGND. External load on VREF is not allowed.
AUXPWR	E2	I	Auxiliary power supply, connected to the battery pack to provide power in high-impedance mode. Bypass it with a 1-µF ceramic capacitor from this pin to PGND.
OTG	D4	I	Boost mode enable control or input current limiting selection pin. When OTG is in active status, bq24152 is forced to operate in boost mode. It has higher priority over I^2C control and can be disabled through control register. The logic voltage level at OTG active status can also be controlled. At POR, the OTG pin is default to be used as the input current limiting selection pin. When OTG = High, Iin – limit = 500 mA and when OTG = Low, Iin – limit = 100 mA, see the Control Register for details.

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ORDERING INFORMATION(1)

Part NO.	MARKING	MEDIUM	QUANTITY
bq24152YFFR	bq24152	Tape and Reel	3000
bq24152YFFT	bq24152	Tape and Reel	250

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

DISSIPATION RATINGS(1)

PACKAGE	$R_{\theta JA}$	$R_{\theta JC}$	$T_A \le 25°C$ POWER RATING	DERATING FACTOR $T_A > 25°C$
WSCP-20 (1)	185°C/W(2)	1.57°C/W	0.54 W	0.0054 W/°C

(1) Maximum power dissipation is a function of $T_J(max)$, $R\theta_{JA}$ and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = [T_J(max)-T_A] / R\theta_{JA}$.
(2) For PCB board with only top trace layer. For PCB board with four layers (top trace layer, buried ground layer, buried signal layer and bottom layer), $R\theta_{JA}$ drops to 75.96°C/W

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
V_{SS}	Supply voltage range (with respect to PGND)	VBUS	–0.3 to 20	V
V_I	Input voltage range (with respect to and PGND)	SCL, SDA, OTG, CSIN, CSOUT, AUXPWR	–0.3 to 7	V
V_O	Output voltage range (with respect to and PGND)	PMID, STAT	–0.3 to 20	V
		VREF	6.5	V
		SW, BOOT	–0.7 to 20	V
	Voltage difference between CSIN and CSOUT inputs ($V_{(CSIN)}$ -$V_{(CSOUT)}$)		±7	V
	Output sink	STAT	10	mA
I_O	Output current (average)	SW	1.25	A
T_A	Operating free-air temperature range		–40 to 85	°C
T_J	Junction temperature		–40 to 150	°C
T_{stg}	Storage temperature		–65 to 150	°C
ESD Rating	Human body model at VBUS, PMID, STAT(2)(3)		800	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.
(2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
(3) Other pins pass 2 kV for human body model.
All voltages are with respect to PGND if not specified. Currents are positive into, negative out of the specified terminal.

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RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{BUS}	Supply voltage, VBUS	4		6 (1)	V
T_J	Operating junction temperature range	0		+125	°C

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the BOOT or SW pins. A tight layout minimizes switching noise.

ELECTRICAL CHARACTERISTICS

Circuit of Figure 1, VBUS = 5 V, HZ_MODE = 0, OPA_MODE = 0 (charger mode operation), T_J = 0°C to 125°C, T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENTS						
$I_{(VBUS)}$	VBUS supply current control	VBUS > VBUS(min), PWM switching		10		mA
		VBUS > VBUS(min), PWM NOT switching			5	
		0°C < T_J < 85°C, VBUS = 5 V, HZ_MODE = 1, $V_{(AUXPWR)}$ > $V_{(LOWV)}$, SCL, SDA, OTG = 0 V or 1.8 V			20	µA
		0°C < T_J < 85°C, VBUS = 5 V, HZ_MODE = 1, $V_{(AUXPWR)}$ < $V_{(LOWV)}$, 32 S mode, SCL, SDA, OTG = 0 V or 1.8 V			35	µA
I_{lkg}	Leakage current from battery to VBUS pin	0°C < T_J < 85°C, $V_{(AUXPWR)}$ = 4.2 V, High impedance mode			5	µA
	Battery discharge current in High Impedance mode, (CSIN, CSOUT, AUXPWR, SW pins)	0°C < T_J < 85°C, $V_{(AUXPWR)}$ = 4.2 V, High impedance mode SCL, SDA, OTG = 0 V or 1.8 V			20	µA
VOLTAGE REGULATION						
$V_{(OREG)}$	Output charge voltage	Operating in voltage regulation, programmable	3.5		4.44	V
	Voltage regulation accuracy	T_A = 25°C	–0.5%		0.5%	
				±1%		
CURRENT REGULATION (FAST CHARGE)						
$I_{O(CHARGE)}$	Output charge current	$V_{(LOWV)}$ ≤ $V_{(AUXPWR)}$ < $V_{(OREG)}$, VBUS > $V_{(SLP)}$, $R_{(SNS)}$ = 68 mΩ Programmable	550		1250	mA
	Regulation accuracy for charge current across $R_{(SNS)}$ $V_{(IREG)}$ = $I_{O(CHARGE)}$ × $R_{(SNS)}$	20 mV ≤ $V_{(IREG)}$ ≤ 40 mV	–5%		5%	
		40 mV < $V_{(IREG)}$	–3%		3%	
WEAK BATTERY DETECTION						
$V_{(LOWV)}$	Weak battery voltage threshold	Programmable	3.4		3.7	V
	Weak battery voltage accuracy		–5%		5%	
	Hysteresis for $V_{(LOWV)}$	Battery voltage falling		100		mV
	Deglitch time for weak battery threshold	Rising voltage, 2 mV overdrive, t_{RISE} = 100 ns		30		ms
OTG PIN LOGIC LEVEL						
V_{IL}	Input low threshold level				0.4	V
V_{IH}	Input high threshold level		1.3			V
CHARGE TERMINATION DETECTION						
$I_{(TERM)}$	Termination charge current	$V_{(AUXPWR)}$ > $V_{(OREG)}$ – $V_{(RCH)}$, VBUS > $V_{(SLP)}$, $R_{(SNS)}$ = 68 mΩ Programmable	50		400	mA
	Deglitch time for charge termination	Both rising and falling, 2 mV overdrive, t_{RISE}, t_{FALL} = 100 ns		30		ms
	Voltage regulation accuracy for termination current across $R_{(SNS)}$ $V_{(IREG_TERM)}$ = $I_{O(TERM)}$ × $R_{(SNS)}$	3 mV ≤ $V_{(IREG_TERM)}$ < 20 mV	–25%		25%	
		20 mV ≤ $V_{(IREG_TERM)}$ ≤ 40 mV	–5%		5%	
INPUT POWER SOURCE DETECTION						
V_{IN}(min)	Input voltage lower limit	Input power source detection	3.6	3.8	4	V
	Deglitch time for VBUS rising above V_{IN}(min)	Rising voltage, 2 mV overdrive, t_{RISE} = 100 ns		30		ms
	Hysteresis for V_{IN}(min)	Input voltage rising	100		200	mV
t_{INT}	Detection Interval	Input power source detection		2		S

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ELECTRICAL CHARACTERISTICS (continued)

Circuit of Figure 1, VBUS = 5 V, HZ_MODE = 0, OPA_MODE = 0 (charger mode operation), T_J = 0°C to 125°C, T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CURRENT LIMITING							
I_{IN}	Input current limiting threshold	USB charge mode	I_{IN} = 100 mA	88	93	98	mA
			I_{IN} = 500 mA	450	475	500	
VREF BIAS REGULATOR							
V_{ref}	Internal bias regulator voltage	VBUS >V_{IN}(min) or $V_{(AUXPWR)}$ > $V_{(BAT)}$min, I(VREF) = 1 mA, C(VREF) = 1 µF		2		6.5	V
	V_{ref} output short current limit				30		mA
	Voltage from BOOT pin to SW pin	During charge or boost operation				6.5	V
BATTERY RECHARGE THRESHOLD							
$V_{(RCH)}$	Recharge threshold voltage	Below $V_{(OREG)}$		100	120	150	mV
	Deglitch time	$V_{(AUXPWR)}$ decreasing below threshold, t_{FALL} = 100ns, 10 mV overdrive			130		ms
STAT OUTPUTS							
$V_{OL(STAT)}$	Low-level output saturation voltage, STAT	I_O = 10 mA, sink current				0.4	V
	High-level leakage current for STAT	Voltage on STAT pin is 5 V				1	µA
I²C BUS LOGIC LEVELS AND TIMING CHARACTERISTICS							
V_{OL}	Output low threshold level	I_O = 10 mA, sink current				0.4	V
V_{IL}	Input low threshold level					0.4	V
V_{IH}	Input high threshold level			1.2			V
$I_{(BIAS)}$	Input bias current	$V_{(pull-up)}$ = 1.8 V, SDA and SCL				1	µA
$f_{(SCL)}$	SCL clock frequency					3.4	MHz
BATTERY DETECTION							
$I_{(DETECT)}$	Battery detection current before charge done (sink current) (1)	Begins after termination detected, $V_{(AUXPWR)}$ ≤ $V_{(OREG)}$			–0.45		mA
	Battery detection time				262		ms
SLEEP COMPARATOR							
$V_{(SLP)}$	Sleep-mode entry threshold, V_{BUS} - V_{AUXPWR}	2.3 V ≤ $V_{(AUXPWR)}$ ≤ $V_{(OREG)}$, V_{BUS} falling		+0.0	+0.04	+0.1	V
$V_{(SLP_EXIT)}$	Sleep-mode exit hysteresis	2.3 V ≤ $V_{(AUXPWR)}$ ≤ $V_{(OREG)}$		40	100	160	mV
	Deglitch time for VBUS rising above $V_{(SLP)}$ + $V_{(SLP_EXIT)}$	Rising voltage, 2-mV overdrive, t_{RISE} = 100ns			30		ms
UNDERVOLTAGE LOCKOUT							
UVLO	IC active threshold voltage	VBUS rising		3.05	3.3	3.55	V
$UVLO_{(HYS)}$	IC active hysteresis	VBUS falling from above UVLO		120	150		mV
PWM							
	Internal top reverse blocking MOSFET on-resistance	$I_{IN(LIMIT)}$ = 500 mA, Measured from VBUS to PMID			180	250	mΩ
	Internal top N-channel Switching MOSFET on-resistance	Measured from PMID to SW			120	250	
	Internal bottom N-channel MOSFET on-resistance	Measured from SW to PGND			150	200	
$f_{(OSC)}$	Oscillator frequency				3		MHz
	Frequency accuracy			–10%		10%	
$D_{(MAX)}$	Maximum duty cycle				99.5%		
$D_{(MIN)}$	Minimum duty cycle			0			
	Synchronous mode to non-synchronous mode transition current threshold (2)	Low side MOSFET cycle by cycle current sensing			100		mA

(1) Negative charge current means the charge current flows from the battery to charger (discharging battery).
(2) Bottom N-channel MOSFET always turns on for ≈60 ns and then turns off if current is too low.

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ELECTRICAL CHARACTERISTICS (continued)

Circuit of Figure 1, VBUS = 5 V, HZ_MODE = 0, OPA_MODE = 0 (charger mode operation), T_J = 0°C to 125°C, T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BOOST MODE OPERATION FOR VBUS (OPA_MODE = 1, HZ_MODE = 0)						
$V_{(BUS_B)}$	Boost output voltage (to pin VBUS)	2.5 V < $V_{(AUXPWR)}$ < 4.5 V, Open loop		5.05		V
	Boost output voltage accuracy	Including line and load regulation		±3%		
$I_{(BO)}$	Maximum output current for boost	$V_{(BUS_B)}$ = 5.05 V, 2.5 V < $V_{(AUXPWR)}$ < 4.5 V	200			mA
$I_{(BLIMIT)}$	Cycle by cycle current limit for boost	$V_{(BUS_B)}$ = 5.05 V, 2.5 V < $V_{(AUXPWR)}$ < 4.5 V		1		A
$VBUS_{(OVP)}$	Overvoltage protection threshold for boost (VBUS pin)	Threshold over VBUS to turn off converter during boost	5.8	6	6.2	V
	$VBUS_{(OVP)}$ hysteresis	VBUS falling from above $VBUS_{(OVP)}$		125		mV
$V_{(BAT)}MAX$	Maximum battery voltage for boost (CSOUT pin)	$V_{(CSOUT)}$ rising edge during boost	4.75	4.9	5.05	V
	$V_{(BAT)}MAX$ hysteresis	$V_{(CSOUT)}$ falling from above VBATMAX		200		mV
$V_{(BAT)}MIN$	Minimum battery voltage for boost (AUXPWR pin)	During boosting		2.5		V
		Before boost starts		2.9	3.05	V
	Boost output resistance at high-impedance mode (From VBUS to PGND)	HZ_MODE = 1	165			kΩ
PROTECTION						
$V_{(OVP-IN)}$	Input VBUS OVP threshold voltage	Threshold over VBUS to turn off converter during charge	6.3	6.5	6.7	V
	$V_{(OVP_IN)}$ hysteresis	VBUS falling from above $V_{(OVP_IN)}$		140		mV
$V_{(OVP)}$	Battery OVP threshold voltage	$V_{(CSOUT)}$ threshold over $V_{(OREG)}$ to turn off charger during charge	110	117	121	$\%V_{(OREG)}$
	$V_{(OVP)}$ hysteresis	Lower limit for $V_{(CSOUT)}$ falling from above $V_{(OVP)}$		11		
$I_{(LIMIT)}$	Cycle-by-cycle current limit for charge	Charge mode operation	1.5	2.3	3	A
$V_{(SHORT)}$	Short-circuit voltage threshold	$V_{(AUXPWR)}$ falling	1.9	2	2.1	V
	$V_{(SHORT)}$ hysteresis	$V_{(AUXPWR)}$ rising from below $V_{(SHORT)}$		100		mV
$I_{(SHORT)}$	Short-circuit current	$V_{(AUXPWR)}$ ≤ $V_{(SHORT)}$	5	10	15	mA
$T_{(SHTDWN)}$	Thermal trip			165		°C
	Thermal hysteresis			10		
$T_{(CF)}$	Thermal regulation threshold(3)	Charge current begins to reduce		120		
$T_{(32S)}$	Time constant for the 32 second timer	32 Second mode	12	32		s

(3) Verified by design

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TYPICAL APPLICATION CIRCUITS

VBUS = 5 V, $I_{(IN_LIMIT)}$ = 500 mA, $I_{(CHARGE)}$ = 750 mA, VBAT = 3.5 V to 4.44 V (adjustable), Safety Timer = 32 minutes or 32 seconds.

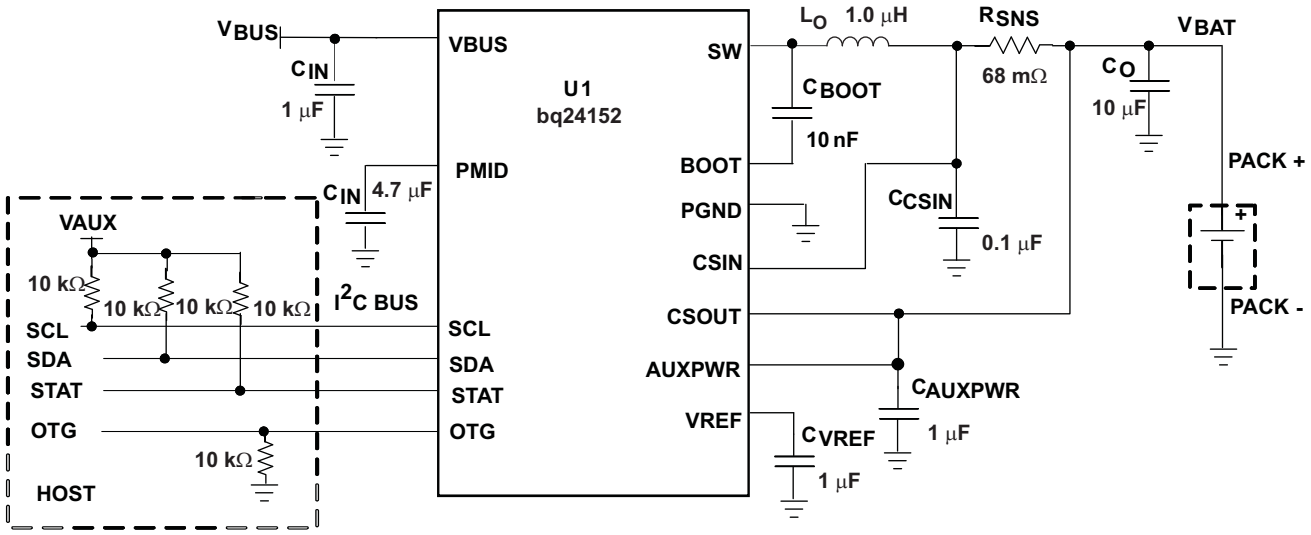


Figure 1. I²C Controlled 1-Cell Charger Application Circuit

VBUS = 5 V, $I_{(IN_LIMIT)}$ = 500 mA, V_{OUT} = 3.5 V to 4.44 V (adjustable), Safety Timer = 32 minutes or 32 seconds.

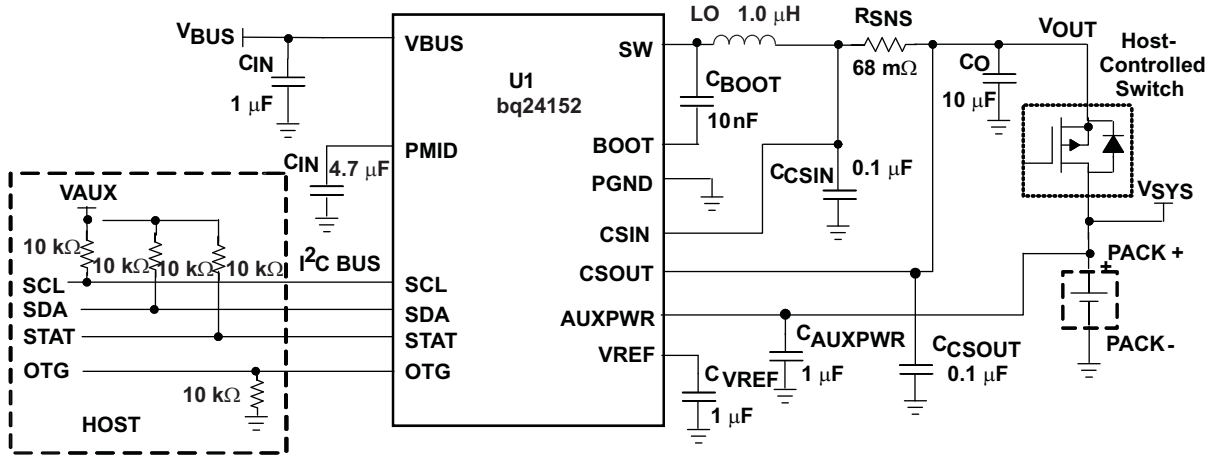


Figure 2. I²C Controlled 1-Cell Pre-Regulator Application

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TYPICAL CHARACTERISTICS

Using circuit shown in Figure 1, T_A = 25°C, unless otherwise specified.

ADAPTER INSERTION

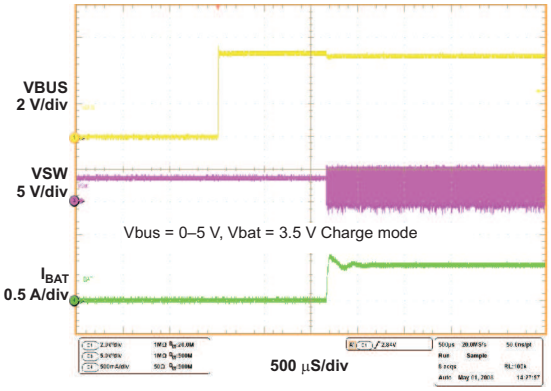


Figure 3.

BATTERY INSERTION/REMOVAL

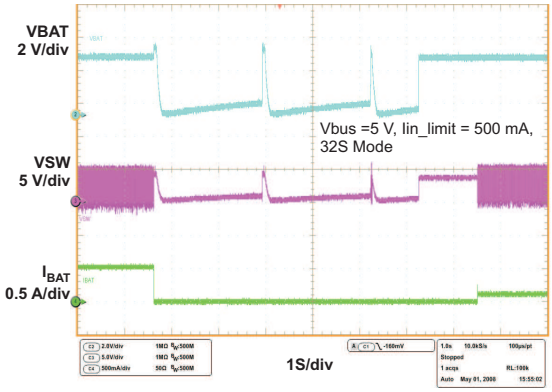


Figure 4.

PWM CHARGING WAVEFORMS

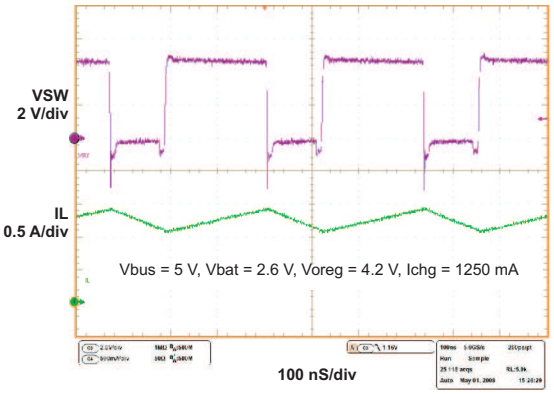


Figure 5.

POOR SOURCE DETECTION

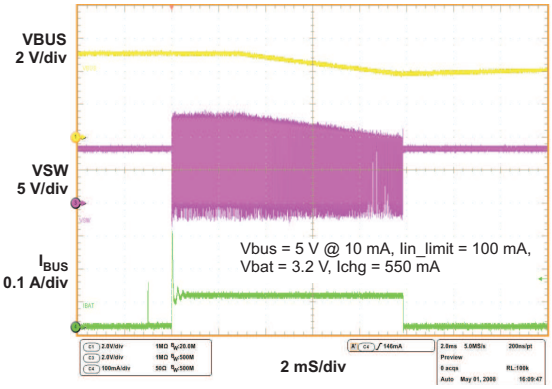


Figure 6.

BATTERY DETECTION AT POWER UP

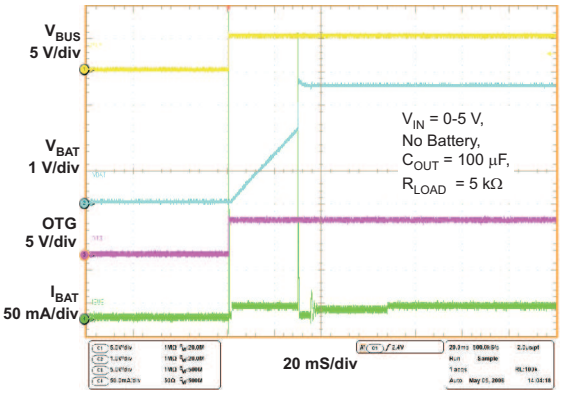


Figure 7.

CYCLE BY CYCLE CURRENT LIMIT IN CHARGE MODE

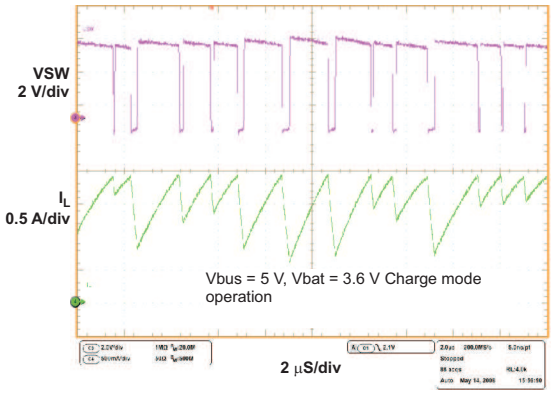


Figure 8.

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TYPICAL CHARACTERISTICS (continued)

INPUT CURRENT CONTROL

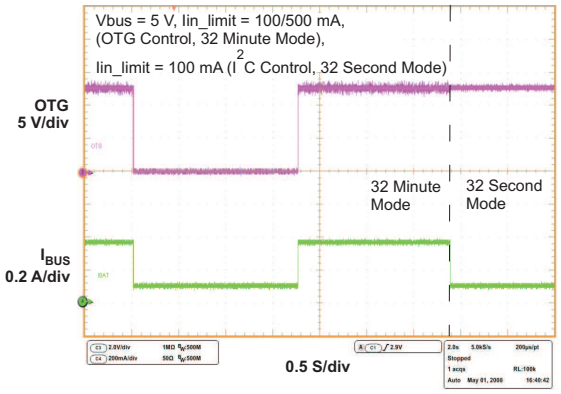


Figure 9.

CHARGER EFFICIENCY

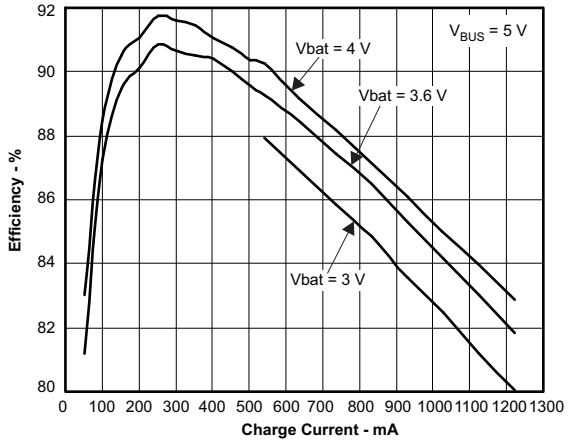


Figure 10.

BOOST WAVEFORM (PWM MODE)

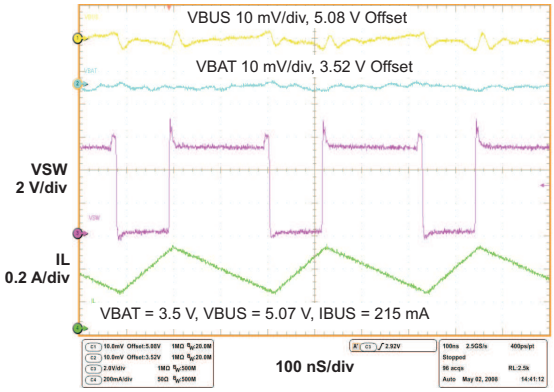


Figure 11.

BOOST WAVEFORM (PFM MODE)

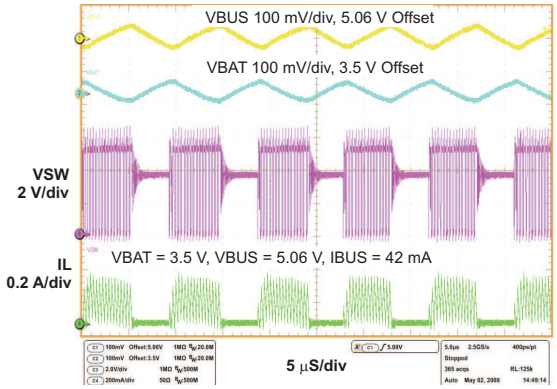


Figure 12.

VBUS OVERLOAD WAVEFORMS (BOOST MODE)

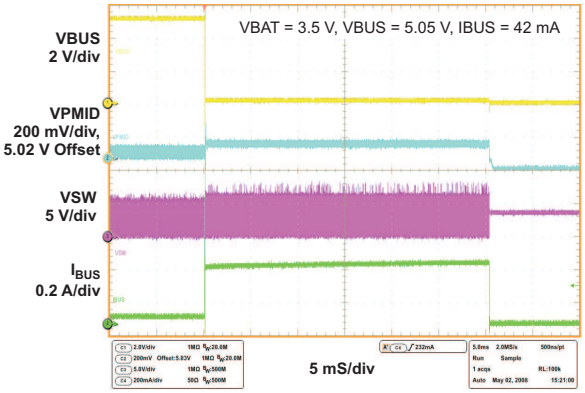


Figure 13.

LOAD STEP UP RESPONSE (BOOST MODE)

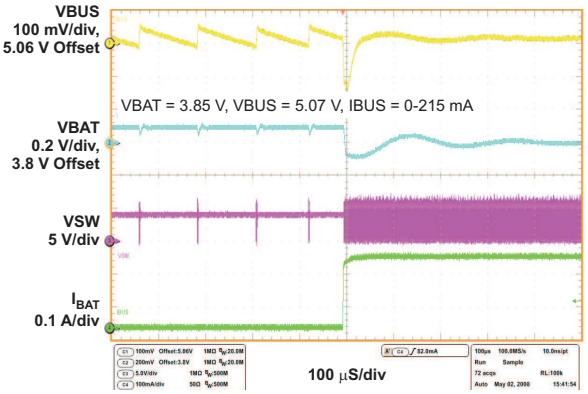


Figure 14.

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TYPICAL CHARACTERISTICS (continued)

LOAD STEP DOWN RESPONSE (BOOST MODE)

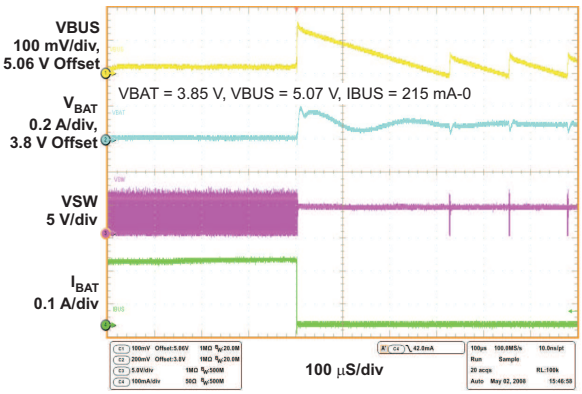


Figure 15.

CYCLE BY CYCLE CURRENT LIMITING IN BOOST MODE

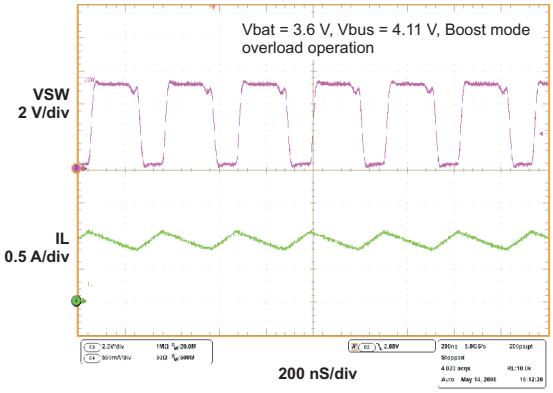


Figure 16.

BOOST TO CHARGE MODE TRANSITION (OTG CONTROL)

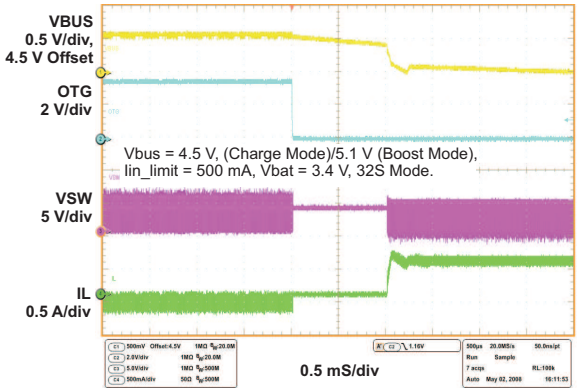


Figure 17.

BOOST EFFICIENCY

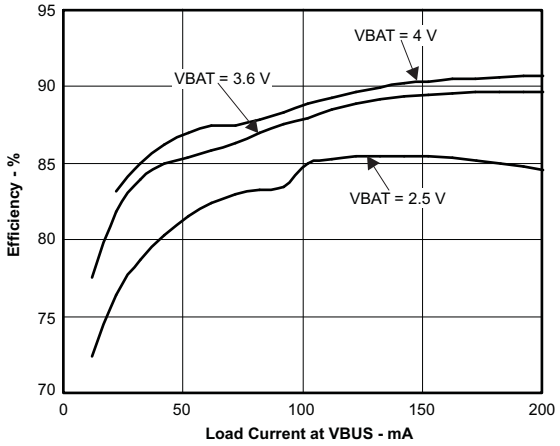


Figure 18.

LINE REGULATION FOR BOOST

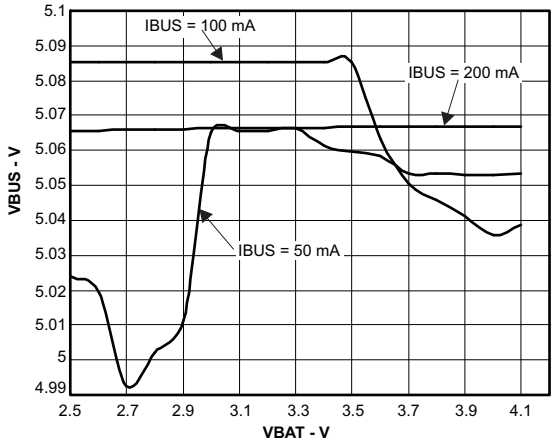


Figure 19.

LOAD REGULATION FOR BOOST

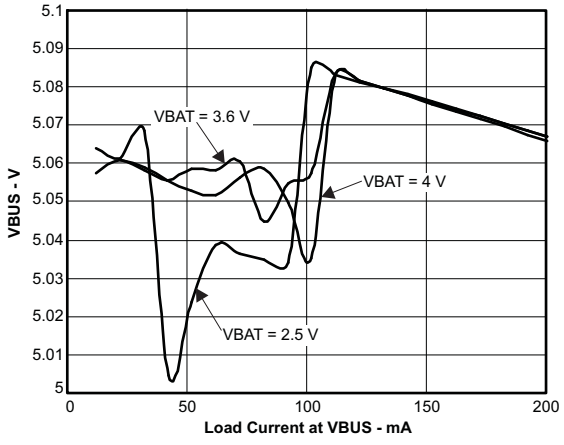


Figure 20.

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FUNCTIONAL BLOCK DIAGRAM (Charge Mode)

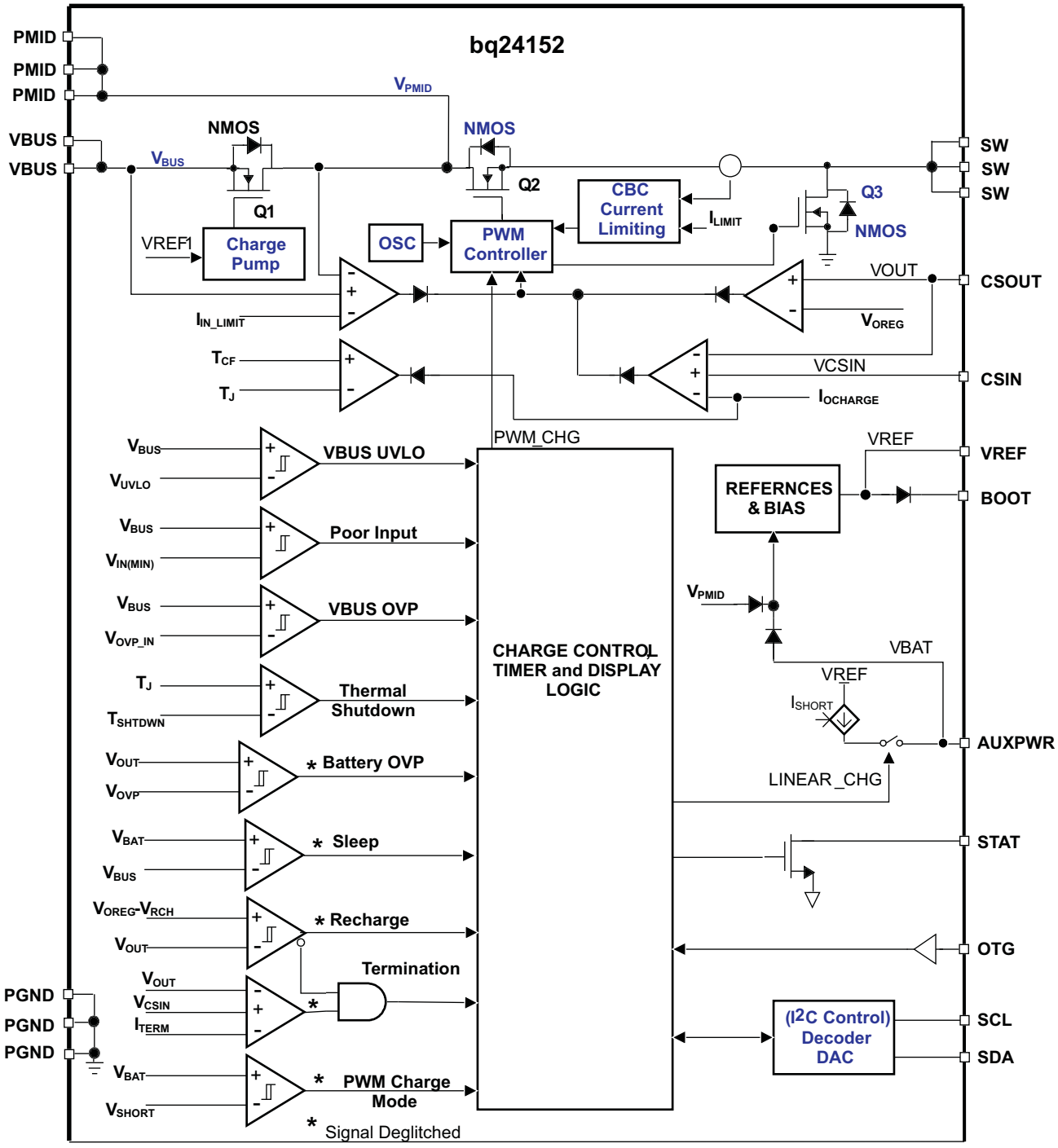


Figure 21. Function Block Diagram of bq24152 in Charge Mode

FUNCTIONAL BLOCK DIAGRAM (Boost Mode)

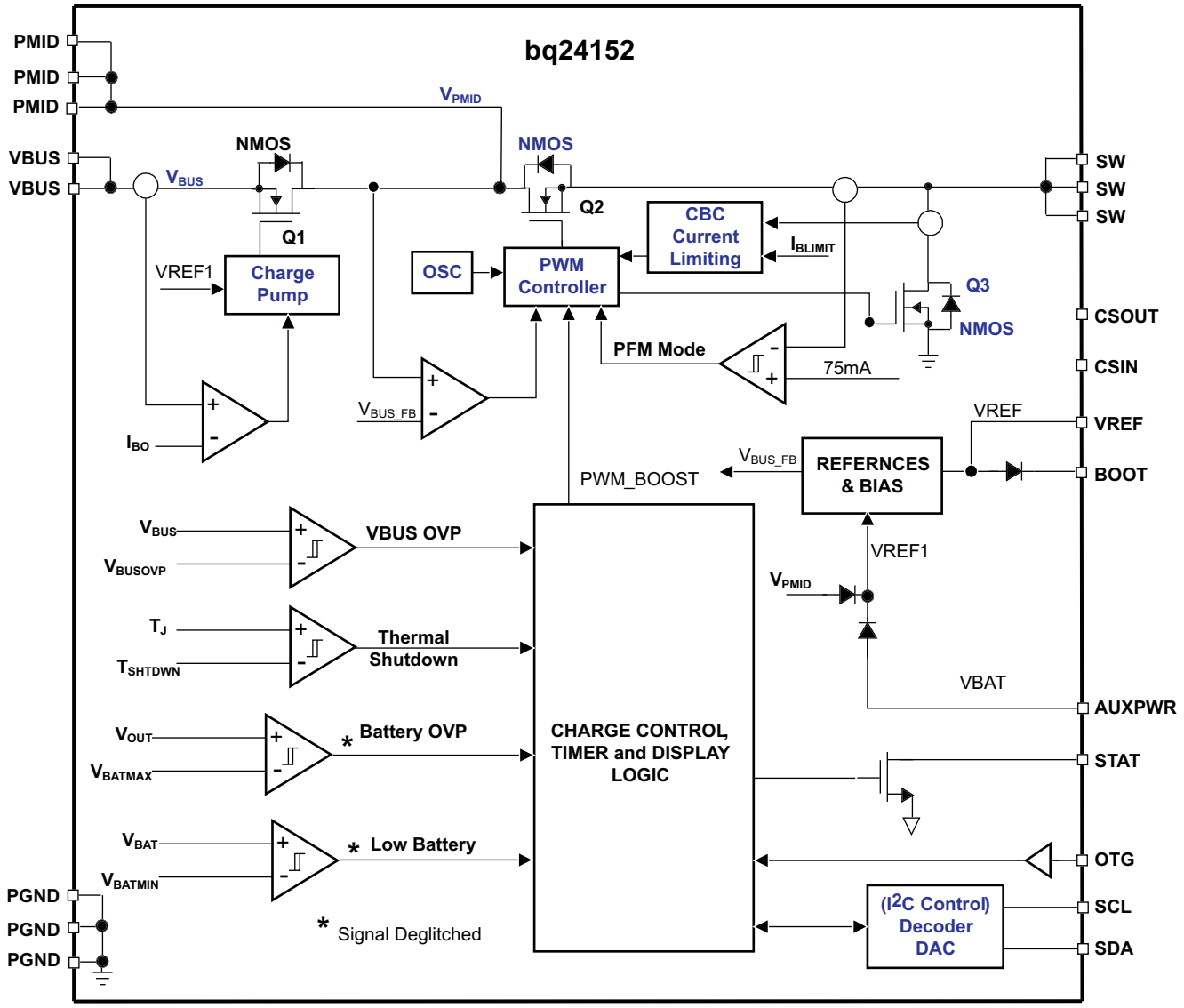


Figure 22. Function Block Diagram of bq24152 in Boost Mode

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OPERATIONAL FLOW CHART

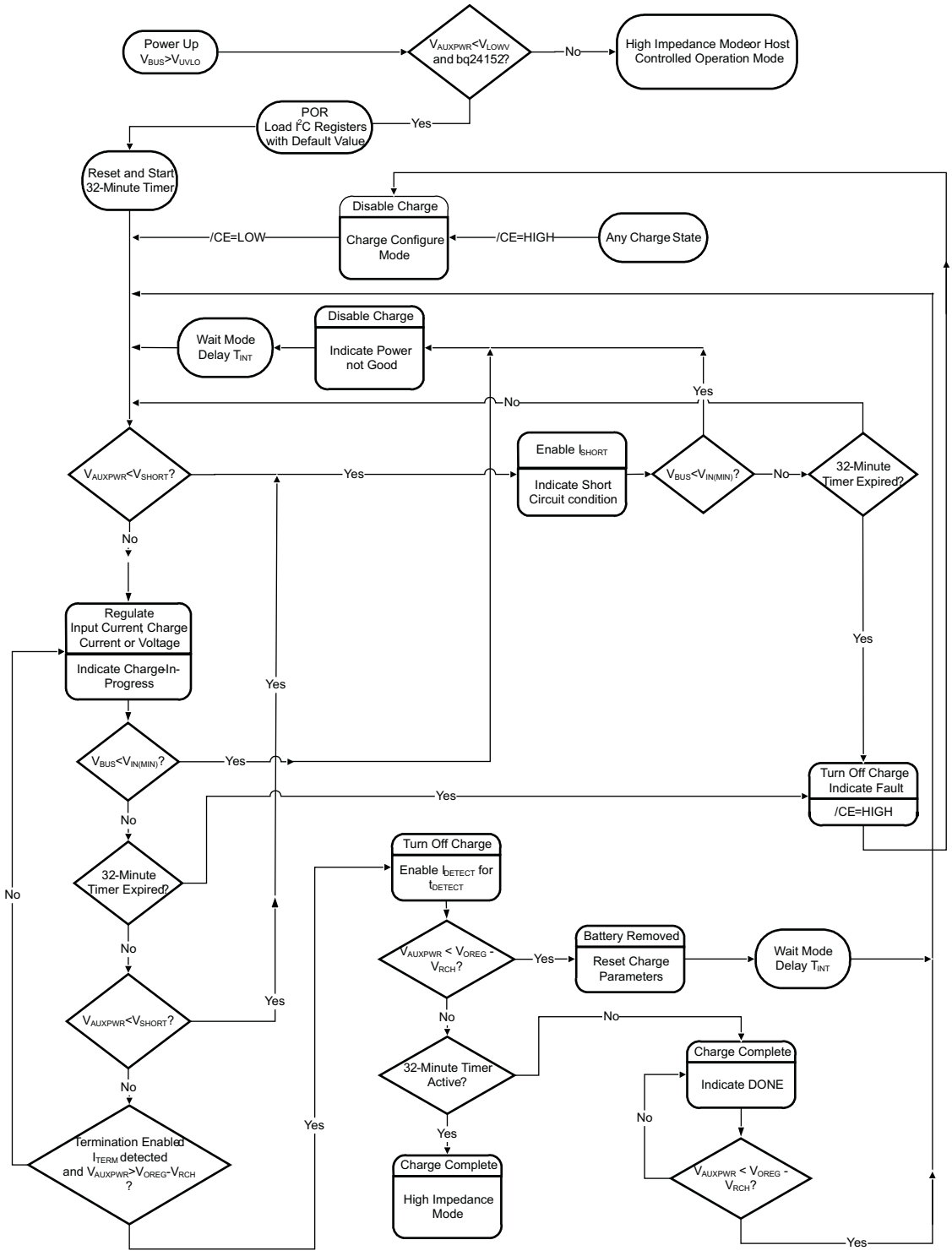


Figure 23. Operational Flow Chart of bq24152 in Charge Mode

DETAILED FUNCTIONAL DESCRIPTION

For a current limited power source, such as a USB host or hub, the high efficiency converter is critical in fully using the input power capacity and charging the battery. Due to the high efficiency in a wide range of the input voltage and battery voltage, the switching mode charger is a good choice for high speed charging with less power loss and better thermal management.

The bq24152 is a highly integrated synchronous switch-mode charger with reverse boost function for USB OTG support, featuring integrated MOSFETs and small external components, targeted at extremely space-limited portable applications powered by 1-cell Li-Ion or Li-polymer battery pack.

The bq24152 usually has three operation modes: charge mode, boost mode, and high impedance mode. In charge mode, the bq24152 supports a precision Li-ion or Li-polymer charging system for single-cell applications. In boost mode, bq24152 boosts the battery voltage to VBUS for powering attached OTG devices. In high impedance mode, the bq24152 stops charging or boosting and operates in a mode with low current from VBUS or battery, to effectively reduce the power consumption when the portable device in standby mode. Through the proper control, bq24152 can achieve the smooth transition among different operation modes.

CHARGE MODE OPERATION

Charge Profile

In charge mode, bq24152 has four control loops to regulate input current, charge current, charge voltage and device junction temperature, as shown in Figure 21. During the charging process, all four loops are enabled and the one that is dominant will take over the control. The bq24152 supports a precision Li-ion or Li-polymer charging system for single-cell applications. Figure 24(a) indicates a typical charge profile without input current regulation loop and it is similar to the traditional CC/CV charge curve, while Figure 24(b) shows a typical charge profile when input current limiting loop is dominant during the constant current mode, and in this case the charge current is higher than the input current so the charge process is faster than the linear chargers. For bq24152, the input current limits, the charge current, termination current, and charge voltage are all programmable using I^2C interface.

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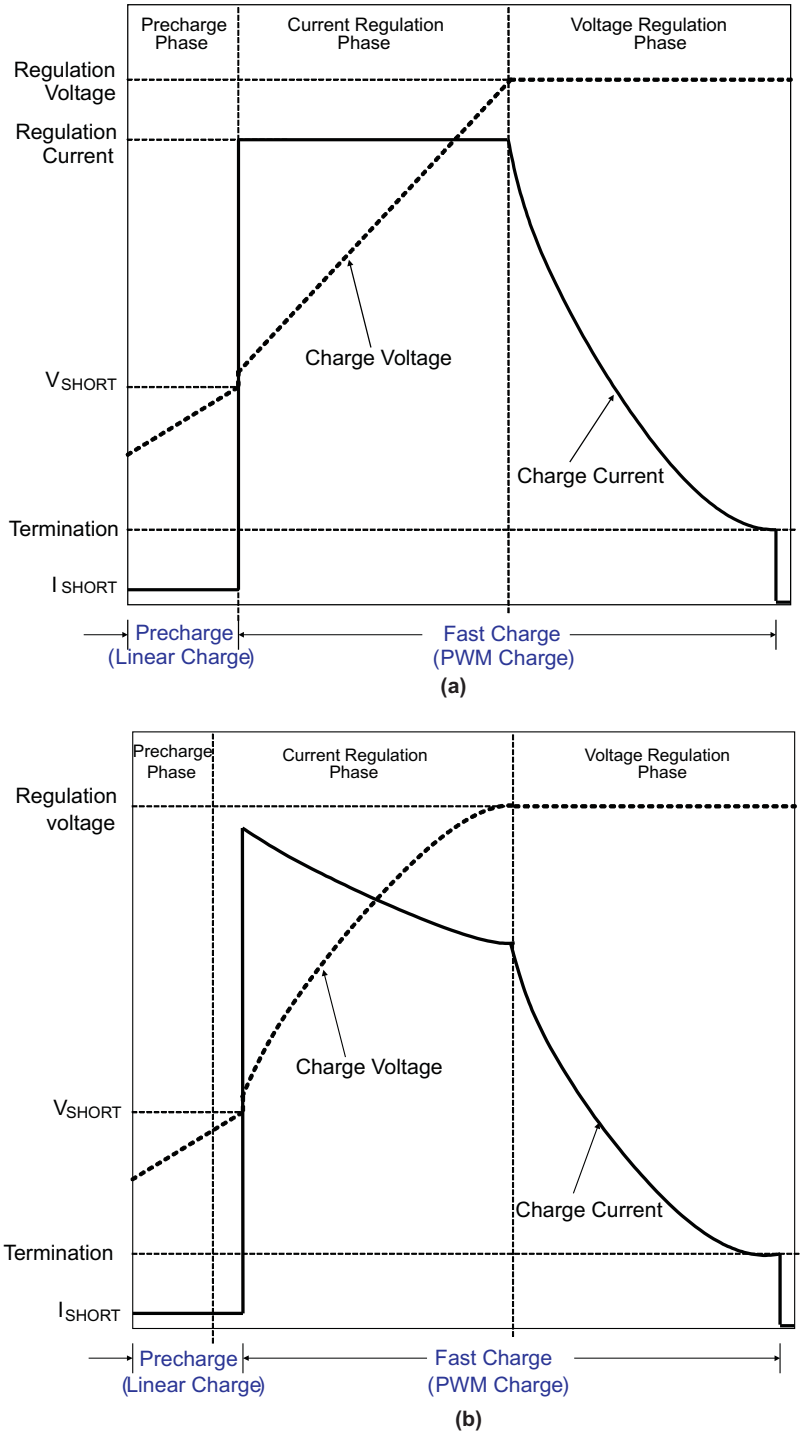


Figure 24. Typical Charging Profile of bq24152 for (a) without Input Current Limit, and (b) with Input Current Limit

PWM Controller in Charge Mode

The bq24152 provides an integrated, fixed 3-MHz frequency voltage-mode controller with Feed-Forward function to regulate charge current or voltage. This type of controller is used to help improve line transient response, thereby, simplifying the compensation network used for both continuous and discontinuous current conduction operation. The voltage and current loops are internally compensated using a Type-III compensation scheme that provides enough phase margin for stable operation, allowing the use of small ceramic capacitors with low ESR. There is a 0.5-V offset on the bottom of the PWM ramp to allow the device to operate between 0% to 99.5% duty cycles.

The bq24152 has two back to back common-drain N-channel MOSFETs at the high side and one N-channel MOSFET at low side. An input N-MOSFET (Q1) prevents battery discharge when VBUS is lower than VAUXPWR. The second high-side N-MOSFET (Q2) behaves as the switching control switch (see Figure 21). A charge pump circuit is used to provide gate drive for Q1, while a boot strap circuit with external boot-strap capacitor is used to boost up the gate drive voltage for Q2.

Cycle-by-cycle current limit is sensed through the internal sense MOSFETs for Q2 and Q3. The threshold for Q2 is set to a nominal 1.9-A peak current. The low-side MOSFET (Q3) also has a current limit that decides if the PWM Controller will operate in synchronous or non-synchronous mode. This threshold is set to 100mA and it turns off the low-side N-channel MOSFET (Q3) before the current reverses, preventing the battery from discharging. Synchronous operation is used when the current of the low-side MOSFET is greater than 100mA to minimize power losses.

Battery Charging Process

At the beginning of precharge, while battery voltage is below the $V_{(SHORT)}$ threshold, the bq24152 applies a short-circuit current, $I_{(SHORT)}$, to the battery.

When the battery voltage is above $V_{(SHORT)}$ and below $V_{(OREG)}$, the charge current ramps up to fast charge current, $I_{O(CHARGE)}$, or a charge current that corresponds to the input current of $I_{(IN_LIMIT)}$. The slew rate for fast charge current is controlled to minimize the current and voltage over-shoot during transient. Both the input current limit (default at 100 mA), IIN_LIMIT, and fast charge current, $I_{O(CHARGE)}$, can be set by the host. Once the battery voltage is close to the regulation voltage, $V_{(OREG)}$, the charge current is tapered down as shown in Figure 24. The voltage regulation feedback occurs by monitoring the battery-pack voltage between the CSOUT and PGND pins. bq24152 is a fixed single-cell voltage version, with adjustable regulation voltage (3.5 V to 4.44 V) programmed through I^2C interface.

The bq24152 monitors the charging current during the voltage regulation phase. Once the termination threshold, ITERM, is detected and the battery voltage is above the recharge threshold, the bq24152 terminates charge. The termination current level is programmable. To disable the charge current termination, the host can set the charge termination bit (I_Term) of charge control register to 0, see the I^2C section for details.

A new charge cycle is initiated when one of the following conditions is detected:

- The battery voltage falls below the $V_{(OREG)} - V_{(RCH)}$ threshold.
- VBUS Power-on reset (POR), if battery voltage is below the $V_{(LOWV)}$ threshold.
- $\overline{CE}$ bit toggle or RESET bit is set (host controlled)

Safety Timer in Charge Mode

At the beginning of charging process, the bq24152 starts a 32-minute timer (T32min) that can be stopped by any write-action performed by host through I^2C interface. Once the 32-minute timer is stopped, a 32-second timer (T32sec) is automatically started. The 32-second timer can be reset by host using I^2C interface. Writing "1" to reset bit of TMR_RST in control register resets the 32-second timer and TMR_RST is automatically set to "0" after the 32-second timer is reset. If the 32-second timer expires, the charge is terminated and charge parameters are reset to default values. Then the 32-minute timer starts and the charge resumes.

During normal charging process, the bq24152 is normally in 32-second mode with host control, and 32-minute mode without host control using I^2C interface. The process repeats until the battery is fully charged. If the 32-minute timer expires, bq24152 turns off the charger and enunciates FAULT on the STATx bits of status register. This function prevents battery over charge if the host fails to reset the safety timer. The safety timer flow chart is shown in Figure 25. Fault condition is cleared by POR and fault status bits can only be updated after the status bits are read out by the host.

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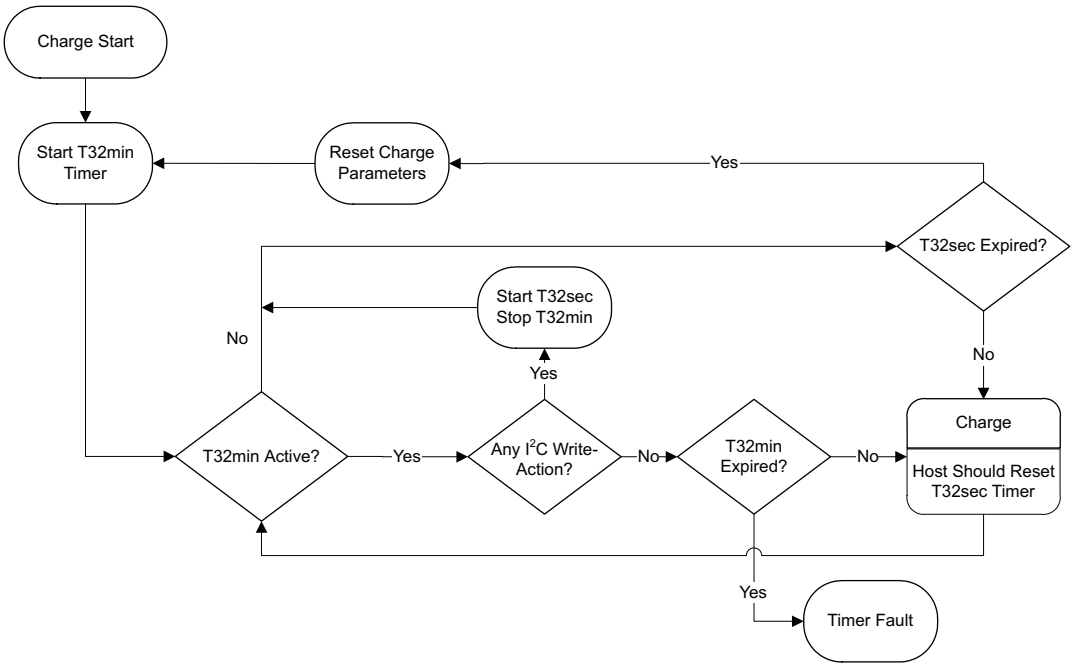


Figure 25. Timer Flow Chart for bq24152 in Charge Mode

USB Friendly Boot-Up Sequence

At power on reset (POR) of VBUS, if the battery voltage is above the weak battery threshold, V_{LOWV}, bq24152 will operate in a mode dictated by the I^2C control registers. On the other hand, if the battery voltage is below V_{LOWV} and the host control through I^2C interface is lost (32 minute mode), bq24152 will reset all I^2C registers with default values and enable the charger with an input current limit dictated by the OTG pin voltage level until the host programs the I^2C registers. During this period, the input current limit is 100 mA when the voltage level of OTG pin is Low; while the input current limit is 500 mA when the voltage level of OTG pin is high. This feature could quickly revive the deeply discharged cell. The charge process continues even the battery is charged to the regulation voltage (default at 3.54 V) since termination is disabled by default. In another case, if the battery voltage is below V_{LOWV} but the host control using I^2C interface is available (32 second mode), bq24152 will operate in a mode dictated by control registers.

Input Current Limiting

To maximize the charge rate of bq24152 without overloading the USB port, the input current for bq24152 can be limited to 100mA or 500mA which is programmed in the control register or OTG pin. Once the input current reaches the input current limiting threshold, the charge current is reduced to keep the input current from exceeding the programmed threshold. For bq14150, the default input current limit is controlled by the OTG pin at VBUS power on reset when $V_{(AUXPWR)}$ is lower than $V_{(LOWV)}$. The input current sensing resistor and control loop are integrated into bq24152. The input current limit can also be disabled using I^2C control, see the definition of control register (01H) for details.

Thermal Regulation and Protection

To prevent overheating the chip during the charging process, the bq24152 monitors the junction temperature, T_J, of the die and begins to taper down the charge current once T_J reaches the thermal regulation threshold, T_{CF}. The charge current is reduced to zero when the junction temperature increases approximately 10°C above T_{CF}. At any state, if T_J exceeds T_{SHTDWN}, bq24152 suspends charging. At thermal shutdown mode, PWM is turned off and all timers are frozen. Charging resumes when T_J falls below T_{SHTDWN} by approximately 10°C.

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Input Voltage Protection in Charge Mode

Sleep Mode

The bq24152 enters the low-power sleep mode if the voltage on VBUS pin falls below sleep-mode entry threshold, V_{AUXPWR} + V_{SLP}, and VBUS is still higher than the poor source detection threshold, V_{IN}(min). This feature prevents draining the battery during the absence of VBUS. During sleep mode, both the reverse blocking switch Q1 and PWM are turned off.

Input Source Detection

During the charging process, bq24152 continuously monitors the input voltage, VBUS. If VBUS falls to the low input voltage threshold, V_{IN}(min), poor input power source is detected. Under this condition, bq24152 terminates the charge process, waits for a delay time of T_{INT} and repeats the charging process, as indicated in Figure 23. This unique function provides intelligence to bq24152 and so prevents USB power bus collapsing and oscillation when connecting to a suspended USB port, or a USB-OTG device with low current capability.

Input Overvoltage Protection

The bq24152 provides a built-in input over-voltage protection to protect the device and other components against damages if the input voltage (Voltage from VBUS to PGND) goes too high. When an input overvoltage condition is detected, bq24152 turns off the PWM converter, sets fault status bits, and sends out fault pulse in STAT pin. Once VBUS drops below the input overvoltage exit threshold, the fault is cleared and charge process resumes.

Battery Protection in Charge Mode

Output Overvoltage Protection

The bq24152 provides a built-in overvoltage protection to protect the device and other components against damage if the battery voltage goes too high, as when the battery is suddenly removed. When an overvoltage condition is detected, bq24152 turns off the PWM converter, sets fault status bits and sends out fault pulse in STAT pin. Once $V_{(CSOUT)}$ drops to the battery overvoltage exit threshold, the fault is cleared and charge process back to normal.

Battery Detection During Normal Charging

For applications with removable battery packs, the bq24152 provides a battery absent detection scheme to reliably detect insertion or removal of battery packs.

During normal charging process with host control, once the voltage at the AUXPWR pin is above the battery recharge threshold, $V_{(OREG)} - V_{(RCH)}$, and the termination charge current is detected, bq24152 turns off the charge and enables a discharge current, $I_{(DETECT)}$, for a period of t_{DETECT}, then checks the battery voltage. If the battery voltage is still above recharge threshold, the battery is present and the charge done is detected. However, if the battery voltage is below battery recharge threshold, the battery is absent. Under this condition, the charge parameters (such as input current limit) are reset to the default values and charge resumes after a delay of T_{INT}, as shown in Figure 23. This function ensures that the charge parameters are reset whenever the battery is replaced.

Power Up Without Battery

When no battery is present, at VBUS power up, bq24152 will charge the output capacitor in short circuit mode (when V_{AUXPWR}<V_{SHORT}) or PWM mode (when V_{AUXPWR}>V_{SHORT}). Once the output voltage at CSOUT pin is charged to the default regulation voltage (3.54V), the voltage is kept constant until the 32-minute timer expires or the host takes over the control through I^2C interface. This unique feature makes bq24152 capable of starting the system without battery.

Battery Short Protection

During the normal charging process, if the battery voltage is lower than the short-circuit threshold, $V_{(SHORT)}$, the charger operates in short circuit mode with a lower charge rate of $I_{(SHORT)}$, as shown in Figure 22.

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Charge Status Output, STAT Pin

The STAT pin is used to indicate operation conditions for bq24152. STAT is pulled low during charging and EN_STAT bit in control register (00H) is set to "1". Under other conditions, the STAT pin acts as a high impedance (open-drain) output. Under fault conditions, a 128-µs pulse is sent out to notify the host. The status of STAT pin at different operation conditions is summarized in Table 1. The STAT pin can be used to drive an LED or communicate to the host processor.

Table 1. STAT Pin Summary

Charge State	STAT
Charge in progress and EN_STAT = 1	Low
Other normal conditions	Open-drain
Charge mode faults: Timer fault, sleep mode, VBUS or battery overvoltage, poor input source, VBUS UVLO, no battery, thermal shutdown	128-µs pulse, then open-drain
Boost mode faults: Timer fault, over load, VBUS or battery overvoltage, low battery voltage, thermal shutdown	128-µs pulse, then open-drain

Control Bits in Charge Mode

$\overline{CE}$ Bit (Charge Mode)

The bit of $\overline{CE}$ in control register is used to disable or enable the charge process. A low logic level (0) on this bit enables the charge and a high logic level (1) disables the charge.

RESET Bit

The bit of RESET in control register is used to reset all the charge parameters. Writing '1" to RESET bit resets all the charge parameters to default values and RESET bit is automatically cleared to zero once the charge parameters are reset. It is designed for charge parameter reset before charge starts, and it is not recommended to set the RESET bit when charging or boosting in progress.

OPA_Mode Bit

OPA_MODE is the operation mode control bit. When OPA_MODE = 0, the bq24152 charges the related operation modes if HZ_MODE is set to "0", refer to Table 2 for detail.

Table 2. Operation Mode Summary

OPA_MODE	HZ_MODE	OPERATION MODE
0	0	Charge (no fault) Charge configure (fault, $V_{bus} > V_{UVLO}$) High impedance ($V_{bus} < V_{UVLO}$)
1	0	Boost (no faults) Any fault go to charge configure mode
X	1	High impedance

Boost Mode Operation

In 32 second mode, when the OTG pin is in active status or the bit of operation mode (OPA_MODE) at control register is set to 1, the bq24152 operates in boost mode and delivers the power to VBUS from the battery. At normal boost mode, bq24152 converts the battery voltage (2.5 V to 4.5 V) to VBUS-B (about 5.05V) and delivers a current as much as $I_{(BO)}$ (approximately 200 mA) to support other USB OTG devices connected to the USB connector.

PWM Controller in Boost Mode

Similar to charge mode operation, in boost mode, the bq24152 provides an integrated, fixed 3 MHz frequency voltage-mode controller to regulate output voltage at PMID pin (VPMID), as shown in Figure 22. The voltage control loop is internally compensated using a Type-III compensation scheme that provides enough phase margin for stable operation with a wide load range and battery voltage range

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In boost mode, the input N-MOSFET (Q1) prevents battery discharge when VBUS pin is overloaded. Cycle-by-cycle current limit is sensed through the internal sense MOSFET for Q3. The threshold for Q3 is set to a nominal 1-A peak current. The upper-side MOSFET (Q2) also has a current limit that decides if the PWM Controller will operate in synchronous or non-synchronous mode. This threshold is set to 75 mA and it turns off the high-side N-channel MOSFET (Q2) before the current reverses, preventing the battery from charging. Synchronous operation is used when the current of the high-side MOSFET is greater than 75 mA to minimize power losses.

Boost Start Up

To prevent the inductor saturation and limit the inrush current, a soft-start control is applied during the boost start up.

PFM Mode at Light Load

In boost mode, the bq24152 operates in pulse skipping mode (PFM mode) to reduce the power loss and improve the converter efficiency at light load condition. During boosting, the PWM converter is turned off once the inductor current is less than 75 mA; and the PWM is turned back on only when the voltage at PMID pin drops to about 99.5% of the rated output voltage. A unique pre-set circuit is used to make the smooth transition between PWM and PFM mode.

Safety Timer in Boost Mode

At the beginning of boost operation, the bq24152 starts a 32-second timer that can be reset by host through I^2C interface. Writing "1" to reset bit of TMR_RST in the control register resets the 32-second timer and TMR_RST is automatically set to "0" after the 32-second timer is reset. To keep in boost mode, the host must reset the 32-second timer repeatedly. Once the 32-second timer expires, the bq24152 turns off the boost converter, enunciate the fault pulse in STAT pin and set fault status bits in status register. Fault condition is cleared by POR or host control.

Protection in Boost Mode

Output Overvoltage Protection

The bq24152 provides a built-in overvoltage protection to protect the device and other components against damage if the VBUS voltage goes too high. When an overvoltage condition is detected, the bq24152 turns off the PWM converter, reset OPA_MODE bit to 0, sets fault status bits, and sends out fault pulse in STAT pin. Once VBUS drops to the normal level, the boost starts after host sets OPA_MODE to "1", or the OTG pin remains in active status.

Output Overload Protection

The bq24152 provides a built-in overload protection to prevent the device and battery from damage when VBUS is over loaded. Once over load condition is detected, Q1 operates in linear mode to limit the output current while VPMID keeps in voltage regulation. If the overload condition lasts for more than 30ms, the overload fault is detected. When an overload condition is detected, the bq24152 turns off the PWM converter, reset OPA_MODE bit to 0, sets fault status bits, and sends out fault pulse in STAT pin. The boost will not start until the host clears the fault register.

Battery Voltage Protection

During boosting, when battery voltage is above the battery overvoltage threshold, $V_{(BATMX)}$, or below the minimum battery voltage threshold, $V_{(BAT)}$min, the bq24152 turns off the PWM converter, reset OPA_MODE bit to 0, sets fault status bits, and sends out fault pulse in STAT pin. Once battery voltage goes back to the normal level, the boost starts after host sets OPA_MODE to "1", or the OTG pin remains in active status.

STAT Pin Boost Mode

During normal boosting process, the STAT pin behaves as a high impedance (open-drain) output. Under fault conditions, a 128-µs pulse is sent out to notify the host.

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High Impedance Mode

When control bit of HZ-MODE is set to "1" and the OTG pin is not in active status, the bq24152 operates in high impedance mode, with the impedance in VBUS pin higher than 165 kΩ. In high impedance mode, a crude 32-second timer is enabled when the battery voltage is below $V_{(LOWV)}$ to monitor the host control is available or not. If the crude 32 second timer expires, the bq24152 operates in 32 minute mode and the crude 32 second timer is disabled. In 32 minute mode, when VBUS is below UVLO, the bq24152 operates in high impedance mode regardless of the setting of the HZ_MODE bit.

Output Inductor and Capacitance Selection Guidelines

The bq24152 provides internal loop compensation. With this scheme, the best stability occurs when the LC resonant frequency, f_o, is approximately 40 kHz (20 kHz to 80 kHz). Equation 1 is used to calculate the value of the output inductor, L_{OUT}, and output capacitor, C_{OUT}.

$$f_o = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (1)$$

To reduce the output voltage ripple, a ceramic capacitor with the capacitance between 4.7 µF and 47 µF is recommended for C_{OUT}, see the application section for components selection.

Pre-Regulator Application

Figure 2 shows a typical pre-regulator application that the bq24152 operates as a DC/DC converter, with the termination disabled. The robust internal compensation design ensures the stable operation when the host-controlled switch is turned off. With the input overvoltage protection, output current regulation and high efficiency power conversion, the bq24152 is an ideal choice for pre-regulator used in pulse charging applications.

State Machine Table and State Diagram

Based on the previously-described operation modes, the definitions of all operation states are shown in Table 3 and Table 4, whereas the relationship among different states is shown in Figure 26.

Table 3. State Machine Table 1 of bq24152

MODE	POWER DOWN	CHARGE CONFIGURE	SHORT CIRCUIT	PWM CHARGE
IN Condition	VBUS < UVLO $V_{(AUXPWR)} < V_{(SHORT)}$	OPA_MODE = 0 HZ_MODE = 0 OTG Inactive VBUS > UVLO VBUS < VBUS(MIN) or VBUS < $V_{(SLP_ENT)}$ or $\overline{CE}$ = HIGH	OPA_MODE = 0 HZ_MODE = 0 OTGIinactive VBUS < VBUS(MIN) VBUS < $V_{(SLP_ENT)}$ +$V_{(SLP_EXIT)}$ $V_{(AUXPWR)} < V_{(SHORT)}$ $\overline{CE}$ = Low No Faults	OPA_MODE = 0 HZ_MODE = 0 OTG Inactive VBUS < VBUS(MIN) VBUS < $V_{(SLP_ENT)}$ +$V_{(SLP_EXIT)}$ $V_{(AUXPWR)} < V_{(SHORT)}$ $\overline{CE}$ = Low No Faults
OUT Condition	VBUS > UVLO $V_{(AUXPWR)} > V_{(SHORT)}$	OPA_MODE = 1 or HZ_MODE = 1 or VBUS > VBUS(MIN) VBUS > $V_{(SLP_ENT)}$ + $V_{(SLP_EXIT)}$ or VBUS > UVLO OTG Active	OPA_MODE = 1 or HZ_MODE = 1 VBUS < VBUS(MIN) VBUS < $V_{(SLP_ENT)}$ or $V_{(AUXPWR)} < V_{(SHORT)}$ $\overline{CE}$ = HIGH or Faults or OTG Active	OPA_MODE = 1 or HZ_MODE = 1 VBUS < VBUS(MIN) VBUS < $V_{(SLP_ENT)}$ or $V_{(AUXPWR)} < V_{(SHORT)}$ $\overline{CE}$ = HIGH or Faults or OTG Active
I^2C	Off	On	On	On
Buck	Off	Off	Off	On
$I_{(SHORT)}$	Off	Off	On	Off
Boost	Off	Off	Off	Off
Q1	Off	On/Off	On	On
Note	POR when out			

Table 4. State Machine Table 2 of bq24152

MODE	HIGH IMPEDANCE	BOOST CONFIGURE	BOOST
IN Condition	OPA_MODE = 1 or OTG inactive VBUS < UVLO, $V_{(AUXPWR)} > V_{(SHORT)}$ or Boost Configure, $V_{(AUXPWR)} + V_{(LOWV)}$ or Boost, $V_{(AUXPWR)} + V_{(BAT)}$MIN	OPA_MODE = 1 or HZ_MODE = 1 or OTG active $V_{(AUXPWR)} > V_{(LOWV)}$ Ready To Start Up or Faults During Boost	OPA_MODE = 1 HZ_MODE = 0 or OTG active $V_{(AUXPWR)} > V_{(BAT)}$MIN Start Up Finished or No Faults
OUT Condition	HZ_MODE = 0, OPA_MODE = 0 VBUS > UVLO or HZ_MODE = 0, OPA_MODE = 1 $V_{(AUXPWR)} > V_{(LOWV)}$ or $V_{(AUXPWR)} + V_{(SHORT)}$ or OTG Active	OPA_MODE = 0 OTG Inactive or HZ_MODE = 1 or $V_{(AUXPWR)} > V_{(LOWV)}$ Boost Start Up Finished	OPA_MODE = 0 OTG Inactive or HZ_MODE = 1 or $V_{(AUXPWR)} > V_{(BAT)}$MIN or Faults
	On	On	On
	Off	Off	Off
	Off	Off	Off
	Off	Off	On
	Off	On/Off(1)	On

(1) Q1 is OFF when VBUS is shorted to ground.

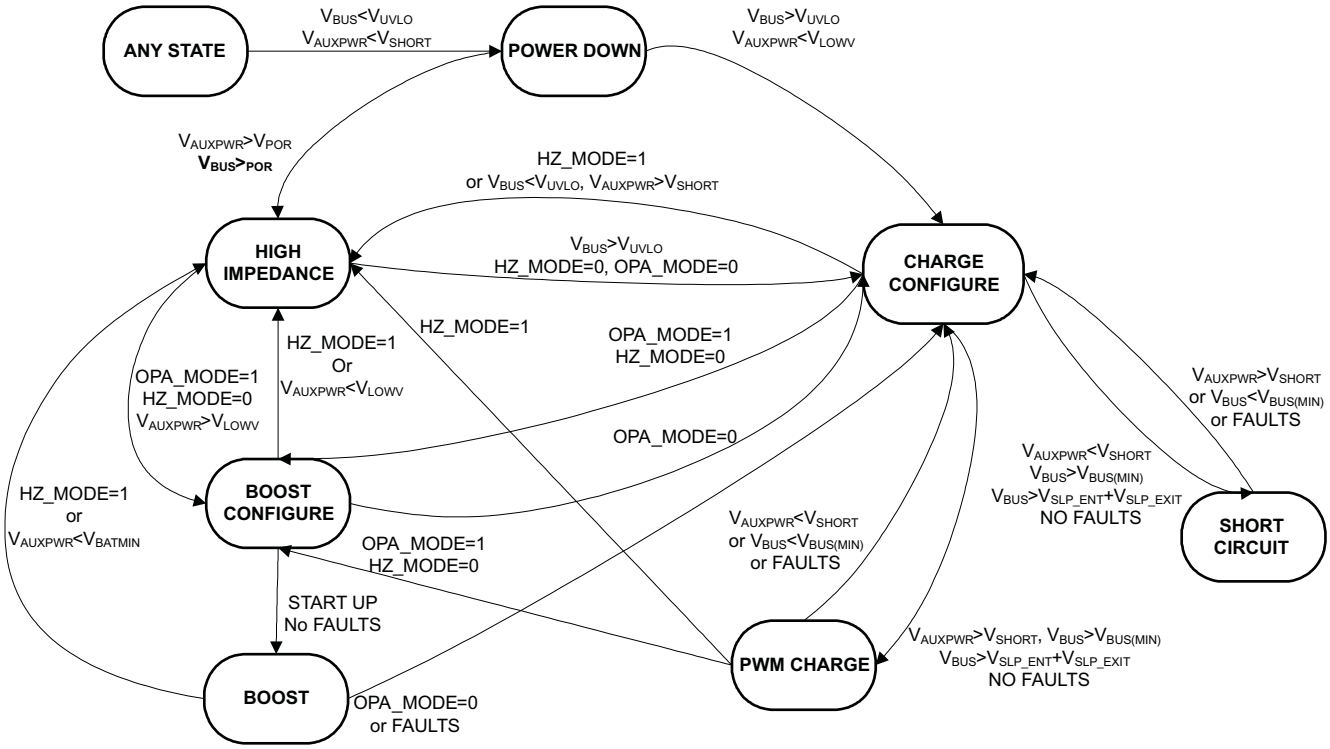


Figure 26. State Diagram for bq24152

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SERIAL INTERFACE DESCRIPTION

I²C™ is a 2-wire serial interface developed by Philips Semiconductor (see I²C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The bq24152 device works as a slave and supports the following data transfer modes, as defined in the I²C-Bus™ Specification: standard mode (100 kbps), fast mode (400 kbps), and high-speed mode (up to 3.4 Mbps in write mode). The interface adds flexibility to the battery charge solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as supply voltage remains above 2.2 V (typical).

The data transfer protocol for standard and fast modes is exactly the same; therefore, they are referred to as the F/S-mode in this document. The protocol for high-speed mode is different from the F/S-mode, and it is referred to as the HS-mode. The bq24152 device only supports 7-bit addressing. The device 7-bit address is defined as '1101011' (6BH).

F/S Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 27. All I²C-compatible devices should recognize a start condition.

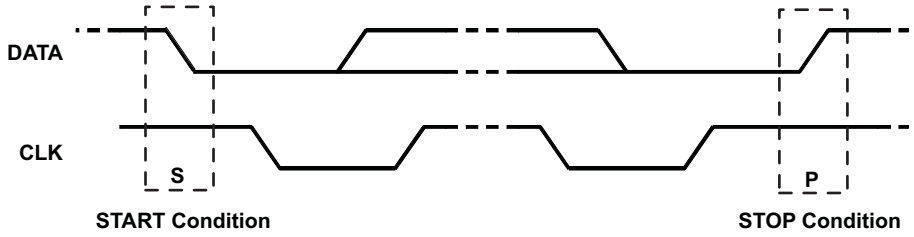


Figure 27. START and STOP Condition

The master then generates the SCL pulses, and transmits the 8-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 28). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 28) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

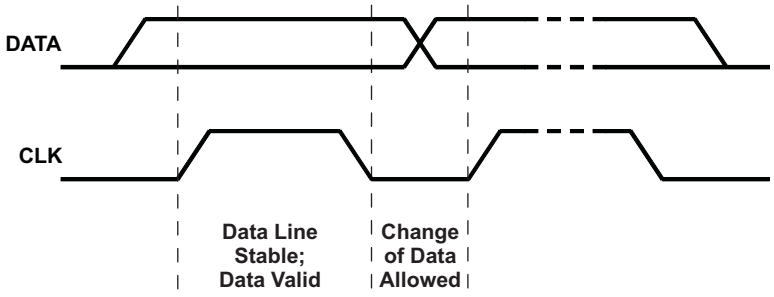


Figure 28. Bit Transfer on the Serial Interface

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an

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acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. the 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 30). This releases the bus and stops the communication link with the addressed slave. All I^2C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and wait for a start condition followed by a matching address. If a transaction is terminated prematurely, the master needs sending a STOP condition to prevent the slave I^2C logic from remaining in a bad state. Attempting to read data from register addresses not listed in this section will result in FFh being read out.

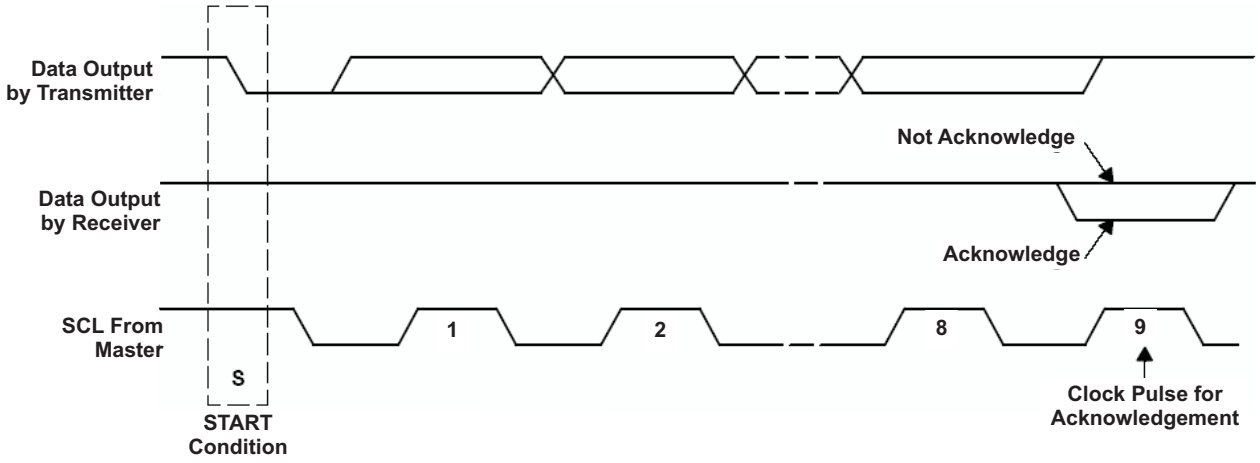


Figure 29. Acknowledge on the I^2C Bus™

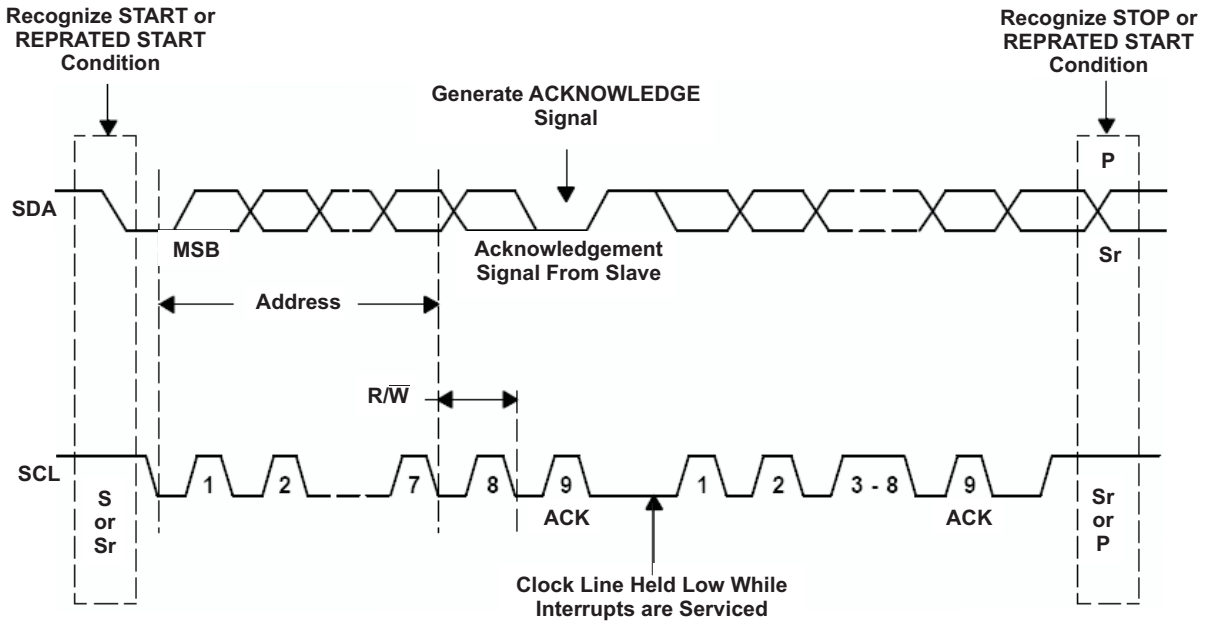


Figure 30. Bus Protocol

H/S Mode Protocol

When the bus is idle, both SDA and SCL lines are pulled high by the pull-up devices.

The master generates a start condition followed by a valid serial byte containing HS master code '00001XXX'. This transmission is made in F/S mode at no more than 400 Kbps. No device is allowed to acknowledge the HS master code, but all devices must recognize it and switch their internal setting to support 3.4-Mbps operation

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The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 3.4 Mbps are allowed. A stop condition ends the HS mode and switches all the internal settings of the slave devices to support the F/S mode. Instead of using a stop condition, repeated start conditions should be used to secure the bus in HS mode. If a transaction is terminated prematurely, the master needs sending a STOP condition to prevent the slave I^2C logic from remaining in a bad state.

Attempting to read data from register addresses not listed in this section results in FFh being read out.

bq24152 I^2C Update Sequence

The bq24152 requires a start condition, a valid I^2C address, a register address byte, and a data byte for a single update. After the receipt of each byte, bq24152 device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I^2C address selects the bq24152. The bq24152 performs an update on the falling edge of the acknowledge signal that follows the LSB byte.

For the first update, bq24152 requires a start condition, a valid I^2C address, a register address byte, a data byte. For all consecutive updates, bq24152 needs a register address byte, and a data byte. Once a stop condition is received, the bq24152 releases the I^2C bus, and awaits a new start conditions.

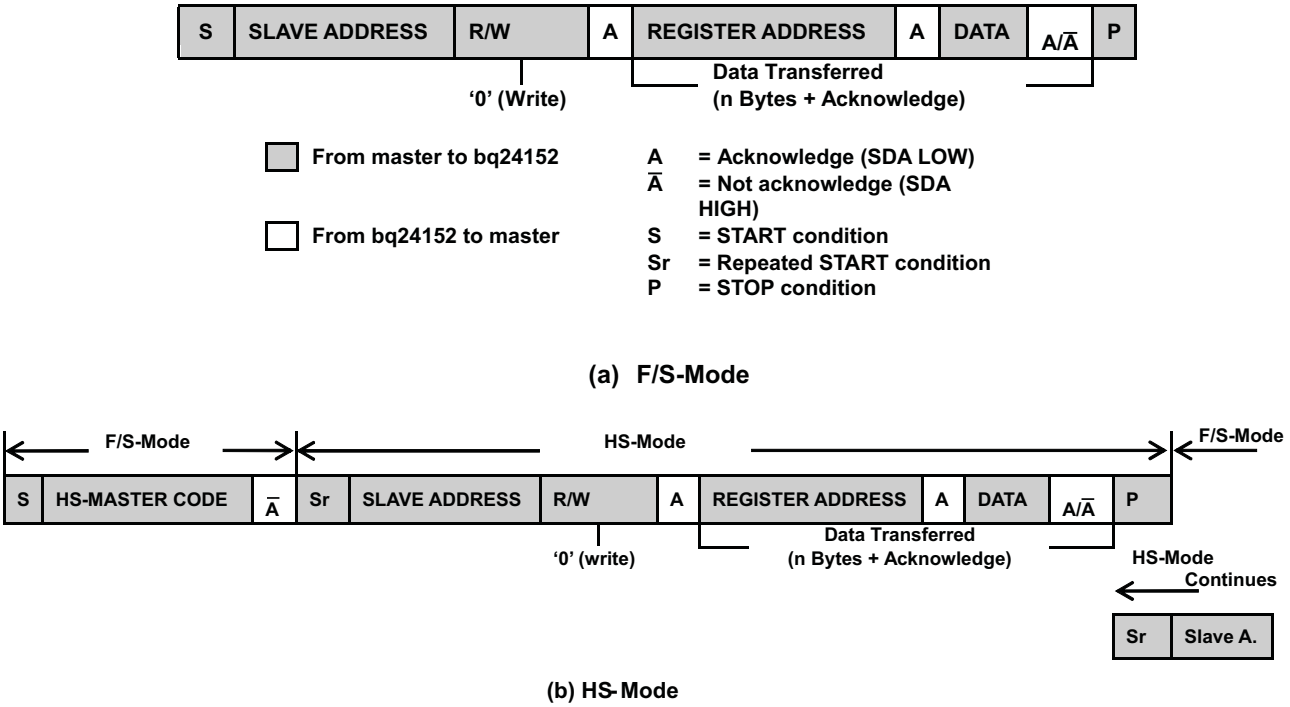


Figure 31. Data Transfer Format in F/S Mode and H/S Mode

Slave Address Byte

MSB							LSB
X	1	1	0	1	0	1	1

The slave address byte is the first byte received following the START condition from the master device. The address bits are factory preset to '1101011'.

Register Address Byte

MSB							LSB
0	0	0	0	0	D2	D1	D0

Following the successful acknowledgment of the slave address, the bus master will send a byte to the bq24152, which contains the address of the register to be accessed. The bq24152 contains five 8-bit registers accessible via a bidirectional I^2C-bus interface. Among them, four internal registers have read and write access; and one has only read access.

I^2C INTERFACE TIMING CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard mode			100	kHz
		Fast mode			400	kHz
		High-speed mode (write operation) CB - 100 pF max			3.4	MHz
		High-speed mode (read operation) CB - 100 pF max			2	
		High-speed mode (write operation) CB - 400 pF max			1.7	
		High-speed mode (read operation) CB - 400 pF max			2	
t_{BUF}	Bus free time between a STOP and START condition	Standard mode	4.7			µs
		Fast mode	1.3			
t_{HD}; t_{STA}	Hold time (repeated) START condition	Standard mode	4			µs
		Fast mode	600			ns
		High-speed mode	160			
t_{LOW}	LOW period of the SCL clock	Standard mode	4.7			µs
		Fast mode	1.3			
		High-speed mode, C_B – 100 pF max	160			ns
		High-speed mode, C_B – 400 pF max	320			
t_{HIGH}	HIGH period of the SCL clock	Standard mode	4			µs
		Fast mode	600			ns
		High-speed mode, C_B – 100 pF max	60			
		High-speed mode, C_B – 400 pF max	120			
t_{SU}; t_{STA}	Setup time for a repeated START condition	Standard mode	4.7			µs
		Fast mode	600			ns
		High-speed mode	160			
t_{SU}; t_{DAT}	Data setup time	Standard mode	250			ns
		Fast mode	100			
		High-speed mode	10			
t_{HD}; t_{DAT}	Data hold time	Standard mode			3.45	µs
		Fast mode			0.9	
		High-speed mode, C_B – 100 pF max			70	ns
		High-speed mode, C_B – 400 pF max			150	

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SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RCL}	Rise time of SCL signal	Standard mode	20+0.1C_B		1000	ns
		Fast mode	20+0.1C_B		300	
		High-speed mode, C_B – 100 pF max	10		40	
		High-speed mode, C_B – 400 pF max	20		80	
t_{RCL1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	Standard mode	20+0.1C_B		1000	ns
		Fast mode	20+0.1C_B		300	
		High-speed mode, C_B – 100 pF max	10		80	
		High-speed mode, C_B – 400 pF max	20		160	
t_{FCL}	Fall time of SCL signal	Standard mode	20+0.1C_B		300	ns
		Fast mode	20+0.1C_B		300	
		High-speed mode, C_B – 100 pF max	10		40	
		High-speed mode, C_B – 400 pF max	20		80	
t_{RDA}	Rise time of SDA signal	Standard mode	20+0.1C_B		1000	ns
		Fast mode	20+0.1C_B		300	
		High-speed mode, C_B – 100 pF max	10		80	
		High-speed mode, C_B – 400 pF max	20		160	
t_{FDA}	Fall time of SDA signal	Standard mode	20+0.1C_B		300	ns
		Fast mode	20+0.1C_B		300	
		High-speed mode, C_B – 100 pF max	10		80	
		High-speed mode, C_B – 400 pF max	20		160	
t_{SU}; t_{STO}	Setup time for STOP condition	Standard mode	4			µs
		Fast mode	600			ns
		High-speed mode	160			
C_B	Capacitive load for SDA and SCL				400	pF

I²C Timing Diagrams

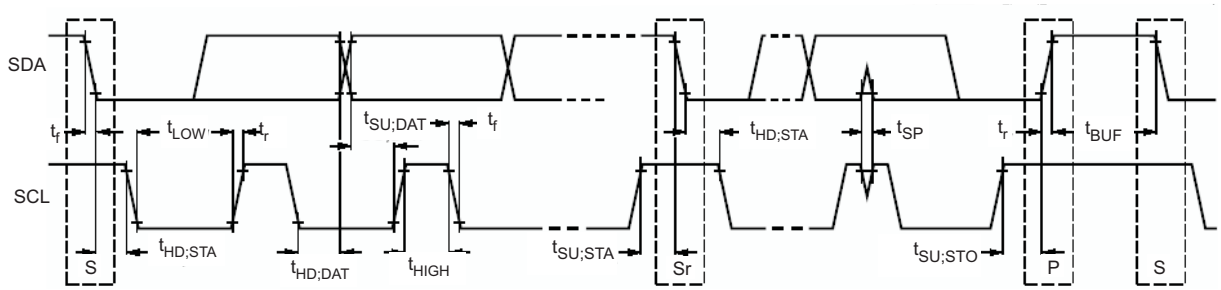


Figure 32. Serial Interface Timing for FS Mode

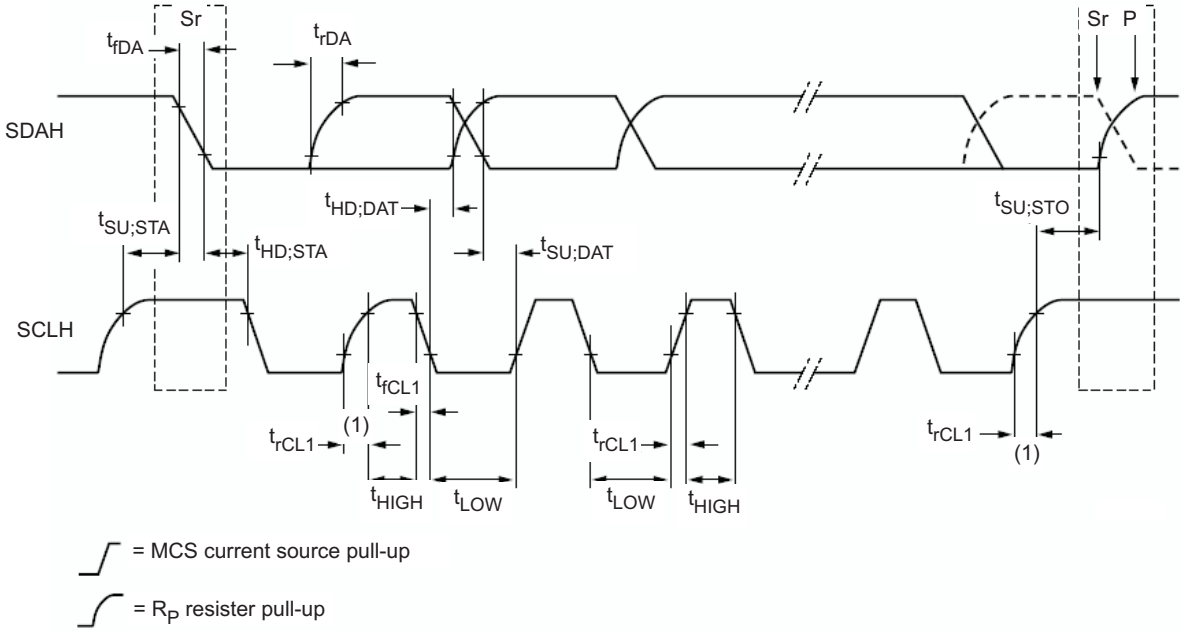


Figure 33. Serial Interface Timing for HS Mode

REGISTER DESCRIPTION

Table 5. Status/Control Register (Read/Write)
Memory Location: 00, Reset State: x1xx 0xxx

BIT	NAME	READ/WRITE	FUNCTION
B7 (MSB)	TMR_RST/OTG	Read/Write	Write: TMR_RST function, write "1" to reset the safety timer (auto clear) Read: OTG pin status, 0-OTG pin at Low level, 1-OTG pin at High level
B6	EN_STAT	Read/Write	0-Disable STAT pin function, 1-Enable STAT pin function (default 1)
B5	STAT2	Read Only	00-Ready, 01-Charge in progress, 10-Charge done, 11-Fault
B4	STAT1	Read Only	
B3	BOOST	Read Only	1-Boost mode, 0-Not in boost mode
B2	FAULT_3	Read Only	Charge mode: 000-Normal, 001-VBUS OVP, 010-Sleep mode, 011-Poor input source or VBUS < UVLO, 100-Battery OVP, 101-Thermal shutdown, 110-Timer fault, 111-No battery Boost mode: 000-Normal, 001-VBUS OVP, 010-Over load, 011-Battery voltage is too low, 100-Battery OVP, 101-Thermal shutdown, 110-Timer fault, 111-NA
B1	FAULT_2	Read Only	
B1 (LSB)	FAULT_1	Read Only	

Table 6. Control Register (Read/Write)
Memory Location: 01, Reset State: 0011 0000 (30H)

BIT	NAME	READ/WRITE	FUNCTION
B7 (MSB)	Iin_Limit_2	Read/Write	00-USB host with 100-mA current limit, 01-USB host with 500-mA current limit, 10-USB host/charger with 800-mA current limit, 11-No input current limit (default 00)
B6	Iin_Limit_1	Read/Write	
B5	VLOWV_2(1)	Read/Write	200-mV weak battery voltage threshold (default 1)
B4	VLOWV_1(1)	Read/Write	100-mV weak battery voltage threshold (default 1)
B3	TE	Read/Write	1-Enable charge current termination, 0-Disable charge current termination (default 0)
B2	$\overline{CE}$	Read/Write	1-Charger is disabled, 0-Charger enabled (default 0)
B1	HZ_MODE	Read/Write	1-High impedance mode, 0-Not high impedance mode (default 0)

(1) The range of the weak battery voltage threshold ($V_{(LOWV)}$) is 3.4 V to 3.7 V and step of 100 mV (default of 3.7 V).

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Table 6. Control Register (Read/Write)
Memory Location: 01, Reset State: 0011 0000 (30H) (continued)

BIT	NAME	READ/WRITE	FUNCTION
B1 (LSB)	OPA_MODE	Read/Write	1-Boost mode, 0-Charger mode (default 0)

Table 7. Control/Battery Voltage Register (Read/Write)
Memory Location: 02, Reset State: 0000 1010 (0AH)

BIT	NAME	READ/WRITE	FUNCTION
B7 (MSB)	$V_{O(REG5)}$	Read/Write	Battery regulation voltage: 640mV (default 0)
B6	$V_{O(REG4)}$	Read/Write	Battery regulation voltage: 320mV (default 0)
B5	$V_{O(REG3)}$	Read/Write	Battery regulation voltage: 160mV (default 0)
B4	$V_{O(REG2)}$	Read/Write	Battery regulation voltage: 80mV (default 0)
B3	$V_{O(REG1)}$	Read/Write	Battery regulation voltage: 40mV (default 1)
B2	$V_{O(REG0)}$	Read/Write	Battery regulation voltage: 20mV (default 0)
B1	OTG_PL	Read/Write	1-Active at High level, 0-Active at Low level (default 1)
B1 (LSB)	OTG_EN	Read/Write	1-Enable OTG Pin, 0-Disable OTG pin (default 0)

Charge voltage range is 3.5 V to 4.44 V with the offset of 3.5 V and step of 20 mV (default is 3.54 V).

Table 8. Vender/Part/Revision Register (Read only)
Memory Location: 03, Reset State: 0100 x001

BIT	NAME	READ/WRITE	FUNCTION
B7 (MSB)	Vender2	Read Only	Vender Code: bit 2 (default 0)
B6	Vender1	Read Only	Vender Code: bit 1 (default 1)
B5	Vender0	Read Only	Vender Code: bit 0 (default 0)
B4	PN1	Read Only	Part Number Code: bit 1 (default 0)
B3	PN0	Read Only	Part Number Code: bit 0 (default 0 for bq24151, default 1 for bq24152)
B2	Revision2	Read Only	000: Revision 1.0; 001: Revision 1.1; 010: Revision 1.2; 011-111: Future Revisions
B1	Revision1	Read Only	
B1 (LSB)	Revision0	Read Only	

Table 9. Battery Termination/Fast Charge Current Register (Read/Write)
Memory Location: 04, Reset State: 1000 1001 (89H)

BIT	NAME	READ/WRITE	FUNCTION
B7 (MSB)	Reset	Read/Write	Write: 1-Charger in reset mode, 0-No effect Read: always get "1"
B6	$V_{I(CHRG2)}$	Read/Write	Charge current sense voltage: 27.2mV (default 0)
B5	$V_{I(CHRG1)}$	Read/Write	Charge current sense voltage: 13.6mV(default 0)
B4	$V_{I(CHRG0)}$	Read/Write	Charge current sense voltage: 6.8mV (default 0)
B3	NA	Read/Write	NA
B2	$V_{I(TERM2)}$	Read/Write	Termination current sense voltage: 13.6mV (default 0)
B1	$V_{I(TERM1)}$	Read/Write	Termination current sense voltage: 6.8mV (default 0)
B1 (LSB)	$V_{I(TERM0)}$	Read/Write	Termination current sense voltage: 3.4mV (default 1)

Default charge current is 55 0mA and default termination current is 100 mA, if a 68-mΩ sensing resistor is used.

Both the termination current range and charge current range are depending on the sensing resistor $R_{(SNS)}$). The termination current step ($I_{O(TERM_STEP)}$) is calculated using Equation 2:

$$I_{O(TERM_STEP)} = \frac{V_{I(TERM0)}}{R_{(SNS)}} \quad (2)$$

Table 10 shows the termination current settings with two sensing resistors.

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Table 10. Termination Current Settings for 68-mΩ and 100-mΩ Sense Resistors

BIT	$V_{I(TERM)}$ (mV)	$I_{(TERM)}$ (mA) $R_{(SNS)}$ = 68mΩ	$I_{(TERM)}$ (mA) $R_{(SNS)}$ = 100mΩ
$V_{I(TERM2)}$	13.6	200	136
$V_{I(TERM1)}$	6.8	100	68
$V_{I(TERM0)}$	3.4	50	34
Offset	3.4	50	34

The charge current step ($I_{O(CHARGE_STEP)}$) is calculated using Equation 3:

$$I_{O(CHARGE_STEP)} = \frac{V_{I(CHRG0)}}{R_{(SNS)}} \quad (3)$$

Table 11 shows the charge current settings with two sensing resistors.

Table 11. Charge Current Settings for 68-mΩ and 100-mΩ Sense Resistors

BIT	$V_{I(REG)}$ (mV)	$I_{O(CHARGE)}$ (mA) $R_{(SNS)}$ = 68mΩ	$I_{O(CHARGE)}$ (mA) $R_{(SNS)}$ = 100mΩ
$V_{I(CHRG2)}$	27.2	400	272
$V_{I(CHRG1)}$	13.6	200	136
$V_{I(CHRG0)}$	6.8	100	68
Offset	37.4	550	374

DESIGN EXAMPLE FOR TYPICAL APPLICATION CIRCUITS

Systems Design Specifications:

- VBUS = 5 V
- $V_{(BAT)}$ = 4.2 V (1-Cell)
- $I_{(charge)}$ = 1.25 A
- Inductor ripple current = 30% of fast charge current

1. Determine the inductor value (L_{OUT}) for the specified charge current ripple:

$$L_{OUT} = \frac{VBAT \times (VBUS - VBAT)}{VBUS \times f \times \Delta I_L}$$

, the worst case is when battery voltage is as close as to half of the input voltage.

$$L_{OUT} = \frac{2.5 \times (5 - 2.5)}{5 \times (3 \times 10^{6}) \times 1.25 \times 0.3}$$

L_{OUT} = 1.11 µH

Select the output inductor to standard 1 µH. Calculate the total ripple current with using the 1 µH inductor:

$$\Delta I_L = \frac{VBAT \times (VBUS - VBAT)}{VBUS \times f \times L_{OUT}}$$

$$\Delta I_L = \frac{2.5 \times (5 - 2.5)}{5 \times (3 \times 10^{6}) \times (1 \times 10^{-6})}$$

ΔI_L = 0.42 A

Calculate the maximum output current:

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$$I_{LPK} = I_{OUT} + \frac{\Delta I_L}{2}$$

$$I_{LPK} = 1.25 + \frac{0.42}{2}$$

I_{LPK} = 1.46 A

Select 2.5mm by 2.0mm 1-µH 1.5-A surface mount multi-layer inductor. The suggested inductor part numbers are shown as following.

Table 12. Inductor Part Numbers

PART NUMBER	INDUCTANCE	SIZE	MANUFACTURER
LQM2HPN1R0MJ0	1 µH	2.5 x 2.0 mm	muRata
MIPS2520D1R0	1 µH	2.5 x 2.0 mm	FDK
MDT2520-CN1R0M	1 µH	2.5 x 2.0 mm	TOKO
CP1008	1 µH	2.5 x 2.0 mm	Inter-Technical

2. Determine the output capacitor value C_{OUT} using 40 kHz as the resonant frequency:

$$f_o = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}}$$

$$C_{OUT} = \frac{1}{4\pi^2 \times f_0^2 \times L_{OUT}}$$

$$C_{OUT} = \frac{1}{4\pi^2 \times (40 \times 10^3)^2 \times (1 \times 10^{-6})}$$

C_{OUT} = 15.8 µF

Select two 0603 X5R 6.3V 10-µF ceramic capacitors in parallel i.e., muRata GRM188R60J106M.

3. Determine the sense resistor using the following equation:

$$R_{(SNS)} = \frac{V_{(RSNS)}}{I_{(CHARGE)}}$$

The maximum sense voltage across sense resistor is 85 mV. In order to get a better current regulation accuracy, $V_{(RSNS)}$ should equal 85 mV, and calculate the value for the sense resistor.

$$R_{(SNS)} = \frac{85mV}{1.25A}$$

$R_{(SNS)}$ = 68 mΩ

This is a standard value. If it is not a standard value, then choose the next close value and calculate the real charge current. Calculate the power dissipation on the sense resistor:

$P_{(RSNS)} = I_{(CHARGE)}^2 \times R_{(SNS)}$

$P_{(RSNS)} = 125^2 \times 0.068$

$P_{(RSNS)}$ = 0.106 W

Select 0402 0.125-W 68-mΩ 2% sense resistor, i.e. Panasonic ERJ2BWGR068.

4. Measured efficiency and total power loss for different inductors are shown in Figure 34.

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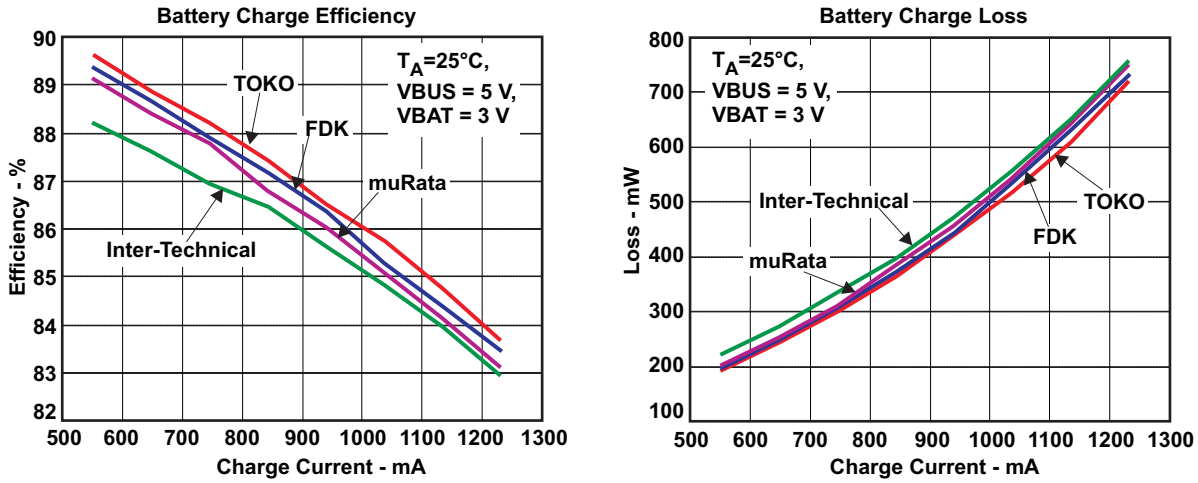


Figure 34. Measured Efficiency and Power Loss

PCB LAYOUT CONSIDERATION

It is important to pay special attention to the PCB layout. The following provides some guidelines:

- To obtain optimal performance, the power input capacitors, connected from input to PGND, should be placed as close as possible to the bq24152. The output inductor should be placed close to the IC and the output capacitor connected between the inductor and PGND of the IC. The intent is to minimize the current path loop area from the SW pin through the LC filter and back to the PGND pin. To prevent high frequency oscillation problems, proper layout to minimize high frequency current path loop is critical (see Figure 35). The sense resistor should be adjacent to the junction of the inductor and output capacitor. Route the sense leads connected across the RSNS back to the IC, close to each other (minimize loop area) or on top of each other on adjacent layers (do not route the sense leads through a high-current path, see Figure 36).
- Place all decoupling capacitor close to their respective IC pin and as close as to PGND (do not place components such that routing interrupts power stage currents). All small control signals should be routed away from the high current paths.
- The PCB should have a ground plane (return) connected directly to the return of all components through vias (two vias per capacitor for power-stage capacitors, two vias for the IC PGND, one via per capacitor for small-signal components). A star ground design approach is typically used to keep circuit block currents isolated (high-power/low-power small-signal) which reduces noise-coupling and ground-bounce issues. A single ground plane for this design gives good results. With this small layout and a single ground plane, there is no ground-bounce issue, and having the components segregated minimizes coupling between signals.
- The high-current charge paths into VBUS, PMID and from the SW pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces. The PGND pins should be connected to the ground plane to return current through the internal low-side FET.

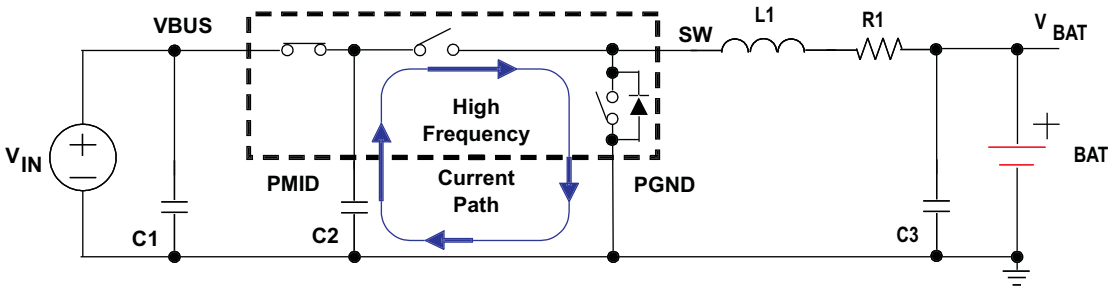


Figure 35. High Frequency Current Path

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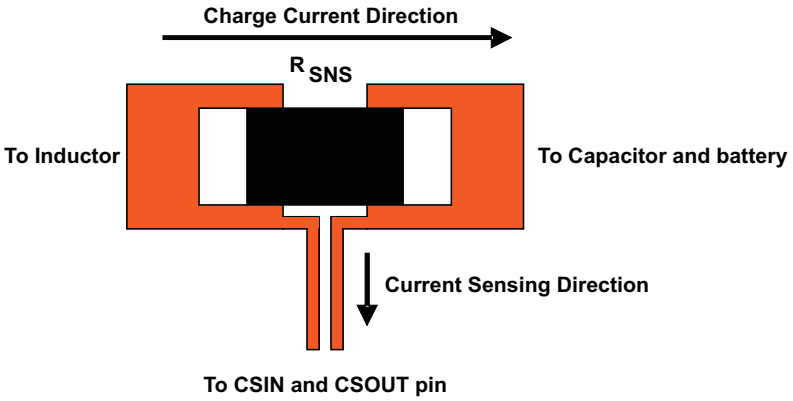
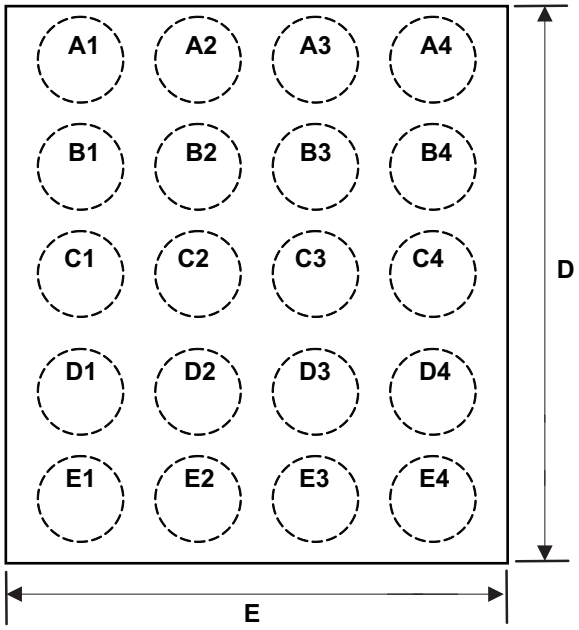


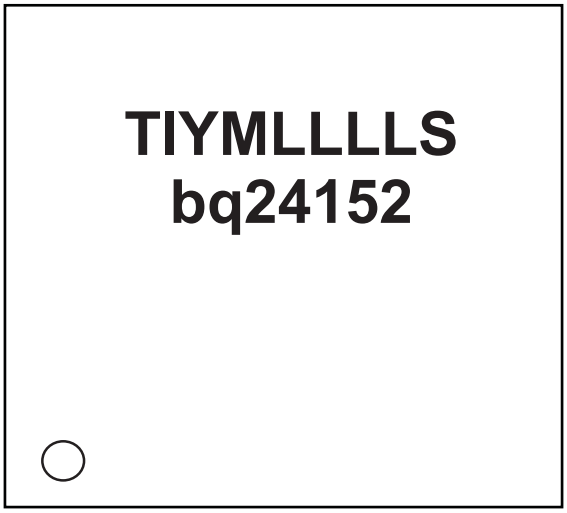
Figure 36. Sensing Resistor PCB Layout

PACKAGE SUMMARY

WCSP PACKAGE
(Top View)



CHIP SCALE PACKAGE
(Top Side Symbol For bq24152)



0-Pin A1 Marker, TI-TI Letters, YM- Year Month Date Code, LLLL-Lot Trace Code, S-Assembly Site Code

CHIP SCALE PACKAGING DIMENSIONS

The bq24152 device is available in a 20-bump chip scale package (YFF, NanoFree™). The package dimensions are:

- D = 1.976 ± 0.05 mm
- E = 1.924 ± 0.05 mm

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
BQ24152YFFR	ACTIVE	DSBGA	YFF	20	3000	Green (RoHS & no Sb/Br)	SnAgCu	Level-1-260C-UNLIM
BQ24152YFFT	ACTIVE	DSBGA	YFF	20	250	Green (RoHS & no Sb/Br)	SnAgCu	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

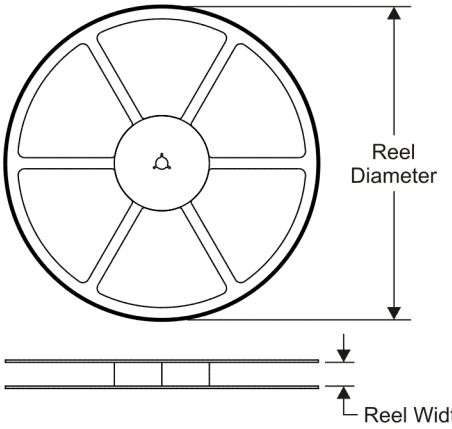
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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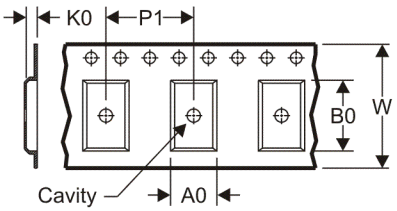
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

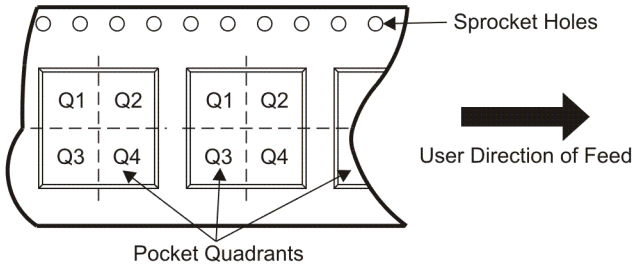


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

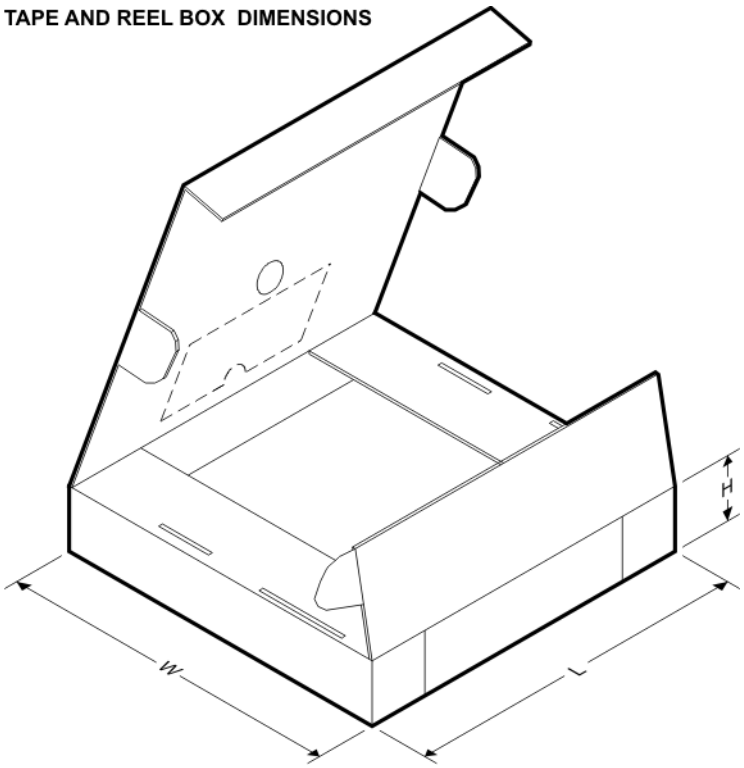
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24152YFFR	DSBGA	YFF	20	3000	178.0	8.4	2.18	2.18	0.81	4.0	8.0	Q1
BQ24152YFFT	DSBGA	YFF	20	250	178.0	8.4	2.18	2.18	0.81	4.0	8.0	Q1

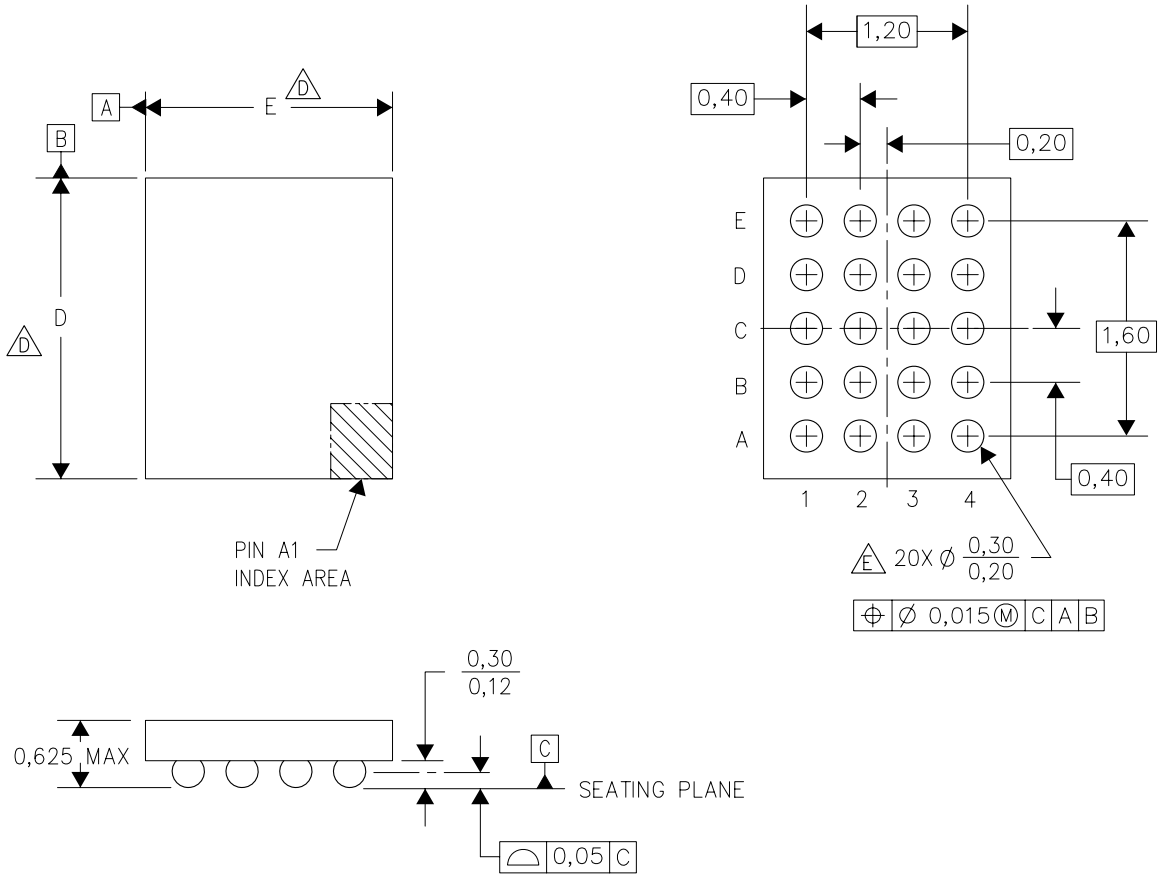
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24152YFFR	DSBGA	YFF	20	3000	217.0	193.0	35.0
BQ24152YFFT	DSBGA	YFF	20	250	217.0	193.0	35.0

YFF (R–XBGA–N20) DIE–SIZE BALL GRID ARRAY



4207625–7/L 07/08

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Devices in YFF package can have dimension D ranging from 1.96 to 2.65 mm and dimension E ranging from 1.56 to 2.25mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E. Reference Product Data Sheet for array population. 5 x 4 matrix pattern is shown for illustration only.
F. This package contains lead–free balls.

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