LOW SKEW, 1-TO-4 DIFFERENTIAL-TO-LVDS FANOUT BUFFER

ICS854S14I

General Description

The ICS854S14I is a high speed 1-to-4 Differential-to-LVDS Fanout Buffer and is a member of the HiPerClockS™ family of high performance clock solutions from IDT. The ICS854S14I is optimized for high speed and very low output skew, making it suitable for use in demanding applications such as SONET, 1 Gigabit and 10 Gigabit Ethernet, and Fibre Channel. The internally terminated differential input and V_{REF_AC} pin allow other differential signal families such as LVPECL, LVDS, and SSTL to be easily interfaced to the input with minimal use of external components. The device also has output enable pins which may be useful for system test and debug purposes.

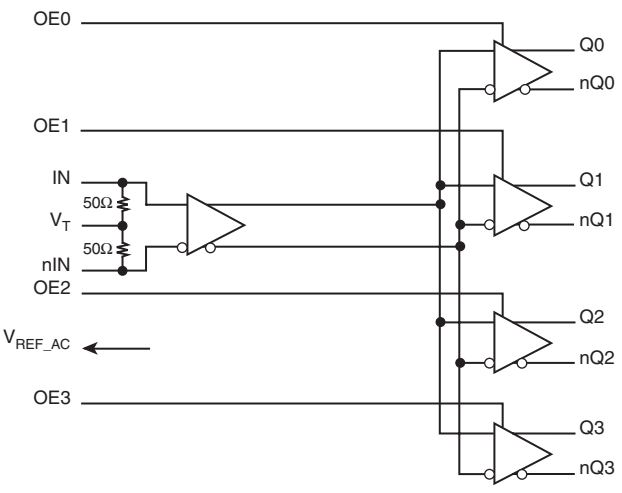
Applications:

- Processor clock distribution
- 622MHz central office clock distribution
- High speed network routing
- Wireless basestations
- Serdes LVPECL output to FPGA LVDS input translator
- Fibre channel clock distribution
- AMC clock driver for ATCA systems
- Gigabit ethernet clock distibution

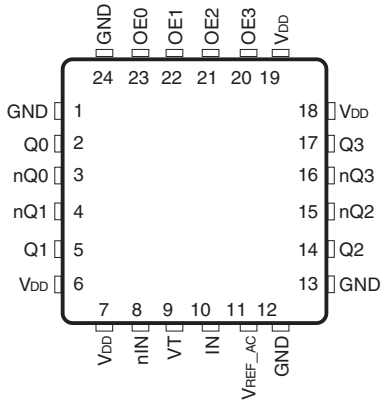
Features

- Four differential LVDS outputs
- IN, nIN pair can accept the following differential input levels: LVPECL, LVDS, SSTL
- 50Ω internal input termination to V_T
- Output frequency: 1.5GHz
- Output skew: 30ps (typical)
- Part-to-part skew: TBD
- Additive phase jitter, RMS: 0.135ps (typical)
- Propagation delay: 1.1ns (typical)
- 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS854S14I
24-Lead VFQFN
4mm x 4mm x 0.95 package body
K Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 12, 13, 24	GND	Power		Power supply ground.
2, 3	Q0, nQ0	Output		Differential output pair. LVDS interface levels.
4, 5	nQ1, Q1	Output		Differential output pair. LVDS interface levels.
6, 7, 18, 19	V_{DD}	Power		Positive supply pins.
8	nIN	Input		Inverting differential clock input. 50Ω internal input termination to V_T.
9	V_T	Input		Termination input.
10	IN	Input		Non-inverting differential clock input. 50Ω internal input termination to V_T.
11	V_{REF_AC}	Output		Reference voltage for AC-coupled applications.
14, 15	Q2, nQ2	Output		Differential output pair. LVDS interface levels.
16, 17	nQ3, Q3	Output		Differential output pair. LVDS interface levels.
20, 21, 22, 23	OE3, OE2, OE1, OE0	Input	Pullup	Active high output enable. When logic HIGH, the output pair is enabled. When logic LOW, the output pair is in a high impedance state. The OEx pins have an internal pullup resistor so the default power-up state of the outputs are enabled. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R_{PULLUP}	Input Pullup Resistor			51		kΩ

TABLE 3. OEx TRUTH TABLE

Inputs			Outputs	
IN	**nIN**	**OE0**	**Q0**	**nQ0**
0	1	1	0	1
1	0	1	1	0
X	X	0	HI-Z	HI-Z
IN	**nIN**	**OE1**	**Q1**	**nQ1**
0	1	1	0	1
1	0	1	1	0
X	X	0	HI-Z	HI-Z
IN	**nIN**	**OE2**	**Q2**	**nQ2**
0	1	1	0	1
1	0	1	1	0
X	X	0	HI-Z	HI-Z
IN	**nIN**	**OE3**	**Q3**	**nQ3**
0	1	1	0	1
1	0	1	1	0
X	X	0	HI-Z	HI-Z

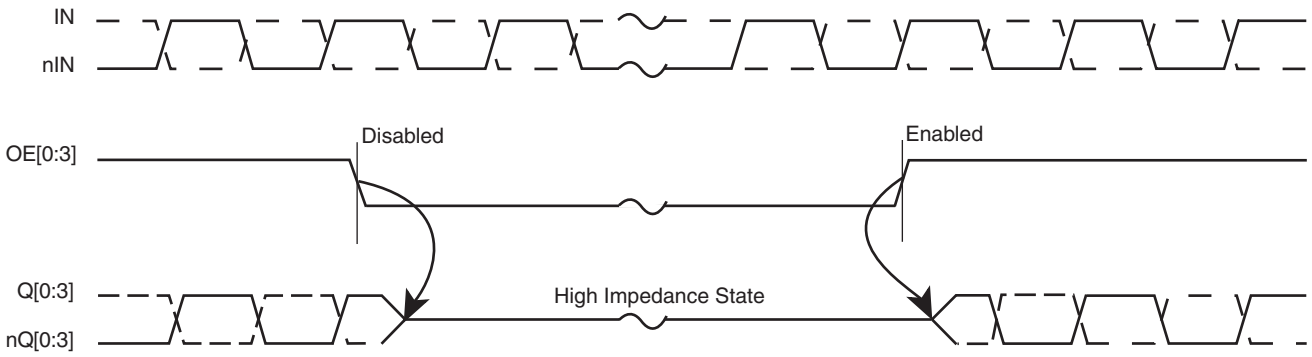


FIGURE 1. OE TIMING DIAGRAM

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, I_O (LVDS)	
Continuous Current	10mA
Surge Current	15mA
Input Current, IN, nIN	±50mA
V_T Current, I_{VT}	±100mA
Input Sink/Source, I_{REF_AC}	± 0.5mA
Operating Temperature Range, TA	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	50.2°C (0 mps)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%; TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			88		mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 2.5V ± 5%; TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			0		0.7	V
I_{IH}	Input High Current	OE[0:3]	V_{DD} = V_{IN} = 2.625V			5	µA
I_{IL}	Input Low Current	OE[0:3]	V_{DD} = 2.625V, V_{IN} = 0V	-150			µA

Table 4C. Differential DC Characteristics, V_{DD} = 2.5V ± 5%; TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
R_{IN}	Differential Input Resistance	(IN, nIN)	IN-to-VT	40	50	60	Ω
V_{IH}	Input High Voltage	(IN, nIN)		1.2		V_{DD}	V
V_{IL}	Input Low Voltage	(IN, nIN)		0		V_{IH} - 0.15	V
V_{IN}	Input Voltage Swing			0.15		2.8	V
V_{REF_AC}	Reference Voltage			V_{DD} - 1.42	V_{DD} - 1.37	V_{DD} - 1.32	V
V_{DIFF_IN}	Differential Input Voltage Swing			0.3		3.4	V
I_{IN}	Input Current; NOTE 1	(IN, nIN)				35	mA

NOTE 1: Guaranteed by design.

TABLE 4D. LVDS DC CHARACTERISTICS, V_{DD} = 2.5V ± 5%; TA = -40°C TO 85°C

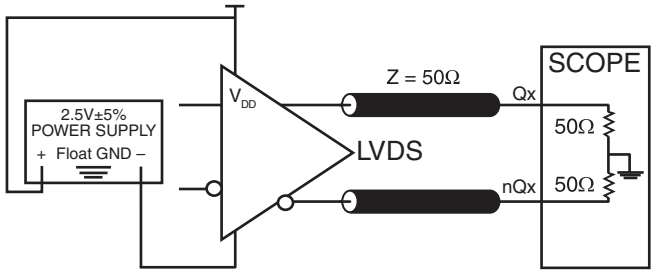
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			350		mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage			1.2		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

TABLE 5. AC CHARACTERISTICS, V_{DD} = 2.5V ± 5%; TA = -40°C TO 85°C

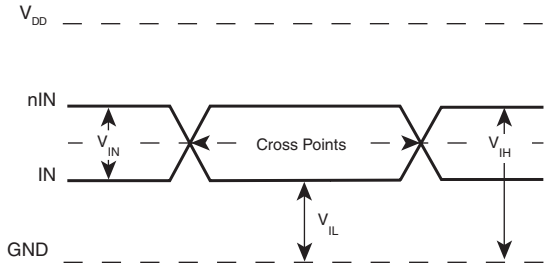
Symbol	Parameter	Condition	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency			1.5		GHz
t_{PD}	Propagation Delay; (Differential); NOTE 1			1.1		ns
*t*sk(o)	Output Skew; NOTE 2, 4			30		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			TBD		ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section	200MHz, Integration Range: 12kHz - 20MHz		0.135		ps
t_R/t_F	Output Rise/Fall Time	20% to 80%		170		ps

All parameters are measured at ≤ 1GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

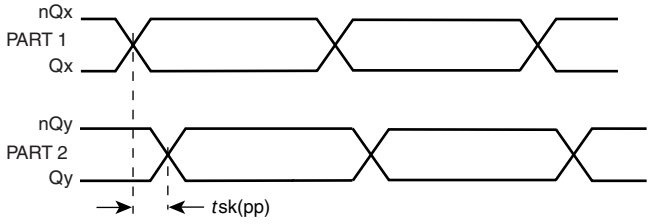
PARAMETER MEASUREMENT INFORMATION



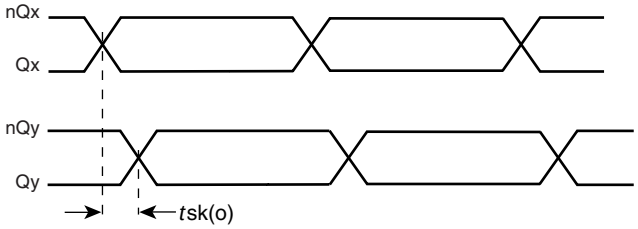
OUTPUT LOAD AC TEST CIRCUIT



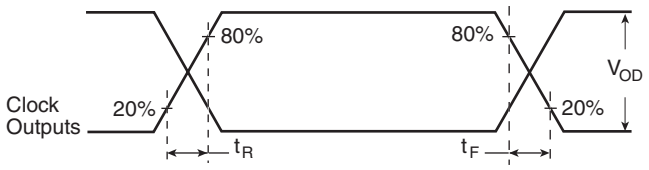
DIFFERENTIAL INPUT LEVEL



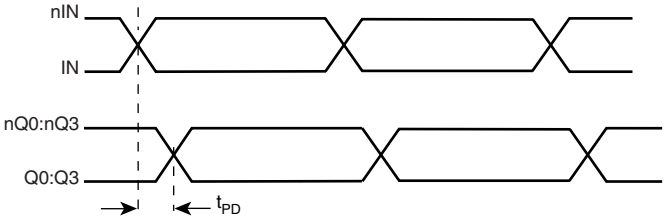
PART-TO-PART SKEW



OUTPUT SKEW



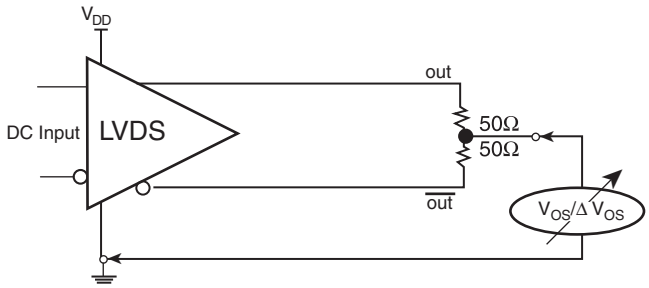
OUTPUT RISE/FALL TIME



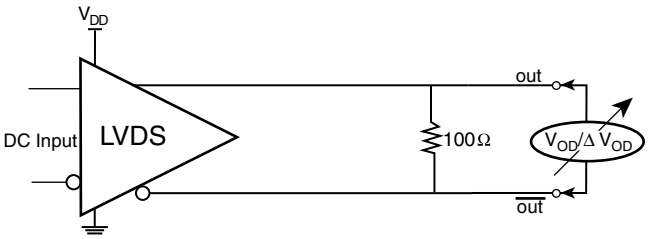
PROPAGATION DELAY



SINGLE ENDED & DIFFERENTIAL INPUT VOLTAGE SWING



OFFSET VOLTAGE SETUP



DIFFERENTIAL OUTPUT VOLTAGE SETUP

APPLICATION INFORMATION

LVPECL INPUT WITH BUILT-IN 50Ω TERMINATIONS INTERFACE

The IN /nIN with built-in 50Ω terminations accepts LVDS, LVPECL, LVHSTL, CML, SSTL and other differential signals. The signal must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2F* show interface examples for the HiPerClockS IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

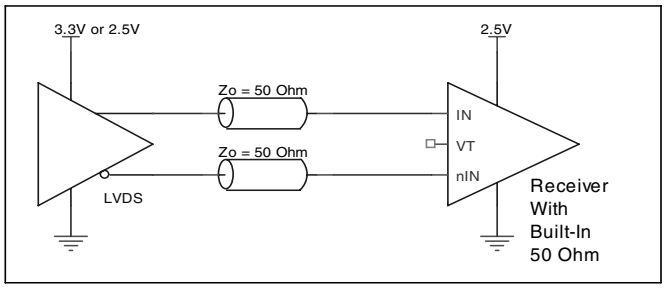


FIGURE 2A. HIPERCLOCKS IN/NIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVDS DRIVER

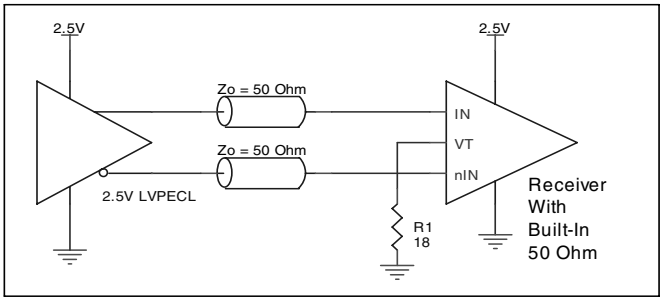


FIGURE 2B. HIPERCLOCKS IN/NIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVPECL DRIVER

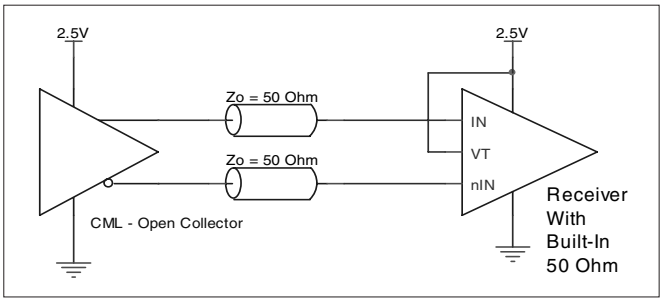


FIGURE 2C. HIPERCLOCKS IN/NIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN OPEN COLLECTOR CML DRIVER

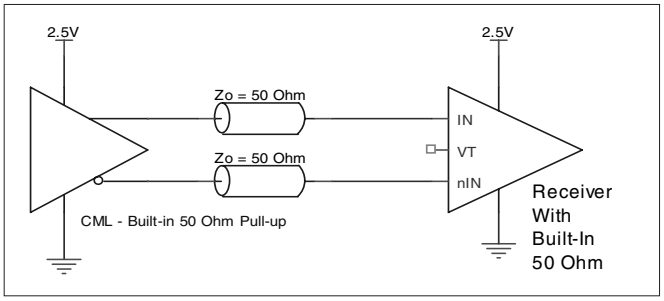


FIGURE 2D. HIPERCLOCKS IN/NIN INPUT WITH BUILT-IN 50Ω DRIVEN BY A CML DRIVER WITH BUILT-IN 50Ω PULLUP

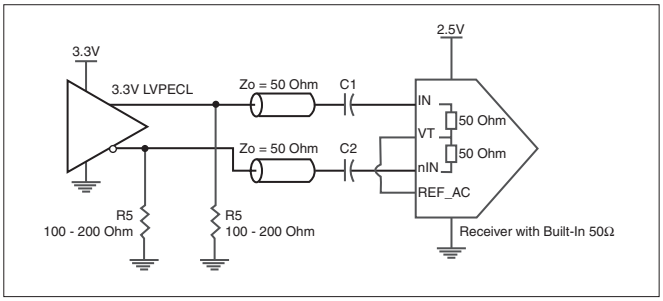


FIGURE 2E. HIPERCLOCKS IN/NIN INPUT WITH BUILT-IN 50Ω DRIVEN BY A 3.3V LVPECL DRIVER

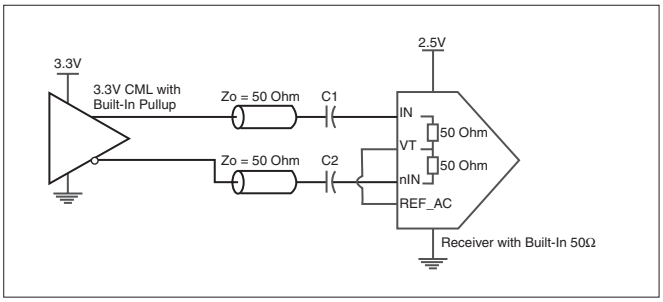


FIGURE 2F. HIPERCLOCKS IN/NIN INPUT WITH BUILT-IN 50Ω DRIVEN BY A 3.3V CML DRIVER WITH BUILT-IN PULLUP

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins:
All control pins have internal pull-ups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Output
All unused LVDS outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

2.5V LVDS Driver Termination

Figure 3 shows a typical termination for LVDS driver in characteristic impedance of 100Ω differential (50Ω single) transmission line environment. For buffer with multiple LVDS driver, it is recommended to terminate the unused outputs.

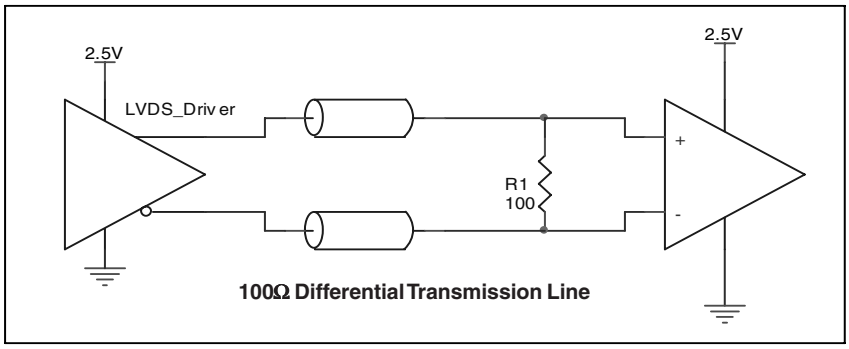


Figure 3. Typical LVDS Driver Termination

Thermal Release Path

The expose metal pad provides heat transfer from the device to the P.C. board. The expose metal pad is ground pad connected to ground plane through thermal via. The exposed pad on the device to the exposed metal pad on the PCB is contacted through solder as shown in *Figure 4.* For further information, please refer to the Application Note on Surface Mount Assembly of Amkor's Thermally /Electrically Enhance Leadframe Base Package, Amkor Technology.

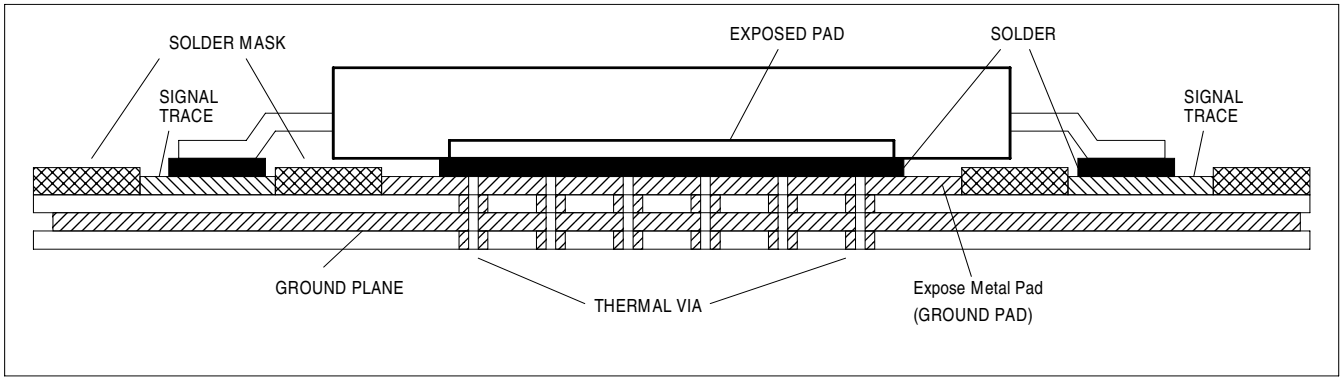


Figure 4. P.C. Board for Exposed Pad Thermal Release Path Example

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS854S14I.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS854S14I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 2.5V + 5% = 2.625V, which gives worst case results.

- Power_$_{MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 2.625V * 88mA = **231mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 43.9°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.231W * 43.9°C/W = 95.1°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 24-PIN VFQFN, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	50.2°C/W	43.9°C/W	39.3°C/W

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD VFQFN

θ_{JA} vs. 0 Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	50.2°C/W	43.9°C/W	39.3°C/W

TRANSISTOR COUNT
The transistor count for ICS854S14I is: 288

PACKAGE OUTLINE - K SUFFIX FOR 24 LEAD VFQFN

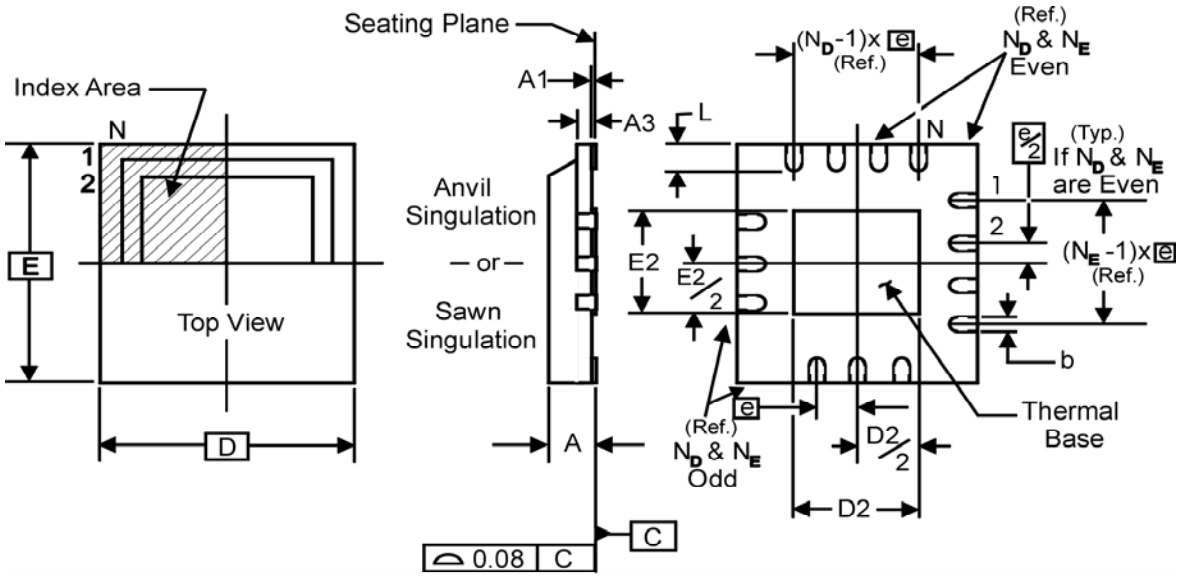


TABLE 8. PACKAGE DIMENSIONS FOR 24 LEAD VFQFN

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**MINIMUM**	**MAXIMUM**
N	24	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	6	
N_E	6	
D	4	
D2	2.30	2.55
E	4	
E2	2.30	2.55
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
854S14AKI	TBD	24 Lead VFQFN,	tube	-40°C to 85°C
854S14AKT	TBD	24 Lead VFQFN	2500 tape & reel	-40°C to 85°C
854S14AKILF	S14AIL	24 Lead "Lead-Free" VFQFN	tube	-40°C to 85°C
854S14AKILFT	S14AIL	24 Lead "Lead-Free" VFQFN	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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