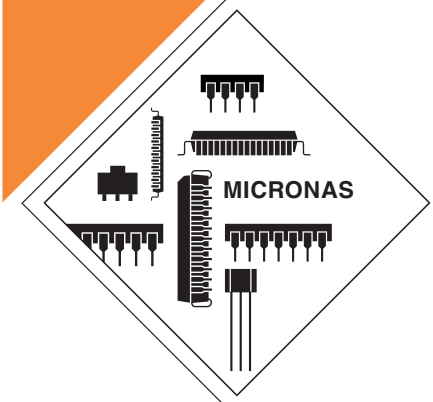


PRELIMINARY DATA SHEET

DPL 4519G
Sound Processor for Digital and Analog Surround Systems

DOLBY SURROUND PRO • LOGIC

VIRTUAL DOLBY SURROUND

Edition Oct. 31, 2000
6251-512-1PD

MICRONAS

Contents

Contents, continued

Sound Processor for Digital and Analog Surround Systems

The hardware and software description in this document is valid for the DPL 4519G version A1 and following versions.

1. Introduction

The DPL 4519G processor is designed as part of the Micronas chip set for digital and analog Surround Systems i. e. Dolby Digital, MPEG 2 Audio, or Dolby Pro-Logic. The combination of MAS 3528E, DPL 4519G, and MSP 44x0G is a complete 5.1 channel Dolby Digital decoder and playback solution, while DPL 4519G and MSP 44x0G alone, represent a complete Dolby Surround Pro Logic system.

The DPL 4519G receives its incoming data via highly flexible I^2S interfaces. The three I^2S input interfaces can be configured as three asynchronous I^2S inputs or two synchronous and one asynchronous interface. In the latter case, the asynchronous interface allows reception of 2-8 channels with arbitrary sample rate ranging from 8 to 48 kHz. The synchronization is performed by means of an adaptive high-quality sample rate converter.

In an application together with the Dolby Digital decoder MAS 3528E, eight channels (left, right, surround left, surround right, center, subwoofer, Pro Logic encoded left, Pro Logic encoded right) are fed in and processed in the DPL 4519G.

Similar to the multichannel I^2S input interface, the DPL is provided with an 8-channel I^2S output interface, which can be connected to a MSP 44x0G. Therefore all 8 channels can be routed to each output in both ICs.

The baseband processing including e.g. balance, bass, treble, and loudness is performed at a fixed sample rate of 48 kHz.

Fig. 1–1 shows a simplified functional block diagram of the DPL 4519G.

The DPL 4519G is pin-compatible to members of the MSP 34xx family. This speeds up PCB development for customers using MSPs.

The software interface of the DPL 4519G is also largely the same as for members of the MSP family.

The ICs are produced in submicron CMOS technology and are available in PQFP80, PLQFP64 and in PSDIP64 packages.

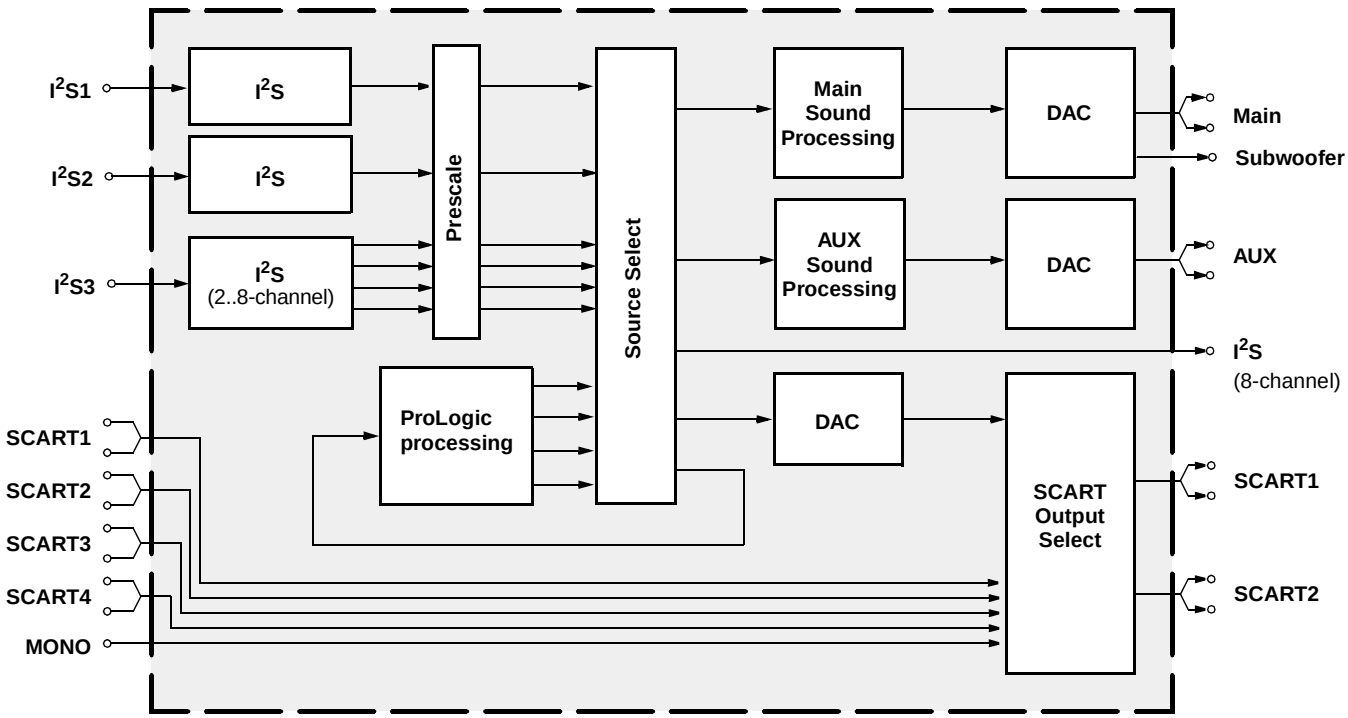


Fig. 1–1: Simplified block diagram of the DPL 4519G

1.1. Features of the DPL 4519G

– 8-channel asynchonous I^2S input interface (multichannel mode)
+ 2 synchronous I^2S input channels (e.g. for MSP and ADR)

or

3 asynchronous two-channel I^2S input interfaces

– Main and AUX channel with balance, bass, treble, loudness, volume

– 5-band graphic equalizer for Main channel

– Dolby Surround Pro Logic Adaptive Matrix

– Micronas Effect Matrix

– Micronas “3D-Panorama” virtualizer compliant to “Virtual Dolby Surround” technology

– Micronas Panorama sound mode (3D Surround sound via two loudspeakers)

– Noise Generator

– Spatial Effect for Surround

– 30-ms Surround delay

– Surround matrix control: Adaptive/Passive/Effect

– Center mode control: Normal/Phantom/Wide/Off

– Surround reproduction control: Rear speaker, Front speaker, Panorama, 3D-Panorama

– Two digital input/output pins controlled by I^2C bus

Fig. 1–2 shows a typical Dolby Digital application using DPL 4519G, MSP 4450G, and MAS 3528E.

1.2. Application Fields of the DPL 4519G

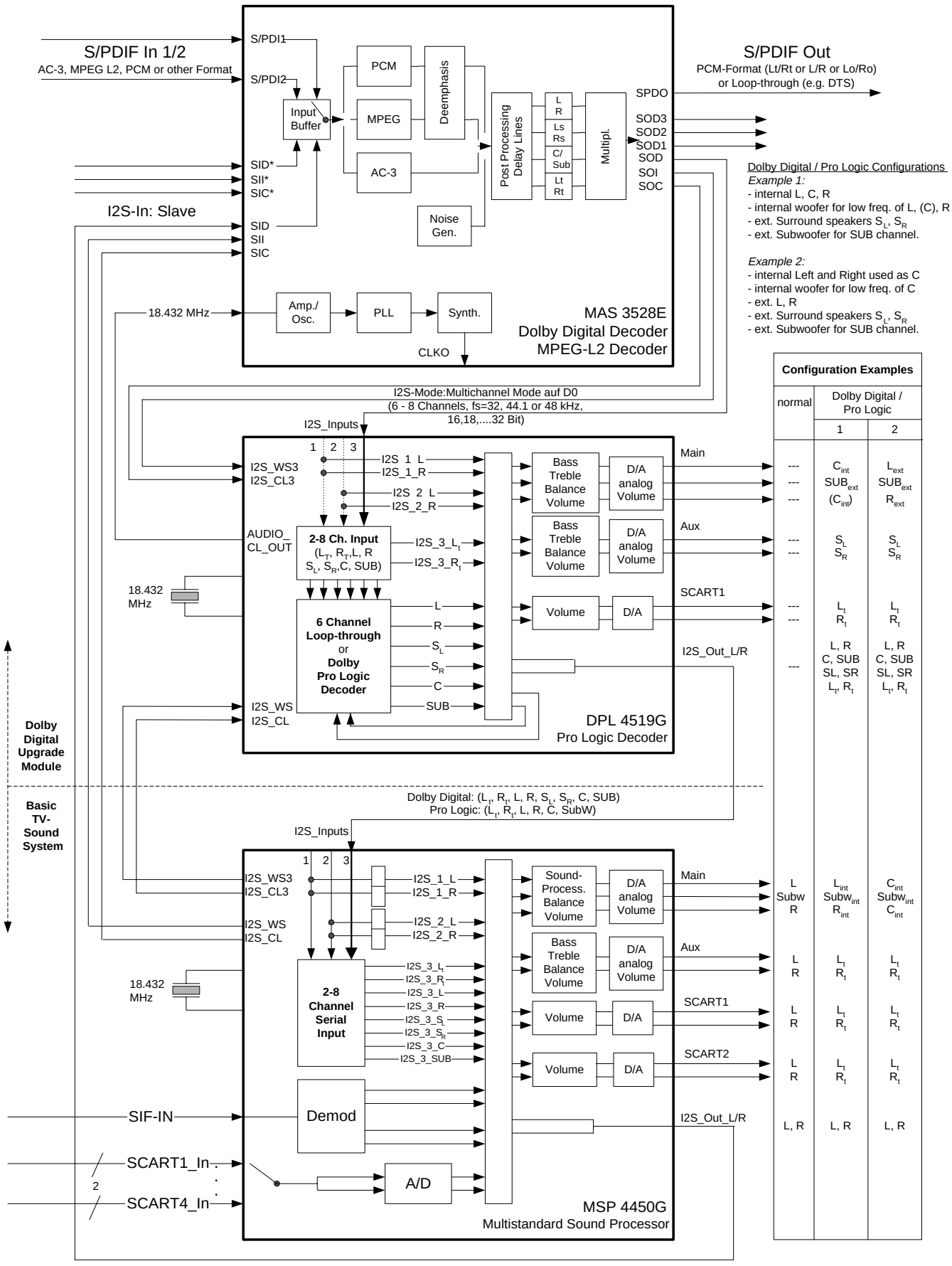


Fig. 1–2: Typical DPL 4519G application

2. Functional Description

2.1. Architecture of the DPL 4519G Family

Fig. 2–1 shows a simplified block diagram of the IC.

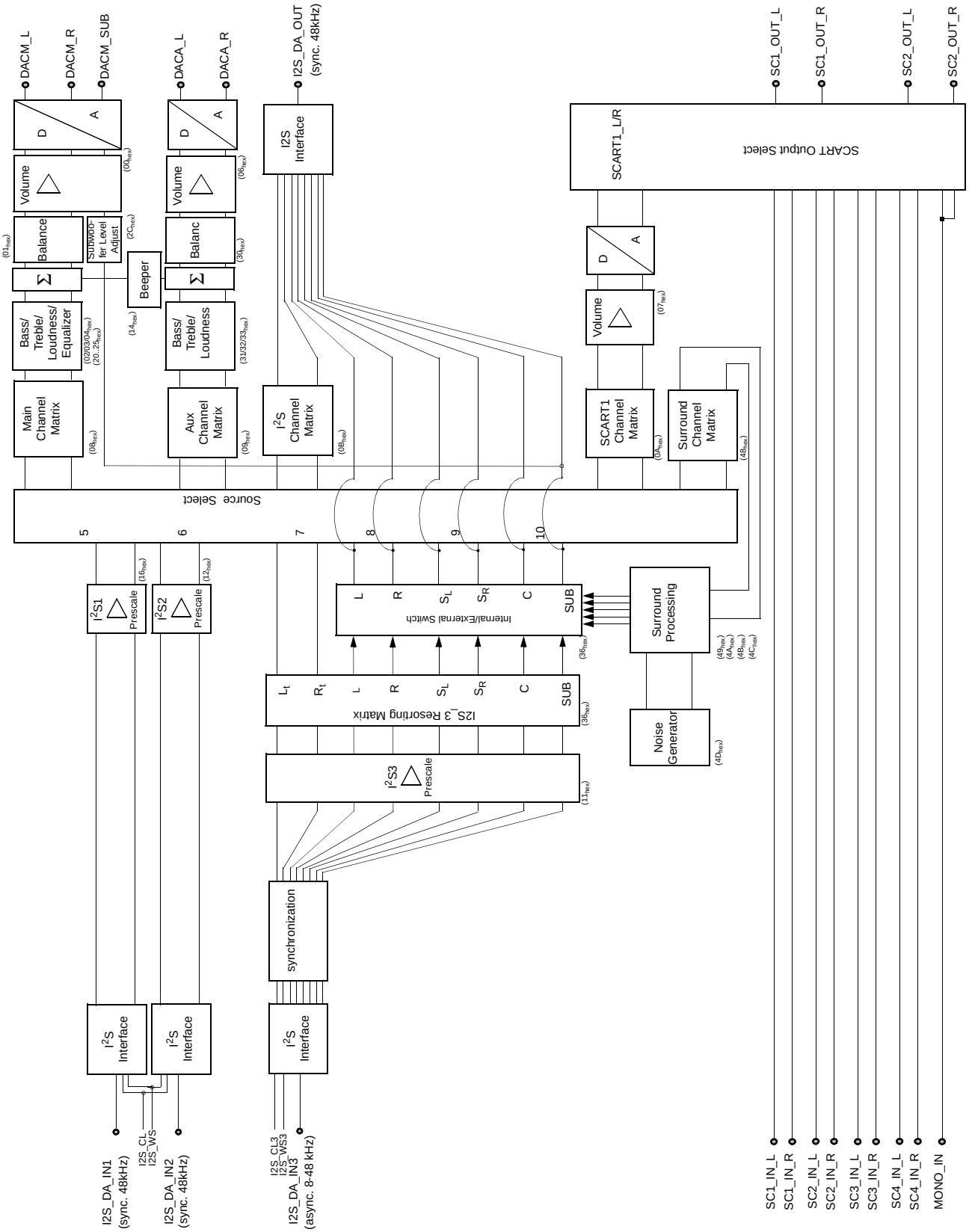


Fig. 2–1: Signal flow block diagram of the DPL 4519G (input and output names correspond to pin names)

2.2. Preprocessing I^2S Input Signals

The I^2S inputs can be adjusted in level by means of the I^2S prescale registers.

The I^2S_3 interface is able to receive more than two channels (see Section 2.6. on page 8). The incoming signals can be resorted by a programmable matrix in order to obtain a certain order, which means an unified postprocessing afterwards.

Since the I^2S_3 interface is asynchronous, incoming sound signals with arbitrary sample rates in the range of 8-48 kHz are interpolated to 48 kHz by means of an adaptive high quality sample rate converter. Therefore all subsequent processing is calculated on a fixed sampling rate, which even can be synchronized to I2S_WS e.g. to a MSP 4450 being locked to an incoming NICAM signal.

2.3. Selection of Internal Processed Surround Signals

Instead of having an multichannel input via the I^2S_3 interface, a multichannel signal can be created by an internal Dolby Pro Logic decoder. In that case channels 3..8 of the multichannel input are replaced by the internally generated signals.

2.4. Source Selection and Output Channel Matrix

The Source Selector makes it possible to distribute all source signals (I^2S input signals) to the desired output channels (Main, Aux, etc.). All input and output signals can be processed simultaneously. Each source channel is identified by a unique source address.

For each output channel, the output channel matrix can be set to sound A (left mono), sound B (right mono), stereo, or mono (sound left and right).

2.5. Audio Baseband Processing

2.5.1. Main and Aux Outputs

The following baseband features are implemented in the Main and Aux output channels: bass/treble, loudness, balance, and volume. A square wave beeper can be added to these outputs. The Main channel additionally supports an equalizer function (this is not simultaneously available with bass/treble).

2.6. Surround Processing

2.6.1. Surround Processing Mode

Surround sound processing is controlled by three functions:

The "Decoder Matrix" defines which method is used to create a multichannel signal (L, C, R, S) out of a stereo input.

The "Surround Reproduction" determines whether the surround signal “S” is fed to surround speakers. If no surround speaker is actually connected, it defines the method that is used to create surround effects.

The “Center Mode” determines how the center signal “C” is to be processed. It can be left unmodified, distributed to left and right, discarded or high pass filtered, whereby the low pass signals are distributed to left and right.

2.6.1.1. Decoder Matrix

The Decoder Matrix allows three settings:

– **ADAPTIVE:**
The Adaptive Matrix is used for Dolby Surround Pro Logic. Even sound material not encoded in Dolby Surround will produce good surround effects in this mode. The use of the Adaptive Matrix requires a license from Dolby Laboratories (See License Notice on page 3).

– **PASSIVE:**
A simple fixed matrix is used for surround sound.

– **EFFECT:**
A fixed matrix that is used for mono sound and special effects. With Adaptive or Passive Matrix no surround signal is present in case of mono, moreover in Adaptive mode even the left and right output channels carry no signal (or just low frequency signals in case of Center Mode = NORMAL). If surround sound is still required for mono signals, the Effect Matrix can be used. This forces the surround channel to be active. The Effect Matrix can be used together with 3D-PANORAMA. The result will be a pseudo stereo effect or a broadened stereo image respectively.

2.6.1.2. Surround Reproduction

Surround sound can be reproduced with four choices:

- **REAR_SPEAKER:**
  If there are any surround speakers connected to the system, this mode should be used. Useful loudspeaker combinations are (L, C, R, S) or (L, R, S).
- **FRONT_SPEAKER:**
  If there is no surround speaker connected, this mode can be used. Surround information is mixed to left and right output but without creating the illusion of a virtual speaker. It is similar to stereo but an additional center speaker can be used. This mode should be used with the Adaptive decoder Matrix only. Useful loudspeaker combinations are (L, C, R) (Note: the surround output channel is muted).
- **PANORAMA:**
  The surround information is mixed to left and right in order to create the illusion of a virtual surround speaker. Useful loudspeaker combinations are (L, C, R) or (L, R) (Note: the surround output channel is muted).
- **3D-PANORAMA:**
  Like PANORAMA with improved effect. This algorithm has been approved by the Dolby Laboratories for compliance with the "Virtual Dolby Surround" technology. Useful loudspeaker combinations are (L, C, R) or (L, R) (Note: the surround output channel is muted).

2.6.1.3. Center Modes

Four center modes are supported:

- **NORMAL:**
  small center speaker connected, L and R speakers have better bass capability. Center signal is high pass filtered.
- **WIDE:**
  L, R, and C speakers all have good bass capability.
- **PHANTOM:**
  No center speaker used. Center signal is distributed to L and R (Note: the center output channel C is muted).
- **OFF:**
  No center speaker used. Center signal C is discarded (Note: the center output channel C is muted).

2.6.1.4. Useful Combinations of Surround Processing Modes

In principle, "Decoder Matrix", "Surround Reproduction", and "Center Modes" are independent settings (all "Decoder Matrix" settings can be used with all "Surround Reproduction" and "Center Modes") but there are some combinations that do not create "good" sound. Useful combinations are

Surround Reproduction and Center Modes

- **REAR_SPEAKER:**
  This mode is used if surround speakers are available. Useful center modes are NORMAL, WIDE, PHANTOM, and OFF.
- **FRONT_SPEAKER:**
  This mode can be used if no surround speaker but a center speaker is connected. Useful center modes are NORMAL and WIDE.
- **PANORAMA or 3D-PANORAMA:**
  No surround speaker used. Two (L and R) or three (L, R, and C) loudspeakers can be used. Useful center modes are NORMAL, WIDE, PHANTOM, and OFF.

Center Modes and Decoder Matrix

- **PHANTOM:**
  Should only be used together with ADAPTIVE Decoder Matrix.
- **NORMAL and WIDE:**
  Can be used together with any Surround Decoder Matrix.
- **OFF:**
  This mode can be used together with the PASSIVE and EFFECT Decoder Matrix (no center speaker connected).

2.6.2. Examples

Table 2–1 shows some examples of how these modes can be used to configure the IC. The list is not intended to be complete, more modes are possible.

Table 2–1: Examples of Surround Configurations

Configurations	**Speaker Config-uration[1)]**	**Surround Processing Mode** Register ($4B_{hex}$)		
		Decoder Matrix [15:8]	**Surround Reproduction [7:4]**	**Center Mode [3:0]**
Stereo				
Stereo	(L,R)	–	–	–
Surround Modes as defined by Dolby Laboratories [2)]				
Dolby Surround Pro Logic	(L,C,R,S)	ADAPTIVE	REAR_ SPEAKER	NORMAL WIDE
	(L,R,S)	ADAPTIVE	REAR_ SPEAKER	PHANTOM
Dolby 3 Stereo	(L,C,R)	ADAPTIVE	FRONT_ SPEAKER	NORMAL WIDE
Virtual Dolby Surround	(L,R)	ADAPTIVE	3D_PANORAMA	PHANTOM
Surround Modes that use the Dolby Adaptive Matrix[2)]				
3-Channel Virtual Surround	(L,C,R)	ADAPTIVE	3D_PANORAMA	NORMAL WIDE
Passive Matrix Surround Sound				
4-Channel Surround	(L,C,R,S)	PASSIVE	REAR_ SPEAKER	NORMAL WIDE
3-Channel Surround	(L,R,S)	PASSIVE	REAR_ SPEAKER	OFF
2-Channel Micronas 3D Surround Sound (MSS)	(L,R)	PASSIVE	3D_PANORAMA	OFF
3-Channel Micronas 3D Surround Sound (MSS)	(L,C,R)	PASSIVE	3D_PANORAMA	NORMAL WIDE
Special Effects Surround Sound				
4-Channel Surround for mono	(L,C,R,S)	EFFECT	REAR_ SPEAKER	NORMAL WIDE
2-Channel Virtual Surround for mono	(L,R)	EFFECT	3D_PANORAMA	OFF
3-Channel Virtual Surround for mono	(L,C,R)	EFFECT	3D_PANORAMA	NORMAL WIDE

[1)] Speakers not in use are muted automatically.
[2)] The implementation in products requires a license from Dolby Laboratories Licensing Corporation (see note on page 3).

2.6.3. Application Tips for using 3D-PANORAMA

2.6.3.1. Sweet Spot

Good results are only obtained in a rather close area along the middle axis between the two loudspeakers: the sweet spot. Moving away from this position degrades the effect.

2.6.3.2. Clipping

For the test at Dolby Labs, it is very important to have no clipping effects even with worst case signals. The I^2S-prescale register has to be set to values of max 10_{hex} (16_{dec}). This is sufficient in terms of clipping.

However, it was found, that by reducing the prescale to a value lower than 16_{dec} more convincing effects are generated in case of very high dynamic signals. A value of 10_{dec} is a good compromise between overall volume and additional headroom.

Test signals: sine sweep with 0 dBFS; L only, R only, L&R equal phase, L&R anti phase.

Listening tests: Dolby Trailers (train trailer, city trailer, canyon trailer...)

2.6.3.3. Loudspeaker Requirements

The loudspeakers used and their positioning inside the TV set will greatly influence the performance of the virtualizer. The algorithm works with the direct sound path. Reflected sound waves reduce the effect. So it's most important to have as much direct sound as possible, compared to indirect sound.

To obtain the approval for a TV set, Dolby Laboratories require mounting the loudspeakers at the front of the set. Loudspeakers radiating to the side of the TV set will not produce convincing effects. Good directionality of the loudspeakers towards the listener is optimal.

The virtualizer was specially developed for implementation in TV sets. Even for rather small stereo TV's, sufficient sound effects can be obtained. For small sets, the loudspeaker placement should be to the side of the CRT; for large screen sets (or 16:9 sets), mounting the loudspeakers below the CRT is acceptable (large separation is preferred, low frequency speakers should be outmost to avoid cancellation effects). Using external loudspeakers with a large stereo base will not create optimal effects.

The loudspeakers should be able to reproduce a wide frequency range. The most important frequency range starts from 160 Hz and ranges up to 5 kHz.

Great care has to be taken with systems that use one common subwoofer: A single loudspeaker cannot reproduce virtual sound locations. The crossover frequency must be lower than 120 Hz.

2.6.3.4. Cabinet Requirements

During listening tests at Dolby Laboratories, no resonances in the cabinet should occur.

Good material to check for resonances are the Dolby Trailers or other dynamic sound tracks.

2.6.4. Input and Output Levels for Dolby Surround Pro Logic

The nominal input level (input sensitivity) for the I^2S-Inputs is –15 dBFS. The highest possible input level of 0 dBFS is accepted without internal overflow. The I^2S-prescale value should be set to values of max 0 dB (16_{dec}).

With higher prescale values lower input sensitivities can be accommodated. A higher input sensitivity is not possible, because at least 15 dB headroom is required for every input according to the Dolby specifications.

A full-scale left only input (0 dBFS) will produce a full-scale left only output (at 0 dB volume). The typical output level is 1.37 Vrms for DACM_L. The same holds true for right only signals (1.37 Vrms for DACM_R). A full-scale input level on both inputs (Lin=Rin=0 dBFS) will give a center only output with maximum level. A full-scale input level on both inputs (but Lin and Rin with inverted phases) will give a surround-only signal with maximum level.

For reproducing Dolby Pro Logic according to its specifications, the center and surround outputs must be amplified by 3 dB with respect to the L and R output signals. This can be done in two ways:

1. By implementing 3 dB more amplification for center and surround loudspeaker outputs.
2. By always selecting volume for L and R 3 dB lower than center and surround. Method 1 is preferable, as method 2 lowers the achievable SNR for left and right signals by 3 dB.

2.7. SCART Signal Routing

2.7.1. SCART Out Select

The SCART Output Select block includes full matrix switching facilities. The switches are controlled by the ACB user register (see page page 30).

2.7.2. Stand-by Mode

If the DPL 4519G is switched off by first pulling STANDBYQ low and then (after >1 µs delay) switching off DVSUP and AVSUP, but keeping AHVSUP (**'Stand-by'-mode**), the SCART switches maintain their position and function. This allows the copying from selected SCART-inputs to SCART-outputs in the TV set's stand-by mode.

In case of power on or starting from stand-by (see details on the power-up sequence in Fig. 4–19 on page 52), all internal registers except the ACB register (page 30) are reset to the default configuration (see Table 3–5 on page 17). The reset position of the ACB register becomes active after the first I^2C transmission into the Baseband Processing part (subaddress 12_{hex}). By transmitting the ACB register first, the reset state can be redefined.

2.8. I^2S Bus Interfaces

The DPL 4519G has two kinds of interfaces: synchron master/slave input/output interfaces running on 48 kHz and an asynchron slave interface.

The interfaces accept a variety of formats with different sample width, bit-orientation, and wordstrobe timing. All I^2S options are set by means of the MODUS or I^2S_CONFIG register.

2.8.1. Synchronous I^2S-Interface(s)

The synchronous I^2S bus interface consists of the pins:

– I2S_DA_IN1, I2S_DA_IN2/3 (I2S_DA_IN2 in PQFP80 package):
I^2S serial data input, 16, 18...32 bits per sample.

– I2S_DA_OUT:
I^2S serial data output, 16, 18...32 bits per sample.

– I2S_CL:
I^2S serial clock.

– I2S_WS:
I^2S word strobe signal defines the left and right sample.

If the DPL 4519G serves as the master on the I^2S interface, the clock and word strobe lines are driven by the DPL 4519G. In this mode, only 16, 32 bits per sample can be selected. In slave mode, these lines are input to the DPL 4519G and the DPL 4519G clock is synchronized to 384 times the I2S_WS rate (48 kHz). An I^2S timing diagram is shown in Fig. 4–21 on page 55.

2.8.2. Asynchronous I^2S-Interface

The asynchronous I^2S slave interface allows the reception of digital audio signals with arbitrary sample rates from 5 to 50 kHz. The synchronization is performed by means of an adaptive sample rate converter. No oversampling clock is required.

The following pins are used for the asynchronous I^2S bus interface (serve only as input):

– I2S_WS3

– I2S_CL3

– I2S_DA_IN2/3 (I2S_DA_IN3 in PQFP80 package).

The interface accepts I^2S-input streams with MSB first and with sample widths of 16,18...32 bits. With left/right alignment and wordstrobe timing polarity, there are additional parameters available for the adaption to a variety of formats in the I2S CONFIGURATION register.

2.8.3. Multichannel I^2S-Output

Bit[0:1] of the I2S CONFIGURATION register (see page 20) switches the output to 8 channel multichannel output mode. The bit resolution per channel is 32 bit in master mode. While the first two channels can be selected on the source select matrix, channels 3-8 are always connected to the I2S_3 input channels 3-8. Both, master and slave mode is possible, as long as as the wordstrobe has only one positive edge per frame in slave mode.

2.8.4. Asynchronous Multichannel I^2S-Input

The DPL 4519G supports two kinds of asynchronous multichannel input:

– the asynchronous I2S_3 interface can be switched to multichannel mode (bit [8] of the I2S CONFIGURATION register is set to 1. The number of channels must be even and less or equal eight.

– All I2S input lines (I2S_DA_IN1, I2S_DA_IN2 and I2S_DA_IN3 in PQFP80 package) can be switched to asynchronous two channel mode (bit[2] set to 1 in the I2S CONFIGURATION register). The common clock is I2S_WS3 and I2S_CL3. No synchronous I2S interfaces are available in this mode.

2.9. Digital Control I/O Pins

The static level of the digital input/output pins D_CTR_I/O_0/1 is switchable between HIGH and LOW via the I^2C-bus by means of the ACB register (see page 30). This enables the controlling of external hardware switches or other devices via I^2C-bus.

The Modus Register can set the digital input/output pins to high impedance (see page 19). So the pins can be used as input. The current state can be read out of the STATUS register (see page page 21).

2.10. Clock PLL Oscillator and Crystal Specifications

The DPL 4519G derives all internal system clocks from the 18.432 MHz oscillator. In I^2S-slave mode of the synchronous interface, the clock is phase-locked to the corresponding source.

For proper performance, the DPL clock oscillator requires a 18.432-MHz crystal. Note that for the phase-locked modes (I^2S-slave), crystals with tighter tolerance are required. The asynchronous I^2S3 slave interface uses a different locking mechanism and does not require tighter crystal tolerances.

3. Control Interface

3.1. I²C Bus Interface

3.1.1. Device and Subaddresses

The DPL 4519G is controlled via the I²C bus slave interface.

The IC is selected by transmitting one of the DPL 4519G device addresses. In order to allow up to three DPL or MSP ICs to be connected to a single bus, an address select pin (ADR_SEL) has been implemented. With ADR_SEL pulled to high, low, or left open, the DPL 4519G responds to different device addresses. A device address pair is defined as a write address and a read address (see Table 3–1).

Writing is done by sending the device write address, followed by the subaddress byte, two address bytes, and two data bytes. Reading is done by sending the write device address, followed by the subaddress byte and two address bytes. Without sending a stop condition, reading of the addressed data is completed by sending the device read address and reading two bytes of data. Refer to Section 3.1.4. for the I²C bus protocol and to Section 3.4. “Programming Tips” on page 34 for proposals of DPL 4519G I²C telegrams. See Table 3–2 for a list of available subaddresses.

Besides the possibility of hardware reset, the DPL can also be reset by means of the RESET bit in the CONTROL register by the controller via I²C bus.

Due to the internal architecture of the DPL 4519G, the IC cannot react immediately to an I²C request. The typical response time is about 0.3 ms. If the DPL cannot accept another complete byte of data until it has performed some other function (for example, servicing an internal interrupt), it will hold the clock line I2C_CL LOW to force the transmitter into a wait state. The positions within a transmission where this may happen are indicated by “Wait” in Section 3.1.4. The maximum wait period of the DPL during normal operation mode is less than 1 ms.

3.1.2. Internal Hardware Error Handling

In case of any internal hardware error (e.g. interruption of the power supply of the DPL), the DPL’s wait period is extended to 1.8 ms. After this time period elapses, the DPL releases data and clock lines.

Indicating and solving the error status:

To indicate the error status, the remaining acknowledge bits of the actual I²C-protocol will be left high. Additionally, bit[14] of CONTROL is set to one. The DPL can then be reset via the I²C bus by transmitting the reset condition to CONTROL.

Indication of reset:

Any reset, even caused by an unstable reset line etc., is indicated in bit[15] of CONTROL.

A general timing diagram of the I²C bus is shown in Fig. 4–21 on page 55.

Table 3–1: I²C Bus Device Addresses

ADR_SEL	Low (connected to DVSS)		High (connected to DVSUP)		Left Open	
Mode	**Write**	**Read**	**Write**	**Read**	**Write**	**Read**
DPL device address	80_{hex}	81_{hex}	84_{hex}	85_{hex}	88_{hex}	89_{hex}

Table 3–2: I²C Bus Subaddresses

Name	Binary Value	Hex Value	Mode	Function
CONTROL	0000 0000	00	Read/Write	Write: Software reset of DPL (see Table 3–3) Read: Hardware error status of DPL
WR_DEM	0001 0000	10	Write	write address demodulator
RD_DEM	0001 0001	11	Write	read address demodulator
WR_DSP	0001 0010	12	Write	write address DSP
RD_DSP	0001 0011	13	Write	read address DSP

3.1.3. Description of CONTROL Register

Table 3–3: CONTROL as a Write Register

Name	Subaddress	Bit[15] (MSB)	Bits[14:0]
CONTROL	00 hex	1 : RESET 0 : normal	0

Table 3–4: CONTROL as a Read Register (only DPL 4519G-versions from A2 on)

Name	Subaddress	Bit[15] (MSB)	Bit[14]	Bits[13:0]
CONTROL	00 hex	Reset status after last reading of CONTROL: 0 : no reset occured 1 : reset occured	Internal hardware status: 0 : no error occured 1 : internal error occured	not of interest
Reading of CONTROL will reset the bits[15,14] of CONTROL. After Power-on, bit[15] of CONTROL will be set; it must be read once to be resetted.				

3.1.4. Protocol Description

Write to DSP

S	write device address	Wait	ACK	sub-addr	ACK	addr-byte high	ACK	addr-byte low	ACK	data-byte-high	ACK	data-byte low	ACK	P

Read from DSP

S	write device address	Wait	ACK	sub-addr	ACK	addr-byte high	ACK	addr-byte low	ACK	S	read device address	Wait	ACK	data-byte-high	ACK	data-byte low	NAK	P

Write to Control

S	write device address	Wait	ACK	sub-addr	ACK	data-byte high	ACK	data-byte low	ACK	P

Read from Control

S	write device address	Wait	ACK	00hex	ACK	S	read device address	Wait	ACK	data-byte-high	ACK	data-byte low	NAK	P

Note: S = I^2C-Bus Start Condition from master
P = I^2C-Bus Stop Condition from master
ACK = Acknowledge-Bit: LOW on I2C_DA from slave (= DPL, light gray) or master (= controller dark gray)
NAK = Not Acknowledge-Bit: HIGH on I2C_DA from master (dark gray) to indicate ‘End of Read’ or from DPL indicating internal error state
Wait = I^2C-Clock line is held low, while the DPL is processing the I^2C command. This waiting time is max. 1 ms

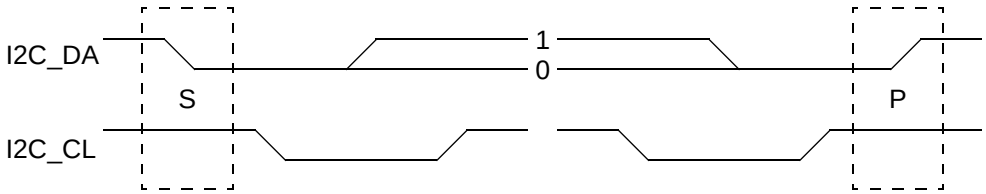


Fig. 3–1: I²C bus protocol (MSB first; data must be stable while clock is high)

3.1.5. Proposals for General DPL 4519G I²C Telegrams

3.1.5.1. Symbols

daw	write device address (80_{hex}, 84_{hex} or 88_{hex})
dar	read device address (81_{hex}, 85_{hex} or 89_{hex})
<	Start Condition
>	Stop Condition
aa	Address Byte
dd	Data Byte

3.1.5.2. Write Telegrams

<daw 00 d0 00>	write to CONTROL register
<daw 10 aa aa dd dd>	write data into demodulator
<daw 12 aa aa dd dd>	write data into DSP

3.1.5.3. Read Telegrams

<daw 00 <dar dd dd>	read data from CONTROL register
<daw 11 aa aa <dar dd dd>	read data from demodulator
<daw 13 aa aa <dar dd dd>	read data from DSP

3.1.5.4. Examples

<80 00 80 00>	RESET DPL statically
<80 00 00 00>	Clear RESET
<80 12 00 08 08 20>	Set Main channel source to I2S3 - L/R
<80 12 00 00 73 00>	Set Main volume to 0 dB

More examples of typical application protocols are listed in Section 3.4. “Programming Tips” on page 34.

3.2. Start-Up Sequence: Power-Up and I²C Controlling

After POWER ON or RESET (see Fig. 4–21), the IC is in an inactive state. All registers are in the reset position, the analog outputs are muted. The controller has to initialize all registers for which a non-default setting is necessary.

3.3. DPL 4519G Programming Interface

3.3.1. User Registers Overview

The DPL 4519G is controlled by means of user registers. The complete list of all user registers is given in the following tables. The registers are partitioned into two sections:

1. Subaddress 10_{hex} for writing, 11_{hex} for reading and
2. Subaddress 12_{hex} for writing, 13_{hex} for reading.

Write and read registers are 16-bit wide, whereby the MSB is denoted bit[15]. Transmissions via I²C bus have to take place in 16-bit words (two byte transfers, with the most significant byte transferred first). All write registers, except MODUS and I2S CONFIGURATION, are readable.

Unused parts of the 16-bit write registers must be zero. **Addresses not given in this table must not be accessed.**

Table 3–5: List of DPL 4519G Write Registers

Write Register	Address (hex)	Bits	Description and Adjustable Range	Reset	See Page
I^2C Subaddress = 10_{hex} ; Registers are *not* readable					
MODUS	00 30	[15:0]	I^2S options, D_CTR_I/O modes	00 00	19
I2S CONFIGURATION	00 40	[15:0]	Configuration of I^2S format	00 00	20
I^2C Subaddress = 12_{hex} ; Registers are *all* readable by using I^2C Subaddress = 13_{hex}					
Volume Main channel	00 00	[15:8]	[+12 dB ... –114 dB, MUTE]	MUTE	24
		[7:5] [4:0]	1/8 dB Steps must be set to 0	000_{bin} 00000_{bin}	
Balance Main channel [L/R]	00 01	[15:8]	[0...100 / 100% and 100 / 0...100%] [–127...0 / 0 and 0 / –127...0 dB]	100%/100%	25
Balance mode Main		[7:0]	[Linear / logarithmic mode]	linear mode	
Bass Main channel	00 02	[15:8]	[+20 dB ... –12 dB]	0 dB	26
Treble Main channel	00 03	[15:8]	[+15 dB ... –12 dB]	0 dB	27
Loudness Main channel	00 04	[15:8]	[0 dB ... +17 dB]	0 dB	28
Loudness filter characteristic		[7:0]	[NORMAL, SUPER_BASS]	NORMAL	
Volume Aux channel	00 06	[15:8]	[+12 dB ... –114 dB, MUTE]	MUTE	24
		[7:5] [4:0]	1/8 dB Steps must be set to 0	000_{bin} 00000_{bin}	
Volume SCART1 output channel	00 07	[15:8]	[+12 dB ... –114 dB, MUTE]	MUTE	29
Main source select	00 08	[15:8]	[I^2S1, I^2S2, I^2S3 ch1&2, I^2S3 ch3&4,...]	undefined	23
Main channel matrix		[7:0]	[SOUNDA, SOUNDB, STEREO, MONO]	SOUNDA	23
Aux source select	00 09	[15:8]	[I^2S1, I^2S2, I^2S3 ch1&2, I^2S3 ch3&4,...]	undefined	23
Aux channel matrix		[7:0]	[SOUNDA, SOUNDB, STEREO, MONO]	SOUNDA	23
SCART1 source select	00 0A	[15:8]	[I^2S1, I^2S2, I^2S3 ch1&2, I^2S3 ch3&4,...]	undefined	23
SCART1 channel matrix		[7:0]	[SOUNDA, SOUNDB, STEREO, MONO]	SOUNDA	23
I^2S source select	00 0B	[15:8]	[I^2S1, I^2S2, I^2S3 ch1&2, I^2S3 ch3&4,...]	undefined	23
I^2S channel matrix		[7:0]	[SOUNDA, SOUNDB, STEREO, MONO]	SOUNDA	23
Prescale I^2S3	00 11	[15:8]	[00_{hex} ... $7F_{hex}$]	10_{hex}	21
Prescale I^2S2	00 12	[15:8]	[00_{hex} ... $7F_{hex}$]	10_{hex}	21
ACB: SCART Switches a. D_CTR_I/O	00 13	[15:0]	Bits [15:0]	00_{hex}	30
Beeper	00 14	[15:0]	[00_{hex} ... $7F_{hex}$]/[00_{hex} ... $7F_{hex}$]	$00/00_{hex}$	30
Prescale I^2S1	00 16	[15:8]	[00_{hex} ... $7F_{hex}$]	10_{hex}	21
Mode tone control	00 20	[15:8]	[BASS/TREBLE, EQUALIZER]	BASS/TREB	26
Equalizer Main ch. band 1	00 21	[15:8]	[+12 dB ... –12 dB]	0 dB	27
Equalizer Main ch. band 2	00 22	[15:8]	[+12 dB ... –12 dB]	0 dB	27
Equalizer Main ch. band 3	00 23	[15:8]	[+12 dB ... –12 dB]	0 dB	27
Equalizer Main ch. band 4	00 24	[15:8]	[+12 dB ... –12 dB]	0 dB	27
Equalizer Main ch. band 5	00 25	[15:8]	[+12 dB ... –12 dB]	0 dB	27
Subwoofer level adjust	00 2C	[15:8]	[0 dB ... –30 dB, mute]	0 dB	29

Table 3–5: List of DPL 4519G Write Registers, continued

Write Register	Address (hex)	Bits	Description and Adjustable Range	Reset	See Page
Balance Aux channel [L/R]	00 30	[15:8]	[0...100 / 100% and 100 / 0...100%] [–127...0 / 0 and 0 / –127...0 dB]	100 %/100 %	25
Balance mode Aux		[7:0]	[Linear mode / logarithmic mode]	linear mode	
Bass Aux channel	00 31	[15:8]	[+20 dB ... –12 dB]	0 dB	26
Treble Aux channel	00 32	[15:8]	[+15 dB ... –12 dB]	0 dB	27
Loudness Aux channel	00 33	[15:8]	[0 dB ... +17 dB]	0 dB	28
Loudness filter characteristic		[7:0]	[NORMAL, SUPER_BASS]	NORMAL	
I^2S3 Resorting	00 36	[15:8]	through, straight eight, l/r eight, l/r six, l/r four, 2ch through	00_{hex}	22
Surround source select	00 48	[15:8]	[I^2S1, I^2S2, I^2S3 ch1&2, I^2S3 ch3&4,...]	undefined	23
Surround channel matrix		[7:0]	[SOUNDA, SOUNDB, STEREO, MONO]	SOUNDA	23
Spatial effect for surround processing	00 49	[15:8]	[0% - 100%]	00_{hex}	31
Virtual surround effect strength	00 4A	[15:8]	[0% - 100%]	00_{hex}	31
Decoder matrix	00 4B	[15:8]	[ADAPTIVE/PASSIVE/EFFECT]	00_{hex}	32
Surround reproduction		[7:4]	[REAR_SPEAKER/FRONT_SPEAKER/PANORAMA/ 3D_PANORAMA]	0_{hex}	32
Center mode		[3:0]	[PHANTOM/NORMAL/WIDE/OFF]	0_{hex}	32
Surround delay	00 4C	[15:0]	[5...31ms]	00_{hex}	32
Noise Generator	00 4D	[15:0]	[NOISEL, NOISEC, NOISER, NOISES]	00_{hex}	32

Table 3–6: List of DPL 4519G Read Registers

Read Register	Address (hex)	Bits	Description and Adjustable Range	See Page
I^2C Subaddress = 11_{hex} ; Registers are *not* writable				
STATUS	02 00	[15:0]	Monitoring of settings e.g. D_CTR_I/O	21
I^2C Subaddress = 13_{hex} ; Registers are *not* writable				
DPL hardware version code	00 1E	[15:8]	[00_{hex} ... FF_{hex}]	33
DPL major revision code		[7:0]	[00_{hex} ... FF_{hex}]	33
DPL product code	00 1F	[15:8]	[00_{hex} ... FF_{hex}]	33
DPL ROM version code		[7:0]	[00_{hex} ... FF_{hex}]	33

3.3.2. Description of User Registers

3.3.2.1. Write Registers on I^2C Subaddress 10_{hex}

Table 3–7: Write Registers on I^2C Subaddress 10_{hex}

Register Address	Function			Name
MODUS				
00 30_{hex}	**MODUS Register**			MODUS
	bit[15:8]	0	undefined, must be 0	
	bit[7]	0/1	active/tristate state of audio clock output pin AUD_CL_OUT	
	bit[6]		word strobe alignment (synchronous I^2S)	
		0	WS changes at data word boundary	
		1	WS changes one clock cycle in advance	
	bit[5]	0/1	master/slave mode of I^2S interface	
	bit[4]	0/1	active/tristate state of I^2S output pins	
	bit[3]		state of digital output pins D_CTR_I/O_0 and _1	
		0	active: D_CTR_I/O_0 and _1 are output pins (can be set by means of the ACB register)	
		1	tristate: D_CTR_I/O_0 and _1 are input pins (level can be read out of STATUS[4,3])	
	bit[2:0]	0	undefined, must be 0	

Table 3–7: Write Registers on I^2C Subaddress 10_{hex}, continued

Register Address	Function	Name
I2S CONFIGURATION		
00 40_{hex}	**I2S CONFIGURATION Register**	I2S_CONFIG
	I2S3[1)]	
	bit[11] I^2S data alignment (must be 0 if bit[2] = 1) 0/1 left/right aligned	I2S3_ALIGN
	bit[10] wordstrobe polarity (must be 0 if bit[2] = 1) 1 0 = right, 1 = left 0 1 = right, 0 = left	I2S3_WS_POL
	bit[9] wordstrobe alignment (asynchronous I2S_3) 0 WS changes at data word boundary 1 WS changes one clock cycle in advance	I2S3_WS_MODE
	bit[8] Sample Mode 0/1 Two/Multi sample	I2S3_MSAMP
	bit[7:4] Word length of each data packet = (n–2)/2 bit[3]=0, bit[8]=1 (multi-sample input mode) 0111 16 bit 1000 18 bit ... 1111 32 bit bit[3]=0, bit[8]=0 (two-sample input mode) xxxx 16...32 bit, 18-bit valid bit[3]=1, bit[8]=1 (multi-sample output mode) 1111 32 bit bit[3]=1, bit[8]=0 (two-sample output mode) 0111 16 bit 1111 32 bit	I2S3_MBIT
	bit[3] I^2S3 Mode 1 output (I2S3 CL/WS active) 0 input (I2S3 CL/WS tristate)	I2S3_MODE
	$I^2S1/2/3$	
	bit[2] $I^2S1/2/3$ Timing 1 I^2S3 timing for all I^2S inputs (1/2/3) 0 default mode	I2S_TIMING
	I^2S Out	
	bit[1:0] I2S_CL frequency and I2S_DA_OUT sample length 00 2 * 16 bit (1.536 MHz Clk) 01 2 * 32 bit (3.072 MHz Clk) 10 8 * 32 bit (12.288 MHz Clk)	

1) I2S_CL3 frequency depends on bit[8] and bits[7:4] as follows:
[8] = 0, [7:4] = 0111 f = fs*(2*16)
[8] = 0, [7:4] = else f = fs*(2*32)
[8] = 1 f = fs*(8*32)

3.3.2.2. Read Registers on I²C Subaddress 11_{hex}

Table 3–8: Read Registers on I²C Subaddress 11_{hex}

Register Address	Function			Name
02 00_{hex}	**STATUS Register** Contains the status of the D_CTR_I/O pins bit[15:5] bit[4] bit[3] bit[2:0]	 0/1 0/1 	 undefined low/high level of digital I/O pin D_CTR_I/O_1 low/high level of digital I/O pin D_CTR_I/O_0 undefined	STATUS

3.3.2.3. Write Registers on I²C Subaddress 12_{hex}

Table 3–9: Write Registers on I²C Subaddress 12_{hex}

Register Address	Function			Name
PREPROCESSING				
00 16_{hex} 00 12_{hex} 00 11_{hex}	**I2S1 Prescale** **I2S2 Prescale** **I2S3 Prescale** Defines the prescale value for digital I²S input signals bit[15:8]	 00_{hex} 10_{hex} $7F_{hex}$	 off 0 dB gain (recommendation) +18 dB gain (maximum gain)	PRE_I2S1 PRE_I2S2 PRE_I2S3

Table 3–9: Write Registers on I^2C Subaddress 12_{hex}, continued

Register Address	Function	Name
I2S3 RESORTING MATRIX		
00 36_{hex}	**I2S3 Resorting Matrix** (not mentioned bit combinations must not be used) Resorting of multichannel inputs bit[15:8] 0000_{hex} : 8 channel, “through” 1,2,3,4,5,6,7,8 → 1,2,3,4,5,6,7,8 L_t,R_t → L_t,R_t,--,--,--,--,--,-- L_t,R_t,$L_{virtual}$,$R_{virtual}$ → L_t,R_t,$L_{virtual}$,$R_{virtual}$,--,--,--,-- 0001_{hex} : 8 channel, “straight eight” 1,2,3,4,5,6,7,8 → 7,8,1,2,3,4,5,6 L,R,S_L,S_R,C,LFE,L_t,R_t → L_t,R_t,L,R,S_L,S_R,C,LFE 0002_{hex} : 8 channel, “left/right eight”, “MAS 3528E” 1,2,3,4,5,6,7,8 → 4,8,1,5,2,6,3,7 L,S_L,C,L_t,R,S_R,LFE,R_t → L_t,R_t,L,R,S_L,S_R,C,LFE 0003_{hex} : 6 channel, “left/right six” 1,2,3,4,5,6 → -,-,1,4,2,5,3,6 L,S_L,C,R,S_R,LFE → --,--,L,R,S_L,S_R,C,LFE 0004_{hex} : 4 channel, “left/right four”, ”External ProLogic” 1,2,3,4 → -,-,1,3,4,4,2,- L,C,R,S → --,--,L,R,S_L,S_R,C,-- 0010_{hex} : 2 channel, “through”; “Internal ProLogic” 1,2 → 1,2,+,+,+,+,+,+ L_t,R_t → L_t,R_t,L_{PL},R_{PL},S_{PL},S_{PL},C_{PL},SUB_{PL} “+”: channel will be replaced by internally generated signal “X_{PL}”: internally generated signal	I2S3_Sort

Table 3–9: Write Registers on I^2C Subaddress 12_{hex}, continued

Register Address	Function	Name
SOURCE SELECT AND OUTPUT CHANNEL MATRIX		
00 08_{hex} 00 09_{hex} 00 $0A_{hex}$ 00 $0B_{hex}$ 00 48_{hex}	**Source for:** **Main Output** **Aux Output** **SCART1 DA Output** **I^2S Output** **Surround Processing** bit[15:8] 5 I^2S1 input 6 I^2S2 input 7 I^2S3 input channels 1&2 (e.g. Lt,Rt)[1)] 8 I^2S3 input channels 3&4 (e.g. L,R)[1)] or Pro Logic processed L, R 9 I^2S3 input channels 5&6 (e.g. SL,SR)[1)] or Pro Logic processed S, S (both channels same signal) 10 I^2S3 input channels 7&8 (e.g. C,SUB)[1)] or Pro Logic processed C, SUB [1)] exemplary channel assignment in a Micronas digital multichannel sound system with MAS 3528E and MSP 4450G.	SRC_MAIN SRC_AUX SRC_SCART1 SRC_I2S SRC_DPL
00 08_{hex} 00 09_{hex} 00 $0A_{hex}$ 00 $0B_{hex}$ 00 48_{hex}	**Channel Matrix for:** **Main Output** **Aux Output** **SCART1 DA Output** **I^2S Output** **Surround Processing** bit[7:0] 00_{hex} Sound A Mono (or Left Mono) 10_{hex} Sound B Mono (or Right Mono) 20_{hex} Stereo (transparent mode) 30_{hex} Mono (L+R)/2 Usually the matrix modes should be set to “Stereo” (transparent).	MAT_MAIN MAT_AUX MAT_SCART1 MAT_I2S MAT_DPL

Table 3–9: Write Registers on I^2C Subaddress 12_{hex}, continued

Register Address	Function	Name
MAIN AND AUX PROCESSING		
00 00_{hex} 00 06_{hex}	**Volume Main** **Volume Aux** bit[15:8] volume table with 1 dB step size $7F_{hex}$ +12 dB (maximum volume) $7E_{hex}$ +11 dB ... 74_{hex} +1 dB 73_{hex} 0 dB 72_{hex} –1 dB ... 02_{hex} –113 dB 01_{hex} –114 dB 00_{hex} Mute (reset condition) FF_{hex} Fast Mute bit[7:5] higher resolution volume table 0 +0 dB 1 +0.125 dB increase in addition to the volume table ... 7 +0.875 dB increase in addition to the volume table bit[4:0] not used must be set to 0 With large scale input signals, positive volume settings may lead to signal clipping. The DPL 4519G Main and Aux Volume function is divided into a digital and an analog section. With Fast Mute, volume is reduced to mute position by digital volume only. Analog volume is not changed. This reduces any audible DC plops. To turn volume on again, the volume step that has been used before Fast Mute was activated must be transmitted.	VOL_MAIN VOL_AUX

Table 3–9: Write Registers on I^2C Subaddress 12_{hex}, continued

Register Address	Function	Name
00 01_{hex} 00 30_{hex}	**Balance Main Channel** **Balance Aux Channel** bit[15:8] Linear Mode $7F_{hex}$ Left muted, Right 100% $7E_{hex}$ Left 0.8%, Right 100% ... 01_{hex} Left 99.2%, Right 100% 00_{hex} Left 100%, Right 100% FF_{hex} Left 100%, Right 99.2% ... 82_{hex} Left 100%, Right 0.8% 81_{hex} Left 100%, Right muted bit[15:8] Logarithmic Mode $7F_{hex}$ Left –127 dB, Right 0 dB $7E_{hex}$ Left –126 dB, Right 0 dB ... 01_{hex} Left –1 dB, Right 0 dB 00_{hex} Left 0 dB, Right 0 dB FF_{hex} Left 0 dB, Right –1 dB ... 81_{hex} Left 0 dB, Right –127 dB 80_{hex} Left 0 dB, Right –128 dB bit[3:0] Balance Mode 0_{hex} linear 1_{hex} logarithmic Positive balance settings reduce the left channel without affecting the right channel; negative settings reduce the right channel leaving the left channel unaffected.	BAL_MAIN BAL_AUX

Table 3–9: Write Registers on I^2C Subaddress 12_{hex}, continued

Register Address	Function	Name
00 20_{hex}	**Tone Control Mode Main Channel** bit[15:8] 00_{hex} bass and treble is active FF_{hex} equalizer is active Defines whether Bass/Treble or Equalizer is activated for the Main channel. Bass/Treble and Equalizer cannot work simultaneously. If Equalizer is used, Bass and Treble coefficients must be set to zero and vice versa.	TONE_MODE
00 02_{hex} 00 31_{hex}	**Bass Main Channel** **Bass Aux Channel** bit[15:8] normal range 60_{hex} +12 dB 58_{hex} +11 dB ... 08_{hex} +1 dB 00_{hex} 0 dB $F8_{hex}$ –1 dB ... $A8_{hex}$ –11 dB $A0_{hex}$ –12 dB bit[15:8] extended range $7F_{hex}$ +20 dB 78_{hex} +18 dB 70_{hex} +16 dB 68_{hex} +14 dB Higher resolution is possible: an LSB step in the normal range results in a gain step of about 1/8 dB, in the extended range about 1/4 dB. With positive bass settings, internal clipping may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set bass to a value that, in conjunction with volume, would result in an overall positive gain.	BASS_MAIN BASS_AUX

Table 3–9: Write Registers on I^2C Subaddress 12_{hex}, continued

Register Address	Function	Name
00 03_{hex} 00 32_{hex}	**Treble Main Channel** **Treble Aux Channel** bit[15:8] 78_{hex} +15 dB 70_{hex} +14 dB ... 08_{hex} +1 dB 00_{hex} 0 dB $F8_{hex}$ –1 dB ... $A8_{hex}$ –11 dB $A0_{hex}$ –12 dB Higher resolution is possible: an LSB step results in a gain step of about 1/8 dB. With positive treble settings, internal clipping may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set treble to a value that, in conjunction with volume, would result in an overall positive gain.	TREB_MAIN TREB_AUX
00 21_{hex} 00 22_{hex} 00 23_{hex} 00 24_{hex} 00 25_{hex}	**Equalizer Main Channel Band 1 (below 120 Hz)** **Equalizer Main Channel Band 2 (center: 500 Hz)** **Equalizer Main Channel Band 3 (center: 1.5 kHz)** **Equalizer Main Channel Band 4 (center: 5 kHz)** **Equalizer Main Channel Band 5 (above: 10 kHz)** bit[15:8] 60_{hex} +12 dB 58_{hex} +11 dB ... 08_{hex} +1 dB 00_{hex} 0 dB $F8_{hex}$ –1 dB ... $A8_{hex}$ –11 dB $A0_{hex}$ –12 dB Higher resolution is possible: an LSB step results in a gain step of about 1/8 dB. With positive equalizer settings, internal clipping may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set equalizer bands to a value that, in conjunction with volume, would result in an overall positive gain.	EQUAL_BAND1 EQUAL_BAND2 EQUAL_BAND3 EQUAL_BAND4 EQUAL_BAND5

Table 3–9: Write Registers on I^2C Subaddress 12_{hex}, continued

Register Address	Function	Name
00 04_{hex} 00 33_{hex}	**Loudness Main Channel** **Loudness Aux Channel** bit[15:8] Loudness Gain 44_{hex} +17 dB 40_{hex} +16 dB ... 04_{hex} +1 dB 00_{hex} 0 dB bit[7:0] Loudness Mode 00_{hex} normal (constant volume at 1 kHz) 04_{hex} Super Bass (constant volume at 2 kHz) Higher resolution of Loudness Gain is possible: An LSB step results in a gain step of about 1/4 dB. Loudness increases the volume of low- and high-frequency signals, while keeping the amplitude of the 1-kHz reference frequency constant. The intended loudness has to be set according to the actual volume setting. Because loudness introduces gain, it is not recommended to set loudness to a value that, in conjunction with volume, would result in an overall positive gain. The corner frequency for bass amplification can be set to two different values. In Super Bass mode, the corner frequency is shifted up. The point of constant volume is shifted from 1 kHz to 2 kHz.	LOUD_MAIN LOUD_AUX

Table 3–9: Write Registers on I^2C Subaddress 12_{hex}, continued

Register Address	Function	Name
00 $2C_{hex}$	**Subwoofer Level Adjustment** bit[15:8] 00_{hex} 0 dB FF_{hex} –1 dB ... $E3_{hex}$ –29 dB $E2_{hex}$ –30 dB ... 80_{hex} Mute	SUBW_LEVEL
SCART OUTPUT CHANNEL		
00 07_{hex}	**Volume SCART1 Output Channel** bit[15:8] volume table with 1 dB step size $7F_{hex}$ +12 dB (maximum volume) $7E_{hex}$ +11 dB ... 74_{hex} +1 dB 73_{hex} 0 dB 72_{hex} –1 dB ... 02_{hex} –113 dB 01_{hex} –114 dB 00_{hex} Mute (reset condition) bit[7:5] higher resolution volume table 0 +0 dB 1 +0.125 dB increase in addition to the volume table ... 7 +0.875 dB increase in addition to the volume table bit[4:0] 01_{hex} this must be 01_{hex}	VOL_SCART1

Table 3–9: Write Registers on I^2C Subaddress 12_{hex}, continued

Register Address	Function	Name
SCART SWITCHES AND DIGITAL I/O PINS		
00 13_{hex}	**ACB Register** Defines the level of the digital output pins and the position of the SCART switches bit[15] 0/1 low/high of digital output pin D_CTR_I/O_1 (MODUS[3]=0) bit[14] 0/1 low/high of digital output pin D_CTR_I/O_0 (MODUS[3]=0) bit[13:5] SCART1 Output Select xx00xx x0x SCART3 input to SCART1 output (RESET position) xx01xx x0x SCART2 input to SCART1 output xx10xx x0x MONO input to SCART1 output xx11xx x0x SCART1 DA to SCART1 output xx01xx x1x SCART1 input to SCART1 output xx10xx x1x SCART4 input to SCART1 output xx11xx x1x mute SCART1 output bit[13:5] SCART2 Output Select 00xxxx 0xx SCART1 DA to SCART2 output (RESET position) 01xxxx 0xx SCART1 input to SCART2 output 10xxxx 0xx MONO input to SCART2 output 01xxxx 1xx SCART2 input to SCART2 output 10xxxx 1xx SCART3 input to SCART2 output 11xxxx 1xx SCART4 input to SCART2 output 11xxxx 0xx mute SCART2 output The RESET position becomes active at the time of the first write transmission on the control bus to the audio processing part. By writing to the ACB register first, the RESET state can be redefined.	ACB_REG
BEEPER		
00 14_{hex}	**Beeper Volume and Frequency** bit[15:8] Beeper Volume 00_{hex} off $7F_{hex}$ maximum volume bit[7:0] Beeper Frequency 01_{hex} 16 Hz (lowest) 40_{hex} 1 kHz FF_{hex} 4 kHz	BEEPER

Table 3–9: Write Registers on I^2C Subaddress 12_{hex}, continued

Register Address	Function	Name
SURROUND PROCESSING		
00 49_{hex}	**Spatial Effects for Surround Processing** bit[15:8] Spatial Effect Strength $7F_{hex}$ Enlargement 100% $3F_{hex}$ Enlargement 50% ... 01_{hex} Enlargement 1.5% 00_{hex} Effect off bit[7:0] 00_{hex} must be 0 Increases the perceived basewidth of the reproduced left and right front channels. Recommended value: 50% = 40_{hex}.	SUR_SPAT
00 $4A_{hex}$	**Virtual Surround Effect Strength** bit[15:8] Virtual Surround Effect Strength $7F_{hex}$ Effect 100% $3F_{hex}$ Effect 50% ... 01_{hex} Effect 1.5% 00_{hex} Effect off bit[7:0] 00_{hex} must be 0 Strength of the surround effect in PANORAMA or 3D-PANORAMA mode. In other Surround Reproduction Modes this value must be set to 0. Recommended value: 66% = 54_{hex}.	SUR_3DEFF

Table 3–9: Write Registers on I^2C Subaddress 12_{hex}, continued

Register Address	Function	Name
00 $4B_{hex}$	**Surround Processing Mode**	SUR_MODE
	bit[15:8] Decoder Matrix	DEC_MAT
	00_{hex} ADAPTIVE (for Dolby Surround Pro Logic and Virtual Surround)	
	10_{hex} PASSIVE (for MSS, Micronas Surround Sound)	
	20_{hex} EFFECT (used for special effects and monophonic signals)	
	bit[7:4] Surround Reproduction	SUR_REPRO
	0_{hex} REAR_SPEAKER: The surround signal is reproduced by rear speakers.	
	3_{hex} FRONT_SPEAKER: The surround signal is redirected to the front channels. There is no physical rear speaker connected.	
	5_{hex} PANORAMA: The surround signal is processed and redirected to the left and right front speakers in order to create the illusion of a virtual rear speaker, although no physical rear speaker is connected.	
	6_{hex} 3D-PANORAMA: The surround signal is processed and redirected to the left and right front speakers in order to create the illusion of a virtual rear speaker, although no physical rear speaker is connected.	
	bit[3:0] Center Mode	C_MODE
	0_{hex} PHANTOM mode (no Center speaker connected)	
	1_{hex} NORMAL mode (small Center speaker)	
	2_{hex} WIDE mode (large Center speaker)	
	3_{hex} OFF mode (Center output of the Surround Decoder is discarded. Useful only in special effect modes)	
00 $4C_{hex}$	**Surround Delay**	SUR_DELAY
	bit[15:8] 05_{hex} 5 ms delay in surround path (lowest)	
	06_{hex} 6 ms delay in surround path	
	...	
	$1F_{hex}$ 31 ms delay in surround path (highest))	
	bit[7:0] 00_{hex} must be 0	
	For Dolby Surround Pro Logic designs, only 20 ms fixed or 15-30 ms variable delay must be used. This register has no effect in 3D-PANORAMA and PANORAMA mode.	
00 $4D_{hex}$	**Noise Generator**	SUR_NOISE
	bit[15:8] 00_{hex} Noise generator off	
	80_{hex} Noise generator on	
	bit[7:0] $A0_{hex}$ Noise on left channel	
	$B0_{hex}$ Noise on center channel	
	$C0_{hex}$ Noise on right channel	
	$D0_{hex}$ Noise on surround channel	
	Determines the active channel for the noise generator.	

3.3.2.4. Read Registers on I^2C Subaddress 13_{hex}

Table 3–10: Read Registers on I^2C Subaddress 13_{hex}

Register Address	Function	Name
DPL 4519G VERSION READOUT Registers		
00 $1E_{hex}$	**DPL Hardware Version Code** bit[15:8] 01_{hex} DPL 4519G-**A**1 A change in the hardware version code defines hardware optimizations that may have influence on the chip's behavior. The readout of this register is identical to the hardware version code in the chip's imprint. **DPL Family Code** bit[7:4] 3_{hex} **DPL 45**19G-A1 **DPL Major Revision Code** bit[3:0] 7_{hex} DPL 4519**G**-A1	DPL_HARD DPL_FAMILY DPL_REVISION
00 $1F_{hex}$	**DPL Product Code** bit[15:8] 13_{hex} DPL 45**19**G - A1 By means of the DPL-Product Code, the control processor is able to decide which TV sound standards have to be considered. **DPL ROM Version Code** bit[7:0] 41_{hex} DPL 4519G - A**1** 42_{hex} DPL 4519G - A**2** A change in the ROM version code defines internal software optimizations, that may have influence on the chip's behavior, e.g. new features may have been included. While a software change is intended to create no compatibility problems, customers that want to use the new functions can identify new DPL 4519G versions according to this number.	DPL_PRODUCT DPL_ROM

3.4. Programming Tips

This section describes the preferred method for initializing the DPL 4519G. The initialization is grouped into four sections: analog signal path, input processing for I^2S, and output processing. See Fig. 2–1 on page 7 for a complete signal flow.

SCART Signal Path

1. Select the source for each analog SCART output with the ACB register.

I^2S Inputs

1. Select preferred prescale for I^2S inputs (set to 0 dB after RESET).
2. Select I2S3 Resorting matrix according to the channel order of your decoding device (e.g. for MAS 3528E chose mode 02_{hex})

Output Channels

1. Select the source channel and matrix for each output.
2. Set audio baseband features
3. Select volume for each output.

3.5. Examples of Minimum Initialization Codes

Initialization of the DPL 4519G according to these listings reproduces sound of the selected standard on the Main output. All numbers are hexadecimal. The examples have the following structure:

1. Perform an I^2C controlled reset of the IC.
2. Write MODUS register
3. Set Source Selection for Main channel (with matrix set to STEREO).
4. Set Volume Main channel to 0 dB.

3.5.1. Micronas Dolby Digital chipset (with MAS 3528E)

```
<84  00  80 00>          // Softreset
<84  00  00 00>
<84  10  00 30  00 20>   // MODUS-Register: I2S slave
<84  10  00 40  01 F2>   // I2S-config-Register
<84  12  00 36  00 02>   // I2S3 Resorting matrix, Mode 2
<84  12  00 0B  07 20>   // Source Sel. I2S_out = I2S3 - Lt/Rt
<84  12  00 08  08 20>   // Source Sel. Main_out = I2S3 - L/R
<84  12  00 00  73 00>   // Main Volume 0 dB
```

4. Specifications

4.1. Outline Dimensions

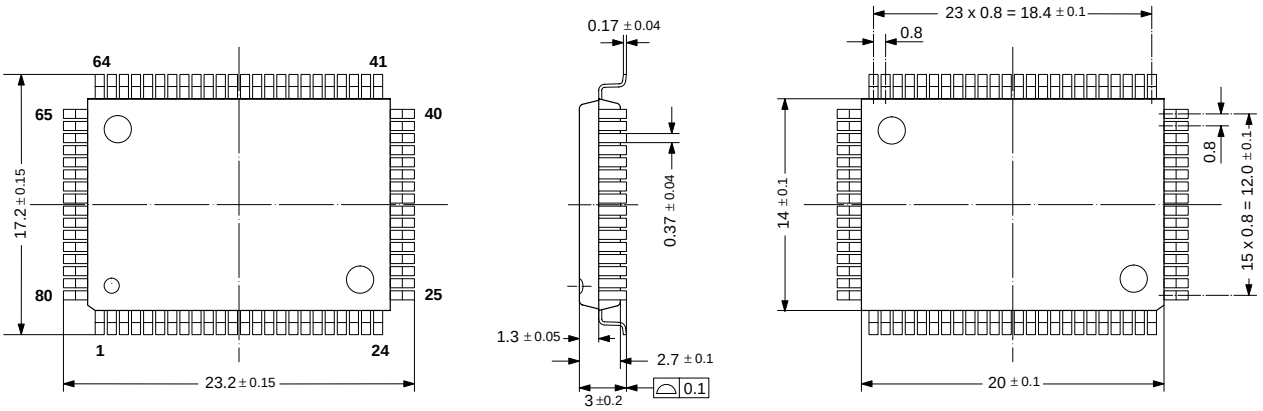


Fig. 4–1:
80-Pin Plastic Quad Flat Pack
(PQFP80)
Weight approximately 1.61 g
Dimensions in mm

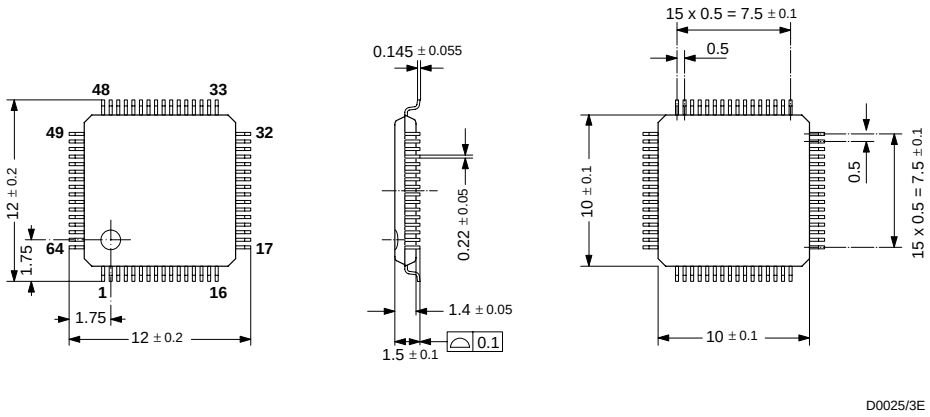


Fig. 4–2:
64-Pin Plastic Low-Profile Quad Flat Pack
(PLQFP64)
Weight approximately 0.35 g
Dimensions in mm

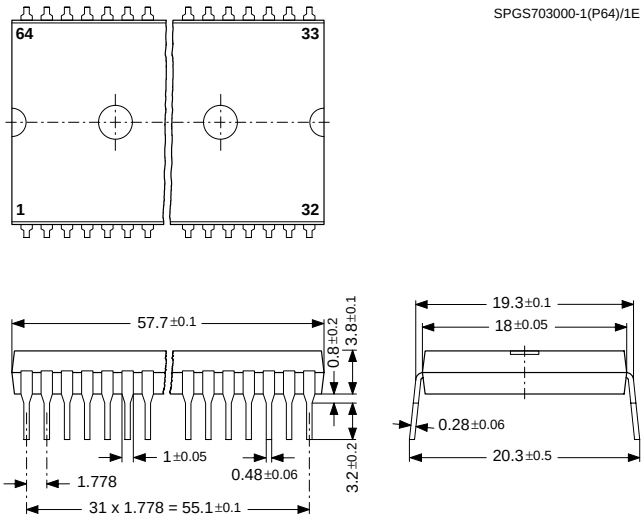


Fig. 4–3:
64-Pin Plastic Shrink Dual-Inline Package
(PSDIP64)
Weight approximately 9.0 g
Dimensions in mm

4.2. Pin Connections and Short Descriptions

NC = not connected (**leave vacant** for future compatibility reasons)
TP = Test Pin (**leave vacant** - pin is used for production test only)
LV = leave vacant
X = obligatory; connect as described in application circuit diagram
AHVSS: connect to AHVSS

Pin No.			Pin Name	Type	Connection (if not used)	Short Description
PQFP 80-pin	PLQFP 64-pin	PSDIP 64-pin				
1	64	8	NC		LV	Not connected
2	1	9	I2C_CL	IN/OUT	X	I^2C clock
3	2	10	I2C_DA	IN/OUT	X	I^2C data
4	3	11	I2S_CL	IN/OUT	LV	I^2S clock
5	4	12	I2S_WS	IN/OUT	LV	I^2S word strobe
6	5	13	I2S_DA_OUT	OUT	LV	I^2S data output
7	6	14	I2S_DA_IN1	IN	LV	I^2S1 data input
8	7	15	TP		LV	Test pin
9	8	16	TP		LV	Test pin
10	9	17	TP		LV	Test pin
11	–	–	DVSUP		X	Digital power supply +5 V
12	–	–	DVSUP		X	Digital power supply +5 V
13	10	18	DVSUP		X	Digital power supply +5 V
14	–	–	DVSS		X	Digital ground
15	–	–	DVSS		X	Digital ground
16	11	19	DVSS		X	Digital ground
–	12	20	I2S_DA_IN2/3	IN	LV	$I^2S2/3$-data input
17	–	–	I2S_DA_IN2	IN	LV	PQFP80: pin 22 separate I2S_DA_IN3
18	13	21	NC		LV	Not connected
19	14	22	I2S_CL3	IN	LV	I^2S3 clock
20	15	23	I2S_WS3	IN	LV	I^2S3 word strobe
21	16	24	RESETQ	IN	X	Power-on-reset
22	–	–	I2S_DA_IN3	IN	LV	I^2S3-data input
23	–	–	NC		LV	Not connected
24	17	25	DACA_R	OUT	LV	Aux out, right
25	18	26	DACA_L	OUT	LV	Aux out, left

Pin No.			Pin Name	Type	Connection (if not used)	Short Description
PQFP 80-pin	PLQFP 64-pin	PSDIP 64-pin				
26	19	27	VREF2		X	Reference ground 2
27	20	28	DACM_R	OUT	LV	Loudspeaker out, right
28	21	29	DACM_L	OUT	LV	Loudspeaker out, left
29	22	30	NC		LV	Not connected
30	23	31	DACM_SUB	OUT	LV	Subwoofer output
31	24	32	NC		LV	Not connected
32	–	–	NC		LV	Not connected
33	25	33	SC2_OUT_R	OUT	LV	SCART output 2, right
34	26	34	SC2_OUT_L	OUT	LV	SCART output 2, left
35	27	35	VREF1		X	Reference ground 1
36	28	36	SC1_OUT_R	OUT	LV	SCART output 1, right
37	29	37	SC1_OUT_L	OUT	LV	SCART output 1, left
38	30	38	CAPL_A		X	Volume capacitor AUX
39	31	39	AHVSUP		X	Analog power supply 8.0 V
40	32	40	CAPL_M		X	Volume capacitor MAIN
41	–	–	NC		LV	Not connected
42	–	–	NC		LV	Not connected
43	–	–	AHVSS		X	Analog ground
44	33	41	AHVSS		X	Analog ground
45	34	42	AGNDC		X	Analog reference voltage
46	–	–	NC		LV	Not connected
47	35	43	SC4_IN_L	IN	LV	SCART 4 input, left
48	36	44	SC4_IN_R	IN	LV	SCART 4 input, right
49	37	45	ASG		AHVSS	Analog Shield Ground
50	38	46	SC3_IN_L	IN	LV	SCART 3 input, left
51	39	47	SC3_IN_R	IN	LV	SCART 3 input, right
52	40	48	ASG		AHVSS	Analog Shield Ground
53	41	49	SC2_IN_L	IN	LV	SCART 2 input, left
54	42	50	SC2_IN_R	IN	LV	SCART 2 input, right
55	43	51	ASG		AHVSS	Analog Shield Ground
56	44	52	SC1_IN_L	IN	LV	SCART 1 input, left

Pin No. PQFP 80-pin	Pin No. PLQFP 64-pin	Pin No. PSDIP 64-pin	Pin Name	Type	Connection (if not used)	Short Description
57	45	53	SC1_IN_R	IN	LV	SCART 1 input, right
58	46	54	NC		LV	Not connected
59	–	–	NC		LV	Not connected
60	47	55	MONO_IN	IN	LV	Mono input
61	–	–	AVSS		X	Analog ground
62	48	56	AVSS		X	Analog ground
63	–	–	NC		LV	Not connected
64	–	–	NC		LV	Not connected
65	–	–	AVSUP		X	Analog power supply +5 V
66	49	57	AVSUP		X	Analog power supply +5 V
67	50	58	NC		LV	Not connected
68	51	59	NC		LV	Not connected
69	52	60	NC		LV	Not connected
70	53	61	TESTEN	IN	AVSS	Test pin
71	54	62	XTAL_IN	IN	X	Crystal oscillator
72	55	63	XTAL_OUT	OUT	X / LV	Crystal oscillator (See also 4.3. Pin descriptions)
73	56	64	TP		LV	Test pin
74	57	1	AUD_CL_OUT	OUT	LV	Audio clock output (18.432 MHz)
-	–	–	NC		LV	Not connected
75	58	2	NC		LV	Not connected
76	59	3	NC		LV	Not connected
77	60	4	D_CTR_I/O_1	IN/OUT	LV	D_CTR_I/O_1
78	61	5	D_CTR_I/O_0	IN/OUT	LV	D_CTR_I/O_0
79	62	6	ADR_SEL	IN	X	I^2C Bus address select
80	63	7	STANDBYQ	IN	X	Stand-by (low-active)

4.3. Pin Descriptions

Pin numbers refer to the 80-pin PQFP package

Pin 1, **NC** – Pin not connected.

Pin 2, **I2C_CL** – I^2C Clock Input/Output (Fig. 4–8)
Via this pin, the I^2C-bus clock signal has to be supplied. The signal can be pulled down by the DPL in case of wait conditions.

Pin 3, **I2C_DA** – I^2C Data Input/Output (Fig. 4–8)
Via this pin, the I^2C-bus data is written to or read from the DPL.

Pin 4, **I2S_CL** – I^2S Clock Input/Output (Fig. 4–11)
Clock line for the I^2S bus. In master mode, this line is driven by the DPL; in slave mode, an external I^2S clock has to be supplied.

Pin 5, **I2S_WS** – I^2S Word Strobe Input/Output (Fig. 4–11)
Word strobe line for the I^2S bus. In master mode, this line is driven by the DPL; in slave mode, an external I^2S word strobe has to be supplied.

Pin 6, **I2S_DA_OUT1** – I^2S Data Output (Fig. 4–7)
Output of digital serial sound data of the DPL on the I^2S bus.

Pin 7, **I2S_DA_IN1** – I^2S Data Input 1 (Fig. 4–9)
First input of digital serial sound data to the DPL via the I^2S bus.

Pin 8, 9, 10, **TP**– Test pins

Pins 11, 12, 13, **DVSUP*** – Digital Supply Voltage
Power supply for the digital circuitry of the DPL. Must be connected to a power supply.

Pins 14, 15, 16, **DVSS*** – Digital Ground
Ground connection for the digital circuitry of the DPL.

Pin 17, **I2S_DA_IN2** – I^2S Data Input 2 (Fig. 4–9)
Second input of digital serial sound data to the DPL via the I^2S bus. In all packages except PQFP-80-pin this pin is also connected to the asynchronous I^2S interface 3.

Pins 18, **NC** – Pin not connected.

Pins 19, **I2S_CL3** – I^2S Clock Input (Fig. 4–9)
Clock line for the I^2S bus. Since only a slave mode is available an external I^2S clock has to be supplied.

Pins 20, **I2S_WS3** – I^2S Word Strobe Input (Fig. 4–9)
Word strobe line for the I^2S bus. Since only a slave mode is available an external I^2S word strobe has to be supplied.

Pin 21, **RESETQ** – Reset Input (Fig. 4–9)
In the steady state, high level is required. A low level resets the DPL 4519G.

Pin 22, **I2S_DA_IN3** – I^2S Data Input 3 (Fig. 4–9)
Asynchronous input of digital serial sound data to the DPL via the I^2S bus.

Pins 23, **NC** – Pin not connected.

Pins 24, 25, **DACA_R/L** – Aux Outputs (Fig. 4–16)
Output of the aux signal. A 1 nF capacitor to AHVSS must be connected to these pins. The DC offset on these pins depends on the selected aux volume.

Pin 26, **VREF2** – Reference Ground 2
Reference analog ground. This pin must be connected separately to ground (AHVSS). VREF2 serves as a clean ground and should be used as the reference for analog connections to the Main and AUX outputs.

Pins 27, 28, **DACM_R/L** – Main Outputs (Fig. 4–16)
Output of the Main signal. A 1 nF capacitor to AHVSS must be connected to these pins. The DC offset on these pins depends on the selected Main volume.

Pin 29 **NC** – Pin not connected.

Pin 30, **DACM_SUB** – Subwoofer Output (Fig. 4–16)
Output of the subwoofer signal. A 1-nF capacitor to AHVSS must be connected to this pin. Due to the low frequency content of the subwoofer output, the value of the capacitor may be increased for better suppression of high-frequency noise. The DC offset on this pin depends on the selected Main volume.

Pins 31, 32 **NC** – Pin not connected.

Pins 33, 34, **SC2_OUT_R/L** – SCART2 Outputs (Fig. 4–18)
Output of the SCART2 signal. Connections to these pins must use a 100-Ω series resistor and are intended to be AC-coupled.

Pin 35, **VREF1** – Reference Ground 1
Reference analog ground. This pin must be connected separately to ground (AHVSS). VREF1 serves as a clean ground and should be used as the reference for analog connections to the SCART outputs.

Pins 36, 37, **SC1_OUT_R/L** – SCART1 Outputs (Fig. 4–18)
Output of the SCART1 signal. Connections to these pins must use a 100-Ω series resistor and are intended to be AC-coupled.

Pin 38, **CAPL_A** – Volume Capacitor Aux (Fig. 4–13)
A 10-µF capacitor to AHVSUP must be connected to this pin. It serves as a smoothing filter for volume changes in order to suppress audible plops. The value of the capacitor can be lowered to 1-µF if faster response is required. The area encircled by the trace lines should be minimized; keep traces as short as possible. This input is sensitive for magnetic induction.

Pin 39, **AHVSUP*** – Analog Power Supply High Voltage
Power is supplied via this pin for the analog circuitry of the DPL. This pin must be connected to the +8 V supply. (+5 V-operation is possible with restrictions in performance)

Pin 40, **CAPL_M** – Volume Capacitor Loudspeakers (Fig. 4–13)
A 10-µF capacitor to AHVSUP must be connected to this pin. It serves as a smoothing filter for volume changes in order to suppress audible plops. The value of the capacitor can be lowered to 1 µF if faster response is required. The area encircled by the trace lines should be minimized; keep traces as short as possible. This input is sensitive for magnetic induction.

Pins 41, 42, **NC** – Pins not connected.

Pins 43, 44, **AHVSS*** – Ground for Analog Power Supply High Voltage
Ground connection for the analog circuitry of the DPL.

Pin 45, **AGNDC** – Internal Analog Reference Voltage
This pin serves as the internal ground connection for the analog circuitry. It must be connected to the VREF pins with a 3.3-µF and a 100-nF capacitor in parallel. This pins shows a DC level of typically 3.73 V.

Pin 46, **NC** – Pin not connected.

Pins 47, 48, **SC4_IN_L/R** – SCART4 Inputs
(Fig. 4–15)
The analog input signal for SCART4 is fed to this pin. Analog input connection must be AC-coupled.

Pin 49, **ASG*** – Analog Shield Ground
Analog ground (AHVSS) should be connected to this pin to reduce cross-coupling between SCART inputs.

Pins 50, 51, **SC3_IN_L/R** – SCART3 Inputs
(Fig. 4–15)
The analog input signal for SCART3 is fed to this pin. Analog input connection must be AC-coupled.

Pin 52, **ASG*** – Analog Shield Ground
Analog ground (AHVSS) should be connected to this pin to reduce cross-coupling between SCART inputs.

Pins 53, 54 **SC2_IN_L/R** – SCART2 Inputs (Fig. 4–15)
The analog input signal for SCART2 is fed to this pin. Analog input connection must be AC-coupled.

Pin 55, **ASG*** – Analog Shield Ground
Analog ground (AHVSS) should be connected to this pin to reduce cross-coupling between SCART inputs.

Pins 56, 57 **SC1_IN_L/R** – SCART1 Inputs (Fig. 4–15)
The analog input signal for SCART1 is fed to this pin. Analog input connection must be AC-coupled.

Pin 58, **NC** – Pin not connected

Pin 59, **NC** – Pin not connected.

Pin 60 **MONO_IN** – Mono Input (Fig. 4–15)
The analog mono input signal is fed to this pin AC-coupled.

Pins 61, 62, **AVSS*** – Analog Power Supply Voltage
Ground connection for the analog IF input circuitry of the DPL.

Pins 63, 64, **NC** – Pins not connected.

Pins 65, 66, **AVSUP*** – Analog Power Supply Voltage
Power is supplied via this pin for the analog IF input circuitry of the DPL. This pin must be connected to the +5 V supply.

Pin 67, 68, 69, **NC** – Pin not connected.

Pin 70, **TESTEN** – Test Enable Pin (Fig. 4–9)
This pin enables factory test modes. For normal operation, it must be connected to ground.

Pins 71, 72 **XTAL_IN, XTAL_OUT** – Crystal Input and Output Pins (Fig. 4–12)
These pins are connected to an 18.432 MHz crystal oscillator which is digitally tuned by integrated capacitances. An external clock can be fed into XTAL_IN (leave XTAL_OUT vacant in this case). The audio clock output signal AUD_CL_OUT is derived from the oscillator. External capacitors at each crystal pin to ground (AVSS) are required. It should be verified by layout, that no supply current for the digital circuitry is flowing through the ground connection point.

Pin 73, **TP** – This pin is needed for factory tests. For normal operation, it must be left vacant.

Pin 74, **AUD_CL_OUT** – Audio Clock Output
(Fig. 4–12)
This is the 18.432 MHz main clock output.

Pins 75, 76, **NC** – Pins not connected.

Pins 77, 78, **D_CTR_I/O_1/0** – Digital Control Input/Output Pins (Fig. 4–11)
General purpose input/output pins.

Pin 79, **ADR_SEL** – I^2C Bus Address Select
(Fig. 4–10)
This pin selects the device address for the DPL. (see Table 3–1).

Pin 80, **STANDBYQ** – Stand-by
In normal operation, this pin must be High. If the DPL is switched to **'Stand-by'-mode**, the SCART switches maintain their position and function. (see Section 2.7.2.)

*** Application Note:**

All ground pins should be connected to one low-resistive ground plane.

All supply pins should be connected separately with short and low-resistive lines to the power supply.

Decoupling capacitors from DVSUP to DVSS, AVSUP to AVSS, and AHVSUP to AHVSS are recommended as closely as possible to these pins. Decoupling of DVSUP and DVSS is most important. We recommend using more than one capacitor. By choosing different values, the frequency range of active decoupling can be extended. In our application boards we use: 220 pF, 470 pF, 1.5 nF, and 10 µF. The capacitor with the lowest value should be placed nearest to the pins.

The ASG pins should be connected as closely as possible to the IC ground. They are intended for leading with the SCART signals as shield lines and should not be connected to ground at the SCART-connector again.

4.4. Pin Configurations

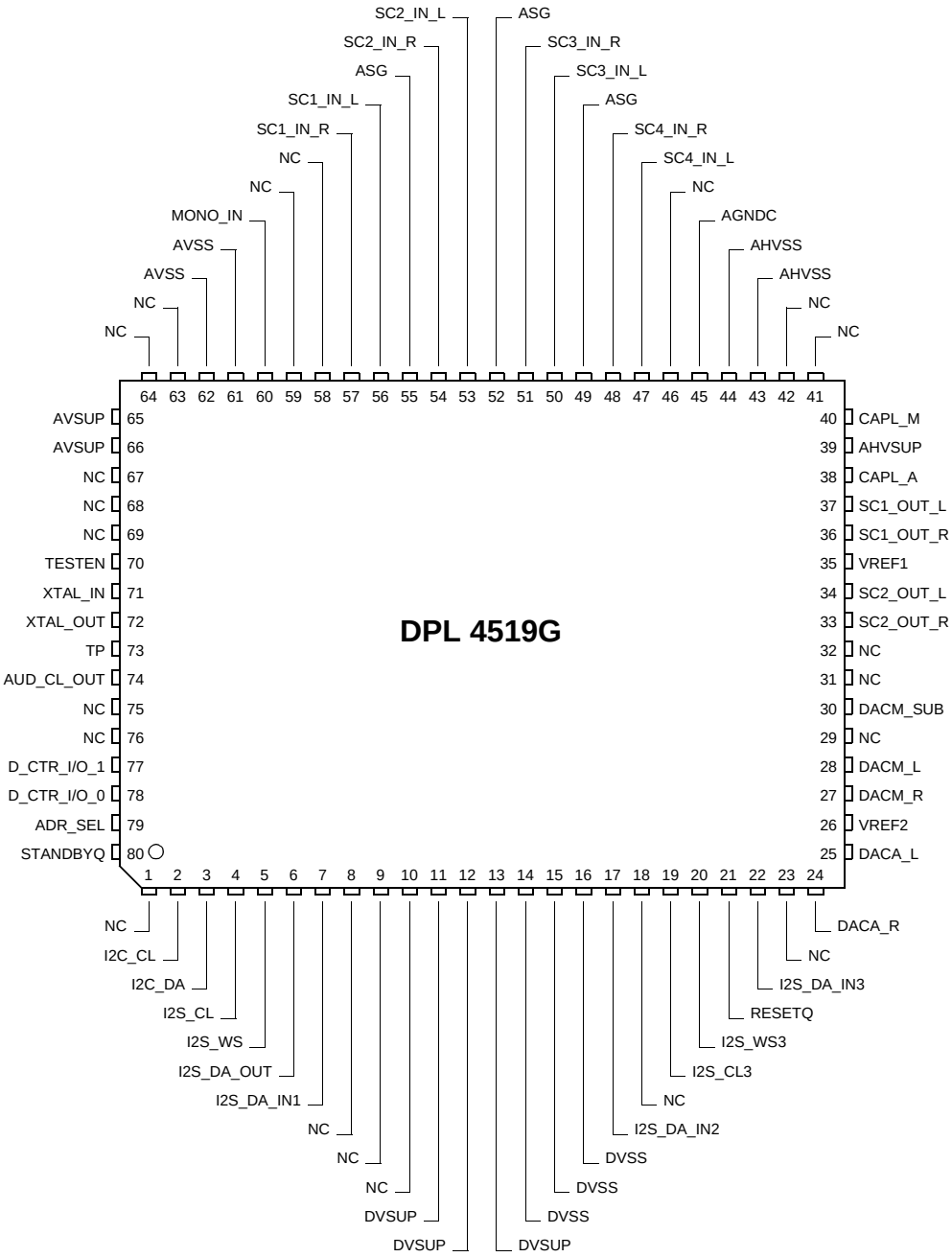


Fig. 4–4: 80-pin PQFP package

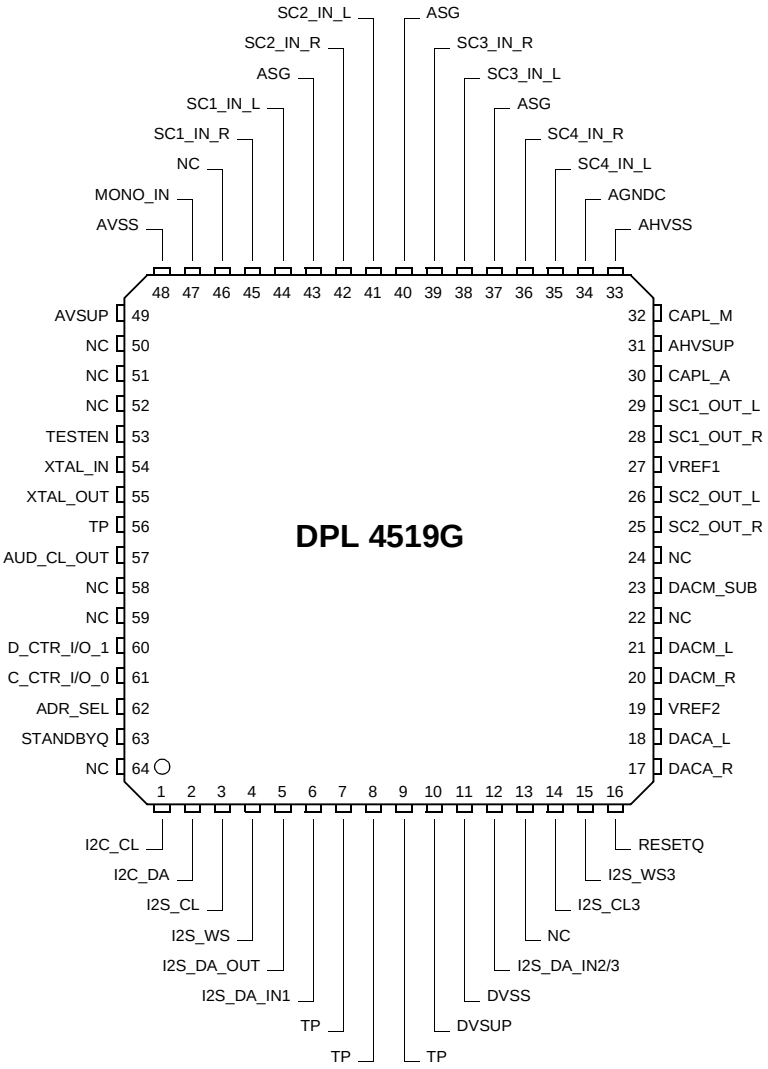


Fig. 4–5: 64-pin PLQFP package

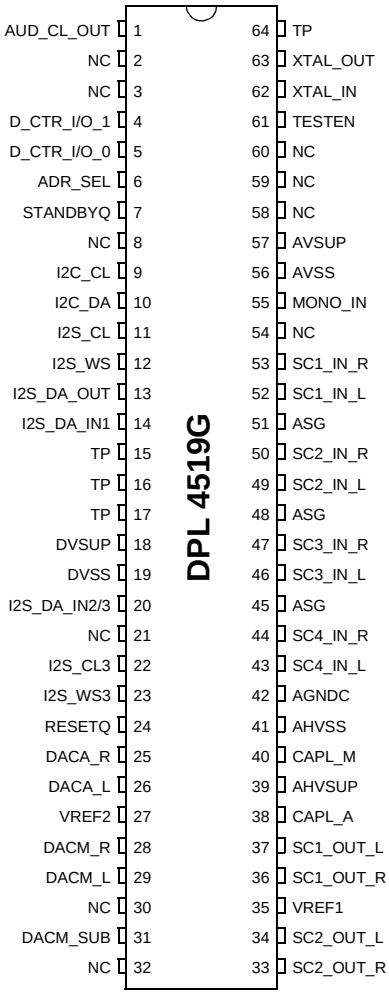


Fig. 4–6: 64-pin PSDIP package

4.5. Pin Circuits

Pin numbers refer to the PQFP80 package.

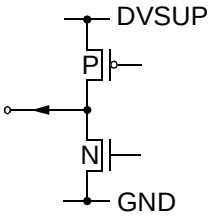


Fig. 4–7: Output Pin 6
(I2S_DA_OUT)

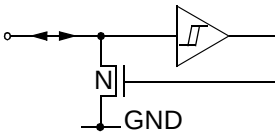


Fig. 4–8: Input/Output Pins 2 and 3
(I2C_CL, I2C_DA)

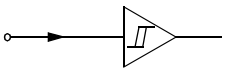


Fig. 4–9: Input Pins 7, 17, 21, 22, 70, and 80
(I2S_DA_IN1..3, RESETQ, TESTEN, STANDBYQ)

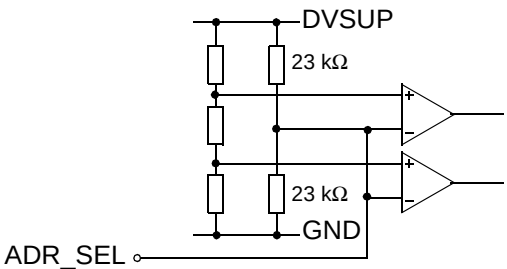


Fig. 4–10: Input Pin 79 **(ADR_SEL)**

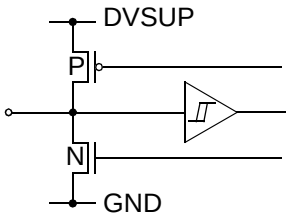


Fig. 4–11: Input/Output Pins 4, 5, 77, and 78
(I2S_CL, I2S_WS, D_CTR_I/O_1, D_CTR_I/O_0)

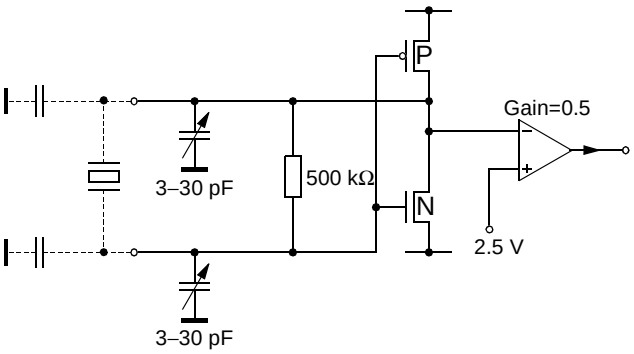


Fig. 4–12: Output/Input Pins 71, 72, and 74
(XTALIN, XTALOUT, AUD_CL_OUT)

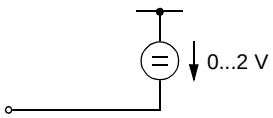


Fig. 4–13: Capacitor Pins 38 and 40
(CAPL_A, CAPL_M)

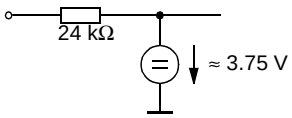


Fig. 4–14: Input Pin 60 **(MONO_IN**)

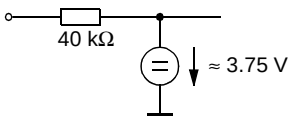


Fig. 4–15: Input Pins 47, 48, 50, 51, 53, 54, 56, and 57
(SC4-1_IN_L/R)

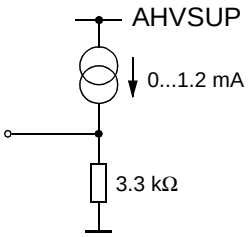


Fig. 4–16: Output Pins 24, 25, 27, 28 and 30
(DACA_R/L, DACM_R/L, DACM_SUB)

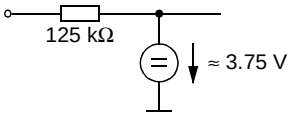


Fig. 4–17: Pin 45 **(AGNDC)**

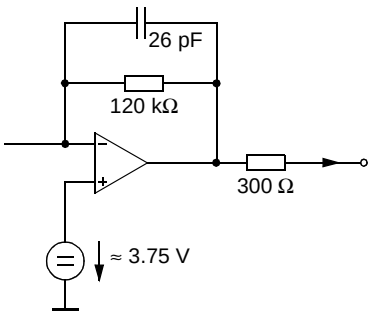


Fig. 4–18: Output Pins 33, 34, 36, and 37
(SC_2_OUT_R/L, SC_1_OUT_R/L)

4.6. Electrical Characteristics

4.6.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	70[1)]	°C
T_S	Storage Temperature	–	–40	125	°C
V_{SUP1}	First Supply Voltage	AHVSUP	–0.3	9.0	V
V_{SUP2}	Second Supply Voltage	DVSUP	–0.3	6.0	V
V_{SUP3}	Third Supply Voltage	AVSUP	–0.3	6.0	V
dV_{SUP23}	Voltage between AVSUP and DVSUP	AVSUP, DVSUP	–0.5	0.5	V
P_{TOT}	Package Power Dissipation PSDIP64 PQFP80 PLQFP64			 1300 1000 960[1)]	mW
V_{Idig}	Input Voltage, all Digital Inputs		–0.3	V_{SUP2}+0.3	V
I_{Idig}	Input Current, all Digital Pins	–	–20	+20	mA[2)]
V_{Iana}	Input Voltage, all Analog Inputs	SCn_IN_s,[3)] MONO_IN	–0.3	V_{SUP1}+0.3	V
I_{Iana}	Input Current, all Analog Inputs	SCn_IN_s,[3)] MONO_IN	–5	+5	mA[2)]
I_{Oana}	Output Current, all SCART Outputs	SCn_OUT_s[3)]	[4), 5)]	[4), 5)]	
I_{Oana}	Output Current, all Analog Outputs except SCART Outputs	DACp_s[3)]	[4)]	[4)]	
I_{Cana}	Output Current, other pins connected to capacitors	CAPL_p,[3)] AGNDC	[4)]	[4)]	

1) PLQFP64: 65 °C
2) positive value means current flowing into the circuit
3) “n” means “1”, “2”, “3”, or “4”, “s” means “L” or “R”, “p” means “M” or “A”
4) The analog outputs are short circuit proof with respect to First Supply Voltage and ground.
5) Total chip power dissipation must not exceed absolute maximum rating.

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

4.6.2. Recommended Operating Conditions (T_A = 0 to 70 °C)

4.6.2.1. General Recommended Operating Conditions

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
V_{SUP1}	First Supply Voltage (8-V Operation)	AHVSUP	7.6	8.0	8.7	V
	First Supply Voltage (5-V Operation)		4.75	5.0	5.25	V
V_{SUP2}	Second Supply Voltage	DVSUP	4.75	5.0	5.25	V
V_{SUP3}	Third Supply Voltage	AVSUP	4.75	5.0	5.25	V
t_{STBYQ1}	STANDBYQ Setup Time before Turn-off of Second Supply Voltage	STANDBYQ, DVSUP	1			µs

4.6.2.2. Analog Input and Output Recommendations

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
C_{AGNDC}	AGNDC-Filter-Capacitor	AGNDC	–20%	3.3		µF
	Ceramic Capacitor in Parallel		–20%	100		nF
C_{inSC}	DC-Decoupling Capacitor in front of SCART Inputs	SCn_IN_s[1)]	–20%	330		nF
V_{inSC}	SCART Input Level				2.0	V_{RMS}
V_{inMONO}	Input Level, Mono Input	MONO_IN			2.0	V_{RMS}
R_{LSC}	SCART Load Resistance	SCn_OUT_s[1)]	10			kΩ
C_{LSC}	SCART Load Capacitance				6.0	nF
C_{VMA}	Main/AUX Volume Capacitor	CAPL_M, CAPL_A		10		µF
C_{FMA}	Main/AUX Filter Capacitor	DACM_s, DACA_s[1)]	–10%	1	+10%	nF

[1)] “n” means “1”, “2”, or “3”, “s” means “L” or “R”, “p” means “M” or “A”

4.6.2.3. Crystal Recommendations

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
General Crystal Recommendations						
f_P	Crystal Parallel Resonance Frequency at 12 pF Load Capacitance			18.432		MHz
R_R	Crystal Series Resistance			8	25	Ω
C_0	Crystal Shunt (Parallel) Capacitance			6.2	7.0	pF
C_L	External Load Capacitance[1)]	XTAL_IN, XTAL_OUT	PSDIP approx. 1.5 P(L)QFP approx. 3.3			pF pF
Crystal Recommendations for Master-Slave Applications (DPL Clock must perform synchronization to I^2S clock)						
f_{TOL}	Accuracy of Adjustment		–20		+20	ppm
D_{TEM}	Frequency Variation versus Temperature		–20		+20	ppm
C_1	Motional (Dynamic) Capacitance		19	24		fF
f_{CL}	Required Open Loop Clock Frequency (T_{amb} = 25 °C)	AUD_CL_OUT	18.431		18.433	MHz
Crystal Recommendations for other Applications (No synchronization to I^2S clock possible)						
f_{TOL}	Accuracy of Adjustment		–100		+100	ppm
D_{TEM}	Frequency Variation versus Temperature		–50		+50	ppm
f_{CL}	Required Open Loop Clock Frequency (T_{amb} = 25 °C)	AUD_CL_OUT	18.429		18.435	MHz
Amplitude Recommendation for Operation with External Clock Input (C_{load} after reset typ. 22 pF)						
V_{XCA}	External Clock Amplitude	XTAL_IN	0.7			V_{pp}

[1)] External capacitors at each crystal pin to ground are required. They are necessary to tune the open-loop frequency of the internal PLL and to stabilize the frequency in closed-loop operation.
Due to different layouts, the accurate capacitor size should be determined with the customer PCB. The suggested values (1.5...3.3 pF) are figures based on experience and should serve as “start value”.

To define the capacitor size, reset the DPL without transmitting any further I2C telegrams. Measure the frequency at AUD_CL_OUT-pin. Change the capacitor size until the free running frequency matches 18.432 MHz as closely as possible. The higher the capacity, the lower the resulting clock frequency.

4.6.3. Characteristics

at T_A = 0 to 70 °C, f_{CLOCK} = 18.432 MHz, V_{SUP1} = 7.6 to 8.7 V, V_{SUP2} = 4.75 to 5.25 V for min./max. values
at T_A = 60 °C, f_{CLOCK} = 18.432 MHz, V_{SUP1} = 8 V, V_{SUP2} = 5 V for typical values,
T_J = Junction Temperature
Main (M) = Main Channel, Aux (A) = Aux Channel

4.6.3.1. General Characteristics

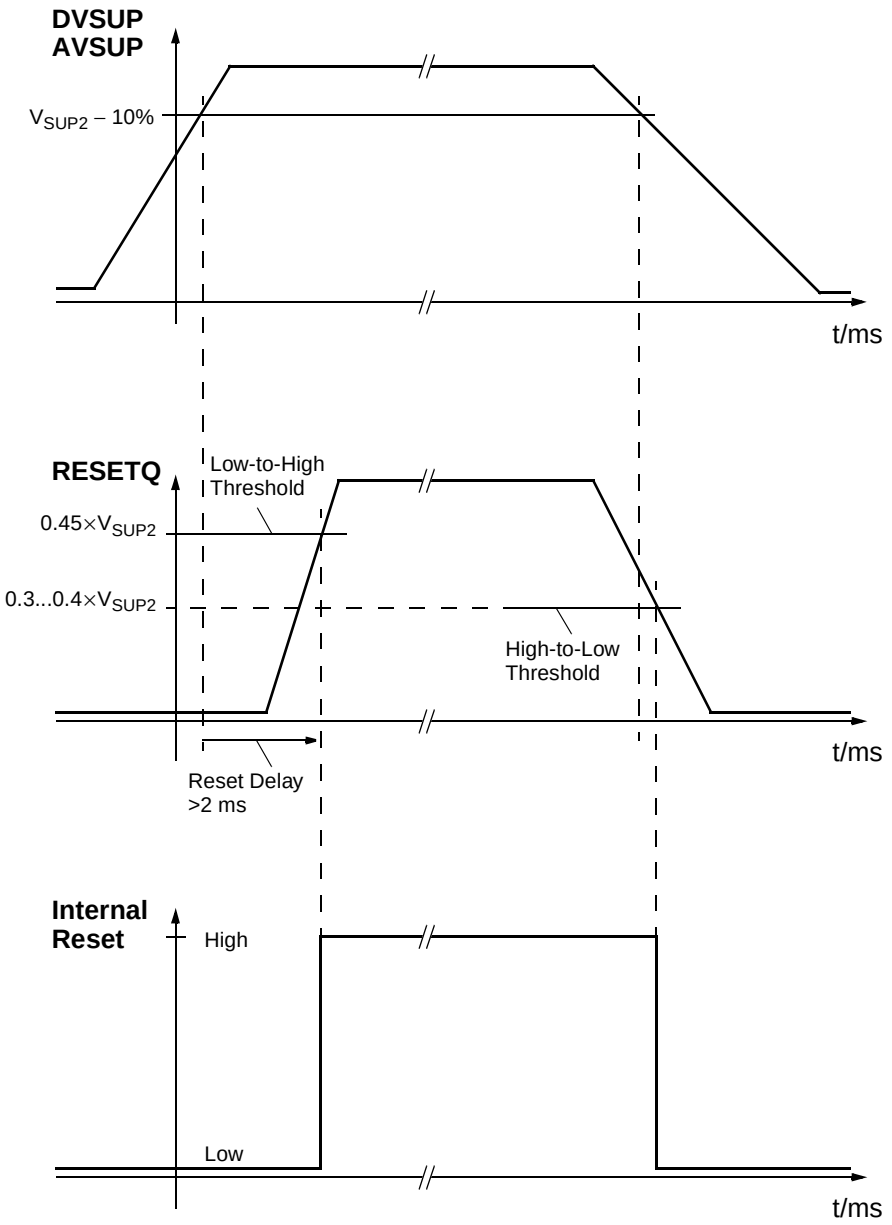
Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Supply							
I_{SUP1A}	First Supply Current (active) (AHVSUP = 8 V)	AHVSUP		18 12	25 17	mA mA	Volume Main and Aux 0 dB Volume Main and Aux -30 dB
	First Supply Current (active) (AHVSUP = 5 V)			12 8	17 11	mA mA	Volume Main and Aux 0 dB Volume Main and Aux -30 dB
I_{SUP2A}	Second Supply Current (active) (DVSUP = 5 V)	DVSUP		70	85	mA	
I_{SUP3A}	Third Supply Current (active)	AVSUP		9	13	mA	
I_{SUP1S}	First Supply Current (AHVSUP = 8 V)	AHVSUP		5.6	7.7	mA	Standby Mode STANDBYQ = low
	First Supply Current (AHVSUP = 5 V)			3.7	5.1	mA	
Clock							
f_{CLOCK}	Clock Input Frequency	XTAL_IN		18.432		MHz	
D_{CLOCK}	Clock High to Low Ratio		45		55	%	
t_{JITTER}	Clock Jitter (Verification not provided in Production Test)				50	ps	
V_{xtalDC}	DC-Voltage Oscillator			2.5		V	
$t_{Startup}$	Oscillator Startup Time at VDD Slew-rate of 1 V/µs	XTAL_IN, XTAL_OUT		0.4	2	ms	
V_{ACLKAC}	Audio Clock Output AC Voltage	AUD_CL_OUT	1.2	1.8		V_{pp}	load = 40 pF
V_{ACLKDC}	Audio Clock Output DC Voltage		0.4		0.6	V_{SUP3}	I_{max} = 0.2 mA
r_{outHF_ACL}	HF Output Resistance			140		Ω	

4.6.3.2. Digital Inputs, Digital Outputs

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Digital Input Levels							
V_{DIGIL}	Digital Input Low Voltage	STANDBYQ D_CTR_I/O_0/1			0.2	V_{SUP2}	
V_{DIGIH}	Digital Input High Voltage		0.5			V_{SUP2}	
Z_{DIGI}	Input Impedance				5	pF	
I_{DLEAK}	Digital Input Leakage Current		–1		1	µA	0 V < U_{INPUT}< DVSUP D_CTR_I/O_0/1: tri-state
V_{DIGIL}	ADR_SEL Input Low Voltage	ADR_SEL			0.2	V_{SUP2}	
V_{DIGIH}	ADR_SEL Input High Voltage		0.8			V_{SUP2}	
I_{ADRSEL}	Input Current		–500	–220		µA	U_{ADR_SEL}= DVSS
				220	500	µA	U_{ADR_SEL}= DVSUP
Digital Output Levels							
V_{DCTROL}	Digital Output Low Voltage	D_CTR_I/O_0 D_CTR_I/O_1			0.4	V	IDDCTR = 1 mA
V_{DCTROH}	Digital Output High Voltage		V_{SUP2} – 0.3			V	IDDCTR = –1 mA

4.6.3.3. Reset Input and Power-Up

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
RESETQ Input Levels							
V_{RHL}	Reset High-Low Transition Voltage	RESETQ	0.3		0.4	V_{SUP2}	
V_{RLH}	Reset Low-High Transition Voltage		0.45		0.55	V_{SUP2}	
Z_{RES}	Input Impedance				5	pF	
I_{RES}	Input Pin Leakage Current		-1		1	µA	0 V < U_{INPUT}< DVSUP



Note: The reset should not reach high level before the oscillator has started. This requires a reset delay of >2 ms

0.3 x V_{SUP2} means 1.5 Volt with V_{SUP2} = 5.0 V

Fig. 4–19: Power-up sequence

4.6.3.4. I²C-Bus Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{I2CIL}	I²C-BUS Input Low Voltage	I2C_CL, I2C_DA			0.3	V_{SUP2}	
V_{I2CIH}	I²C-BUS Input High Voltage		0.6			V_{SUP2}	
t_{I2C1}	I²C START Condition Setup Time		120			ns	
t_{I2C2}	I²C STOP Condition Setup Time		120			ns	
t_{I2C5}	I²C-Data Setup Time before Rising Edge of Clock		55			ns	
t_{I2C6}	I²C-Data Hold Time after Falling Edge of Clock		55			ns	
t_{I2C3}	I²C-Clock Low Pulse Time	I2C_CL	500			ns	
t_{I2C4}	I²C-Clock High Pulse Time		500			ns	
f_{I2C}	I²C-BUS Frequency				1.0	MHz	
V_{I2COL}	I²C-Data Output Low Voltage	I2C_CL, I2C_DA			0.4	V	I_{I2COL} = 3 mA
I_{I2COH}	I²C-Data Output High Leakage Current				1.0	µA	V_{I2COH} = 5 V
t_{I2COL1}	I²C-Data Output Hold Time after Falling Edge of Clock		15			ns	
t_{I2COL2}	I²C-Data Output Setup Time before Rising Edge of Clock		100			ns	f_{I2C} = 1 MHz

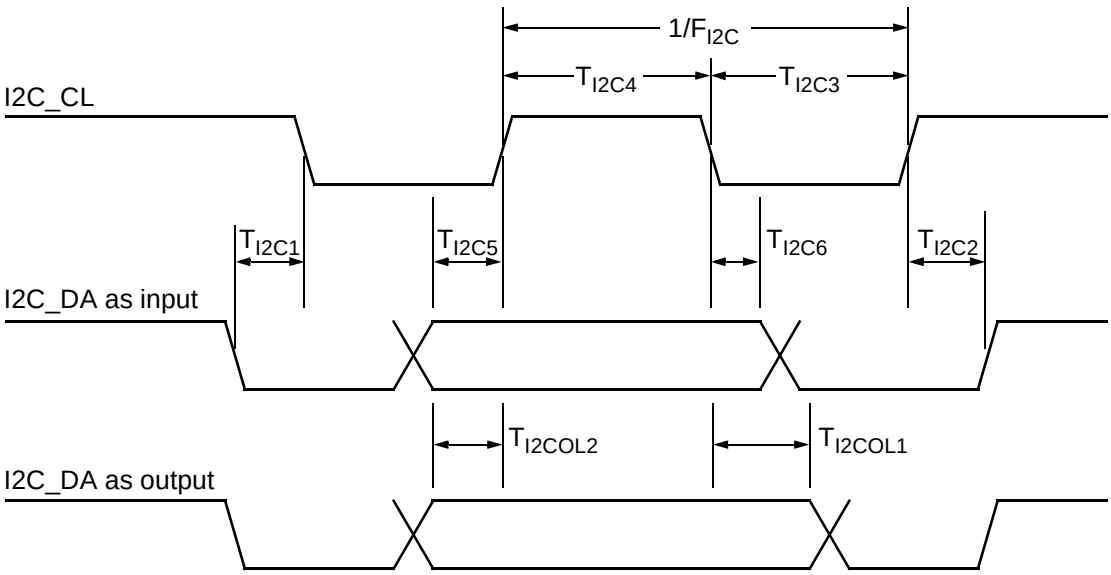
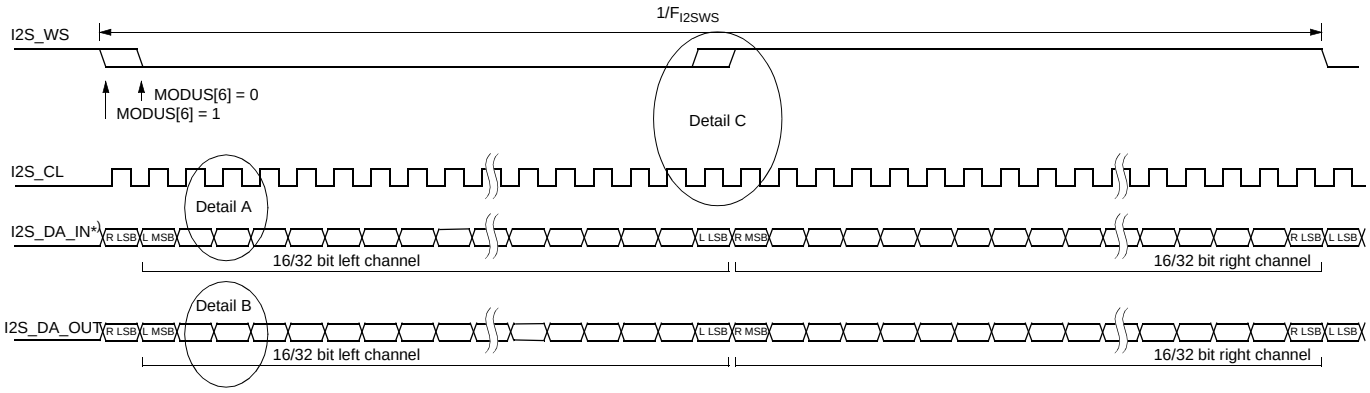


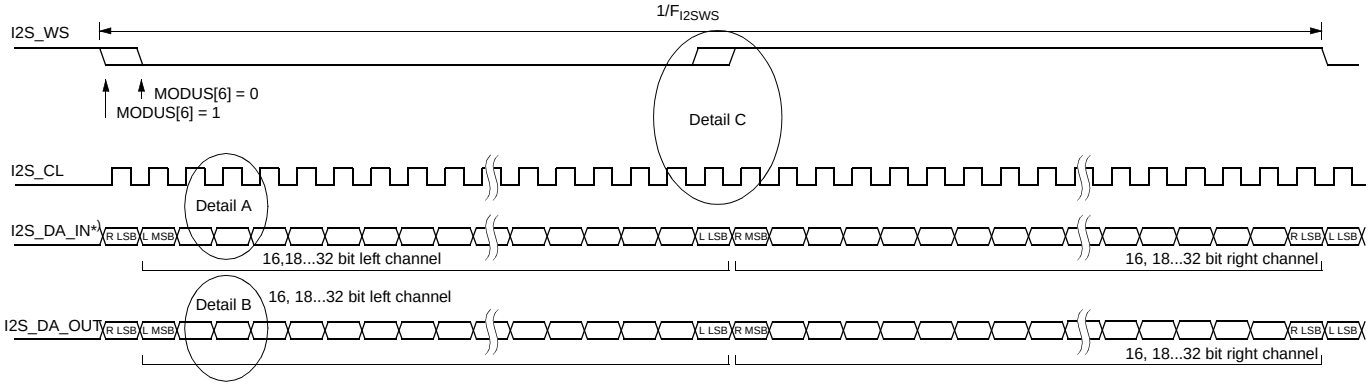
Fig. 4–20: I²C bus timing diagram

4.6.3.5. I^2S-Bus Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{I2SIL}	Input Low Voltage	I2S_CL I2S_WS I2S_CL3 I2S_WS3 I2S_DA_IN1..3			0.2	V_{SUP2}	
V_{I2SIH}	Input High Voltage		0.5			V_{SUP2}	
Z_{I2SI}	Input Impedance				5	pF	
$I_{LEAKI2S}$	Input Leakage Current		–1		1	µA	0 V < U_{INPUT}< DVSUP
V_{I2SOL}	I^2S Output Low Voltage	I2S_CL I2S_WS I2S_DA_OUT			0.4	V	I_{I2SOL} = 1 mA
V_{I2SOH}	I^2S Output High Voltage		V_{SUP2} – 0.3			V	I_{I2SOH} = –1 mA
f_{I2SOWS}	I^2S-Word Strobe Output Frequency	I2S_WS		48.0		kHz	
f_{I2SOCL}	I^2S-Clock Output Frequency	I2S_CL	1.536	3.072	12.288	MHz	
$R_{I2S10/I2S20}$	I^2S-Clock Output High/Low-Ratio		0.9	1.0	1.1		
Synchronous I^2S Interface							
t_{s_I2S}	I^2S Input Setup Time before Rising Edge of Clock	I2S_DA_IN1/2 I2S_CL	12			ns	for details see Fig. 4–21 “I^2S timing diagram (synchronous interface)”
t_{h_I2S}	I^2S Input Hold Time after Rising Edge of Clock		40			ns	
t_{d_I2S}	I^2S Output Delay Time after Falling Edge of Clock	I2S_CL I2S_WS I2S_DA_OUT			28	ns	C_L=30 pF
f_{I2SWS}	I^2S-Word Strobe Input Frequency	I2S_WS		48.0		kHz	
f_{I2SCL}	I^2S-Clock Input Frequency	I2S_CL	1.536	3.072	12.288	MHz	
R_{I2SCL}	I^2S-Clock Input Ratio		0.9		1.1		
Asynchronous I^2S Interface							
t_{s_I2S3}	I^2S3 Input Setup Time before Rising Edge of Clock	I2S_CL3 I2S_WS3 I2S_DA_IN3	4			ns	for details see Fig. 4–22 “I^2S timing diagram (asynchronous interface)”
t_{h_I2S3}	I^2S3 Input Hold Time after Rising Edge of Clock		40			ns	
f_{I2S3WS}	I^2S3-Word Strobe Input Frequency	I2S_WS3	5		50	kHz	
f_{I2S3CL}	I^2S3-Clock Input Frequency	I2S_CL3			3.2	MHz	
R_{I2S3CL}	I^2S3-Clock Input Ratio		0.9		1.1		



Data: MSB first, I^{2}S synchronous master



Data: MSB first, I^{2}S synchronous slave

Note:

1) I2S_DA_IN can be
– I2S_DA_IN1,
– I2S_DA_IN2, or
– I2S_DA_IN2/3

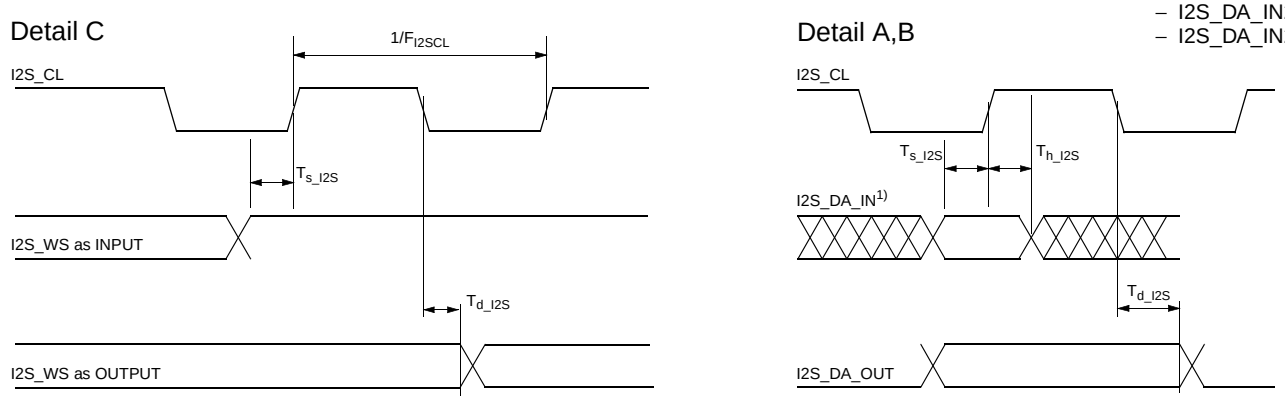
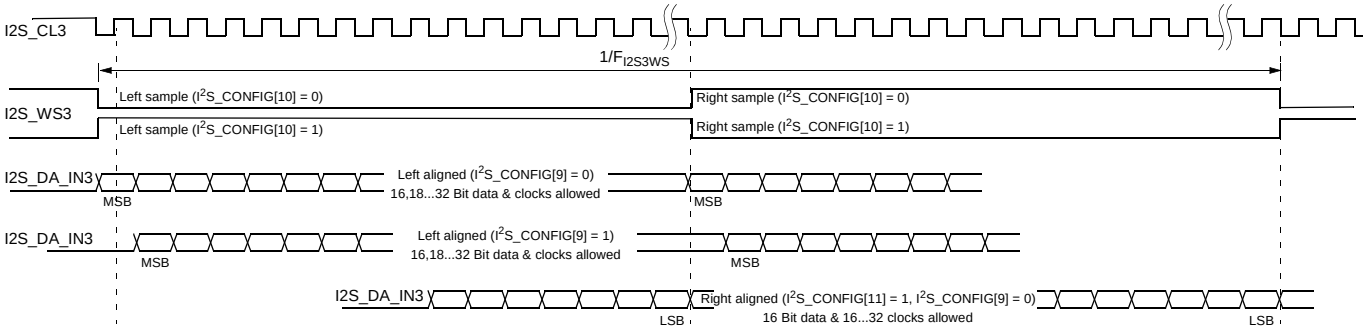


Fig. 4–21: I^{2}S timing diagram (synchronous interface)



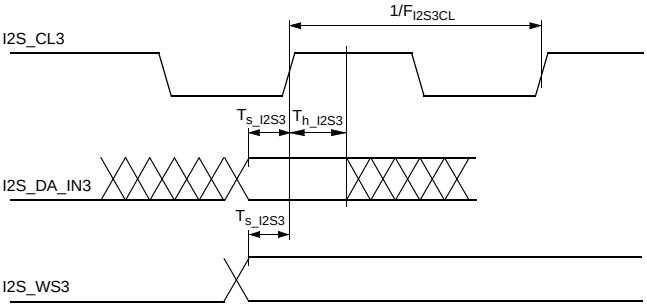


Fig. 4–22: I^2S timing diagram (asynchronous interface)

4.6.3.6. Analog Baseband Inputs and Outputs, AGNDC

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Analog Ground							
V_{AGNDC0}	AGNDC Open Circuit Voltage AHVSUP = 8 V AHVSUP = 5 V	AGNDC		 3.8 2.5		 V V	R_{load} ≥10 MΩ
R_{outAGN}	AGNDC Output Resistance AHVSUP = 8 V AHVSUP = 5 V		 70 47	 125 83	 180 120	 kΩ kΩ	3 V ≤ V_{AGNDC} ≤ 4 V
Analog Input Resistance							
R_{inSC}	SCART Input Resistance from T_A = 0 to 70 °C	SCn_IN_s[1)]	25	40	58	kΩ	f_{signal} = 1 kHz, I = 0.05 mA
R_{inMONO}	MONO Input Resistance from T_A = 0 to 70 °C	MONO_IN	15	24	35	kΩ	f_{signal} = 1 kHz, I = 0.1 mA

1) “n” means “1”, “2”, “3”, or “4”; “s” means “L” or “R”

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Audio Analog-to-Digital-Converter							
V_{AICL}	Analog Input Clipping Level for Analog-to-Digital-Conversion (AHVSUP=8 V)	SCn_IN_s,[1] MONO_IN	2.00		2.25	V_{RMS}	f_{signal} = 1 kHz
	Analog Input Clipping Level for Analog-to-Digital-Conversion (AHVSUP=5 V)		1.13		1.51	V_{RMS}	
SCART Outputs							
R_{outSC}	SCART Output Resistance	SCn_OUT_s[1]	200 200	330	460 500	Ω Ω	f_{signal} = 1 kHz, I = 0.1 mA, T_j = 27°C, T_A = 0 to 70°C
dV_{OUTSC}	Deviation of DC-Level at SCART Output from AGNDC Voltage		−70		+70	mV	
A_{SCtoSC}	Gain from Analog Input to SCART Output	SCn_IN_s,[1] MONO_IN → SCn_OUT_s[1]	−1.0		+0.5	dB	f_{signal} = 1 kHz
$f_{rSCtoSC}$	Frequency Response from Analog Input to SCART Output		−0.5		+0.5	dB	with resp. to 1 kHz 20 Hz to 20 000 Hz
V_{outSC}	Signal Level at SCART-Output (AHVSUP=8 V)	SCn_OUT_s[1]	1.8	1.9	2.0	V_{RMS}	f_{signal} = 1 kHz full scale Digital Input from I^2S
	Signal Level at SCART-Output (AHVSUP=5 V)		1.17	1.27	1.37	V_{RMS}	
Main and Aux Outputs							
R_{outMA}	Main/Aux Output Resistance	DACp_s[1]	2.1 2.1	3.3	4.6 5.0	kΩ kΩ	f_{signal} = 1 kHz, I = 0.1 mA T_j = 27°C from T_A = 0 to 70°C
$V_{outDCMA}$	DC-Level at Main/Aux-Output (AHVSUP=8 V)		1.80	2.04 61	2.28	V mV	Volume = 0 dB Volume = -30 dB
	DC-Level at Main/Aux-Output (AHVSUP=5 V)		1.12	1.36 40	1.60	V mV	Volume = 0 dB Volume = -30 dB
V_{outMA}	Signal Level at Main/Aux-Output (AHVSUP=8 V)		1.23	1.37	1.51	V_{RMS}	f_{signal} = 1 kHz full scale Digital Input from I^2S
	Signal Level at Main/Aux-Output (AHVSUP=5 V)		0.76	0.90	1.04	V_{RMS}	Volume = 0 dB

[1] "n" means "1", "2", "3", or "4"; "s" means "L" or "R"; "p" means "M" or "A"

4.6.3.7. Power Supply Rejection

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
PSRR: Rejection of Noise on AHVSUP at 1 kHz							
PSRR	AGNDC	AGNDC		80		dB	
	From Analog Input to I^2S Output	MONO_IN, SCn_IN_s[1)]		70		dB	
	From Analog Input to SCART Output	MONO_IN, SCn_IN_s[1)] SCn_OUT_s[1)]		70		dB	
	From I^2S Input to SCART Output	SCn_OUT_s[1)]		60		dB	
	From I^2S Input to Main/Aux Output	DACp_s[1)]		80		dB	

1) “n” means “1”, “2”, “3”, or “4”; “s” means “L” or “R”; “p” means “M” or “A”

4.6.3.8. Analog Performance

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Specifications for AHSUP=8 V							
SNR	Signal-to-Noise Ratio						
	from Analog Input to I^2S Output	MONO_IN, SCn_IN_s[1)]	90	93		dB	Input Level = –20 dB with resp. to V_{AICL}, f_{sig} = 1 kHz, A-weighted 20 Hz…20 kHz
	from Analog Input to SCART Output	MONO_IN, SCn_IN_s[1)] → SCn_OUT_s[1)]	93	96		dB	Input Level = –20 dB, f_{sig} = 1 kHz, A-weighted 20 Hz…20 kHz Volume = 0 dB
	from I^2S Input to SCART Output	SCn_OUT_s[1)]	90	93		dB	
	from I^2S Input to Main/Aux-Output	DACp_s[1)]	90	93		dB	
THD	Total Harmonic Distortion						
	from Analog Input to I^2S Output	MONO_IN, SCn_IN_s[1)]		0.01	0.03	%	Input Level = –3 dBr with resp. to V_{AICL}, f_{sig} = 1 kHz, unweighted 20 Hz…20 kHz
	from Analog Input to SCART Output	MONO_IN, SCn_IN_s → SCn_OUT_s[1)]		0.01	0.03	%	Input Level = –3 dBr, f_{sig} = 1 kHz, unweighted 20 Hz…20 kHz
	from I^2S Input to SCART Output	SCn_OUT_s[1)]		0.01	0.03	%	
	from I^2S Input to Main or Aux Output	DACA_s, DACM_s[1)]		0.01	0.03	%	

1) “n” means “1”, “2”, “3”, or “4”; “s” means “L” or “R”; “p” means “M” or “A”

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Specifications for AHSUP=5 V							
SNR	Signal-to-Noise Ratio						
	from Analog Input to I^2S Output	MONO_IN, SCn_IN_s[1)]	87	90		dB	Input Level = –20 dB with resp. to V_{AICL}, f_{sig} = 1 kHz, A-weighted 20 Hz…20 kHz
	from Analog Input to SCART Output	MONO_IN, SCn_IN_s[1)] → SCn_OUT_s[1)]	90	93		dB	Input Level = –20 dB, f_{sig} = 1 kHz, A-weighted 20 Hz…20 kHz Volume = 0 dB
	from I^2S Input to SCART Output	SCn_OUT_s[1)]	87	90		dB	
	from I^2S Input to Main/Aux-Output for Analog Volume at 0 dB for Analog Volume at –30 dB	DACp_s[1)]	87 75	90 80		dB dB	
THD	Total Harmonic Distortion						
	from Analog Input to I^2S Output	MONO_IN, SCn_IN_s[1)]		0.03	0.1	%	Input Level = –3 dBr with resp. to V_{AICL}, f_{sig} = 1 kHz, unweighted 20 Hz…20 kHz
	from Analog Input to SCART Output	MONO_IN, SCn_IN_s → SCn_OUT_s[1)]			0.1	%	Input Level = –3 dBr, f_{sig} = 1 kHz, unweighted 20 Hz…20 kHz
	from I^2S Input to SCART Output	SCn_OUT_s[1)]			0.1	%	
	from I^2S Input to Main or Aux Output	DACA_s, DACM_s[1)]			0.1	%	

[1)] “n” means “1”, “2”, “3”, or “4”; “s” means “L” or “R”; “p” means “M” or “A”

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Crosstalk Specifications							
XTALK	Crosstalk Attenuation						Input Level = –3 dB, f_{sig} = 1 kHz, unused analog inputs connected to ground by Z < 1 kΩ
	between left and right channel within SCART Input/Output pair (L→R, R→L)						unweighted 20 Hz...20 kHz
	SCn_IN → SCn_OUT[1)]		80			dB	
	SC1_IN or SC2_IN → I²S Output		80			dB	
	SC3_IN → I²S Output		80			dB	
	I²S Input → SCn_OUT[1)]		80			dB	
	between left and right channel within Main or Aux Output pair						unweighted 20 Hz...20 kHz
	I²S Input → DACp[1)]		75			dB	
	between SCART Input/Output pairs[1)]						(unweighted 20 Hz...20 kHz) same signal source on left and right disturbing channel, effect on each observed output channel
	D = disturbing program O = observed program						
	D: MONO/SCn_IN → SCn_OUT O: MONO/SCn_IN → SCn_OUT[1)]		100			dB	
	D: MONO/SCn_IN → SCn_OUT or unsel. O: MONO/SCn_IN → I²S Output		95			dB	
	D: MONO/SCn_IN → SCn_OUT O: I²S Input → SCn_OUT[1)]		100			dB	
	D: MONO/SCn_IN → unselected O: I²S Input → SC1_OUT[1)]		100			dB	
	Crosstalk between Main and Aux Output pairs						(unweighted 20 Hz...20 kHz) same signal source on left and right disturbing channel, effect on each observed output channel
	I²S Input DSP → DACp[1)]		90			dB	
XTALK	Crosstalk from Main or Aux Output to SCART Output and vice versa						(unweighted 20 Hz...20 kHz) same signal source on left and right disturbing channel, effect on each observed output channel
	D = disturbing program O = observed program						
	D: MONO/SCn_IN/DSP → SCn_OUT O: I²S Input → DACp[1)]		80			dB	SCART output load resistance 10 kΩ
	D: MONO/SCn_IN/DSP → SCn_OUT O: I²S Input → DACp[1)]		85			dB	SCART output load resistance 30 kΩ
	D: I²S Input → DACp O: MONO/SCn_IN → SCn_OUT[1)]		95			dB	
	D: I²S Input → DACM O: I²S Input → SCn_OUT[1)]		95			dB	

[1)] "n" means "1", "2", "3", or "4"; "s" means "L" or "R"; "p" means "M" or "A"

5. Appendix A: Application Information

5.1. Phase Relationship of Analog Outputs

The analog output signals: Main, Aux, and SCART2 all have the same phases. The SCART1 output has opposite phase.

Using the I^2S-outputs for other DSPs or D/A converters, care must be taken to adjust for the correct phase.

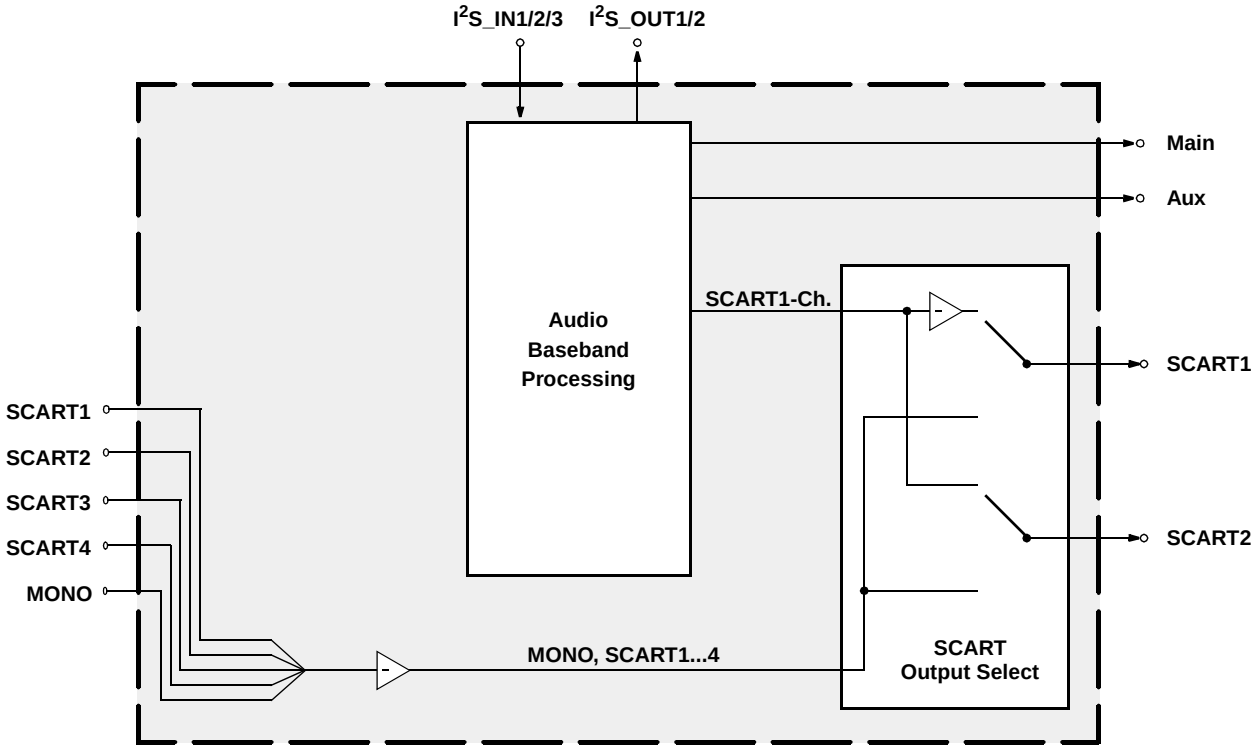
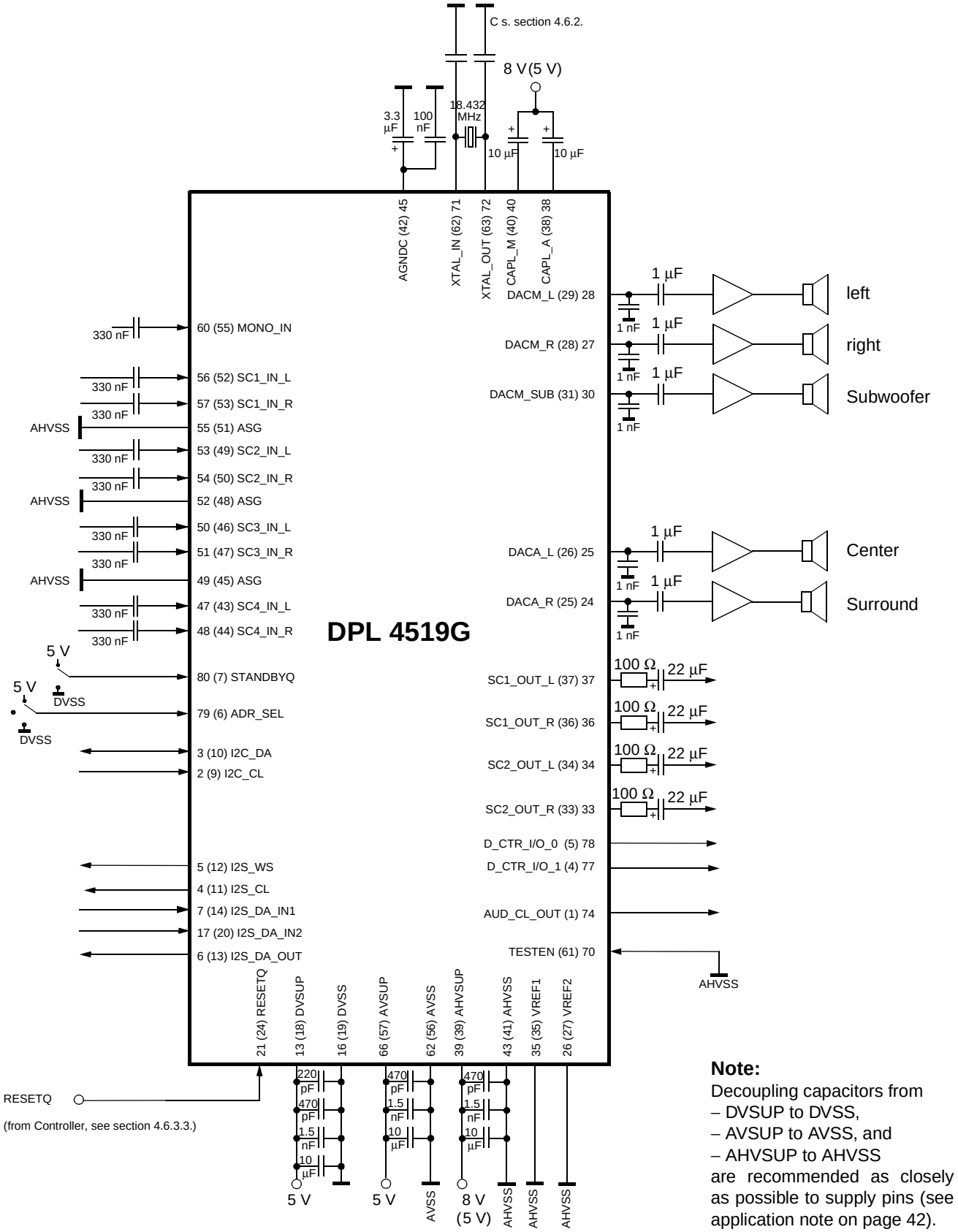


Fig. 5–1: Phase diagram of the DPL 4519G

5.2. Application Circuit



Note: Pin numbers refer to the PQFP80 package, numbers in brackets refer to the PSDIP64 package.

6. Data Sheet History

1. Preliminary data sheet: "DPL 4519G Sound Processor for Digital and Analog Surround Systems", Oct. 31, 2000, 6251-512-1PD.
First release of the preliminary data sheet.

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Printed in Germany
Order No. 6251-512-1PD