SC2602/SC2602A
Synchronous Voltage Mode Controller for Distributed Power Supply Applications

Description

The SC2602 and SC2602A are low-cost, full featured, synchronous voltage-mode controllers designed for use in single ended power supply applications where efficiency is of primary concern. Synchronous operation allows for the elimination of heat sinks in many applications. The SC2602s are ideal for implementing DC/DC converters needed to power advanced microprocessors in low cost systems, or in distributed power applications where efficiency is important. Internal level-shift, high-side drive circuitry, and preset shoot-thru control, allows the use of inexpensive N-channel power switches.

SC2602s features include temperature compensated voltage reference, triangle wave oscillator and current sense comparator circuitry. Power good signaling, shutdown, and over voltage protection are also provided.

The SC2602 operates at a fixed 200kHz and the SC2602A at 500kHz, providing a choice for optimum compromise between efficiency, external component size, and cost.

Two SC2602s can be used together to sequence power up of telecom systems. The power good of the first SC2602 connected to the enable of the second SC2602 makes this possible.

Features

- Synchronous operation for high efficiency (95%)
- $R_{DS(ON)}$ current sensing
- On-chip power good and OVP functions
- Small size with minimum external components
- Soft Start
- Enable function

Applications

- Microprocessor core supply
- Low cost synchronous applications
- Voltage Regulator Modules (VRM)
- DDR termination supplies
- Networking power supplies
- Sequenced power supplies

Typical Application Circuit

Typical Distributed Power Supply

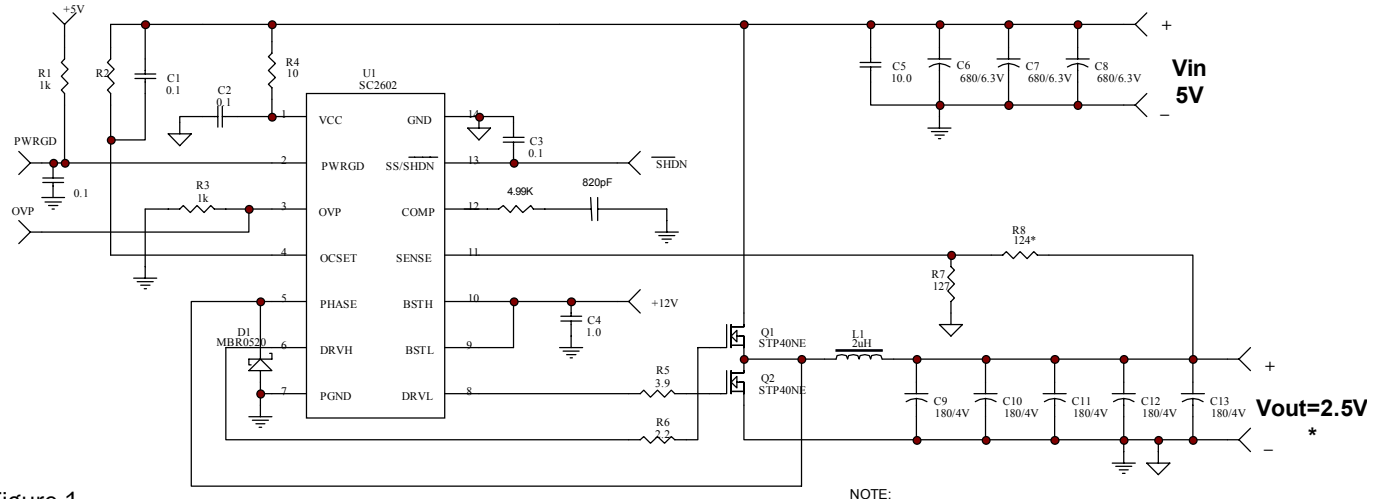


Figure 1.

NOTE:
*) Vout = 1.265 x (1+R8/R7)

Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
VCC, BSTL to GND	V_{IN}	-1.0 to 16 (20V Surge)	V
PGND to GND		± 0.5	V
PHASE to GND(1)		-0.5 to 18 (20V Surge)	V
BSTH to PHASE		16 (20V Surge)	V
Thermal Resistance Junction to Case	θ_{JC}	45	°C/W
Thermal Resistance Junction to Ambient	θ_{JA}	115	°C/W
Operating Temperature Range	T_A	-40 to +85	°C
Maximum Junction Temperature	T_J	125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	300	°C
ESD Rating (Human Body Model)	ESD	2	kV

Note: (1) -1.5V to 20V for 25ns repetitive every cycle.

Electrical Characteristics

Unless specified: V_{CC} = 4.75V to 12.6V; GND = PGND = 0V; FB = V_O; V_{BSTL} = 12V; $V_{BSTH-PHASE}$ = 12V; T_J = 25°C

Parameter	Conditions	Min	Typ	Max	Units
Power Supply					
Supply Voltage	VCC	4.2		12.6	V
Supply Current	EN = VCC		6	10	mA
Line Regulation	VO = 2.5V		0.5		%
Error Amplifier					
Gain (AOL)			50		dB
Input Bias			5	8	µA
Oscillator					
Oscillator Frequency	SC2602	180	200	220	kHz
	SC2602A	450	500	550	
Oscillator Max Duty Cycle		90	95		%
MOSFET Drivers					
DH Source/Sink	BSTH - DH = 4.5V, DH- PHASE = 2V	1			A
DL Source/Sink	BSTL - DL = 4.5V. DL - PGND. = 2V	1			A

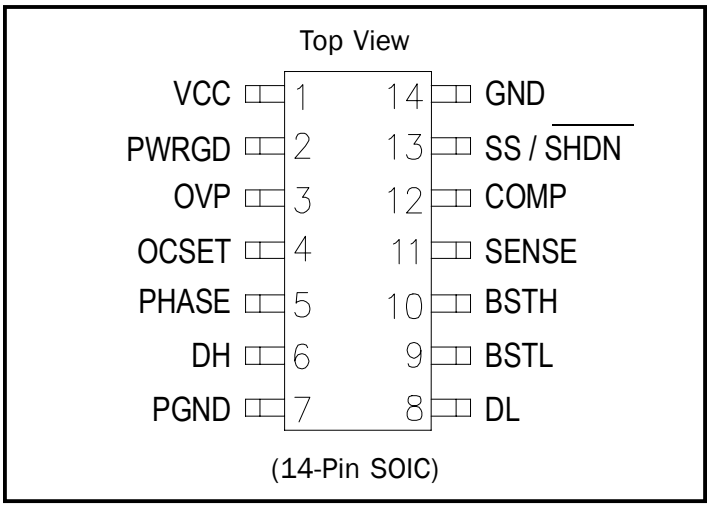
Electrical Characteristics (Cont.)

Unless specified: V_{CC} = 4.75V to 12.6V; GND = PGND = 0V; FB = V_O; V_{BSTL} = 12V; $V_{BSTH-PHASE}$ = 12V; T_J = 25°C

Parameter	Conditions	Min	Typ	Max	Units
PROTECTION					
OVP Threshold Voltage			20		%
OVP Source Current	V_{OVP} = 3V	10			mA
Power Good Threshold		88		112	%
Dead Time		45		100	ns
Over current Set Isink	2.0V ≤ V_{OCSET} ≤ 12V	180	200	220	µA
Reference					
Reference Voltage	0°C to 70°C	1.252	1.265	1.278	V
Accuracy		-1		+1	%
Soft Start					
Charge Current	V_{SS} = 1.5V	8.0	10	12	µA
Discharge Current	V_{SS} = 1.5V		1.5		µA

Note:
(1) Specification refers to application circuit (Figure 1).

Pin Configuration



Ordering Information

Device (1)(2)	Frequency	Package
SC2602STRT	200kHz	SO-14
SC2602ASTRT	500kHz	
SC2602EVB	Evaluation Board	

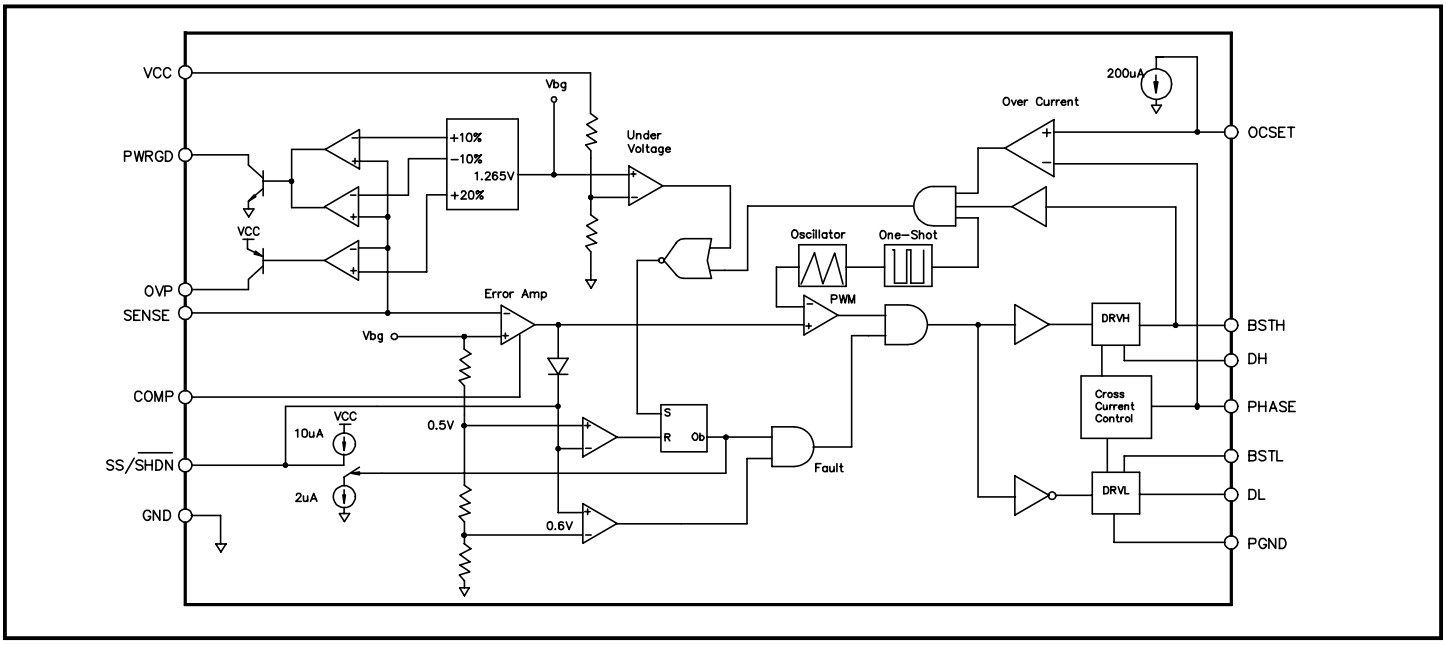
Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead free product.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	VCC	Chip supply voltage.
2	PWRGD	Logic high indicates correct output voltage.
3	OVP	Over voltage protection.
4	OCSET	Sets the converter overcurrent trip point.
5	PHASE	Input from the phase node between the MOSFETs.
6	DH	High side driver output.
7	PGND	Power ground.
8	DL	Low side driver output.
9	BSTL	Bootstrap, low side driver.
10	BSTH	Bootstrap, high side driver.
11	SENSE	Voltage sense input.
12	COMP	Compensation pin.
13	SS/$\overline{\text{SHDN}}$	Soft start. A capacitor to ground sets the slow start time.
14	GND	Signal ground.

Note:
(1) All logic level inputs and outputs are open collector TTL compatible.

Block Diagram



Theory of Operation

Synchronous Buck Converter

Primary V_{CORE} power is provided by a synchronous, voltage-mode pulse width modulated (PWM) controller. This section has all the features required to build a high efficiency synchronous buck converter, including "Power Good" flag, shut-down, and cycle-by-cycle current limit.

The output voltage of the synchronous converter is set and controlled by the output of the error amplifier. The external resistive divider reference voltage is derived from an internal trimmed-bandgap voltage reference (See Fig. 1). The inverting input of the error amplifier receives its voltage from the SENSE pin.

The internal oscillator uses an on-chip capacitor and trimmed precision current sources to set the oscillation frequency to 200kHz/500kHz. The triangular output of the oscillator sets the reference voltage at the inverting input of the comparator. The non-inverting input of the comparator receives it's input voltage from the error amplifier. When the oscillator output voltage drops below the error amplifier output voltage, the comparator output goes high. This pulls DL low, turning off the low-side FET, and DH is pulled high, turning on the high-side FET (once the cross-current control allows it). When the oscillator voltage rises back above the error amplifier output voltage, the comparator output goes low. This pulls DH low, turning off the high-side FET, and DL is pulled high, turning on the low-side FET (once the cross-current control allows it).

As SENSE increases, the output voltage of the error amplifier decreases. This causes a reduction in the on-time of the high-side MOSFET connected to DH, hence lowering the output voltage.

Under Voltage Lockout

The under voltage lockout circuit of the SC2602 assures that the high-side MOSFET driver outputs remain in the off state whenever the supply voltage drops below set parameters. Lockout occurs if V_{CC} falls below 4.1V. Normal operation resumes once V_{CC} rises above 4.2V.

Over-Voltage Protection

The over-voltage protection pin (OVP) is high only when the voltage at SENSE is 20% higher than the target value programmed by the external resistor divider. The OVP pin is internally connected to a PNP's collector.

Power Good

The power good function is to confirm that the regulator outputs are within +/-10% of the programmed level. PWRGD remains high as long as this condition is met. PWRGD is connected to an internal open collector NPN transistor.

Applications Information (Cont.)

Soft Start

Initially, SS/$\overline{\text{SHDN}}$ sources 10µA of current to charge an external capacitor. The outputs of the error amplifiers are clamped to a voltage proportional to the voltage on SS/$\overline{\text{SHDN}}$. This limits the on-time of the high-side MOSFETs, thus leading to a controlled ramp-up of the output voltages.

$R_{DS(ON)}$ Current Limiting

The current limit threshold is set by connecting an external resistor from the V_{CC} supply to OCSET. The voltage drop across this resistor is due to the 200µA internal sink sets the voltage at the pin. This voltage is compared to the voltage at the PHASE node. This comparison is made only when the high-side drive is high to avoid false current limit triggering due to uncontributing measurements from the MOSFETs off-voltage. When the voltage at PHASE is less than the voltage at OCSET, an overcurrent condition occurs and the soft start cycle is initiated. The synchronous switch turns off and SS/$\overline{\text{SHDN}}$ starts to sink 2µA. When SS/$\overline{\text{SHDN}}$ reaches 0.8V, it then starts to source 10µA and a new cycle begins.

Hiccup Mode

During power up, the SS/$\overline{\text{SHDN}}$ pin is internally pulled low until VCC reaches the undervoltage lockout level of 4.2V. Once V_{CC} has reached 4.2V, the SS/$\overline{\text{SHDN}}$ pin is released and begins to source 10µA of current to the external soft-start capacitor. As the soft-start voltage rises, the output of the internal error amplifier is clamped to this voltage. When the error signal reaches the level of the internal triangular oscillator, which swings from 1V to 2V at a fixed frequency of 200kHz/500kHz, switching occurs. As the error signal crosses over the oscillator signal, the duty cycle of the PWM signal continues to increase until the output comes into regulation. If an over-current condition has not occurred the soft-start voltage will continue to rise and level off at about 2.2V.

An over-current condition occurs when the high-side drive is turned on, but the PHASE node does not reach the voltage level set at the OCSET pin. The PHASE node is sampled only once per cycle during the valley of the triangular oscillator. Once an over-current occurs, the high-side drive is turned off and the low-side drive turns on and the SS/$\overline{\text{SHDN}}$ pin begins to sink 2µA. The soft-start voltage will begin to decrease as the 2µA of current discharges the external capacitor. When the soft-start voltage reaches 0.8V, the SS/$\overline{\text{SHDN}}$ pin will begin to source 10µA and begin to charge the external capacitor causing the soft-start voltage to rise again. Again, when the soft-start voltage reaches the level of the internal oscillator, switching will occur.

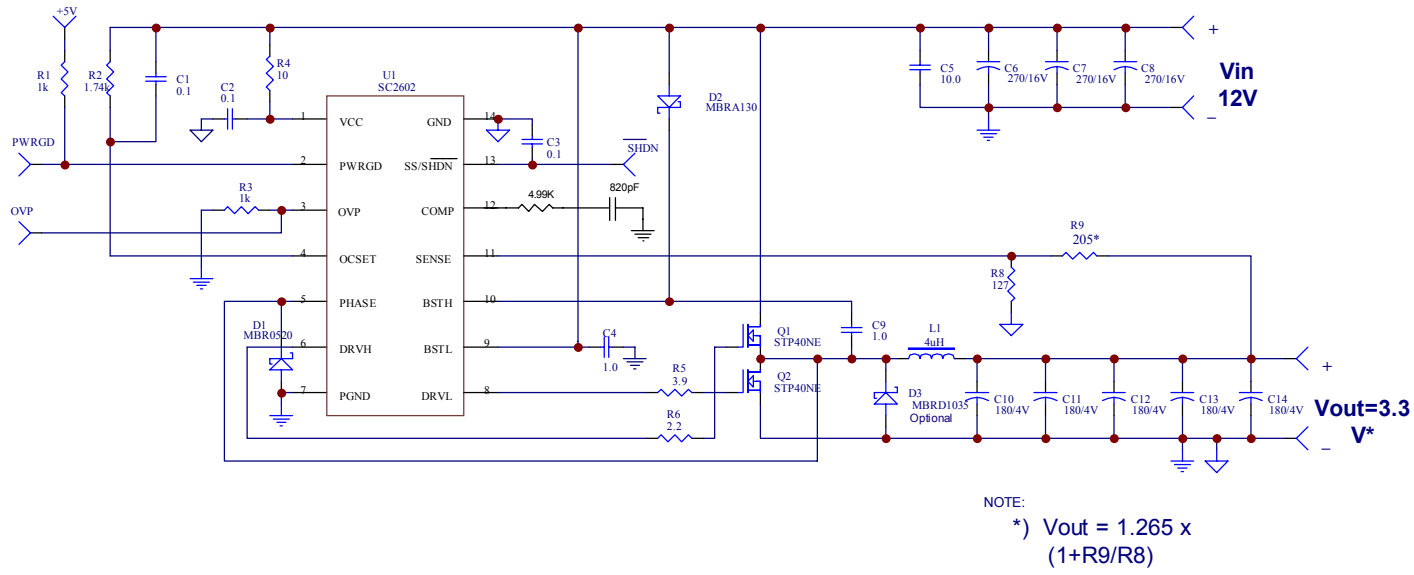
If the over-current condition is no longer present, normal operation will continue. If the over-current condition is still present, the SS/$\overline{\text{SHDN}}$ pin will again begin to sink 2µA. This cycle will continue indefinitely until the over-current condition is removed.

In conclusion, below is shown a typical “12V Application Circuit” which has a BSTH voltage derived by bootstrapping input voltage to the PHASE node through diode D1. This circuit is very useful in cases where only input power of 12V is available.

In order to prevent substrate glitching, a small-signal diode should be placed in close proximity to the chip with cathode connected to PHASE and anode connected to PGND.

Application Circuit

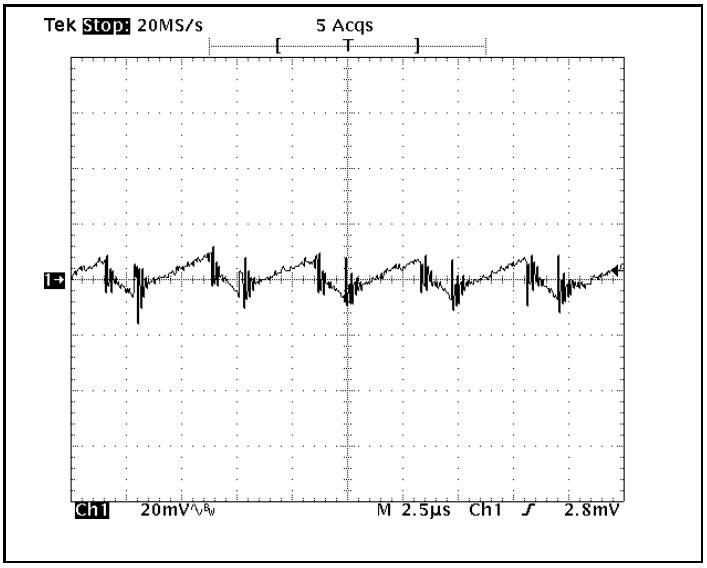
Typical 12V Application Circuit with Bootstrapped BSTH

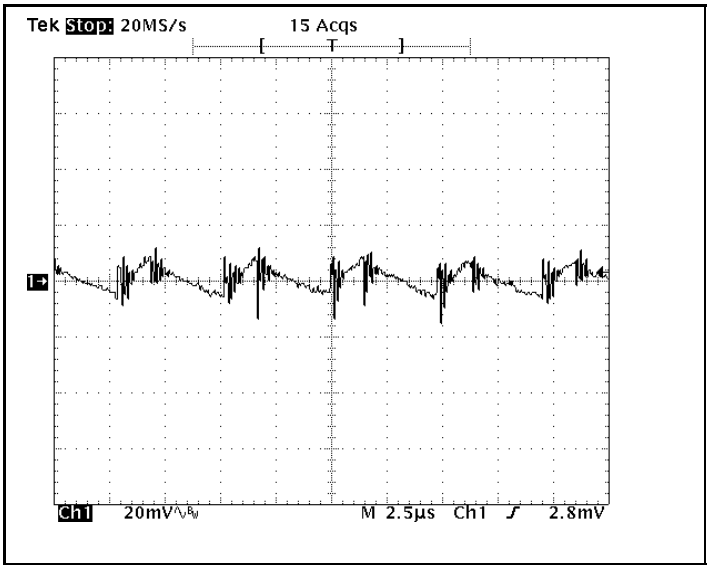


Typical Characteristics

Output Ripple Voltage
Ch1: Vo_rpl

1. V_{IN} = 5V; V_O = 3.3V; I_{OUT} = 12A

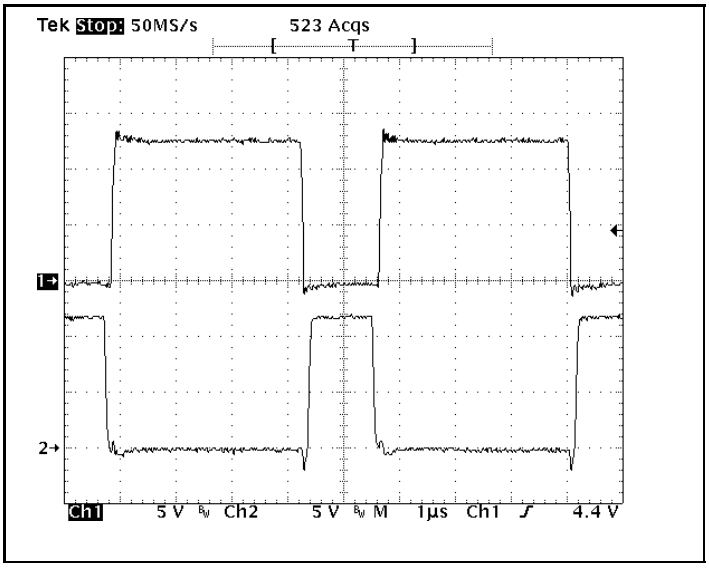


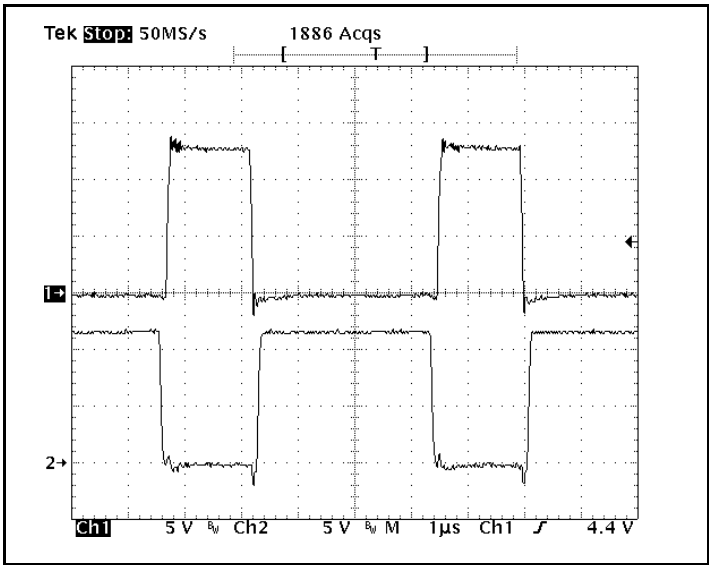


Ch1: Vo_rpl
2. V_{IN} = 5V; V_{OUT} = 1.3V; I_{OUT} = 12A

Wave forms are shown for SC2602 and are similiar for SC2602A but at higher frequency.

Gate Drive Waveforms
Ch1: Top FET
Ch2: Bottom FET

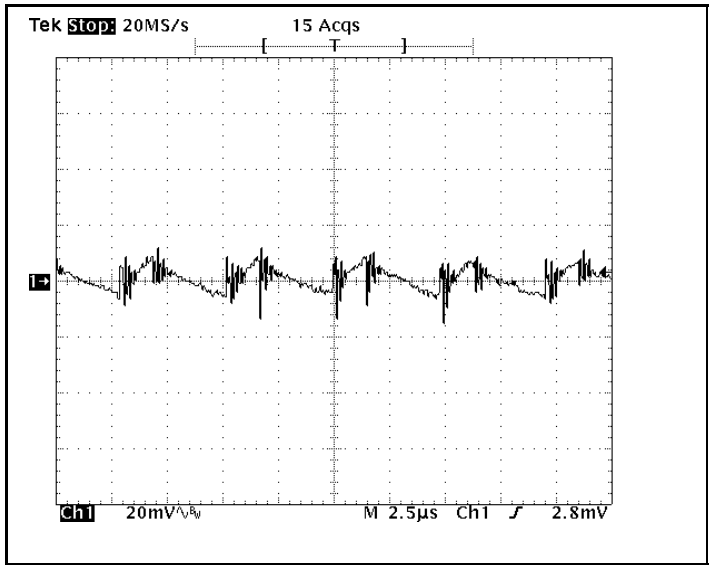




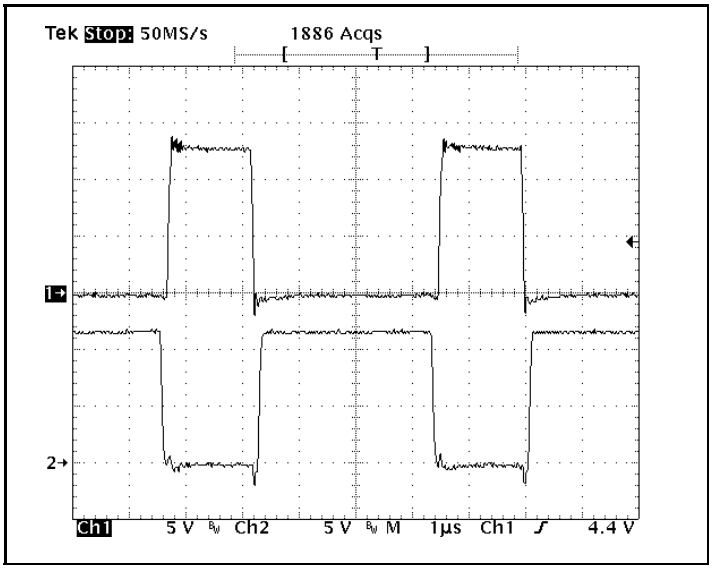
Ch1: Top FET
Ch2: Bottom FET

Typical Characteristics (Cont.)

Ch1: Vo_rpl
2. V_{IN} = 5V; V_{OUT} = 1.3V; I_{OUT} = 12A

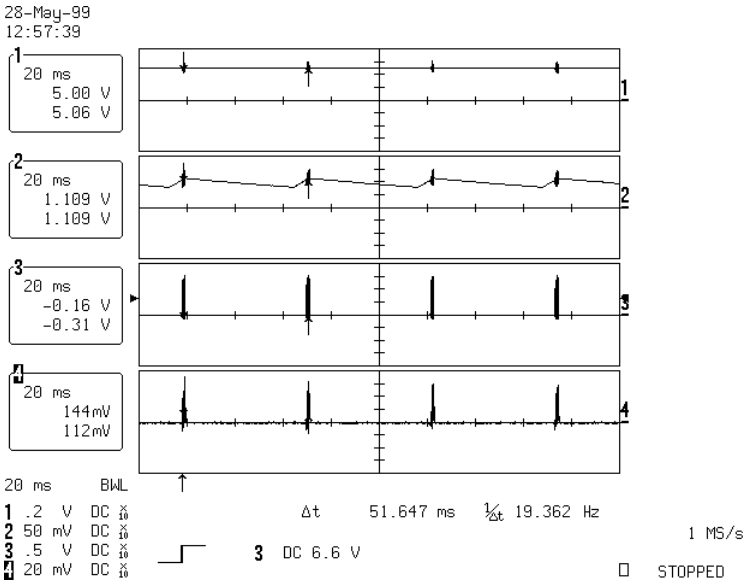


Ch1: Top FET
Ch2: Bottom FET



Typical Characteristics (Cont.)

Hiccup Mode

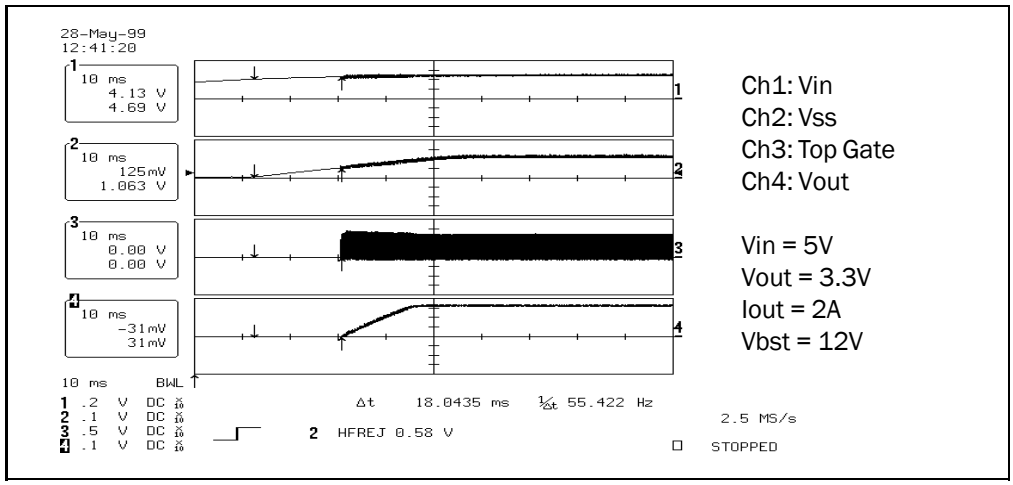


Ch1: Vin
Ch2: Vss
Ch3: Top Gate
Ch4: Vout

Vin = 5V
Vout = 3.3V
Vbst = 12V

Iout = S.C.

Start Up Mode



Ch1: Vin
Ch2: Vss
Ch3: Top Gate
Ch4: Vout

Vin = 5V
Vout = 3.3V
Iout = 2A
Vbst = 12V

Typical Characteristics (Cont.)

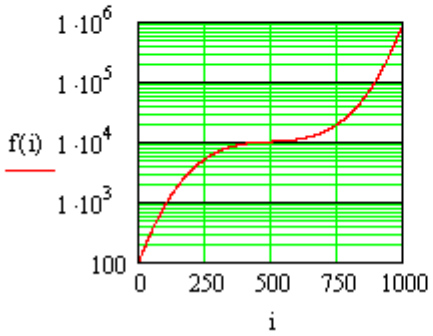
Math Cad Close Loop Stability Analysis

General Equationsl Sample Frequencies Calculations

$i := 1,2..10^3$

$Fc := 10 \cdot 10^3$

$f(i) := Fc \cdot 1.0005^{i-500+10^{-4.16}\cdot(i-500)^3}$

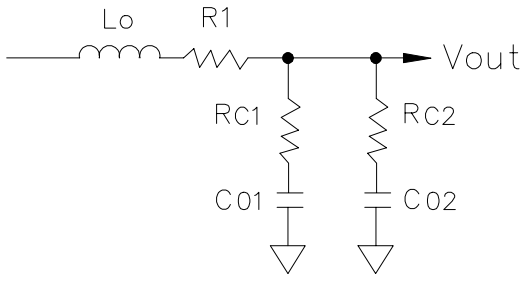


$g(i) := if\left(i - 900 \geq 0, \frac{i - 900}{100}, 0\right)$

$j := (-1)^5$

$W(i) := 2 \cdot \pi \cdot j \cdot f(i)$

Output Filter Schematic:



Typical Characteristics (Cont.)

Output filter calculation

$$Lo := 4.3\cdot10^{-6} \quad R1 := 5\cdot10^{-3} \quad Co1 := 1500\cdot10^{-6} \quad Rc1 := 20\cdot10^{-3} \quad Co2 := 100\cdot10^{-6} \quad Rc2 := 1\cdot10^{-3}$$

$$Zc1(i) := Rc1 + \frac{1}{Co1\cdot W(i)} \qquad Zc2(i) := Rc2 + \frac{1}{Co2\cdot W(i)} \qquad Zc(i) := \frac{Zc1(i)\cdot Zc2(i)}{Zc1(i) + Zc2(i)}$$

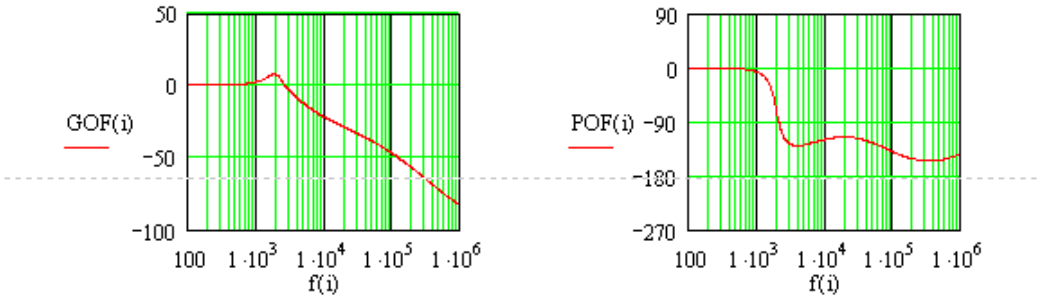
$$OF(i) := \frac{Zc(i)}{R1 + Lo\cdot W(i) + Zc(i)} \qquad Gof(i) := \left(Re(OF(i))^2 + Im(OF(i))^2\right)^{.5}$$

$$GOF(i) := 20\cdot\log(Gof(i))$$

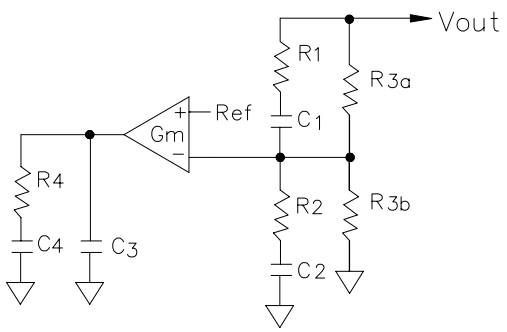
$$C(i) := \frac{Re\left(OF(i)\cdot j^{g(i)}\right)}{Gof(i)} \qquad S(i) := \frac{Im\left(OF(i)\cdot j^{g(i)}\right)}{Gof(i)}$$

$$POF(i) := \frac{360}{2\cdot\pi}\cdot acos(C(i))\cdot if(S(i) \geq 0, 1, -1) + 180\cdot if(S(i) \geq 0, -2, 0) - 90\cdot g(i)$$

Output Filter Plots



Error Amplifier Schematic



Typical Characteristics (Cont.)

Error Amplifier calculation

$R3a := 10 \cdot 10^{3}$ $R1 := .1 \cdot 10^{3}$ $R2 := .1 \cdot 10^{3}$ $R4 := 15 \cdot 10^{3}$ $C3 := .01 \cdot 10^{-9}$

$R3b := 10 \cdot 10^{3}$ $C1 := 30 \cdot 10^{-9}$ $C2 := 1000 \cdot 10^{-9}$ $C4 := 100 \cdot 10^{-9}$ $Gm := 1.5 \cdot 10^{-3}$

$$Z1(i) := \frac{R3a \cdot \left(R1 + \frac{1}{C1 \cdot W(i)}\right)}{R3a + R1 + \frac{1}{C1 \cdot W(i)}} \qquad Z2(i) := \frac{R3b \cdot \left(R2 + \frac{1}{C2 \cdot W(i)}\right)}{R3b + R2 + \frac{1}{C2 \cdot W(i)}} \qquad Z3(i) := \frac{\left(R4 + \frac{1}{C4 \cdot W(i)}\right) \cdot \frac{1}{C3 \cdot W(i)}}{R4 + \frac{1}{C4 \cdot W(i)} + \frac{1}{C3 \cdot W(i)}}$$

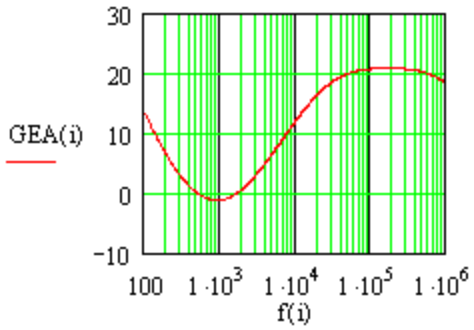
$$EA(i) := -\frac{Z2(i)}{Z1(i) + Z2(i)} \cdot Z3(i) \cdot Gm \qquad Gea(i) := \left(Re(EA(i))^{2} + Im(EA(i))^{2}\right)^{.5}$$

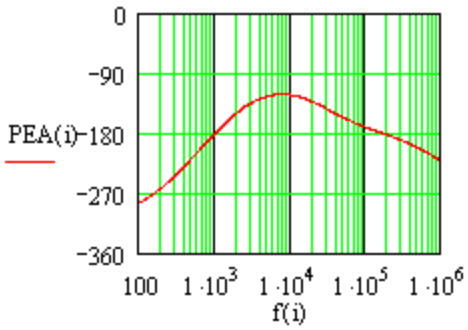
$$GEA(i) := 20 \cdot \log(Gea(i))$$

$$C(i) := \frac{Re\left(EA(i) \cdot j^{g(i)}\right)}{Gea(i)} \qquad S(i) := \frac{Im\left(EA(i) \cdot j^{g(i)}\right)}{Gea(i)}$$

$$PEA(i) := \frac{360}{2 \cdot \pi} \cdot acos(C(i)) \cdot if(S(i) \geq 0, 1, -1) + 180 \cdot if(S(i) \geq 0, -2, 0) - 90 \cdot g(i)$$

Error Amplifier plots





Typical Characteristics (Cont.)

Close Loop Calculation

$Vin := 3.3$

$Vpp := \frac{1}{1.7}$

$CL(i) := OF(i) \cdot EA(i) \cdot \frac{Vin}{Vpp}$

$Gcl(i) := \left(Re(CL(i))^2 + Im(CL(i))^2\right)^{.5}$

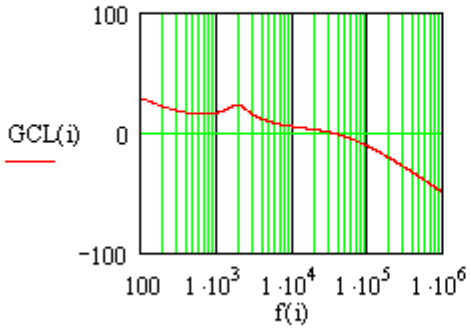
$GCL(i) := 20 \cdot \log(Gcl(i))$

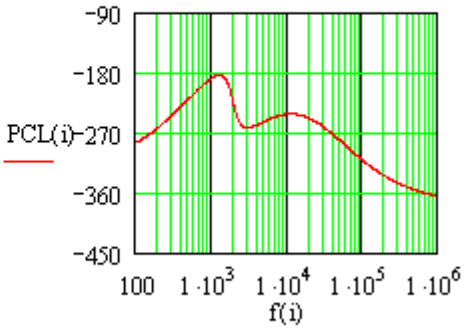
$C(i) := \frac{Re\left(CL(i) \cdot j^{g(i)}\right)}{Gcl(i)}$

$S(i) := \frac{Im\left(CL(i) \cdot j^{g(i)}\right)}{Gcl(i)}$

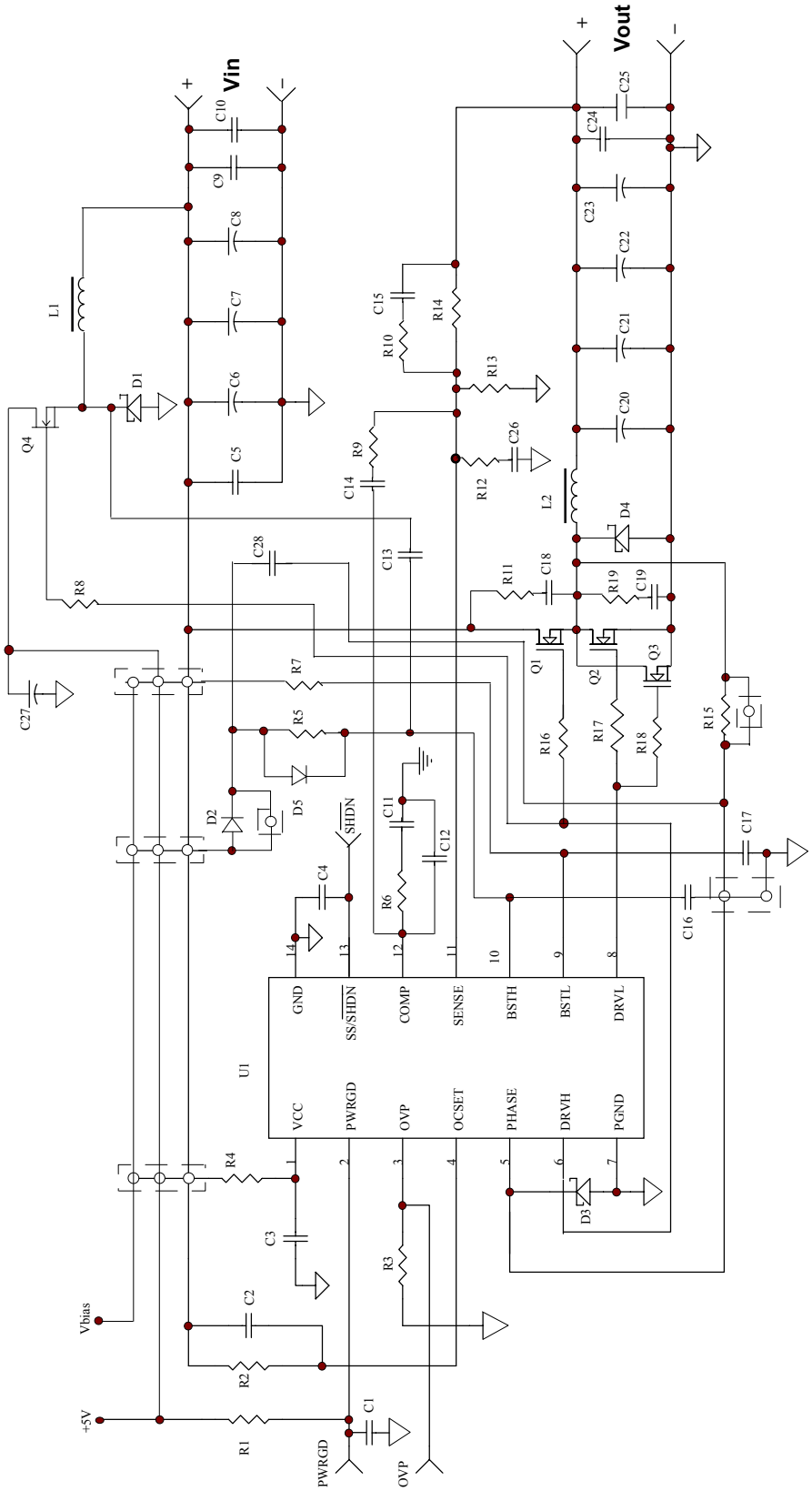
$PCL(i) := \frac{360}{2 \cdot \pi} \cdot acos(C(i)) \cdot if(S(i) \geq 0, 1, -1) + 180 \cdot if(S(i) \geq 0, -2, 0) - 90 \cdot g(i)$

Close Loop plots



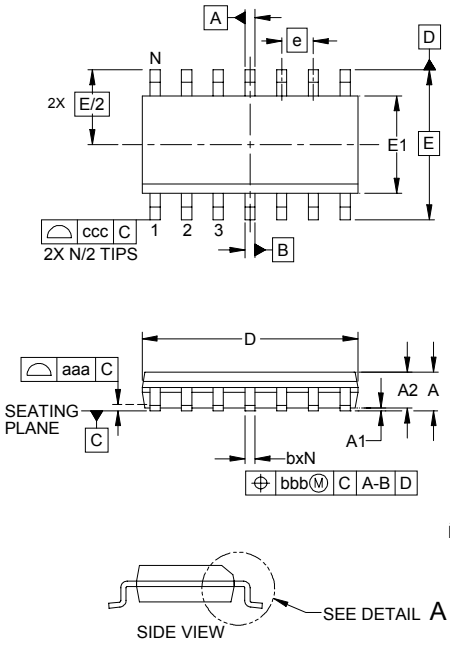


Evaluation Board Schematic



POWER MANAGEMENT

Outline Drawing - S0-14

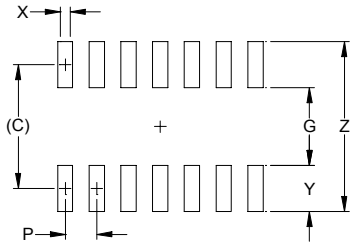


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.004	-	.010	0.10	-	0.25
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.337	.341	.344	8.55	8.65	8.75
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.04)		
N	14			14		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION AB.

Land Pattern - S0-14



DIM	INCHES	MILLIMETERS
C	(.205)	(5.20)
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 302A.

Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805)498-2111 FAX (805)498-3804