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RF2480

DIRECT QUADRATURE MODULATOR

RoHS Compliant & Pb-Free Product
Package Style: SOIC-16

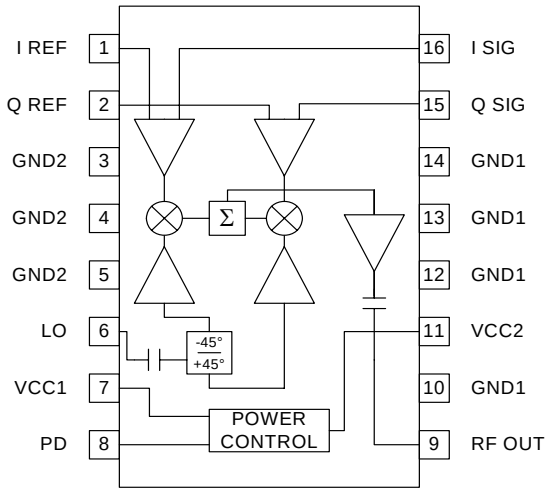


Features

- Typical Carrier Suppression > 35 dBc over temperature with highly linear operation
- Single 5 V Power Supply
- Integrated RF quadrature network
- Digitally controlled Power Down mode
- 800 MHz to 2500 MHz operation

Applications

- Dual-Band CDMA Base Stations
- TDMA/TDMA-EDGE Base Stations
- GSM-EDGE/EGSM Base Stations
- W-CDMA Base Stations
- WLAN and WLL Systems
- TETRA Systems



Functional Block Diagram

Product Description

The RF2480 is a monolithic integrated quadrature modulator IC capable of universal direct modulation for high-frequency AM, PM, or compound carriers. This low-cost IC features excellent linearity, noise floor, and over-temperature carrier suppression performance. The device implements differential amplifiers for the modulation inputs, 90° carrier phase shift network, carrier limiting amplifiers, two matched double-balanced mixers, summing amplifier, and an output RF amplifier which will drive 50Ω from 800 MHz to 2500 MHz. Component matching is used to obtain excellent amplitude balance and phase accuracy.

Ordering Information

RF2480	Direct Quadrature Modulator
RF2480 PCBA	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☑ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +7.5	V_{DC}
Input LO and RF Levels	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

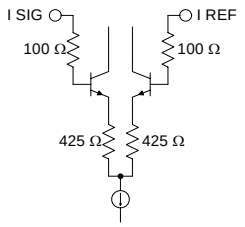
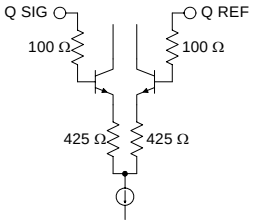
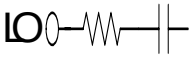
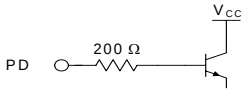
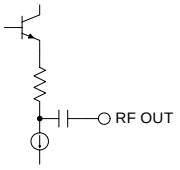
RoHS status based on EUDirective2002/95/EC (at time of this document revision).

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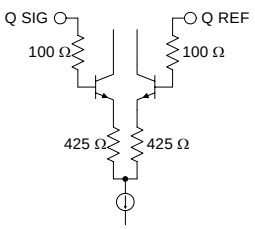
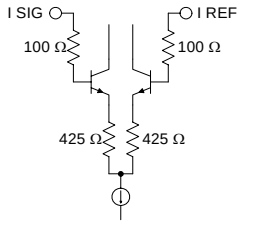
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Carrier Input					T=25°C, V_{CC}=5V
Frequency Range	800		2500	MHz	
Power Level	-6		+6	dBm	
Input VSWR		4.5:1			At 900MHz unmatched
		2:1			At 1800MHz unmatched
		2:1			At 2500MHz unmatched
Modulation Input					
Frequency Range	DC		250	MHz	
Reference Voltage (V_{REF})		3.0		V	
Maximum Modulation (I&Q)			V_{REF}±1.0	V	
Gain Asymmetry		0.2		dB	
Quadrature Phase Error		3		°	
Input Resistance		30		kΩ	
Input Bias Current			40	μA	
RF Output (~800MHz)					LO=800MHz, -5dBm; SSB
Maximum Output Power	-3	0	+2	dBm	TETRA I&Q Amplitude=2V_{PP} Over operating temperature.
High-Linearity Output Power	-6	-5		dBm	TETRA I&Q Amplitude=1.1V_{PP} with an ACPR of -47dBc. Over operating temperature.
Adjacent Channel Power Rejection	-47	-52		dBc	TETRA modulation applied with P_{OUT}=-5dBm. Over operating temperature.
Output P1dB	+2	+3		dBm	Over operating temperature.
IM3 Suppression	-39	-40		dBc	2kHz offset (9kHz, 11kHz) at -6dBm/tone. Over operating temperature.
IM5 Suppression	-49	-59		dBc	2kHz offset (9kHz, 11kHz) at -6dBm/tone. Over operating temperature.
IM7 Suppression	-49	-71		dBc	2kHz offset (9kHz, 11kHz) at -6dBm/tone. Over operating temperature.
Carrier Suppression	-25	-30		dBc	Unadjusted performance.
Sideband Suppression	-25	-30		dBc	Unadjusted performance.
Broadband Noise Floor		-150	-145	dBm/Hz	26MHz offset with TETRA signal applied P_{OUT}=-5dBm.

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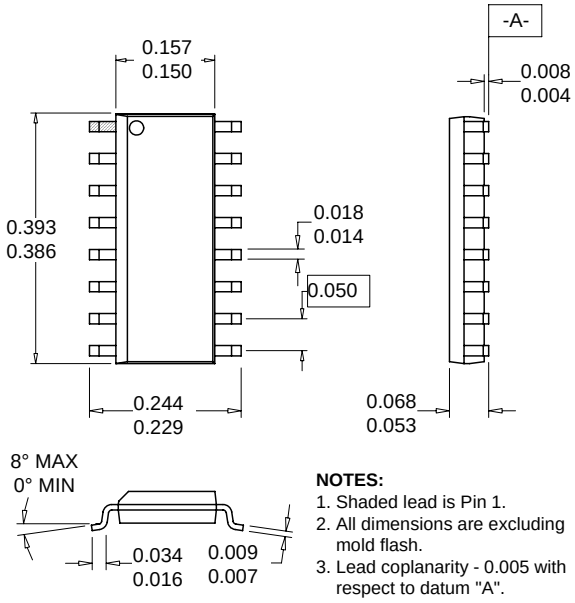
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
RF Output (~900MHz)					LO=880MHz, -5dBm; SSB
Maximum Output Power	0	+4		dBm	I&Q Amplitude=2V_{PP}
High-Linearity Output Power		-11		dBm	I&Q Amplitude=0.325V_{PP}
Carrier Suppression	50			dB	T=25°C; P_{OUT}=-11dBm (meets CDMA base station requirements); optimized I,Q DC offsets
	35			dB	Over Temperature (Temperature cycled from -40°C to +85°C after optimization at T=25°C; P_{OUT}=-11dBm)
Sideband Suppression	50			dB	T=25°C; P_{OUT}=-11dBm; optimized I,Q DC offsets
	35			dB	Over Temperature (Temperature cycled from -40°C to +85°C after optimization at T=25°C; P_{OUT}=-11dBm)
Output Impedance		13-j:25		Ω	
Broadband Noise Floor		-153.0		dBm/Hz	At 20MHz offset, V_{CC}=5V; Tied to V_{REF}: ISIG, QSIG, IREF, and QREF.
RF Output (~2000MHz)					LO=2000MHz, -5dBm; SSB
Maximum Output Power	-7	-3		dBm	I&Q Amplitude=2V_{PP}
High-Linearity Output Power		-17		dBm	I&Q Amplitude=0.325V_{PP}
Carrier Suppression	50			dB	T=25°C; P_{OUT}=-17dBm; optimized I,Q DC offsets
	35			dB	Temperature cycled from -40°C to +85°C after optimization at T=25°C; P_{OUT}=-17dBm
Sideband Suppression	50			dB	T=25°C; P_{OUT}=-17dBm; optimized I,Q DC offsets
	40			dB	Temperature cycled from -40°C to +85°C after optimization at T=25°C; P_{OUT}=-17dBm
Output Impedance		58-j11		Ω	
Broadband Noise Floor		-158.0		dBm/Hz	At 20MHz offset, V_{CC}=5V; Tied to V_{REF}: ISIG, QSIG, IREF, and QREF.
Power Down					
Turn On/Off Time			100	ns	
PD Input Resistance	50			kΩ	
Power Control “ON”			2.8	V	Threshold voltage
Power Control “OFF”	1.0	1.2		V	Threshold voltage
Power Supply					
Voltage		5		V	Specifications
	4.5		6.0	V	Operating Limits
Current		50		mA	Operating
			25	μA	Power Down

Pin	Function	Description	Interface Schematic
1	I REF	Reference voltage for the I mixer. This voltage should be the same as the DC voltage supplied to the I SIG pin. A voltage of 3.0V is recommended. The SIG and REF inputs are inputs of a differential amplifier. Therefore the REF and SIG inputs are interchangeable. If swapping the I SIG and I REF pins, the Q SIG and Q REF also need to be swapped to maintain the correct phase. It is also possible to drive the SIG and REF inputs in a balanced mode. This will increase the gain. For optimum carrier suppression, the DC voltages on I REF, Q REF, I SIG and Q SIG should be adjusted slightly to compensate for inherent undesired internal DC offsets; for optimum sideband suppression, phase and signal amplitude on IREF, Q REF, I SIG and Q SIG should be adjusted slightly to compensate for inherent undesired internal offsets. See RFMD AN0001 for more detail.	
2	Q REF	Reference voltage for the Q mixer. This voltage should be the same as the DC voltage supplied to the Q SIG pin. A voltage of 3.0V is recommended. See pin 1 for more details.	
3	GND2	Ground connection of the LO phase shift network. This pin should be connected directly to the ground plane.	
4	GND2	Same as pin 3.	
5	GND2	Same as pin 3.	
6	LO	The input of the phase shifting network. This pin has an internal DC blocking capacitor. This port is voltage driven so matching at different frequencies is not required.	
7	VCC1	Power supply for all circuits except the RF output stage. An external capacitor is needed if no other low frequency bypass capacitor is nearby.	
8	PD	Power Down control. When this pin is "low", all circuits are shut off. A "low" is typically 1.2V or less at room temperature.When this pin is "high" (V_{CC}), all circuits are operating normally. If PD is below V_{CC}, output power and performance will be degraded. Operating in this region is not recommended, although it might be useful in some applications where power control is required.	
9	RF OUT	RF Output. This pin has an internal DC blocking capacitor. At some frequencies, external matching may be needed to optimize output power.	
10	GND3	Ground connection for the RF output stage. This pin should be connected directly to the ground plane.	
11	VCC2	Power supply for the RF output amplifier. An external capacitor is needed if no other low frequency bypass capacitor is near by.	
12	GND1	Ground connection for the LO and baseband amplifiers, and for the mixers. This pin should be connected directly to the ground plane.	
13	GND1	Same as pin 12.	
14	GND1	Same as pin 12.	

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Pin	Function	Description	Interface Schematic
15	Q SIG	Baseband input to the Q mixer. This pin is DC-coupled. Maximum output power is obtained when the input signal has a peak to peak amplitude of 2V; for highly linear operation, the input signal (and output power) must be reduced appropriately. The recommended DC level for this pin is 3.0V. The peak minimum voltage on this pin (V_{REF} - peak modulation amplitude) should never drop below 2.0V. The peak maximum voltage on this pin (V_{REF} + peak modulation amplitude) should never exceed 4.0V. See pin 1 for more details.	
16	I SIG	Baseband input to the I mixer. This pin is DC-coupled. Maximum output power is obtained when the input signal has a peak to peak amplitude of 2V; for highly linear operation, the input signal (and output power) must be reduced appropriately. The recommended DC level for this pin is 3.0V. The peak minimum voltage on this pin (V_{REF} - peak modulation amplitude) should never drop below 2.0V. The peak maximum voltage on this pin (V_{REF} + peak modulation amplitude) should never exceed 4.0V. See pin 1 for more details.	

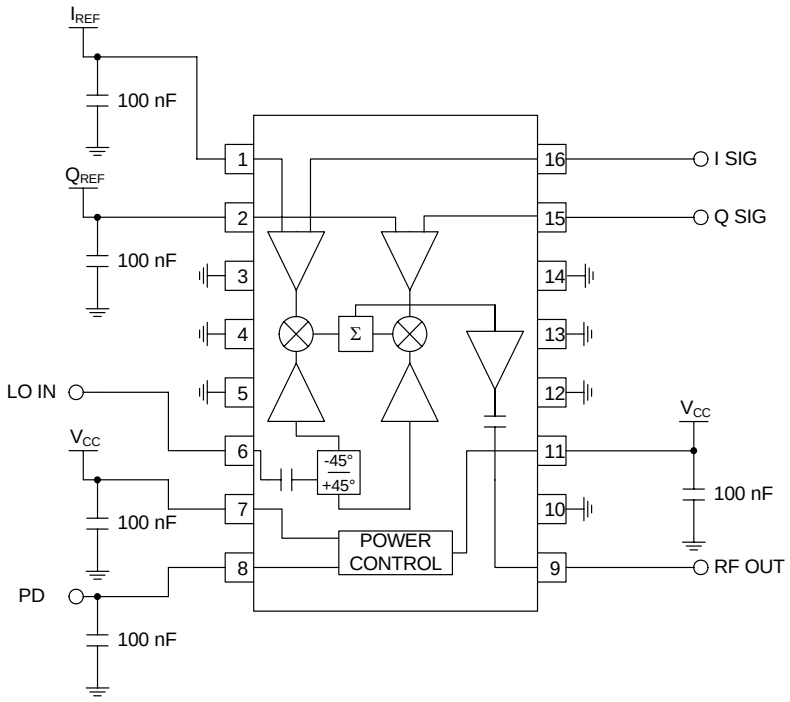
Package Drawing



NOTES:
1. Shaded lead is Pin 1.
2. All dimensions are excluding mold flash.
3. Lead coplanarity - 0.005 with respect to datum "A".

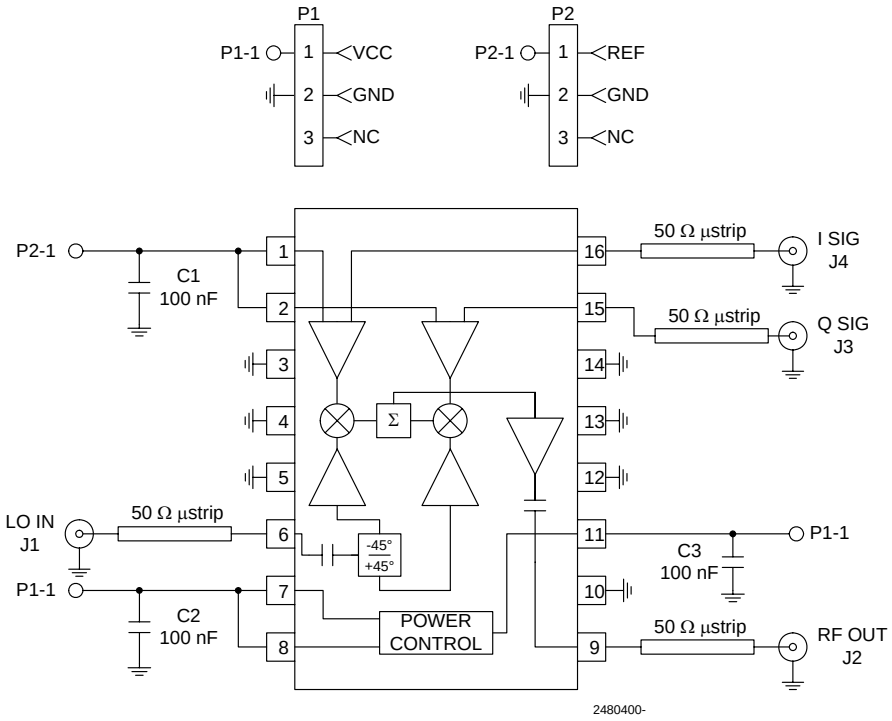
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Application Schematic
DC-Coupled

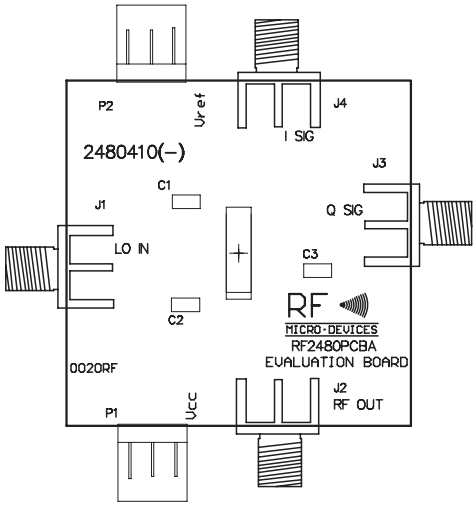


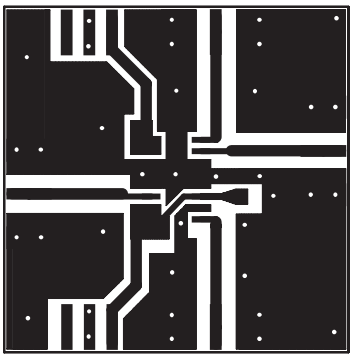
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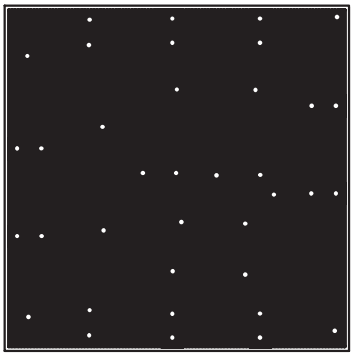
Evaluation Board Schematic



Evaluation Board Layout
Board Size 1.510" x 1.510"
Board Thickness 0.031", Board Material FR-4







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