GDU 90-20422

Gate Drive Unit

Replaces March 1998 version, DS4566-2.1

DS4566-3.0 January 2000

This datasheet should be used in conjunction with the application note AN4571, GDU9X-XXXXX Series, Gate Drive Unit.

APPLICATIONS

■ Used with Gate Turn-Off Thyristors in high current switching applications

KEY PARAMETERS

I_{FGM}	**30A**
$I_{G(ON)}$	**7A**
dI_{GQ}/dt	**40A/µs**

CONDITIONS - (UNLESS STATED OTHERWISE)

V_1 = +5V	V_2 = +15V	V_3 = -15V
Test circuit GTO	DG646BH	
GDU connection to GTO	500mm CO - AX cable type RC5327230	
Test circuit emitter and gate drive emitter	Honeywell sweetspot HFE 4020 - 013	
Test circuit emitter current	30mA	
Test circuit receiver and gate drive receiver	Honeywell sweetspot HFD 3029 - 002	

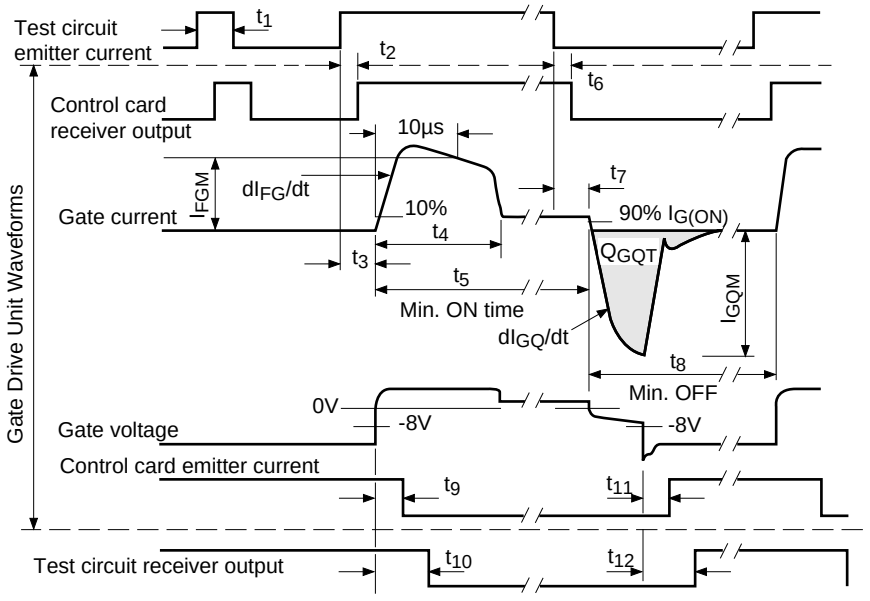
ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{V1}	+5V PSU current	700Hz, 50% duty cycle	-	-	3.80	A
I_{V2}	+15V PSU current	700Hz	-	-	0.73	A
I_{V3}	-15V PSU current	700Hz, I_T = 2000A GTO T_j = 125˚C	-	-	9.20	A
$V_{1(Min)}$	+5V PSU minimum	-	3.8	-	-	V
$V_{2(Min)}$	+15V PSU minimum	-	14.0	-	-	V
$V_{3(Min)}$	-15V PSU minimum	-	14.0	-	-	V
I_{FGM}	Peak forward gate current	-	30	-	-	A
$I_{G(ON)}$	On-state gate current	-	-	7	-	A
dI_{FG}/dt	Rate of rise of positive gate current	Measured 10 - 75% I_{FGM}	-	30	-	A/µs
dI_{GQ}/dt	Rate of rise of negative gate current	I_T = 2000A, 90% $I_{G(ON)}$ - 50% I_{GQM}	-	40	-	A/µs

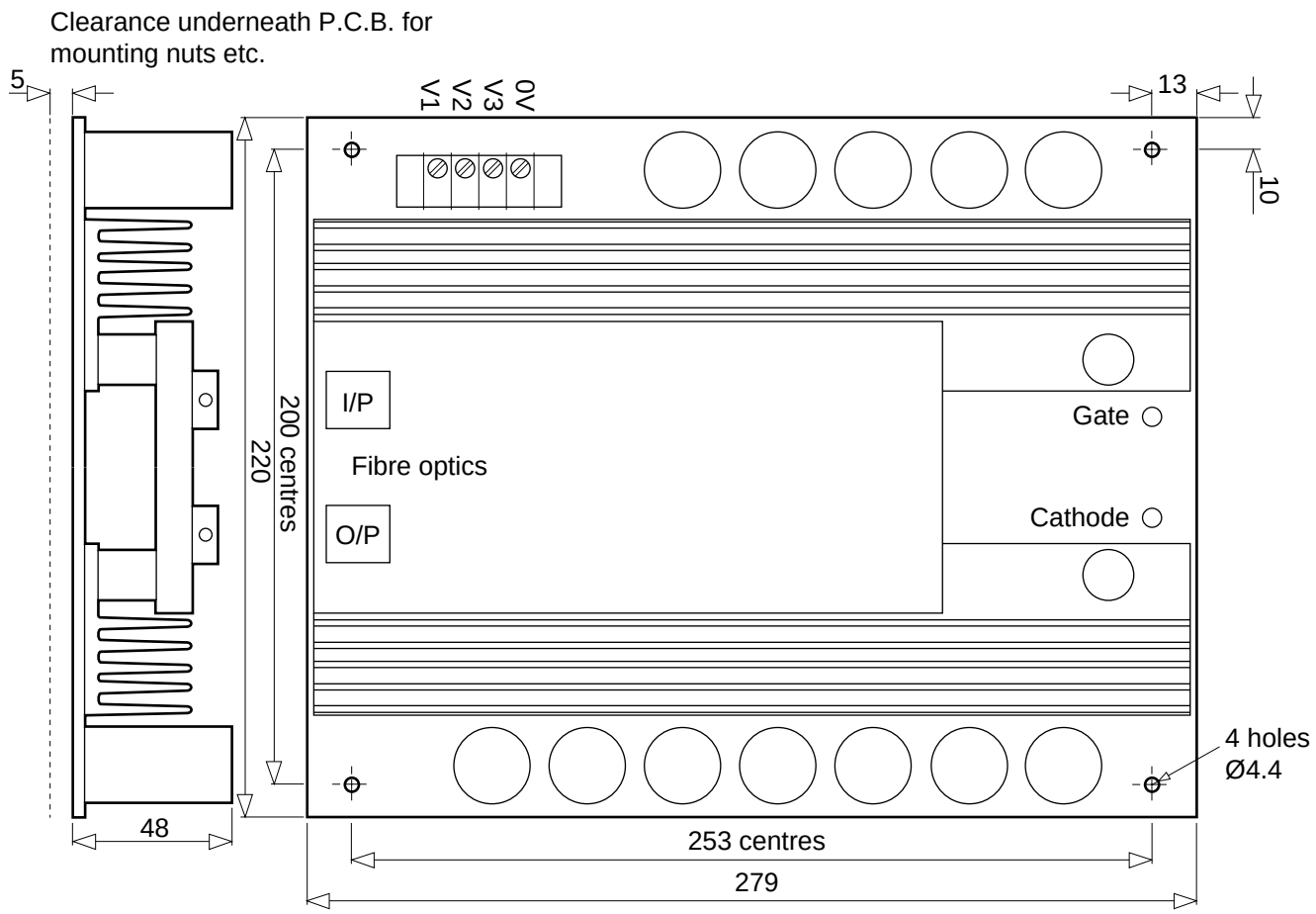
TIMING CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_1*†	No response pulse width of input signal	Adjustable by R81 + R82	2	-	3	µs
t_2	Delay time emitter current to receiver o/p	-	0.4	-	0.8	µs
t_3*†	Turn-on delay emitter current to 10% I_{FGM}	-	5.2	-	6.2	µs
t_4	I_{FGM} pulse width	-	-	25	-	µs
t_5*	Minimum on time 10% I_{FGM} to 90% $I_{G(ON)}$	Adjustable by R37	80	-	110	µs
t_6	Receiver storage time	-	0.5	-	0.9	µs
t_7	Turn-off delay. Emitter current to 90% $I_{G(ON)}$	-	1.5	-	2.3	µs
t_8*	Minimum off time 90% $I_{G(ON)}$ to 10% I_{FGM}	Adjustable by R38	80	-	110	µs
t_9	Delay time Gate volts to o/p emitter current	-	-	0.1	-	µs
t_{10}	Turn-off delay Gate volts to test receiver o/p	-	-	0.7	-	µs
t_{11}	Storage time Gate volts to o/p emitter current	Measured at low I_{GQM}	-	0.1[1]	-	µs
t_{12}	Turn-on delay Gate volts to test receiver o/p	Measured at low I_{GQM}	-	0.8[1]	-	µs

* t_1,t_3,t_5,t_8 are factory settings. † Adjustment of t_1 alters t_3. 1. Varies with I_{GQM} due to gate lead impedance.



OUTLINE



Weight: 1.89Kg

All dimensions in mm, unless stated otherwise. DO NOT SCALE.

POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink / clamping systems in line with advances in device types and the voltage and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group continues to offer high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

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Disc devices require the correct clamping force to ensure their safe operation. The PACs range offers a varied selection of pre-loaded clamps to suit all of our manufactured devices. This include cube clamps for single side cooling of 'T' 22mm

Clamps are available for single or double side cooling, with high insulation versions for high voltage assemblies.

Please refer to our application note on device clamping, AN4839

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Target Information: This is the most tentative form of information and represents a very preliminary specification. No actual design work on the product has been started.

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Advance Information: The product design is complete and final characterisation for volume production is well in hand.

No Annotation: The product parameters are fixed and the product is available to datasheet specification.

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