

Features

- CMOS High Voltage Process: 9V-30V Display Panel Supply Compatible
- 240 Output Channels, Cascadable
- Token-Based Bidirectional Data Transfer: Direct User Control of Scan Rate
- Current Source Magnitude User Control: 4 μ A to 1 mA
- 6-Bit Monochromatic/Color Gray-Scale User Control
- Current matching accuracy: $\pm 2\% \pm 1.5 \mu$ A intra-die $\pm 1\%$ inter-die
- Monochromatic/Color Voltage Precharge Options
- Built-In A-to-D Converter Monitoring of Display Panel Characteristics
- 3.3 V to 5 V logic supply
- Up to 35 MHz clock frequency
- Gold-Bumped Die @ 60 micron Output Pitch
- TCP packaging
- Companion to Clare Micronix MXED202 128-Channel OLED Row Driver

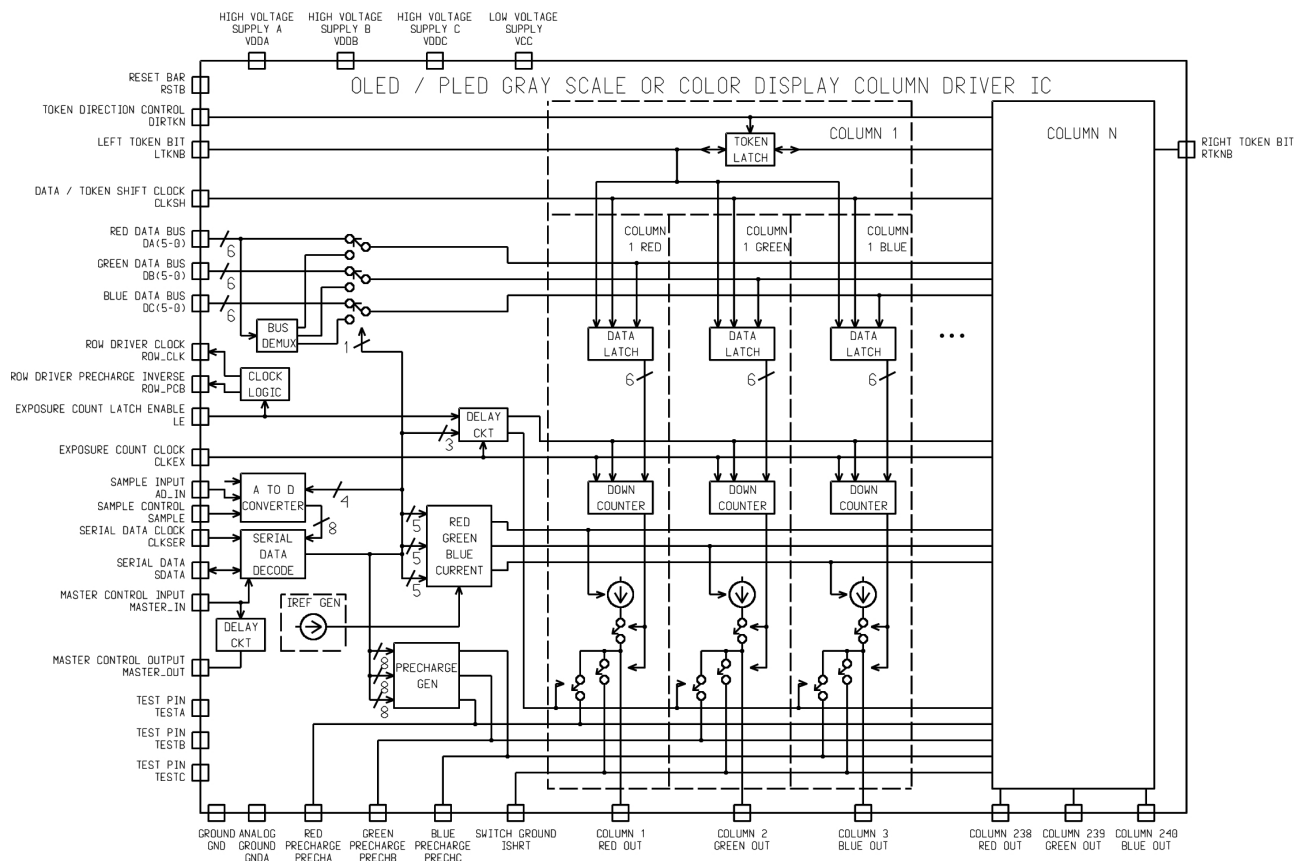
Description

The MXED102 is Clare's second-generation OLED column driver offering, which supports up to 240-mono-chromatic or 80-color OLED pixels. The MXED102's exceptionally tight current-matching of adjacent and cascaded outputs, precharge options, and OLED monitoring capability, ensures uniform luminance and high-quality greyscaling in both monochromatic and RGB mode. This is the first ASSP production driver for OLED module OEM's building a new standard in flat-panel displays.

For All Passive-Matrix Organic-Light-Emitting-Diode Displays

- Monochrome and Color
- Small-Molecule and Polymer
- Current-Sourcing Anode Drivers

Column Driver Block Diagram



Preliminary

PRELIMINARY ELECTRICAL DATA SHEET

This document is a specification for a digital data driver for Passive Matrix Organic Light Emitting Diode (OLED) and Polymer Light Emitting displays (PLED, PolyLED, LEP, . . . ,etc) with anodes connected to the columns. The output stage of each channel has a resistive switch to an on chip generated voltage used during precharge and a current source used during data output to minimize non-uniformity caused by spatial and temporal variations of the LED characteristics and by line resistances. The data driver chip is manufactured in a high voltage (30 V) CMOS process and provided in bumped die and TCP (Tape Carrier Package) form.

Description of Operation:

Overview: The MXED102 is configured via a serial port, and pixel data is updated on a per-row basis via a parallel data bus.

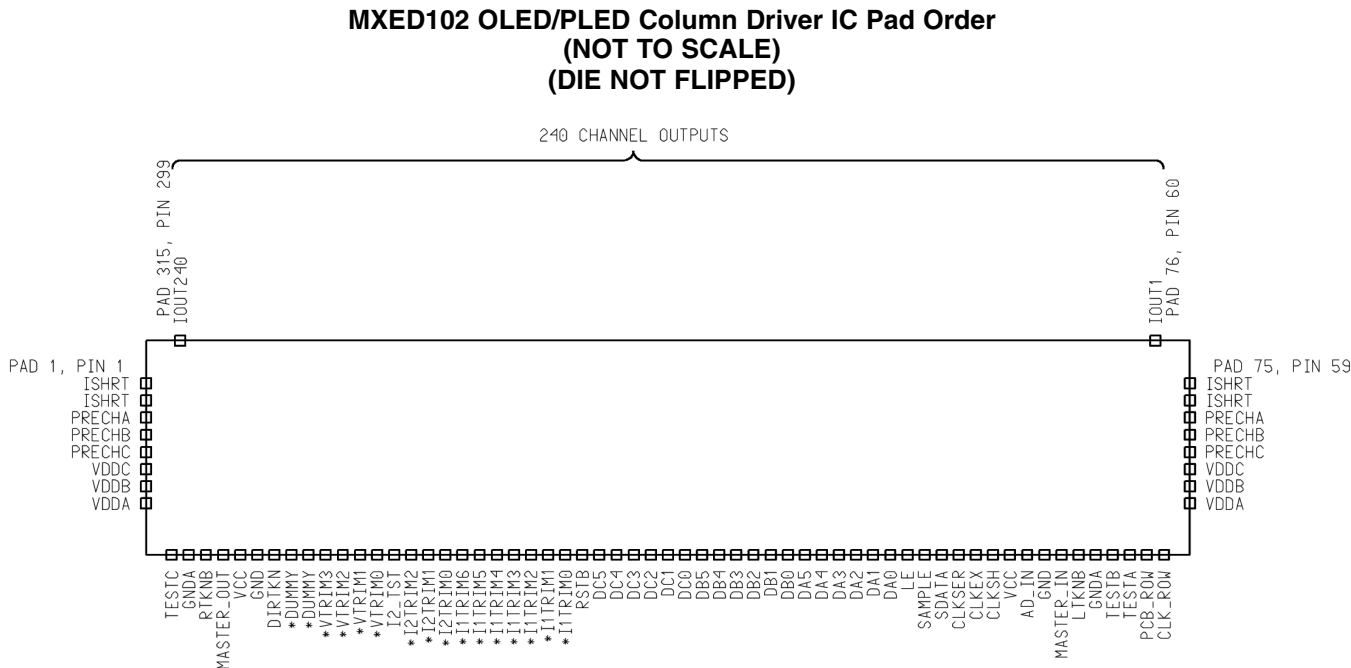
Dynamic Pixel Control: Gray-Scale Control data is loaded into the 6-bit Column Exposure Counters each row scan time, while the previously loaded data is being output to the OLED Display Panel. The control data sets the exposure time from 0 to 63 Exposure Clock times. Successive counters are accessed upon coincidence with the token bit, which is shifted the length of the MXED102 by the Token Shift Clock. In 6-bit Data Mode, Databus C {DC(5-0)} is used to enter per-pixel data, and the Token traverses length of the Chip in 240 Token Shift Clocks. In 18-bit Data Mode, Databusses A, B, and C are used to load three successive pixels in parallel, and the Token traverses length of the Chip in 80 Token Shift Clocks.

Chip Configuration: A display controller may use the serial bus to set the characteristics of all column driver ICs by writing to all column driver ICs in parallel. During write, the controller writes the entire data packet. The controller can also interrogate a single column driver IC, whose MASTER pin is pulled high. Only one column driver IC on a given bus can be designated as master. During read, the controller writes the preamble, start of frame delimiter, register address, and turn around bits. It then tri-states for the bus tri-state and data bits and reads the data.

Color/Monochrome: The MXED102 supports three-each interleaved column Current Magnitude settings and three Precharge Voltages, A,B and C, which may be mapped to R,G,B. Monochrome mode is selected by setting the Color control bit to zero, in which case the Current Magnitude and Precharge Voltage is common.

Package and Pin Out

Below is a diagram of the chip pinout:



Pin List

Name	I/O/A	Description
VDDA, Vddb, VDDC	-	High voltage supply A/B/C:
VCC	-	Logic supply:
GND	-	Ground:
GNDA	-	Analog ground:
ISHRT	-	Ground used to short output channels: There can be high currents on this line. It should be separated from the circuit ground pads (GND) to prevent ground bounce.
PRECHA, PRECHB, PRECHC	O/A	Precharge A/B/C: Column precharge voltage outputs. PRECHA/B/C should be tied to PRECHA/B/C of all other column drivers to ensure a uniform display precharge and should be bypassed to ground with a capacitor at least 50 times the display capacitance.
MASTER_IN	I	Master In: High input implies chip is master. This input is pulled low internally.
MASTER_OUT	O	Master Out: MASTER_IN delayed by 1 LE clock cycle, sampled on rising edge of LE.
RSTB	I	Reset Bar: Input signal used to reset digital logic for test purposes. This input is pulled high internally.
CLKSH	I	Token Shift Clock: Input signal used to shift tokens down the length of the driver IC and latch data into the corresponding columns. The direction of token shift is determined by DIRTKN pin.
LTKNB	I/O	Left Token Bit: Input for shift right, output for shift left. Signal is used to pass the tokens into and out of the driver IC. High state represents the presence of token.
RTKNB	I/O	Right Token Bit: Input for shift left, output for shift right. Signal is used to pass the tokens into and out of the driver IC. High state represents the presence of token.
DIRTKN	I	Token Direction Input: Input signal which, when high, causes the token to shift left to right in the driver IC. A low signal causes the token to shift right to left. In the parallel data mode the token passes through the chip in 80 CLKSH clocks, in the serial data mode the token passes through the chip in 240 CLKSH clocks. This input is pulled high internally.
LE	I	Latch Enable: Input signal used to begin data output. When data output begins, new data input for the following row can begin.
DA(5-0), DB(5-0), DC(5-0)	I	Data A/B/C: Signal buses used to input the exposure data.
CLKEX	I	Exposure Clock: Input signal used to clock the driver IC's exposure counter from 0 to 63 for a row exposure. The signal must be cycled at least 64 times between LE pulses to completely cycle the counter. Cycles of CLKEX beyond 64 will have no effect.
CLKSER	I	Serial Clock: Clock to write serial data into all column drivers or read serial data from the master column driver.
SDATA	I/O	Serial Data: Serial data written to all column drivers or read from the master column driver.
SAMPLE	I	Initiate A/D sample. This input is pulled low internally.

Pin List (continued)

AD_IN	A	A to D Input: The part can do an A to D conversion on the voltage on this input.
TESTA, TESTB, TESTC	A	Test Outputs: The A, B, and C driver bank outputs are muxed to the TESTA, TESTB, and TESTC pads respectively when these pads are pulled low. During normal operation they are left open or tied to VDD.
I1TRIM (6:0)	A	Current Source 1 Trim: These pins must be left open.
I2TRIM (3:0)	A	Current Source 2 Trim: These pins must be left open.
VTRIM (3:0)	A	Voltage Source Trim: These pins must be left open.
I2_TST	A	Current Source 2 Monitor: This pin must be left open.
IOUT(240-1)	A	Channel Outputs: The outputs of the driver IC that directly drives the display panel
CLK_ROW	O	Row Clock: Signal intended to drive the row driver IC shift data clock
PCB_ROW	O	Row Precharge: Signal intended to drive the row driver IC precharge input

Note: A => analog, I => digital input, O => digital output

ELECTRICAL SPECIFICATIONS

Positive currents flow into the part, negative currents flow out of the part, largest currents are currents with the greatest absolute magnitude.

Absolute Maximum Ratings:

Parameter	Operating Condition	Min	Typ	Max	Units
Ambient temp	-	-65	-	155	°C
Low voltage supply	-	-0.3	-	7.0	V
High voltage supply	-	-0.3	-	35.0	V

Operating Conditions:

Unless otherwise stated, all parameters are specified for the following operating conditions.

Parameter	Sym	Operating Condition	Min	Typ	Max	Units
Ambient temp	TA	-	0	-	70	°C
Low voltage supply	VCC	-	3.0	-	5.5	V
High voltage supplies	VDDA, VDDb, VDDC	-	9.0	-	30	V

Supply Currents:

Parameter	Sym	Operating Condition	Min	Typ	Max	Units
High voltage supply current during standby	IDD (stby)	-	-	-	TBD	uA
Internal high voltage supply current during operation	IDD (int)	Current from VDD not flowing out outputs or into precharge circuit Iout = per channel	-	-	14 mA+ 12xIout	mA
Low voltage supply current during standby	ICC (stby)	-	-	-	TBD	uA
Low voltage supply current during operation	ICC	-	-	-	10	mA

Digital Inputs:

Parameter	Sym	Operating Condition	Min	Typ	Max	Units
Input low voltage	VIL	-	-	-	0.5	V
Input high voltage	VIH	-	VCC-0.5	-	-	V
Input current	II	-	-10	-	10	uA

Digital Outputs:

Parameter	Sym	Operating Condition	Min	Typ	Max	Units
Output low voltage	VOL	Iout = 100 uA	-	-	0.4	V
Output high voltage	VOH	Iout = -100 uA	VCC-0.4	-	-	V
Output rise/fall time	TRF	10 to 90 %, Cload=5 pF	-	-	2.0	nS

Serial Configuration Bus:
Bus Operation:

The controller uses the serial bus to set the characteristics of all column driver ICs by writing to all column driver ICs in parallel. During write, the controller writes the entire data packet. The controller can also interrogate a single column driver IC, who's MASTER pin is pulled high. Only 1 column driver IC on a given bus can be designated as master. During read, the controller writes the preamble, start of frame delimiter, register address, and turn around bits. It then tri-states for the bus tri-state and data bits and reads the data.

Data Packet:

The data packet consists of:

- 14 bit preamble of all 1's
- 2 bit start of frame delimiter (SFD)
- 6 bit register address - MSB first
- 1 turn around bit (TA)
- 1 bus tristate (BT)
- 8 bit data packet - MSB first

Write => write data to all column driver ICs

Read => read data from master column driver IC

Data order => Preamble first, data last; MSB first, LSB last

R/W	Preamble	SFD	Reg Address	TA	BT	Data
write	1111 1111 1111 11	00	AAAA AA	0	0	DDDD DDDD
read	1111 1111 1111 11	01	AAAA AA	0	Z	DDDD DDDD

Input Registers

Register Address 0 - Test Register

Eight bits of data can be written to and read from this register in order to test the serial port. This register has no effect on the column driver.

Register Address 1 - Control Register 1

Bit(s)	Name	Description	Default
7	Freeze Master	Modes: 1 => MASTER_OUT pin is not changed 0 => Normal, MASTER_OUT is updated to MASTER_IN on rising edge of LE	0
6	Disable Precharge Driver	Modes: 1 => Precharge circuit is disabled 0 => Normal	0
5	Standby	Modes: 1 => Part is operating normally 0 => Part is in low power standby mode	0
4	Short Channels	Modes: 1 => Channels are all shorted to ground after the CLKEX count reaches 64 0 => Each channel is individually shorted to ground after its current source is tristated	0
3	Color Mode	Modes: 0 => Monochrome mode 1 => Color mode	0
2	Data Mux	Modes: 0 => DA(5-0), DB(5-0), DC(5-0) data words are read serially from the DC(5-0) pins. The DA(5-0) and DB(5-0) pins are unused. 1 => DA(5-0), DB(5-0), DC(5-0) pins used to read their respective data words.	0
1-0	Test Mode(1:0)	Modes: 00 => Normal operation 01 => Test mode 1 10 => Test mode 2 11 => Test mode 3	00

Register Address 2 - Control Register 2

Bit(s)	Name	Description	Default
7-2	Undefined	-	-
1	Fast Conversion	Modes:	-
-	-	0 => Normal operation	0
-	-	1 =>	-
0	High A/D Gain	Modes:	-
-	-	0 => Normal operation	0

Register Address 3 - A Output Group Data Current Magnitude Register

The 5 LSB bits determine the magnitude of A output group current during data output.

Register Address 4 - B Output Group Data Current Magnitude Register

The 5 LSB bits determine the magnitude of B output group current during data output.

Register Address 5 - C Output Group Data Current Magnitude Register

The 5 LSB bits determine the magnitude of C output group current during data output.

Register Address 6 - A Output Group Precharge Voltage Magnitude Register

The 8 bits determine the magnitude of A output group voltage during precharge.

Register Address 7 - B Output Group Precharge Voltage Magnitude Register

The 8 bits determine the magnitude of B output group voltage during precharge.

Register Address 8 - C Output Group Precharge Voltage Magnitude Register

The 8 bits determine the magnitude of C output group voltage during precharge.

Register Address 9 - Precharge Count Register

The 3 LSB bits set the precharge time to 0 to 7 CLKEX clock counts.

Register Address 10- A/D Converter Control Register

This register determines which signal is monitored by the A/D converter.

Bit(s)	Name	Description	Default
7-4	UNDEFINED	-	-
3-0	ad_sel(3:0)	0xF => Measure VDDA (Low Gain) 0xE => Measure TESTA (Low Gain) 0xD => Measure IOOUT231 (Low Gain) 0xC => Measure IOOUT6 (Low Gain) 0xB=> Measure VDDDB (Low Gain) 0xA => Measure TESTB (Low Gain) 0x9 => Measure IOOUT232 (Low Gain) 0x8 => Measure IOOUT7 (Low Gain) 0x7 => Measure VDDC (Low Gain) 0x6 => Measure TESTC (Low Gain) 0x5 => Measure IOOUT233 (Low Gain) 0x4 => Measure IOOUT8 (Low Gain) 0x3 - 0x2 => Undefined 0x1 => Measure AD_IN input (High Gain) 0x0 => Input grounded	0000



Registers 11 thru 63 - Undefined

Output Registers

Register Address 0 - Test Register

Register Address 1 - Status Register 0

Bit(s)	Name	Description	Default
7-0	Undefined	-	-

Register Address 2 - A/D Converter Output Register

Registers 3 thru 63 - Undefined

Power on Reset:

The part contains a power on reset circuit that ensures that the serial bus data registers come up in their default value when VCC is cycled on. This brings up the part in its standby mode.

Digital Timing:

Parameter	Sym	Operating Conditions	Min	Typ	Max	Unit
Shift clock frequency	-	-	-	-	25	MHz
Shift clock minimum high or low pulse width	-	-	16	-	-	nS
Exposure clock frequency	-	Control reg 2, bit 1 = 0	1.0	-	10	MHz
		Control reg 2, bit 1 = 1	-	-	1.0	MHz
Exposure clock minimum high or low pulse width	-	-	80	-	-	nS
Data and token setup/hold time	t_{DSU} , t_{TSU} , t_{DHD} , t_{THD}	-	10	-	-	nS
Latch enable setup/hold time	t_{LSU} , t_{LHD}	-	40	-	-	nS
Token bit output delay	t_{TD}	-	-	-	15	nS
Last data to latch enable time	t_{DLD}	-	200	-	-	nS
Latch disable to new data time	t_{LDD}	-	10	-	-	nS

Precharge Voltage Generator:

Parameter	Sym	Operating Condition	Min	Typ	Max	Unit
Precharge voltage generator voltage and voltage error	V_{PRE}	$V_{PRE} = 30 * N / 256$ for N = reg value, $0 < N < 256$	- 2	0	+ 2	%
		$4 < V_{PRE} < VDD-4$ $-30 \text{ mA} < I_{PRE} < -50 \text{ mA}$				
		$4 < V_{PRE} < VDD-3$ $-5 \text{ mA} < I_{PRE} < -30 \text{ mA}$				
Precharge voltage generator output impedance	-	$5 < V_{PRE} < VDD-4$, $I = -15 \text{ mA}$	-	-	TBD	ohms
Load capacitance	-	-	-	-	5	uF

Output Current Channels:

Parameter	Sym	Operating Condition	Min	Typ	Max	Unit
Channel output impedance during precharge	-	$5 < V_{PRE} < VDD-4$, $V_{PRE} - V_{IOUT} < 4 \text{ V}$	-	-	2000	ohms
Channel output charging current during precharge	-	$5 < V_{PRE} < VDD-4$, $V_{PRE} - V_{IOUT} > 4 \text{ V}$	-2.3	-	-	mA
Driver output current source current and current error	I_{OUT}	$I_{OUT} = -4 \text{ uA} \times 1.2 \times N$ for $N = \text{reg value}$, $0 \leq N < 32$, $0 < V_{IOUT} < VDD-3$	-	-	-	-
		$-20 \text{ uA} < I_{OUT} < -75 \text{ uA}$	-3	-	+3	uA
		$-75 \text{ uA} < I_{OUT} < -1 \text{ mA}$	-4	-	+4	%
Single die, per bank driver output current source matching	-	$0 < V_{IOUT} < VDD-3$, $V_{IOUT} \text{ mismatch} < 2 \text{ V}$	-	-	-	-
		$-20 \text{ uA} < I_{OUT} < -75 \text{ uA}$	-1.5	-	+1.5	uA
		$-75 \text{ uA} < I_{OUT} < -1 \text{ mA}$	-2	-	+2	%
Die to die, per bank average driver output current source matching	-	$0 < V_{IOUT} < VDD-3$, $V_{OUT} \text{ mismatch} < 2 \text{ V}$	-	-	-	-
		$20 \text{ uA} < I_{OUT} < 150 \text{ uA}$	-1.5	-	1.5	uA
		$-150 \text{ uA} < I_{OUT} < -1 \text{ mA}$	-1	-	1	%
Exposure clock rising edge to output going high/low	-	Delay to 50% point	-	-	220	nS
Channel output current rise/fall time	-	10% to 90%	-	-	250	nS
Shorting switch on resistance to ISHRT pin	-	$V_{IOUT} < 8 \text{ V}$	-	-	400	ohms
Shorting switch discharge current to ISHRT pin	-	$V_{IOUT} > 8 \text{ V}$	25	-	-	mA

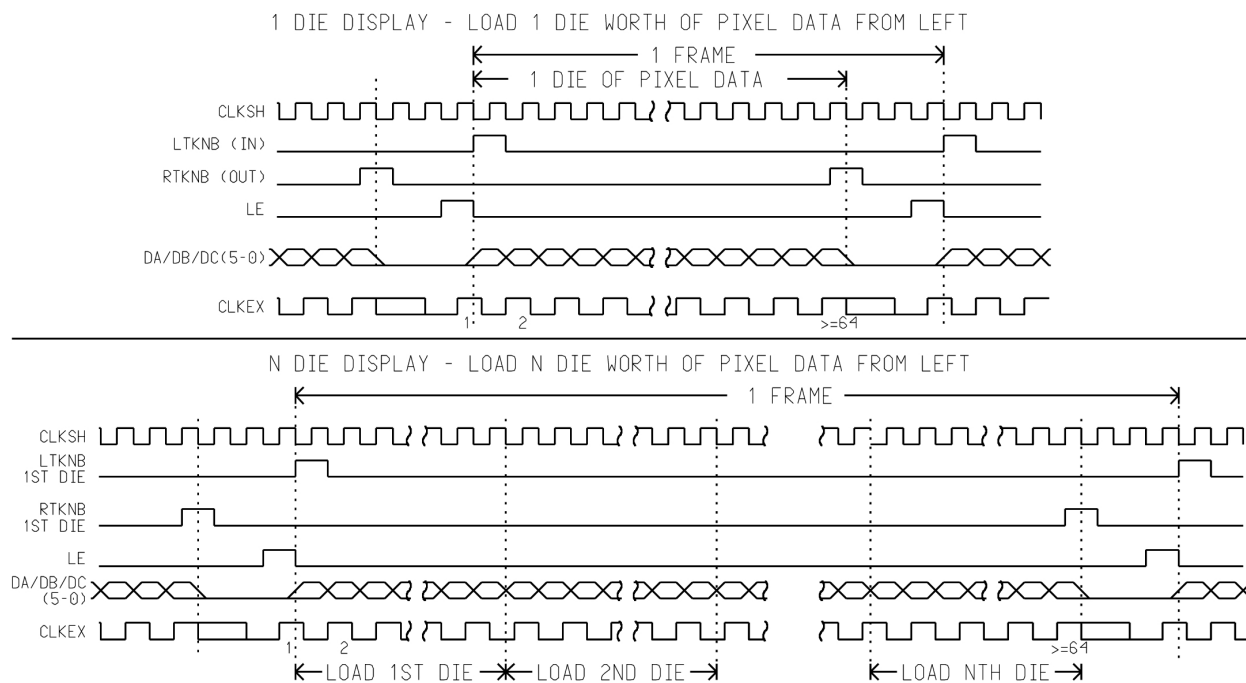
Chip Monitor Analog to Digital Converter:

The ADC is intended to be used to calibrate the precharge circuit. The ADC on the column driver chip designated as the master can be monitored by the controller. Which parameter the ADC is monitoring is determined by the A/D Converter Control Register. Results can be monitored on the A/D Converter Output Register.

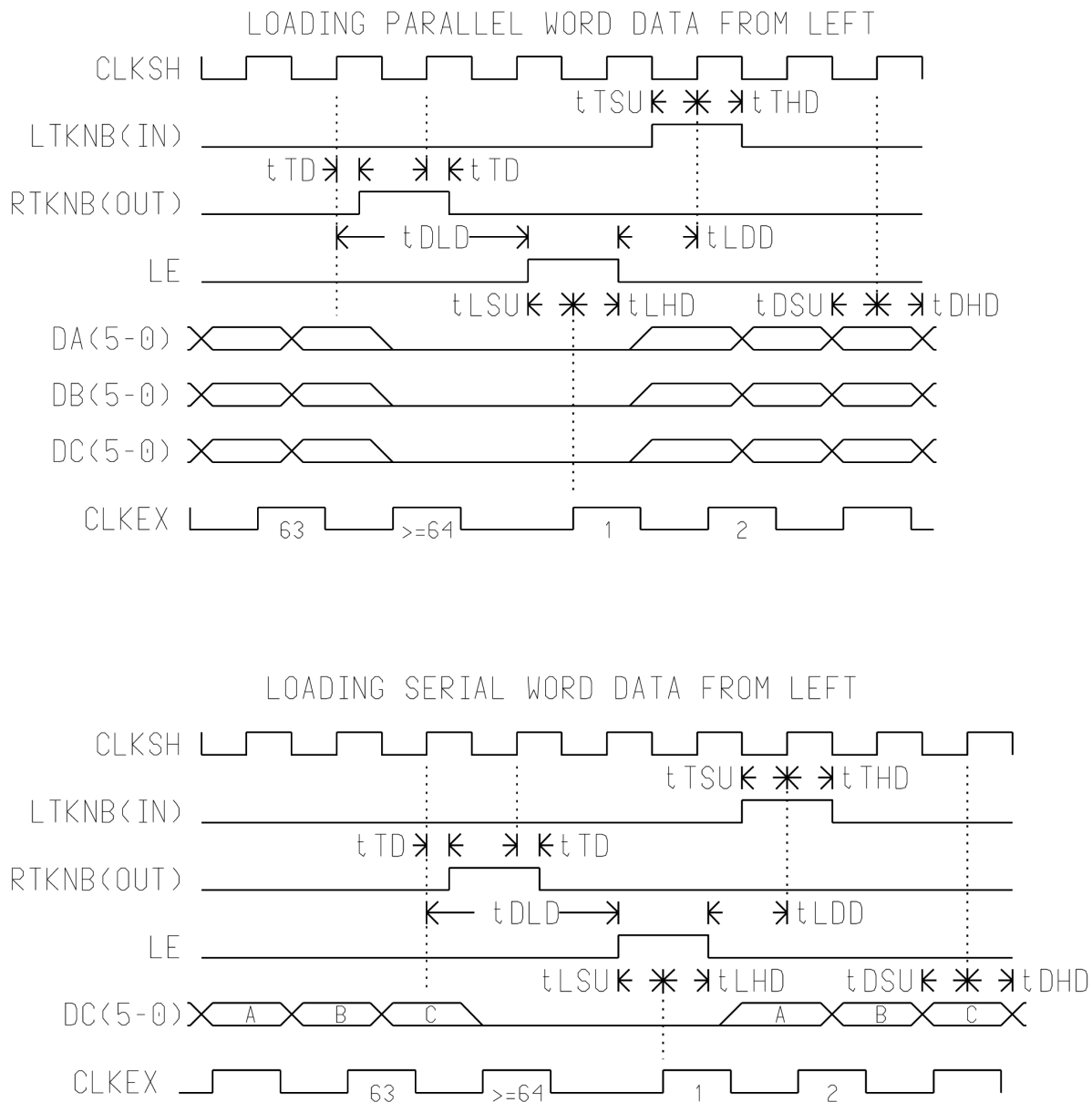
Parameter	Sym	Operating Condition	Min	Typ	Max	Unit
Bits	-	-	-	8	-	-
Linearity	-	-	- .5 LSB	-	.5 LSB	-
Accuracy	-	-	- 1 LSB	-	1 LSB	-
Output for low voltage input	-	$V_{out}(8 \text{ bit word}) = 255 * V_{in} / 5.0$	-	-	-	-
Output for high voltage input	-	$V_{out}(8 \text{ bit word}) = 255 * V_{in} / 30.0$	-	-	-	-
Conversion time in CLKEX counts	-	Control reg 2, bit 1 = 0	896	-	-	CLKEX counts
		Control reg 2, bit 1 = 1	112	-	-	

Timing Diagrams:

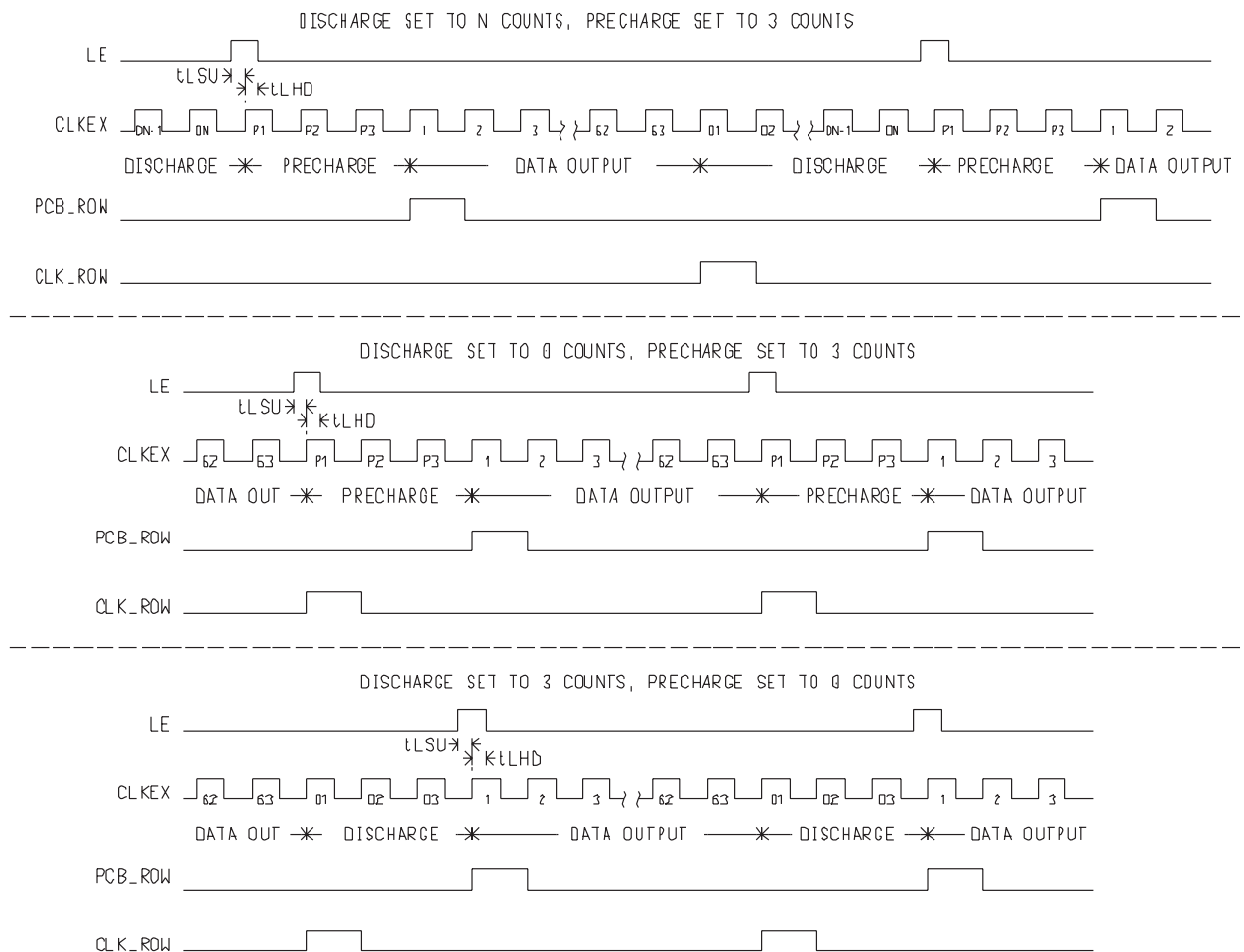
Load Data Pattern Macro Timing



Load Data Pattern Timing

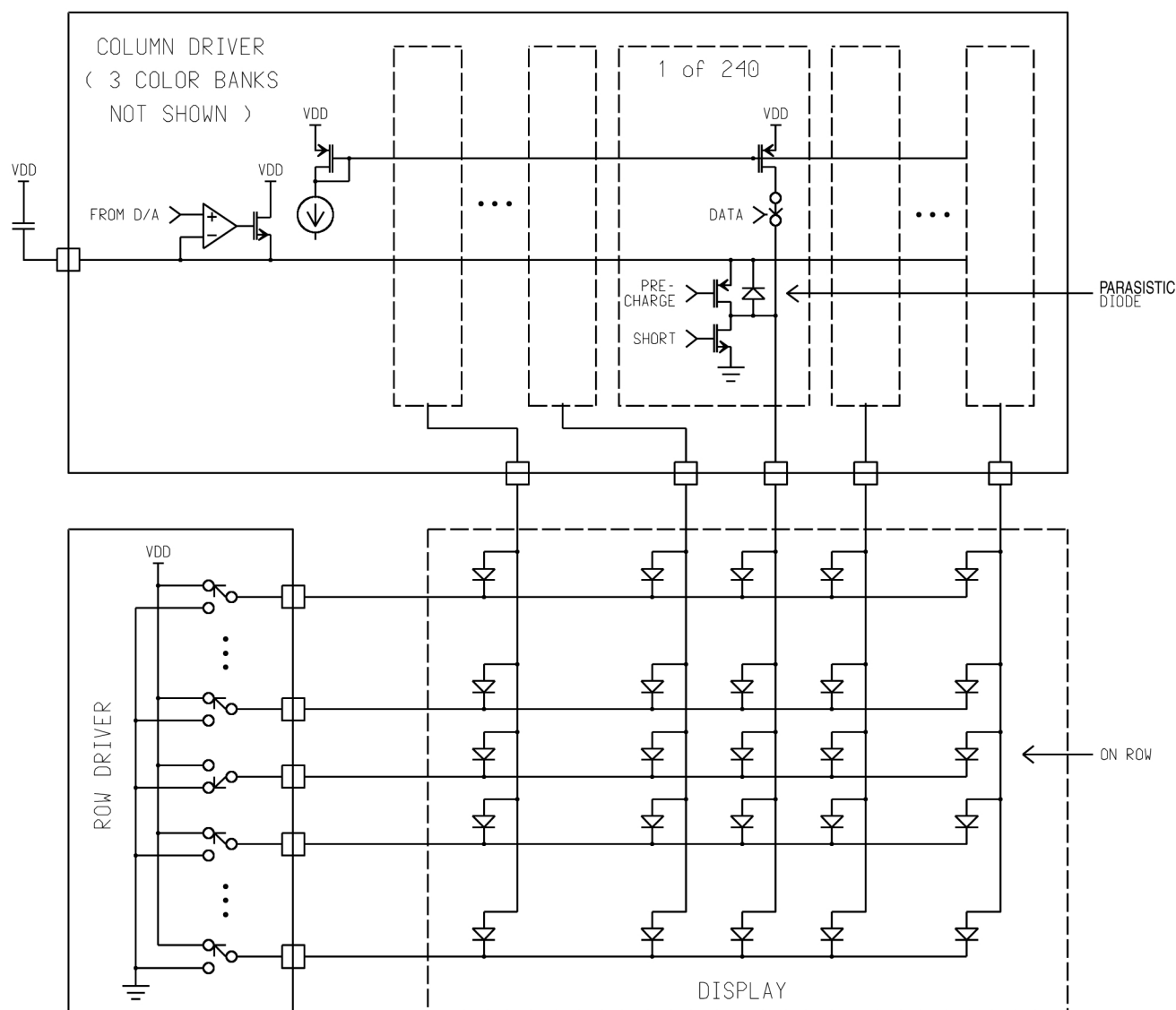


Data Output Timing



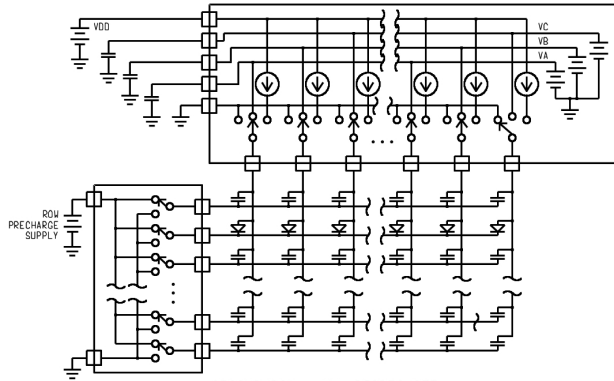
APPLICATION NOTES:**Application Note 1 - Parasitic Diode in Precharge Circuit:**

The MX823 has a parasitic diode connected between the precharge reference pin PRECHA and column outputs 1, 4, ... , 238, and between PRECHB and outputs 2, 5, ... , 239, and between PRECHC and outputs 3, 6, ..., 240 as shown below. This means that the precharge voltage must be set above the display diode anode voltages during calibration and at or above display diode anode voltages during operation or output current will flow through the parasitic diodes and not the display.

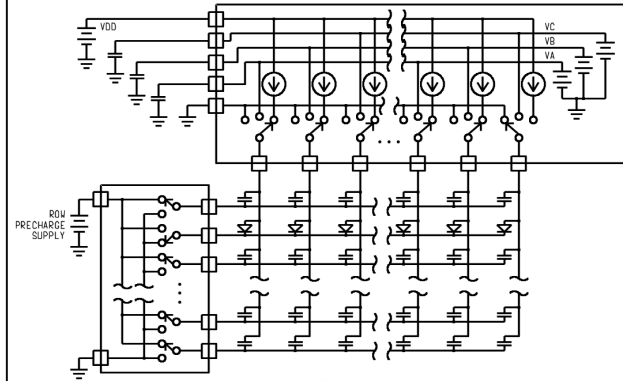
Display Block Diagram

Application Note 2 - Display Switching Pattern:

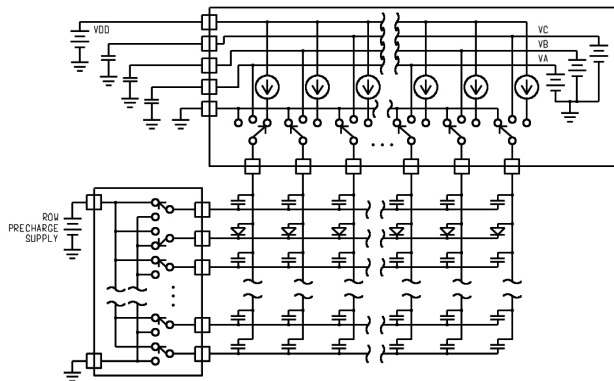
The diagram below shows the switching sequence the row and column drivers go through.



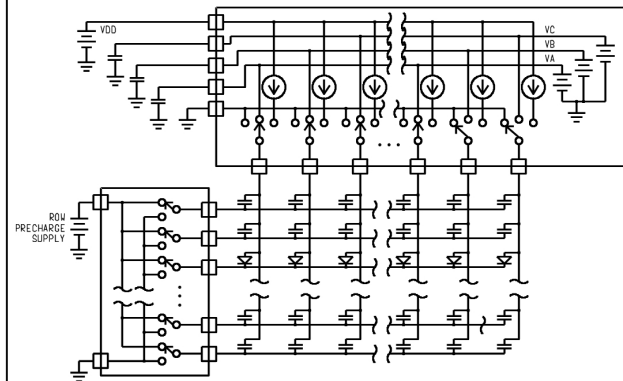
SECOND ROW - ALL DIODES OFF
PRECHARGE - 1ST CLKEX COUNT AFTER LD SIGNAL
SHOWN WITH ALL COLUMNS EXCEPT LAST HAVING DATA



SECOND ROW ON
DATA OUTPUT BEGINS - 1ST CLKEX COUNT AFTER PRECHARGE
SHOWN WITH ALL COLUMNS EXCEPT LAST HAVING DATA



SECOND ROW ON
DATA OUTPUT ENDS - 63RD CLKEX COUNT AFTER PRECHARGE
SHOWN WITH ONLY FIRST COLUMN STILL HAVING DATA



THIRD ROW - ALL DIODES OFF - REPEATS CYCLE
PRECHARGE - 1ST CLKEX COUNT AFTER LD SIGNAL
SHOWN WITH ALL COLUMNS EXCEPT LAST 2 HAVING DATA

SEMICONDUCTOR DIE DATA SHEET

The MXED102 is a digital data driver for Passive Matrix Organic Light Emitting Diode (OLED) and Polymer Light Emitting Diode (PLED, PolyLED, LEP, . . . etc.) displays, with anodes connected to the columns. This document specifies the physical and mechanical properties of MXED102 semiconductor die, as provided in wafer form.

DIMENSIONS

Die Size

"X Dimension" Center Scribe to Center Scribe

"Y Dimension" Scribe to Center Scribe

Die Thickness

Unthinned (Non Back Lapped Wafer) Thickness: 25 mils

BONDING PADS

Locations and Sizes - Driver Outputs

MXED102 PAD LOCATIONS											
COORDINATES REFERENCE TO CENTER OF PAD											
SQUARE(60X BY 60Y)			RECT(40X BY 60Y)			RECT(40X BY 60Y)			RECT(40X BY 60Y)		
NAME	X	Y	NAME	X	Y	NAME	X	Y	NAME	X	Y
IOUT0	338.6	30	IOUT61	4249.3	30	IOUT124	8214.1	30	IOUT187	12179.1	30
IOUT1	424.9	30	IOUT62	4309.3	30	IOUT125	8274.1	30	IOUT188	12239.1	30
IOUT2	511.3	30	IOUT63	4369.3	30	IOUT126	8334.1	30	IOUT189	12299.1	30
RECT(40X BY 60Y)			IOUT64	4429.3	30	IOUT127	8394.1	30	IOUT190	12359.1	30
NAME	X	Y	IOUT65	4489.3	30	IOUT128	8454.1	30	IOUT191	12419.1	30
IOUT3	584.4	30	IOUT66	4549.3	30	IOUT129	8514.1	30	IOUT192	12479.1	30
IOUT4	644.4	30	IOUT67	4609.3	30	IOUT130	8574.1	30	IOUT193	12539.1	30
IOUT5	704.4	30	IOUT68	4669.3	30	IOUT131	8634.1	30	IOUT194	12599.1	30
IOUT6	764.4	30	IOUT69	4729.3	30	IOUT132	8694.1	30	IOUT195	12659.1	30
IOUT7	824.4	30	IOUT70	4789.3	30	IOUT133	8754.1	30	IOUT196	12719.1	30
IOUT8	884.4	30	IOUT71	4849.3	30	IOUT134	8814.1	30	IOUT197	12779.1	30
IOUT9	944.4	30	IOUT72	4909.3	30	IOUT135	8874.1	30	IOUT198	12839.1	30
IOUT10	1004.4	30	IOUT73	4969.3	30	IOUT136	8934.1	30	IOUT199	12899.1	30
IOUT11	1064.4	30	IOUT74	5029.3	30	IOUT137	8994.1	30	IOUT200	12959.1	30
IOUT12	1124.4	30	IOUT75	5089.3	30	IOUT138	9054.1	30	IOUT201	13019.1	30
IOUT13	1184.4	30	IOUT76	5149.3	30	IOUT139	9114.1	30	IOUT202	13079.1	30
IOUT14	1244.4	30	IOUT77	5209.3	30	IOUT140	9174.1	30	IOUT203	13139.1	30
IOUT15	1304.4	30	IOUT78	5269.3	30	IOUT141	9234.1	30	IOUT204	13199.1	30
IOUT16	1364.4	30	IOUT79	5329.3	30	IOUT142	9294.1	30	IOUT205	13259.1	30
IOUT17	1424.4	30	IOUT80	5389.3	30	IOUT143	9354.1	30	IOUT206	13319.1	30
IOUT18	1484.4	30	IOUT81	5449.3	30	IOUT144	9414.1	30	SQUARE(60X BY 60Y)		
IOUT19	1544.4	30	IOUT82	5509.3	30	IOUT145	9474.1	30	NAME	X	Y
IOUT20	1604.4	30	IOUT83	5569.3	30	IOUT146	9534.1	30	IOUT207	13392	30
IOUT21	1664.4	30	IOUT84	5629.3	30	SQUARE(60X BY 60Y)			IOUT208	13478.4	30
IOUT22	1724.4	30	IOUT85	5689.3	30	NAME	X	Y	IOUT209	13564.7	30
IOUT23	1784.4	30	IOUT86	5749.3	30	IOUT147	9607	30	IOUT210	13678.2	30
IOUT24	1844.4	30	SQUARE(60X BY 60Y)			IOUT148	9693.4	30	IOUT211	13764.5	30
IOUT25	1904.4	30	NAME	X	Y	IOUT149	9779.7	30	IOUT212	13850.9	30
IOUT26	1964.4	30	IOUT87	5822.2	30	IOUT150	9893.4	30	RECT(40X BY 60Y)		
SQUARE(60X BY 60Y)			IOUT88	5908.6	30	IOUT151	9979.7	30	NAME	X	Y
NAME	X	Y	IOUT89	5994.9	30	IOUT152	10066.1	30	IOUT213	13924	30
IOUT27	2037.3	30	IOUT90	6108.4	30	RECT(40X BY 60Y)			IOUT214	13984	30
IOUT28	2123.7	30	IOUT91	6194.7	30	NAME	X	Y	IOUT215	14044	30
IOUT29	2210	30	IOUT92	6281.1	30	IOUT153	10139.1	30	IOUT216	14104	30
IOUT30	2323.6	30	RECT(40X BY 60Y)			IOUT154	10199.1	30	IOUT217	14164	30
IOUT31	2409.9	30	NAME	X	Y	IOUT155	10259.1	30	IOUT218	14224	30
IOUT32	2496.3	30	IOUT93	6354.1	30	IOUT156	10319.1	30	IOUT219	14284	30
RECT(40X BY 60Y)			IOUT94	6414.1	30	IOUT157	10379.1	30	IOUT220	14344	30
NAME	X	Y	IOUT95	6474.1	30	IOUT158	10439.1	30	IOUT221	14404	30
IOUT33	2569.3	30	IOUT96	6534.1	30	IOUT159	10499.1	30	IOUT222	14464	30
IOUT34	1629.3	30	IOUT97	6594.1	30	IOUT160	10559.1	30	IOUT223	14524	30
IOUT35	2689.3	30	IOUT98	6654.1	30	IOUT161	10619.1	30	IOUT224	14584	30
IOUT36	2749.3	30	IOUT99	6714.1	30	IOUT162	10679.1	30	IOUT225	14644	30
IOUT37	2809.3	30	IOUT100	6774.1	30	IOUT163	10739.1	30	IOUT226	14704	30
IOUT38	2869.3	30	IOUT101	6834.1	30	IOUT164	10799.1	30	IOUT227	14764	30
IOUT39	2929.3	30	IOUT102	6894.1	30	IOUT165	10859.1	30	IOUT228	14824	30
IOUT40	2989.3	30	IOUT103	6954.1	30	IOUT166	10919.1	30	IOUT229	14884	30
IOUT41	3049.3	30	IOUT104	7014.1	30	IOUT167	10979.1	30	IOUT230	14944	30
IOUT42	3109.3	30	IOUT105	7074.1	30	IOUT168	11039.1	30	IOUT231	15004	30
IOUT43	3169.3	30	IOUT106	7134.1	30	IOUT169	11099.1	30	IOUT232	15064	30
IOUT44	3229.3	30	IOUT107	7194.1	30	IOUT170	11159.1	30	IOUT233	15124	30
IOUT45	3289.3	30	IOUT108	7254.1	30	IOUT171	11219.1	30	IOUT234	15184	30
IOUT46	3349.3	30	IOUT109	7314.1	30	IOUT172	11279.1	30	IOUT235	15244	30
IOUT47	3409.3	30	IOUT110	7374.1	30	IOUT173	11339.1	30	IOUT236	15304	30
IOUT48	3469.3	30	IOUT111	7434.1	30	IOUT174	11399.1	30	SQUARE(60X BY 60Y)		
IOUT49	3529.3	30	IOUT112	7494.1	30	IOUT175	11459.1	30	NAME	X	Y
IOUT50	3589.3	30	IOUT113	7554.1	30	IOUT176	11519.1	30	IOUT237	15376.9	30
IOUT51	3649.3	30	IOUT114	7614.1	30	IOUT177	11579.1	30	IOUT238	15463.3	30
IOUT52	3709.3	30	IOUT115	7674.1	30	IOUT178	11639.1	30	IOUT239	15549.6	30
IOUT53	3769.3	30	IOUT116	7734.1	30	IOUT179	11699.1	30			
IOUT54	3829.3	30	IOUT117	7794.1	30	IOUT180	11759.1	30			
IOUT55	3889.3	30	IOUT118	7854.1	30	IOUT181	11819.1	30			
IOUT56	3949.3	30	IOUT119	7914.1	30	IOUT182	11879.1	30			
IOUT57	4009.3	30	IOUT120	7974.1	30	IOUT183	11939.1	30			
IOUT58	4069.3	30	IOUT121	8034.1	30	IOUT184	11999.1	30			
IOUT59	4129.3	30	IOUT122	8094.1	30	IOUT185	12059.1	30			
IOUT60	4189.3	30	IOUT123	8154.1	30	IOUT186	12119.1	30			

The information contained on this page is preliminary. Although the order of the bond pad will remain the same, the XY dimensions in the final document may vary slightly. Please take this possibility into consideration when doing any chip on board layouts.

Interface I/O

MXED102 PAD LOCATIONS						
COORDINATES REFERENCE LOWER LEFT EDGE						
SQUARE(85X BY 85Y)						
NAME	X	Y		NAME	X	Y
CLK_ROW	314.2	1853.3		ISHRT	0	110.1
PCB_ROW	734.2	1853.3		ISHRT	0	237
TESTA	1100.5	1853.3		PRECHA	0	514.3
TESTB	1392.8	1853.3		PRECHB	0	1093.9
GND	1614.2	1853.3		PRECHC	0	1338.9
LTKNB	1942.2	1853.3		VDDC	0	1639.6
MASTER_IN	2226.9	1853.3		Vddb	0	1808.6
GND	2442.7	1853.3		VDDA	0	816.6
AD_IN	2720	1853.3		ISHRT	15877.8	110.1
VCC	2943.9	1853.3		ISHRT	15877.8	237
CLKSH	3070.7	1853.3		PRECHA	15877.8	514.3
CLKEX	3286.4	1853.3		PRECHB	15877.8	816.6
CLKSER	3502.1	1853.3		PRECHC	15877.8	1093.9
SDATA	3853.1	1853.3		VDDC	15877.8	1338.9
SAMPLE	4137.8	1853.3		Vddb	15877.8	1639.6
LE	4353.5	1853.3		VDDA	15877.8	1808.5
DA0	4569.2	1853.3		DUMMY	13591.2	1853.3
DA1	4784.9	1853.3		DUMMY	13738.6	1853.3
DA2	5000.6	1853.3		DUMMY	5215.6	1853.3
DA3	7927.8	1853.3		DUMMY	5430.6	1853.3
DA4	8143.5	1853.3		DUMMY	5645.6	1853.3
DA5	8359.2	1853.3		DUMMY	5860.6	1853.3
DB0	8574.9	1853.3		DUMMY	6075.6	1853.3
DB1	8790.6	1853.3		DUMMY	6280.6	1853.3
DB2	9006.3	1853.3		DUMMY	6495.6	1853.3
DB3	9222	1853.3		DUMMY	6710.6	1853.3
DB4	9437.7	1853.3		DUMMY	6925.6	1853.3
DB5	9653.4	1853.3		DUMMY	7140.6	1853.3
DC0	9869.1	1853.3		DUMMY	7355.6	1853.3
DC1	10084.8	1853.3		DUMMY	7570.6	1853.3
DC2	10300.5	1853.3		DUMMY	170	0
DC3	10516.2	1853.3		DUMMY	15707.8	0
DC4	10731.9	1853.3				
DC5	10947.6	1853.3				
RSTB	11163.3	1853.3				
I1TRIM0	11307	1853.3				
I1TRIM1	11447.9	1853.3				
I1TRIM2	11588.8	1853.3				
I1TRIM3	11729.7	1853.3				
I1TRIM4	11870.6	1853.3				
I1TRIM5	12011.5	1853.3				
I1TRIM6	12152.4	1853.3				
I2TRIM0	12290.7	1853.3				
I2TRIM1	12431.6	1853.3				
I2TRIM2	12572.5	1853.3				
I2_TEST	12783.7	1853.3				
VTRIM0	13018.8	1853.3				
VTRIM1	13159.7	1853.3				
VTRIM2	13300.6	1853.3				
VTRIM3	13441.5	1853.3				
DRTKN	13885.6	1853.3				
GND	14101.4	1853.3				
VCC	14294.1	1853.3				
MASTER_OUT	14556.2	1853.3				
RTKNB	14976.2	1853.3				
GND	15261	1853.3				
TESTC	15538.3	1853.3				



Notes:

Notes:



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