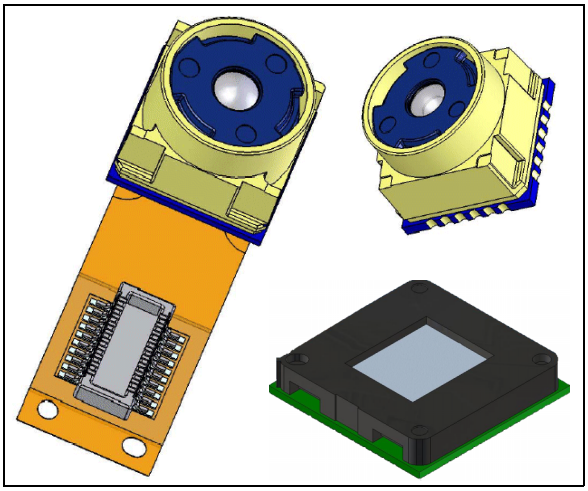
VL6624
VS6624

1.3 Megapixel single-chip camera module

Preliminary Data

Features

- 1280H x 1024V active pixels
- 3.0 µm pixel size, 1/3 inch optical format
- RGB Bayer color filter array
- Integrated 10-bit ADC
- Integrated digital image processing functions, including defect correction, lens shading correction, image scaling, demosaicing, sharpening, gamma correction and color space conversion
- Embedded camera controller for automatic exposure control, automatic white balance control, black level compensation, 50/60 Hz flicker cancelling and flashgun support
- Fully programmable frame rate and output derating functions
- Up to 15 fps SXGA progressive scan
- Low power 30 fps VGA progressive scan
- ITU-R BT.656-4 YUV (YCbCr) 4:2:2 with embedded syncs, YUV (YCbCr) 4:0:0, RGB 565, RGB 444, Bayer 10-bit or Bayer 8-bit output formats
- 8-bit parallel video interface, horizontal and vertical syncs, 54MHz (max) clock
- Two-wire serial control interface
- On-chip PLL, 6.5 to 54 MHz clock input
- Analog power supply, from 2.4 to 3.0 V
- Separate I/O power supply, 1.8 or 2.8 V levels
- Integrated power management with power switch, automatic power-on reset and power-safe pins
- Low power consumption, ultra low standby current
- Triple-element plastic lens, F# 3.2, 52° Horizontal field of view (VS6624)
- 8.0 x 8.0 x 6.1mm fixed focus camera module with embedded passives (VS6624)



- 20-wire FPC attachment with board-to-board connector, 22 mm total length, for mobile application only
- 24-pin (ITU) shielded socket options

Applications

- Mobile phone
- Videophone
- Medical
- Machine vision
- Toys
- PDA
- Biometry
- Bar code reader
- Lighting control

Description

The VL6624/VS6624 is an SXGA CMOS color digital camera featuring low size and low power consumption targeting mobile applications. This complete camera module is ready to connect to camera enabled baseband processors, back-end IC devices or PDA engines.

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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1 Overview

The VL6624/VS6624 is a SXGA resolution CMOS imaging device designed for low power systems.

Manufactured using ST 0.18 µm CMOS Imaging process, it integrates a high-sensitivity pixel array, a digital image processor and camera control functions.

The VS6624 is capable of streaming SXGA video up to 15 fps, with ITU-R BT.656-4 YUV 4:2:2 frame format. It supports both 1.8 V and 2.8 V interface and requires a 2.4 to 3.0 V analog power supply. Typically, the VS6624 can operate as a 2.8 V single supply camera or as a 1.8 V interface / 2.8 V supply camera. The integrated PLL allows for low frequency system clock, and flexibility for successful EMC integration.

The VS6624 camera module uses ST's 2nd generation "SmOP2" packaging technology: the sensor, lens and passives are assembled, tested and focused in a fully automated process, allowing high volume and low cost production.

The device contains an embedded video processor and delivers fully color processed images at up to 15 frames per second SXGA and up to 30 fps VGA.

The video data is output over an 8-bit parallel bus in RGB, YCbCr or bayer formats.

The VL6624/VS6624 requires an analogue power supply of between 2.4 V to 3.0 V and a digital supply of either 1.8 V or 2.8 V (dependant on interface levels required). An input clock is required in the range 6.5 MHz to 54 MHz.

The VL6624/VS6624 is controlled via an I²C interface.

It also includes a wide range of image enhancement functions, designed to ensure high image quality, these include:

- Automatic exposure control
- Automatic white balance
- Lens shading compensation
- Defect correction algorithms
- Demosaic (Bayer to RGB conversion)
- Colour space conversion
- Sharpening
- Gamma correction
- Flicker cancellation
- NoRA Noise Reduction Algorithm
- Intelligent image scaling

2 Electrical interface

The VL6624/VS6624 FPC board to board connector has 20 electrical connections which are listed in *Table 1*. the package details of the flex connector are shown in *Figure 39* and*Figure 40*.

Table 1. VS6624 signal description of 20-pin flex connector
Table 2:

Pad	Pad name	I/O	Description
1	GND	PWR	Analogue ground
2	HSYNC	OUT	Horizontal synchronization output
3	VSYNC	OUT	Vertical synchronization output
4	SCL	IN	I²C clock input
5	CLK	IN	Clock input - 6.5MHz to 54MHz
6	SDA	I/O	I²C data line
7	VDD	PWR	Digital supply 1.8 V OR 2.8 V
8	AVDD	PWR	Analogue supply 2.4 V to 3.0 V
9	PCLK	OUT	Pixel qualification clock
10	CE	IN	Chip enable signal active HIGH
11	D5	OUT	Data output D5
12	D4	OUT	Data output D4
13	GND	PWR	Digital ground
14	D3	OUT	Data output D3
15	D2	OUT	Data output D2
16	D1	OUT	Data output D1
17	D0	OUT	Data output D0
18	D6	OUT	Data output D6
19	D7	OUT	Data output D7
20	FSO	OUT	Flash output

The package details and electrical connections of the 24pin socket device are shown in *Figure 37* and *Figure 38*.

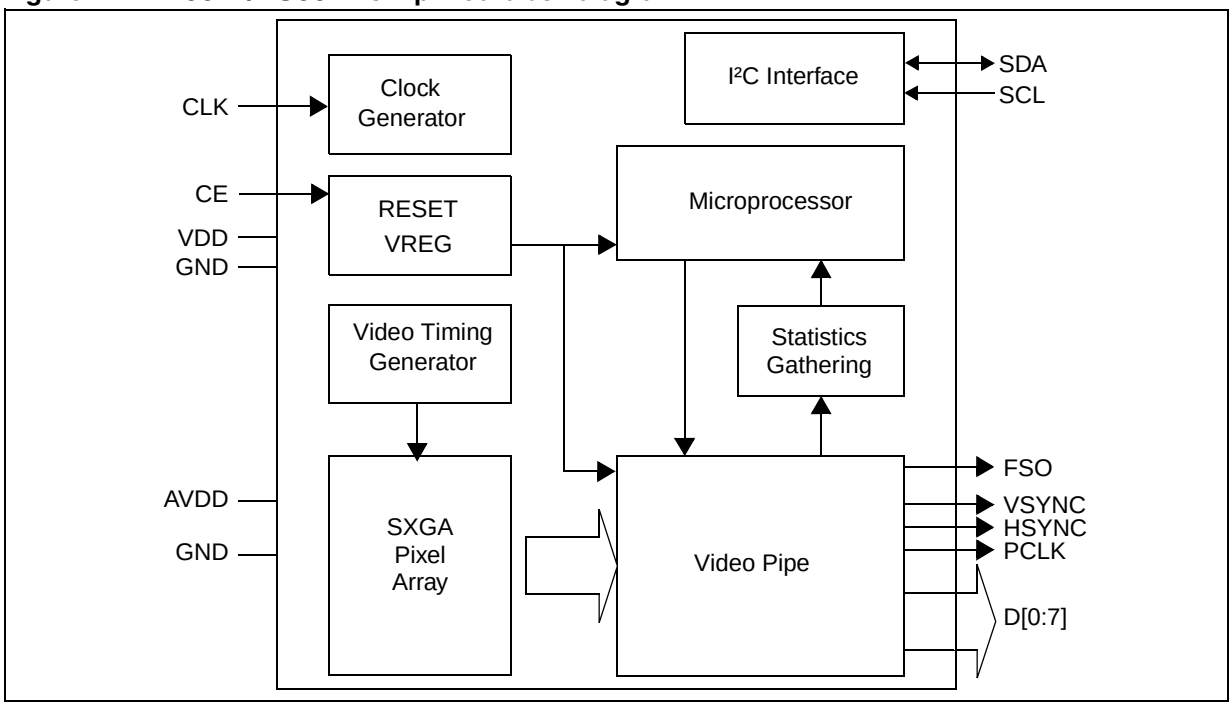
3 System architecture

The VS6624 consists of the following main blocks:

- SXGA-sized pixel array
- Video timing generator
- Video pipe
- Statistics gathering unit
- Clock generator
- Microprocessor

A simplified block diagram is shown *Figure 1*.

Figure 1. VL6624/VS6624 simplified block diagram



3.1 Operation

A video timing generator controls a SXGA-sized pixel array to produce raw bayer images. The analogue pixel information is digitized and passed into the video pipe. The video pipe contains a number of different functions (explained in detail later). At the end of the video pipe data is output to the host system over an 8-bit parallel interface along with qualification signals.

The whole system is controlled by an embedded microprocessor that is running firmware stored in an internal ROM. The external host communicates with this microprocessor over an I²C interface. The microprocessor does not handle the video data itself but is able to control all the functions within the video pipe. Real-time information about the video data is gathered by a statistics engine and is available to the microprocessor. The processor uses

this information to perform real-time image control tasks such as automatic exposure control.

3.2 Video pipe

The main functions contained within the VL6624/VS6624 video processing pipe are as follows.

Gain and offset This function is used to apply gain and offset to data coming from the sensor array. The microprocessor applies gain and offset values are controlled by the automatic exposure and white balance algorithms.

Anti-vignette This function is used to compensate for the radial roll-off in intensity caused by the lens. By default the anti-vignette setting matches the lens used in this module and does not need to be adjusted.

Crop This function allows the user to select an arbitrary Window Of Interest (WOI) from the SXGA-sized pixel array, note that the crop size should not be smaller that the output size. It is fully accessible to the user.

Scaler The scaler module performs real time downscaling, in both the horizontal and vertical domain, of the bayer image data this is achieved by sample-rate conversion. The scaler is capable of downscaling from 1.0x to 10x the input number of pixels and lines, in steps of 1/16.

Derating The VS6624 contains an internal derating module. This is designed to reduce the peak output data rate of the device by spreading the data over the whole frame period and allowing a subsequent reduction in output clock frequency.

The maximum achievable derating factor is x100 for an equivalent scale factor of x10 downscale. As a general rule the allowable derating factor is equal to the square of the scaling factor.

Note: The interline period is not guaranteed consistent for all derating ratios. This means the host capture system must be able to cope with use of the sync signals or embedded codes rather than relying on fixed line counts.

Defect correction This function runs a defect correction filter over the data in order to remove defects from the final output. This function has been optimized to attain the minimum level of defects from the system and does not need to be adjusted.

NoRA The noise reduction module implements an algorithm based on the human-visual system and adaptive pixel filtering that reduces perceived noise in an image whilst maintaining areas of high definition.

Demosaic This module performs an interpolation on the Bayer data from the sensor array to produce a sRGB data. At this point an anti-alias filter is applied.

Anti-Zipper The demosaic process produces an RGB frame with a noise signal at pixel frequency. To remove this artefact an anti-zipper filter is employed.

Sharpening This module increases the high frequency content of the image in order to compensate for the low-pass filtering effects of the previous modules.

Gamma This module applies a programmable gain curve to the output data. It is user adjustable.

YUV conversion This module performs color space conversion from RGB to YUV. It is used to control the contrast and color saturation of the output image as well as the fade to black feature.

Dither This module is used to reduce the contouring effect seen in RGB images with truncated data.

Output formatter This module controls the embedded codes which are inserted into the data stream to allow the host system to synchronize with the output data. It also controls the optional HSYNC and VSYNC output signals.

3.3 Microprocessor functions

The microprocessor inside the VL6624/VS6624 performs the following tasks:

Host communication handles the I²C communication with the host processor.

Video pipe configuration configures the video pipe modules to produce the output required by the host.

Automatic exposure control In normal operation the VL6624/VS6624 determines the appropriate exposure settings for a particular scene and outputs correctly exposed images.

Flicker cancellation The 50/60Hz flicker frequency present in the lighting (due to fluorescent lighting) can be cancelled by the system.

Automatic white balance The microprocessor adjusts the gains applied to the individual color channels in order to achieve a correctly color balanced image.

Frame rate control VS6624 contains a firmware based programmable timing generator. This automatically designs internal video timings, PLL multipliers, clock dividers etc. to achieve a target frame rate with a given input clock frequency.

Optionally an automatic frame rate controller can be enabled. This system examines the current exposure status, integration time and gain and adapts the frame rate based on that. This function is typically useful in low-light scenarios where reducing the frame rate extends the useful integration period. This reduces the need for the application of analog and digital gain and results in better quality images.

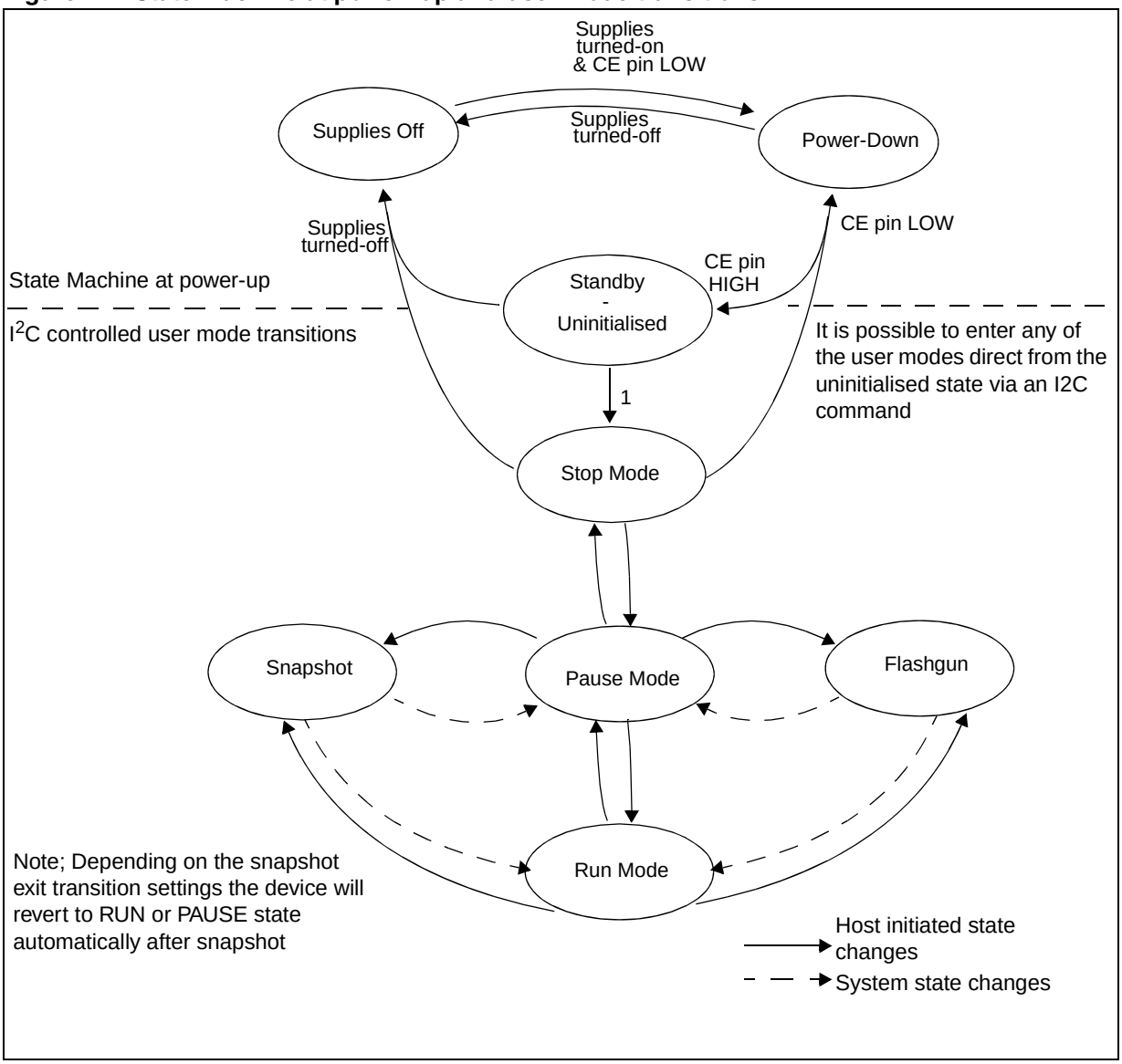
Dark calibration The microprocessor uses information from special dark lines within the pixel array to apply an offset to the video data and ensure a consistent ‘black’ level.

Active noise management The microprocessor is able to modify certain video pipe functions according to the current exposure settings determined by the automatic exposure controller. The main purpose of this is to improve the noise level in the system under low lighting conditions. Functions which ‘strength’ is reduced under low lighting conditions (e.g. sharpening) are controlled by ‘dampers’. Functions which ‘strength’ is increased under low lighting conditions are controlled by ‘promoters’. The fade to black operation is also controlled by the microprocessor

4 Operational modes

VL6624/VS6624 has a number of operational modes. The power down mode is entered and exited by driving the hardware CE signal. Transitions between all other modes are initiated by I²C transactions from the host system or automatically after time-outs.

Figure 2. State machine at power -up and user mode transitions



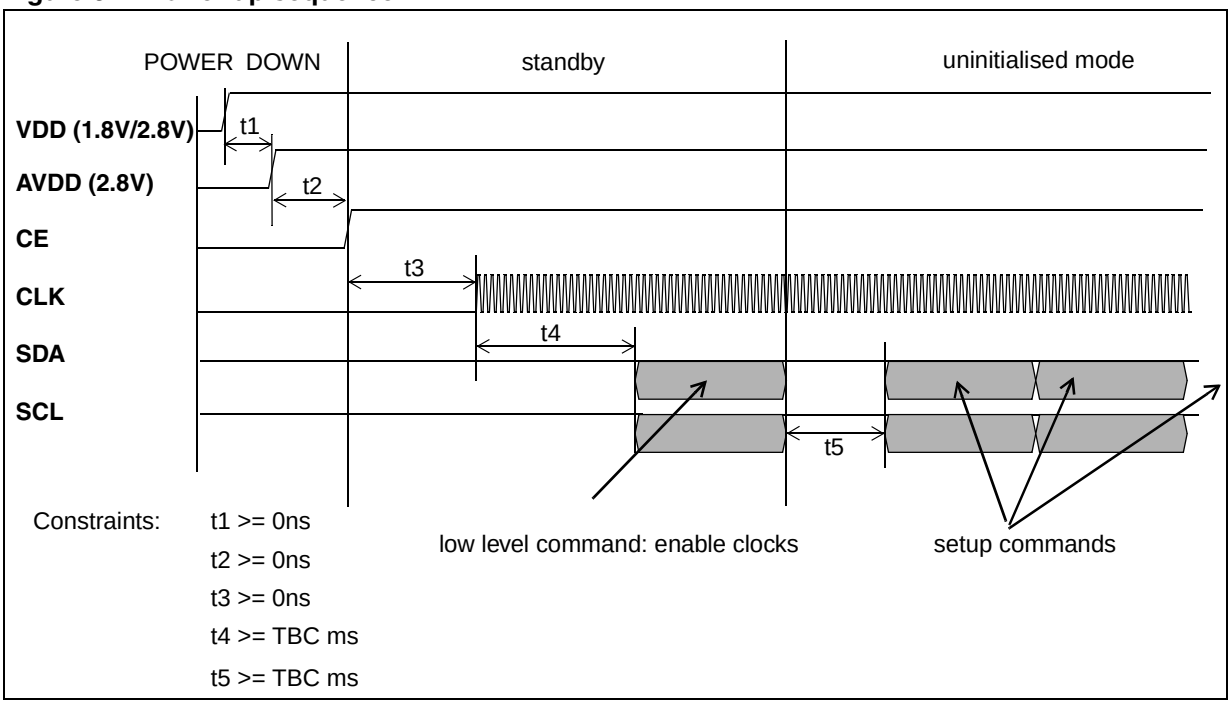
Power Down/Up The power down state is entered from all other modes when CE is pulled low or the supplies are removed.
During the power-down state (CE = logic 0)

- The internal digital supply of the VL6624/VS6624 is shut down by an internal switch mechanism. This method allows a very low power-down current value.
- The device input / outputs are fail-safe, and consequently can be considered high impedance.

During the power-up sequence (CE = logic 1)

- The digital supplies must be on and stable.
- The internal digital supply of the VL6624/VS6624 is enabled by an internal switch mechanism.
- All internal registers are reset to default values by an internal power on reset cell.

Figure 3. Power up sequence



STANDBY mode The VL6624/VS6624 enters STANDBY mode when the CE pin on the device is pulled HIGH. Power consumption is very low, most clocks inside the device are switched off.
In this state I²C communication is possible when CLK is present and when the microprocessor is enabled.

All registers are reset to their default values. The device I/O pins have a very high-impedance.

Uninitialised = RAW The initialize mode is defined as supplies present, the CE signal is logic 1 and the microcontroller clock has been activated.

During initialize mode the device firmware may be patched. This state is provided as an intermediary configuration state and is not central to regular operation of the device.
The analogue video block is powered down, leading to a lower global consumption

STOP mode This is a low power mode. The analogue section of the VL6624/VS6624 is switched off and all registers are accessed over the I²C interface. A run command received in this state automatically sets a transition through the Pause state to the run mode.

Note: The device must be in Stop mode to adjust output size.

The analogue video block is powered down, leading to a lower global consumption.

Pause mode In this mode all VL6624/VS6624 clocks are running and all registers are accessible but no data is output from the device. The device is ready to start streaming but is halted. This mode is used to set up the required output format before outputting any data.

The analogue video block is powered down, leading to a lower global consumption

Note: The PowerManagement register can be adjusted in PAUSE mode but has no effect until the next RUN to PAUSE transition.

4.1 Streaming modes

RUN mode This is the fully operational mode. In running mode the device outputs a continuous stream of images, according to the set image format parameters and frame rate control parameters. The image size is derived through downscaling of the SXGA image from the pixel array.

ViewLive this feature allows different sizes, formats and reconstruction settings to be applied to alternate frames of data, while in run mode.

Snapshot mode The device can be configured to output a single frame according to the size, format and reconstruction settings in the relevant pipe setup bank. In normal operation this frame will be output, once the exposure, white balance and dark-cal systems are stable. To reduce the latency to output, the user may manually override the stability flags.

The snapshot mode command can be issued in either Run or Stop mode and the device will automatically return previous state after the snapshot is taken. The snapshot mode must not be entered into while viewlive is selected.

FLASHGUN mode In flashgun mode, the array is configured for use with an external flashgun. A flash is triggered and a single frame of data is output and the device automatically switches to Pause Mode.

VS6624 supports the following flashgun configurations:

- Torch Mode - user can manually switch on/off the FSO IO pin via a register setting. Independent of mode.
- Pulsed Mode - the flash output is synchronized to the image stream. There are two options available:
  - Pulsed flash with snapshot. Device outputs a single frame synchronized to flash.
  - Pulsed flash with viewfinder. Device outputs a flash pulse synchronized to a single frame in the image stream.
  - In the pulsed mode there are two possible pulse configurations:
  - Single pulse during the interframe period when all image lines are exposed. This is suitable for SCR and IGBT flash configurations. The falling edge of the pulse can be programmed to vary the width of the pulse.
  - Single pulse over entire integration period of frame. This is suitable for LED flash configurations.

4.2 Mode transitions

Transitions between operating modes are normally controlled by the host by writing to the *Host interface manager control* register. Some transitions can occur automatically after a time out. If there is no activity in the Pause state then an automatic transition to the Stop state occurs. This functionality is controlled by the Power management register, writing 0xFF disables the automatic transition to Stop.

The users control allows a transition between Stop and Run, at the state level the system will transition through a Pause state.

5 Clock control

Input clock

The VS6624 requires provision of an external reference clock. The external clock should be a DC coupled square wave. The clock signal may have been RC filtered. The clock input is fail-safe in power down mode.

The VL6624/VS6624 contains an internal PLL allowing it to produce accurate frame rates from a wide range of input clock frequencies. The allowable input range is from 6.5MHz to 54MHz. The input clock frequency must be programmed in the registers. To program an input frequency of 6.5 MHz, the numerator can be set to 13 and the denominator to 2. The default input frequency is 12 MHz.

The VS6624 may be configured as a master or slave device. In normal (master operation) the input clock can be a different frequency to the output PCLK and all output clock configuration is based on the internal PLL. In slave configuration, the input clock is the same frequency and phase as the output PCLK. i.e. parallel output data is synchronized to the input clock.

6 Frame control

Sensor mode control

The VS6624 device can operate it's sensor array in three modes controlled by register SensorMode within *Mode setup*.

- SensorMode_SXGA - the full array is readout and the max frame rate achievable is 15fps
- SensorMode_VGA_analogue binning - the full array operates and a technique of analogue binning is used to output VGA at up to 30fps
- SensorMode_VGA_subsampled - the array is sub-sampled to output VGA at up to 30fps

Image size

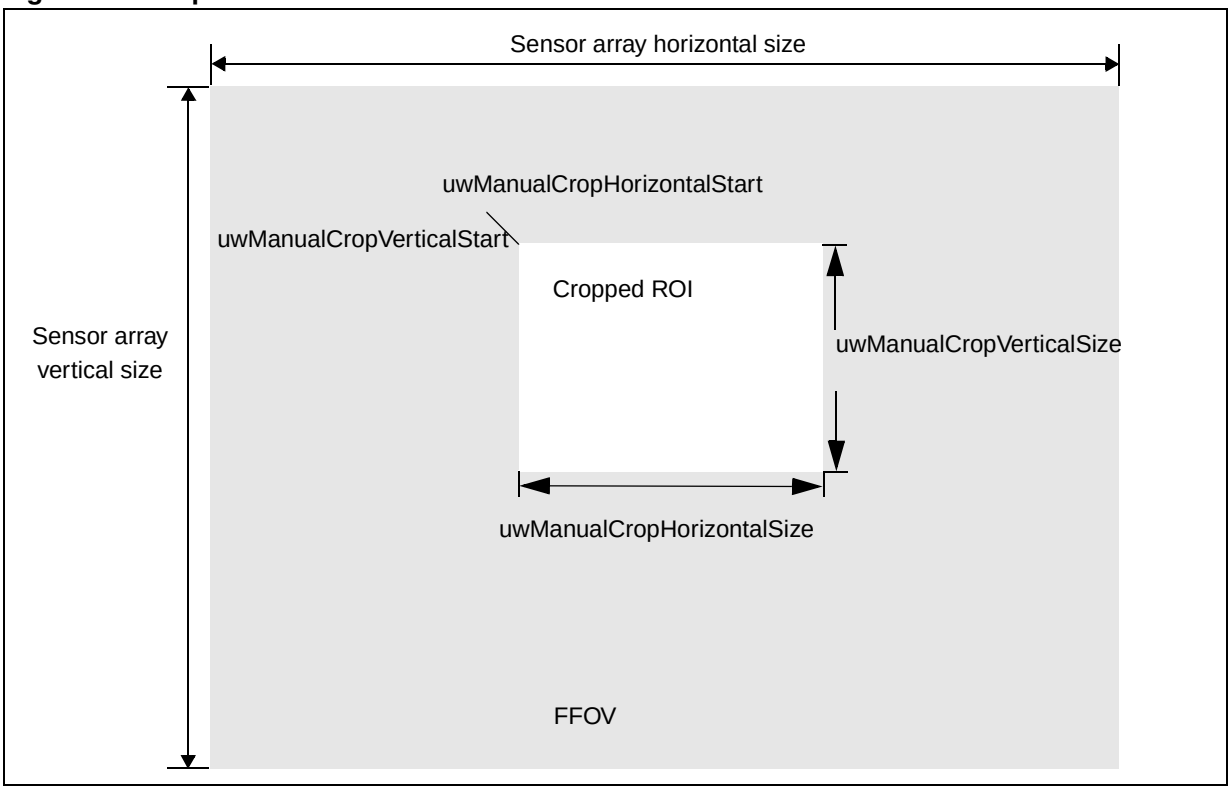
An output frame consists of a number of active lines and a number of interframe lines. Each line consists of embedded line codes (if selected), active pixel data and interline blank data. Note that by default the interline blanking data is *not* qualified by the PCLK and therefore is not captured by the host system.

The image size can be either the full output from the sensor, depending on sensor mode, or a scaled output, The output image size can be chosen from one of 7 pre-selected sizes or a manual image size can be input.

Cropping module

The VL6624/VS6624 contains a cropping module which can be used to define a window of interest within the full SXGA array size. The user can set a start location and the required output size. *Figure 4* shows the example with pipe setup bank0.

Figure 4. Crop controls



Zoom

It is possible to zoom between the sensor size selected and the output size (if the output size selected equals the sensor mode size then no zoom can take place).

The zoom step size in both the horizontal and vertical directions are selectable and zoom controlled with the commands zoom_in, zoom_out and zoom_stop.

Pan

It is possible to pan left, right, up and down when the output size selected is smaller than the sensor size selected. (if the output size selected equals the sensor mode size then no pan can take place).

The pan step size in both the horizontal and vertical directions are selectable.

Frame rate control

The VL6624/VS6624 features an extremely flexible frame rate controller. Using registers uwDesiredFrameRate_Num, and uwDesiredFrameRate_Den any desired frame rate between 2 and 15 fps can be selected for the SXGA sensor mode and between 1 and 30fps for a VGA sensor mode. To program a required frame rate of 7.5 fps the numerator can be set to 15 and the denominator to 2.

Horizontal mirror and vertical flip

The image data output from the VL6624/VS6624 can be mirrored horizontally or flipped vertically (or both).

Video pipe setup

The VS6624 has a single video pipe, the control of this pipe can be loaded from either of two possible setups Pipesetupbank0 and Pipesetupbank1;

Pipe setup bank0 and *Pipe setup bank1*, control the operations shown below,

- image size
- zoom control
- pan control
- Crop control
- Image format (YUV 4:2:2, RGB565, etc....)
- Image controls (Contrast, Color saturation, Horizontal and vertical flip)

Pipe 0 RGB to YUV matrix manual control and *Pipe 1 RGB to YUV matrix manual control*, allow different RGB to YUV matrixes to be used for each pipe setup,

Pipe 0 gamma manual control and *Pipe 1 Gamma manual control*, allow different gamma settings to be used for each pipe setup.

Context switching

In normal operation, it is possible to control which pipe setup bank is used and to switch between banks without the need to stop streaming, the change will occur at the next frame boundary after the change to the register has been made.

For example this function allows the VL6624/VS6624 to stream an output targeting a display (e.g. QQVGA RGB 444) then switch to capture an image (e.g. SXGA YUV 4:2:2) with no need to stop streaming or enter any other operating mode.

It is important to note the output size selected for both pipe setups must be appropriate to the sensor mode used, i.e. to configure PipeSetupBank0 to QQVGA and PipeSetupBank1 to SXGA the sensor mode must be set to SXGA.

The register *Mode setup* allows selection of the pipe setup bank, by default the Pipe setup bank 0 is used.

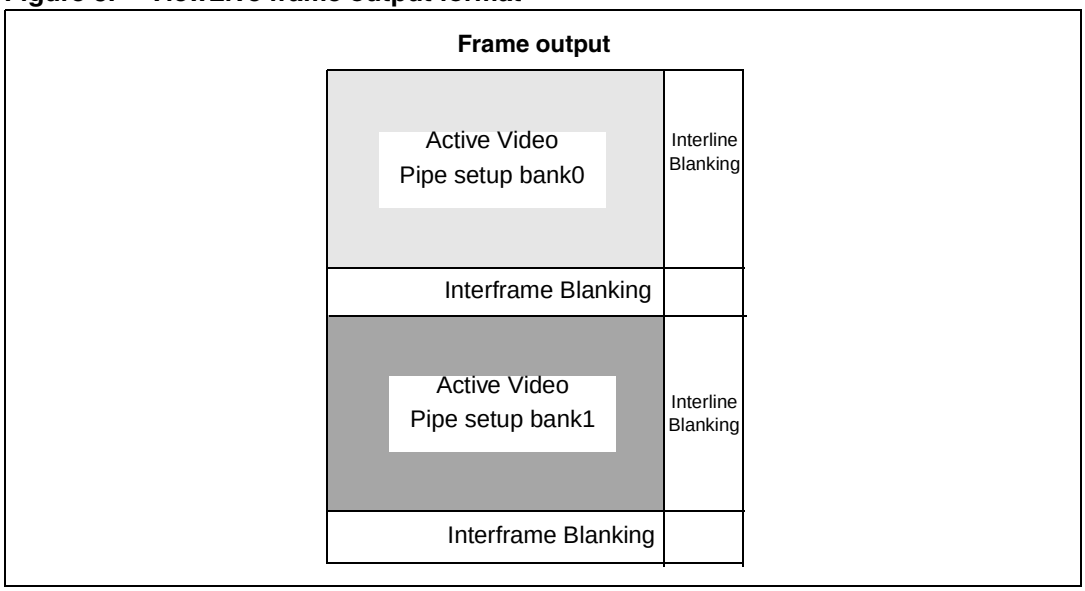
ViewLive Operation

ViewLive is an option which allows a different pipe setup bank to be applied to alternate frames of the output data.

The controls for VIewLive function are found in the register bank where the fEnable register allows the host to enable or disable the function and the binitialPipeSetupBank register selects which pipe setup bank is output first.

When ViewLive is enabled the output data switches between *Pipe setup bank0* and *Pipe setup bank1* on each alternate frame.

Figure 5. ViewLive frame output format



7 Output data formats

The VL6624/VS6624 supports the following data formats:

- YUV4:2:2
- YUV4:0:0
- RGB565
- RGB444 (encapsulated as 565)
- RGB444 (zero padded)
- Bayer 10-bit
- Bayer 8-bit

The required data format is selected using the bdataFomat control found in the pipe setup bank registers. The various options available for each format are controlled using the bRgbsetup and bYuvSetup registers found in the *Output formatter control* registers.

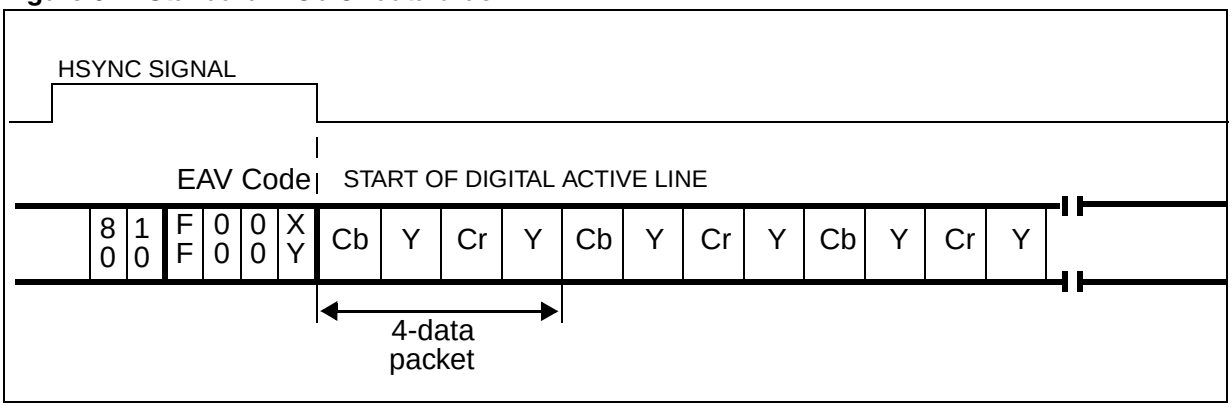
Line / Frame Blanking Data

The values which are output during line and frame blanking are an alternating pattern of 0x10 and 0x80 by default. These values may be changed by writing to the BlankData_MSB and BlankData_LSB registers in the *Output formatter control* bank.

YUV 4:2:2 data format

YUV 422 data format requires 4 bytes of data to represent 2 adjacent pixels. ITU601-656 defines the order of the Y, Cb and Cr components as shown in *Figure 6*.

Figure 6. Standard Y Cb Cr data order



The VL6624/VS6624 bYuvSetup register can be programmed to change the order of the components as follows:

Figure 7. Y Cb Cr data swapping options register 0x2294 bYuvSetup

	Bit [1] Y first	Bit [0] Cb first	Components order in 4-byte data packet 1st	2nd	3rd	4th
	1	1	Y	Cb	Y	Cr
DEFAULT	0	1	Cb	Y	Cr	Y
	1	0	Y	Cr	Y	Cb
	0	0	Cr	Y	Cb	Y

YUV 4:0:0

The ITU protocol allows the encapsulation of various data formats over the link. The following data formats are also proposed encapsulated in ITU601-656 protocol:

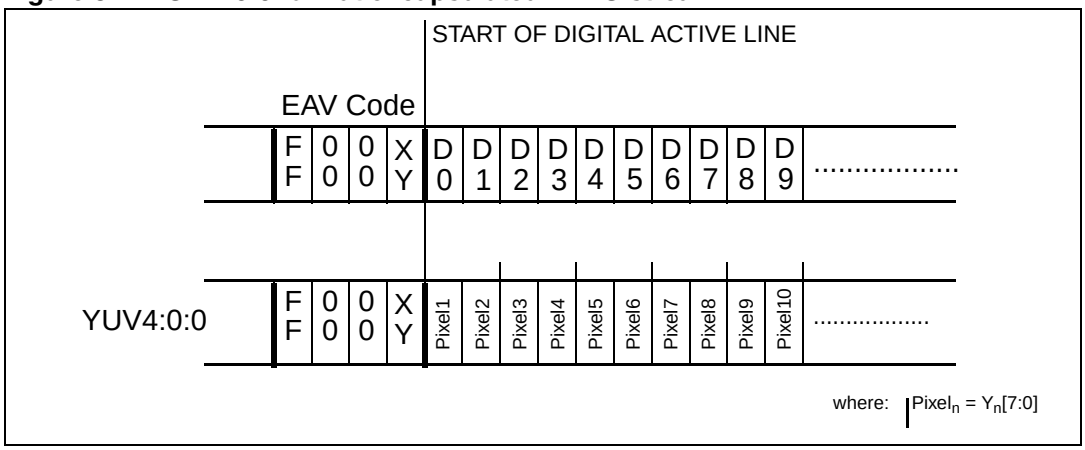
- YUV 4:0:0 - luminance data channel

This is done as described in *Figure 8*. In this output mode the output data per pixel is a single byte. Therefore the output PCLK and data rate is halved.

It is possible to reverse the overall bit order of the component through a register programming.

Note: False synchronization codes are avoided in the LSByte by adding or subtracting a value of one, dependent on detection of a 0 code or 255 code respectively.

Figure 8. YUV 4:0:0 format encapsulated in ITU stream



See *Output formatter control* for user interface control of output data formats.

RGB and Bayer 10 bit data formats

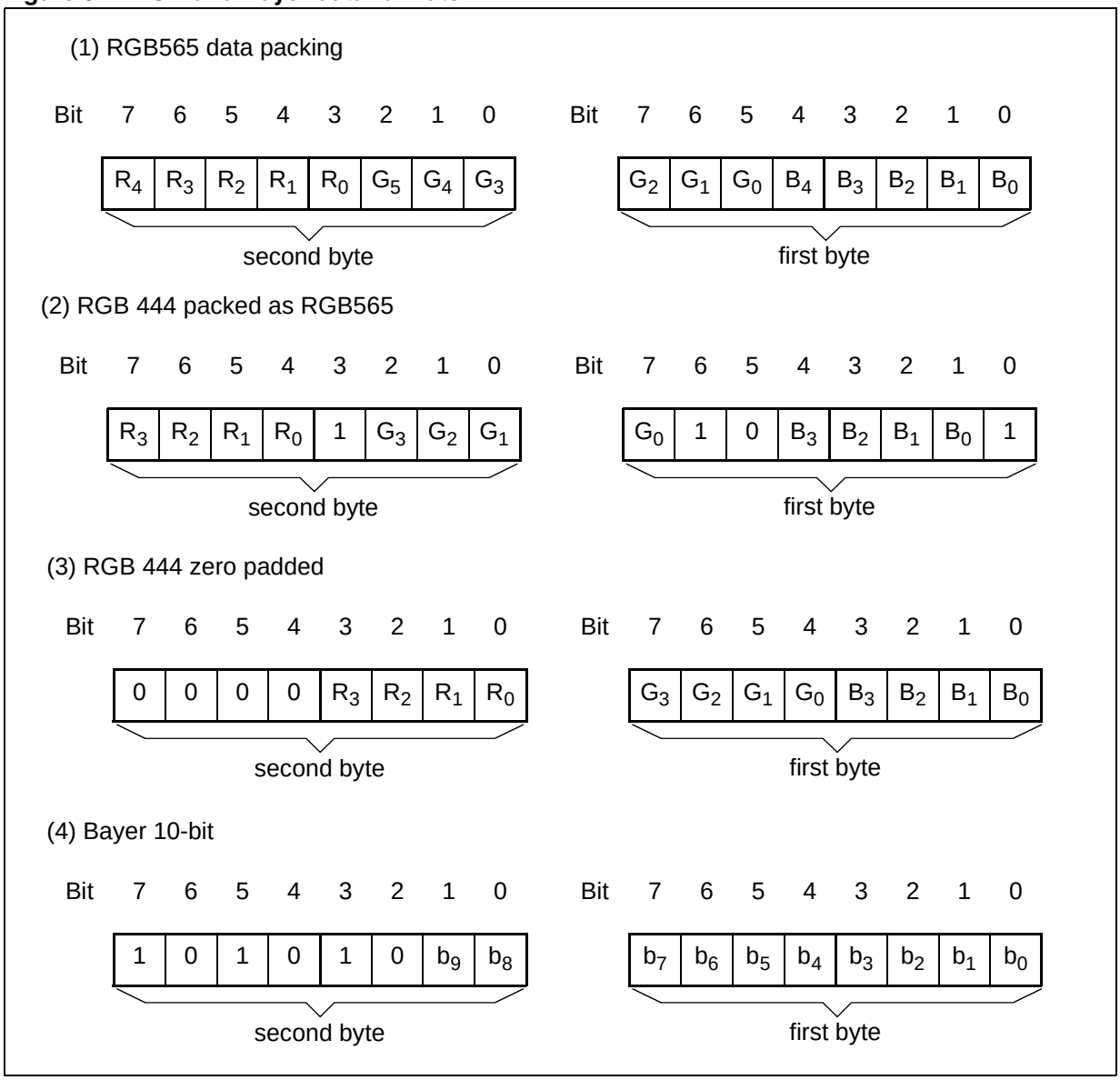
The VL6624/VS6624 can output data in the following formats:

- RGB565
- RGB444 (encapsulated as RGB565)
- RGB444 (zero padded)
- Bayer 10-bit

Note: Pixels in Bayer 10-bit data output are defect corrected, correctly exposed and white balanced. Any or all of these functions can be disabled.

In each of these modes 2 bytes of data are required for each output pixel. The encapsulation of the data is shown in *Table 9*.

Figure 9. RGB and Bayer data formats



Manipulation of RGB data

It is possible to modify the encapsulation of the RGB data in a number of ways:

- swap the location of the RED and BLUE data
- reverse the bit order of the individual color channel data
- reverse the order of the data bytes themselves

Dithering

An optional dithering function can be enabled for each RGB output mode to reduce the appearance of contours produced by RGB data truncation. This is enabled through the DitherControl register.

Bayer 8-bit

The ITU protocol allows the encapsulation of various data formats over the link. The following data formats are also proposed encapsulated in ITU601-656 protocol:

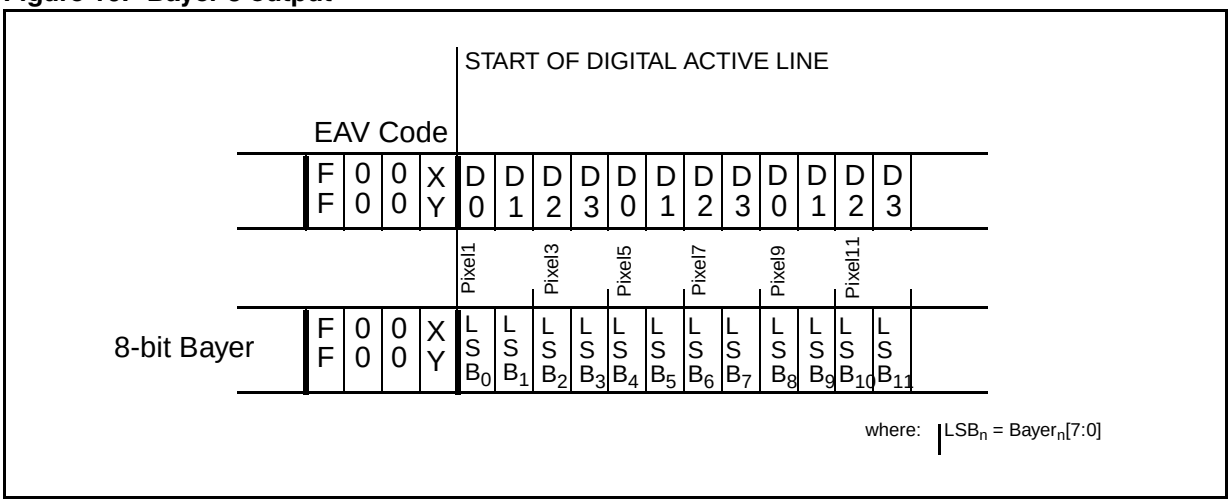
- RAW 8-bit bayer
- Truncated from 10-bit
- DPCM encoded from 10-bit

This is done as described in *Figure 10*. In this output mode the output data per pixel is a single byte. Therefore the output PCLK and data rate is halved.

It is possible to reverse the overall bit order of the individual bayer pixels through a register programming.

Note: False synchronization codes are avoided in the LSByte by adding or subtracting a value of one, dependent on detection of a 0 code or 255 code respectively.

Figure 10. Bayer 8 output



8 Data synchronization methods

External capture systems can synchronize with the data output from VL6624/VS6624 in one of two ways:

1. Synchronization codes are embedded in the output data
2. Via the use of two additional synchronization signals: VSYNC and HSYNC

Both methods of synchronization can be programmed to meet the needs of the host system.

Embedded codes

The embedded code sequence can be inserted into the output data stream to enable the external host system to synchronize with the output frames. The code consists of a 4-byte sequence starting with 0xFF, 0x00, 0x00. The final byte in the sequence depends on the mode selected.

Two types of embedded codes are supported by the VL6624/VS6624: Mode 1 (ITU656) and Mode 2. The bSyncCodeSetup register is used to select whether codes are inserted or not and to select the type of code to insert.

When embedded codes are selected each line of data output contains 8 additional clocks: 4 before the active video data and 4 after it.

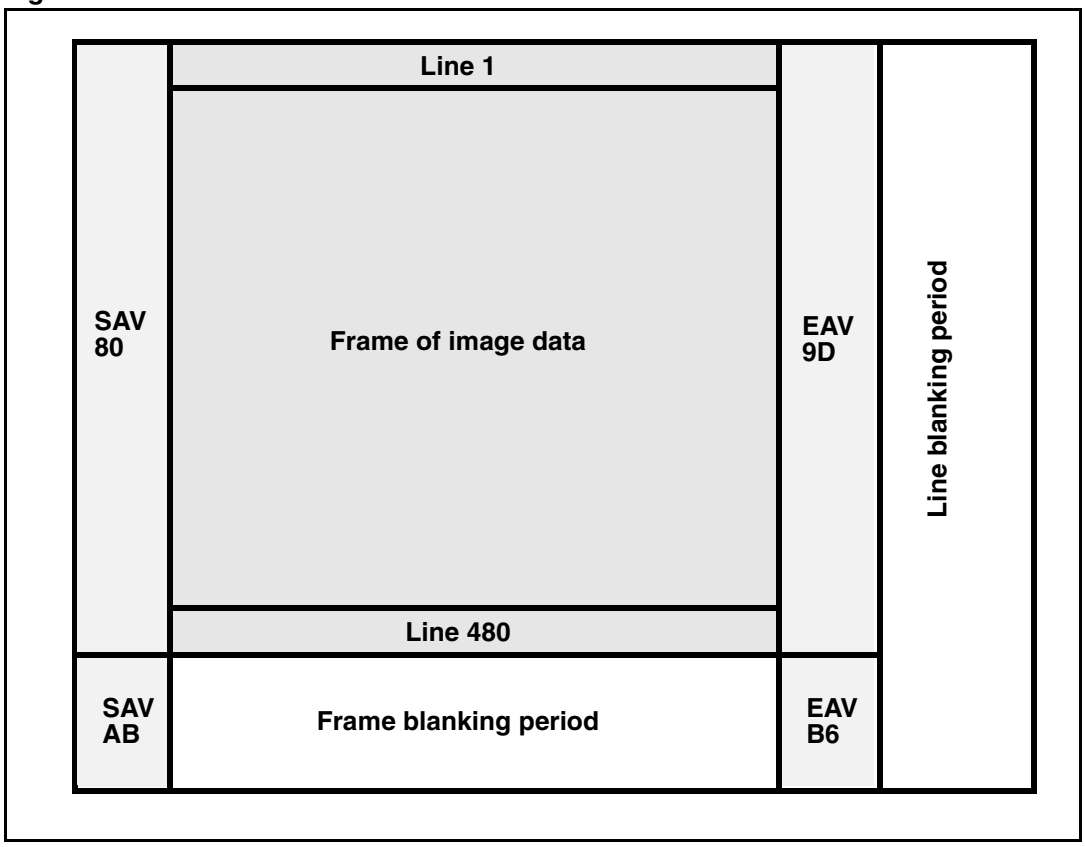
Prevention of false synchronization codes

The VL6624/VS6624 is able to prevent the output of 0xFF and/or 0x00 data from being misinterpreted by a host system as the start of synchronization data. This function is controlled the bCodeCheckEnable register.

Mode 1 (ITU656 compatible)

The structure of an image frame with ITU656 codes is shown in *Figure 11*.

Figure 11. ITU656 frame structure with even codes



The synchronization codes for odd and even frames are listed in *Table 3* and *Table 4*. By default all frames output from the VL6624/VS6624 are EVEN. It is possible to set all frames to be ODD or to alternate between ODD and EVEN using the SyncCodeSetup register in the *Output formatter control* register bank.

Table 3. ITU656 embedded synchronization code definition (even frames)

Name	Description	4-byte sequence
SAV	Line start - active	FF 00 00 80
EAV	Line end - active	FF 00 00 9D
SAV (blanking)	Line start - blanking	FF 00 00 AB
EAV (blanking)	Line end - blanking	FF 00 00 B6

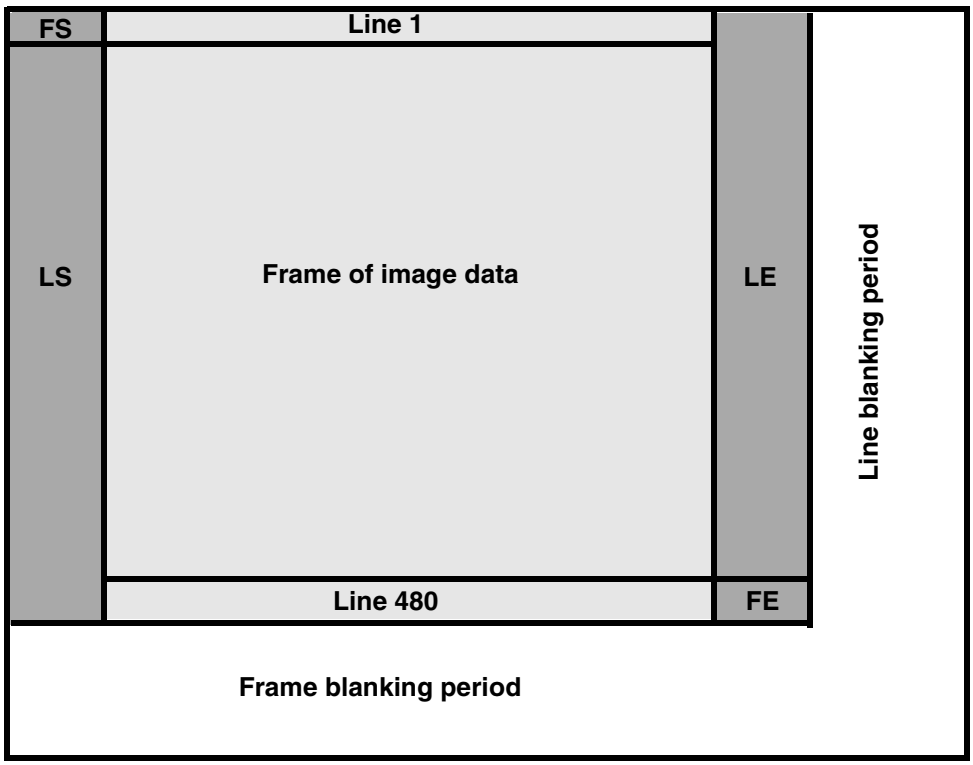
Table 4. ITU656 embedded synchronization code definition (odd frames)

Name	Description	4-byte sequence
SAV	Line start - active	FF 00 00 C7
EAV	Line end - active	FF 00 00 DA
SAV (blanking)	Line start - blanking	FF 00 00 EC
EAV (blanking)	Line end - blanking	FF 00 00 F1

Mode 2

The structure of a mode 2 image frame is shown *Figure 12*.

Figure 12. Mode 2 frame structure (VGA example)



For mode 2, the synchronization codes are as listed in *Table 5*.

Table 5. Mode 2 - embedded synchronization code definition

Name	Description	4-byte sequence
LS	Line start	FF 00 00 00
LE	Line end	FF 00 00 01
FS	Frame Start	FF 00 00 02
FE	Frame End	FF 00 00 03

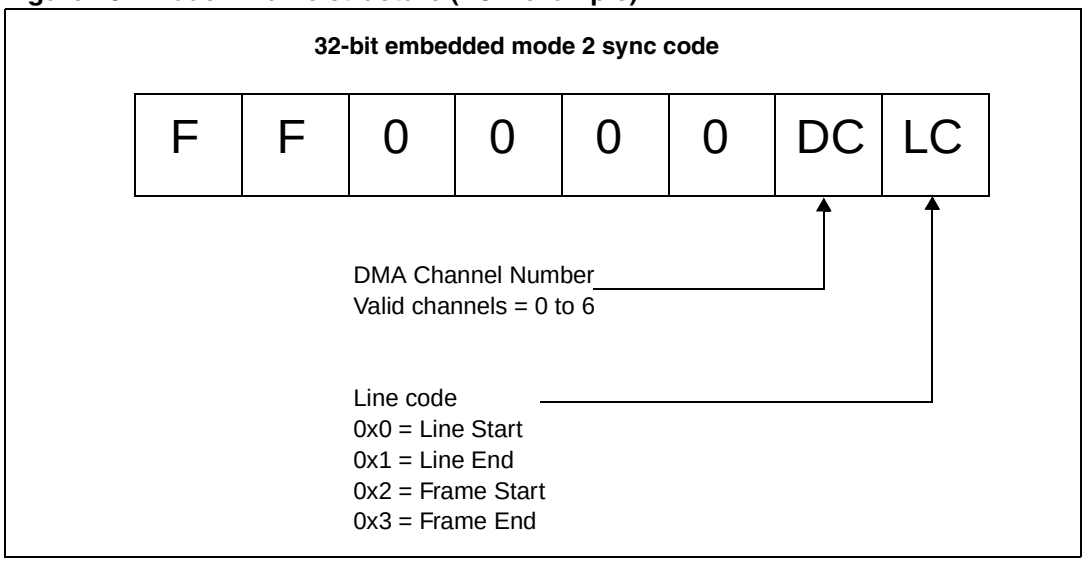
Mode 2 Logical DMA channels

The purpose of logical channels is to separate different data flows which are interleaved in the data stream, in the case of the VS6624 this allows the identification of the pipe setup bank used for an image frame. The DMA channel identifier number is directly encoded in the 4-byte mode2 embedded sync codes. The receiver can then monitor the DMA channel identifier and de-multiplex the interleaved video streams to their appropriate DMA channel. The bChannelID register can have the value 0 to 6. The DMA channel identifier must be fully programmable to allow the host to configure which DMA channels the different video data stream use.

- Logical channel control

The channel identifier is a part of Mode2 synchronization code, upper four bits of last byte of synchronization code. *Figure 13.* illustrates the synchronization code with logical channel identifiers.

Figure 13. Mode 2 frame structure (VGA example)



VSYNC and HSYNC

The VL6624/VS6624 can provide two programmable hardware synchronization signals: VSYNC and HSYNC. The position of these signals within the output frame can be programmed by the user or an automatic setting can be used where the signals track the active video portion of the output frame regardless of its size.

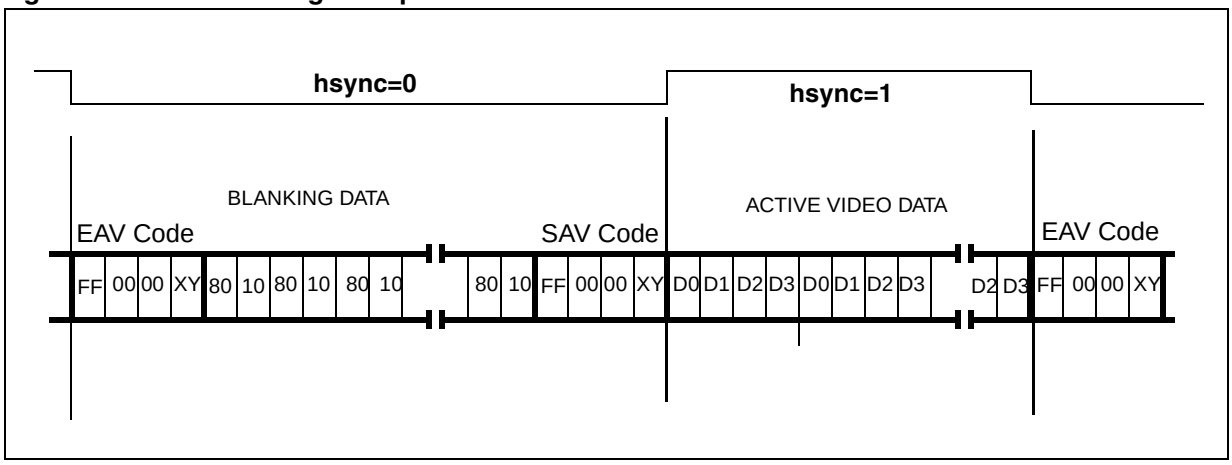
Horizontal synchronization signal (HSYNC)

The HSYNC signal is controlled by the bHSyncSetup register. The following options are available:

- enable/disable
- select polarity
- all lines or active lines only
- manual or automatic

In automatic mode the HSYNC signal envelops all the active video data on every line in the output frame regardless of the programmed image size. Line codes (if selected) fall outside the HSYNC envelope as shown in *Figure 14*.

Figure 14. HSYNC timing example



If manual mode is selected then the pixel positions for HSYNC rising edge and falling edge are programmable. The pixel position for the rising edge of HSYNC is programmed in the bHSyncRising registers. The pixel position for the falling edge of HSYNC is programmed in the bHSyncFalling registers.

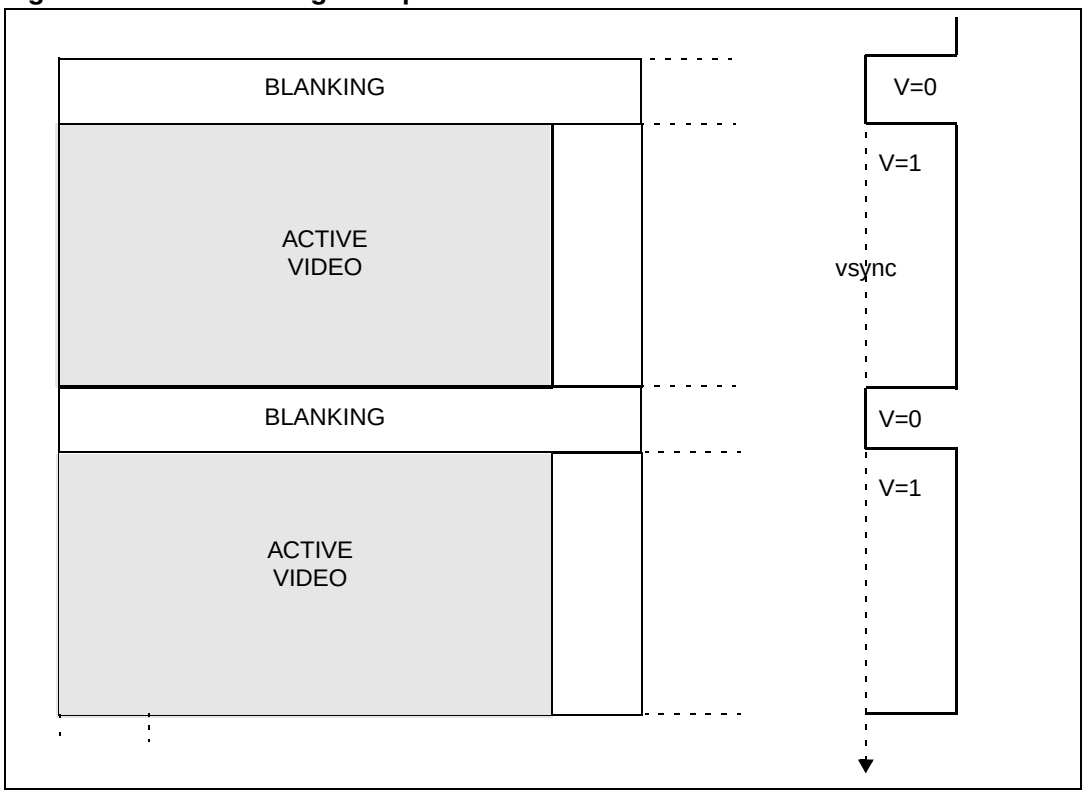
Vertical synchronization (VSYNC)

The VSYNC signal is controlled by the bSyncSetup register. The following options are available:

- enable/disable
- select polarity
- manual or automatic

In automatic mode the VSYNC signal envelops all the active video lines in the output frame regardless of the programmed image size as shown in *Figure 15*.

Figure 15. VSYNC timing example



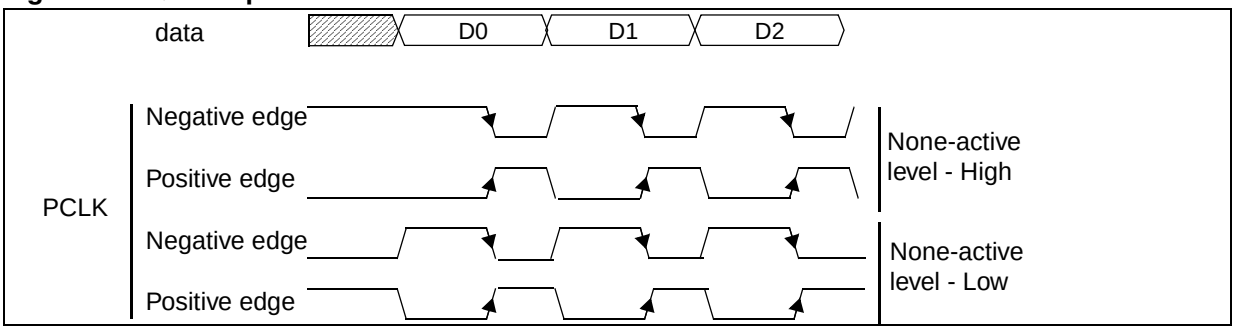
If manual mode is selected then the line number for VSYNC rising edge and falling edge is programmable. The rising edge of VSYNC is programmed in the bVsyncRisingLine registers, the pixel position for VSYNC rising edge is programmed in the bVsyncRisingPixel registers. Similarly the line count for the falling edge position is specified in the bVsyncFallingLine registers, and the pixel count is specified in the bVsyncFallingPixel registers.

Pixel clock (PCLK)

The PCLK signal is controlled by the *Output formatter control* register. The following options are available:

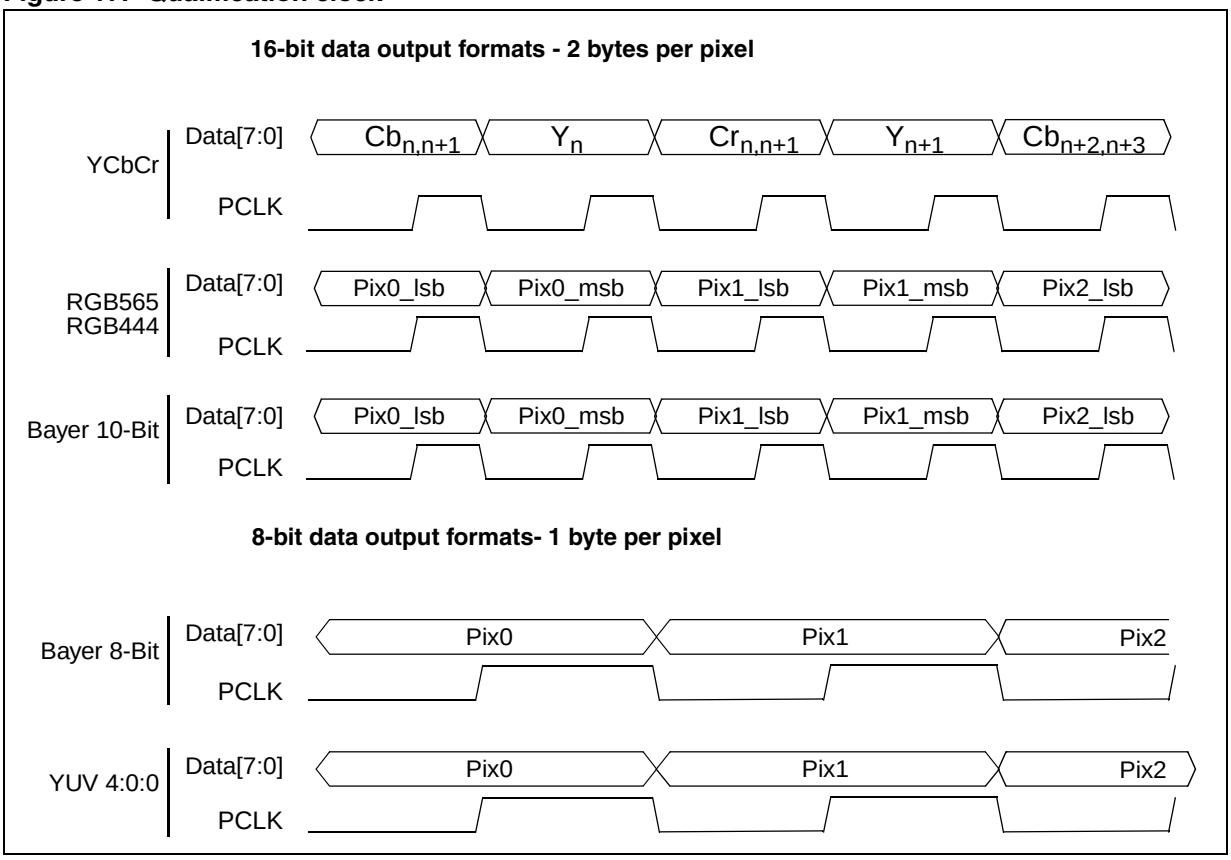
- enable/disable
- select polarity
- select starting phase
- qualify/don't qualify embedded synchronization codes
- enable/disable during horizontal blanking

Figure 16. QCLK options



The YUV, RGB and bayer timings are represented on *Figure 17*, with the associated qualifying pclk clock. The output clock rate is effectively halved for the bayer 8-bit and YUV4:0:0 modes where only one byte of output data is required per pixel.

Figure 17. Qualification clock



Master / Slave operation of PLCK

In normal operation VS6624 acts as a master. PCLK is independent of the input clock frequency and does not have a determined phase relation to the input clock.

In SLAVE operation the input clock frequency is the same as the output clock frequency and the output data is guaranteed with a certain phase relationship to the input clock. Internally, the VS6624 uses clocks generated from the internal PLL, but a retiming stage is used to re-sync the output to the input clock. In this output mode, derating is not possible.

9 Getting started

Initial power up

Before any communication is possible with the VL6624/VS6624 the following steps must take place:

1. Apply VDD (1.8V or 2.8V)
2. Apply AVDD (2.8V)
3. Apply an external CLOCK (6.5MHz to 54MHz)
4. Assert CE line HIGH

These steps can all take place simultaneously. After these steps are complete a delay of 200 µs is required before any I²C communication can take place, see *Figure 3: Power up sequence*.

Minimum startup command sequence

1. Enable the microprocessor - before any commands can be sent to the VL6624/VS6624, the internal microprocessor must be enabled by writing the value 0x02 to the MicroEnable register 0xC003 found in the *Low level control registers* Section.
2. Enable the digital I/O - after power up the digital I/O of the VL6624/VS6624 is in a high-impedance state ('tri-state'). The I/O are enabled by writing the value 0x01 to the DIO_Enable register 0xC044 found in the *Low level control registers* Section.
3. The user can then program the system clock frequency and setup the required output format before placing the VL6624/VS6624 in RUN mode by writing 0x02 to the *Host interface manager control* register 0x0180.

The above three commands represent the absolute minimum required to get video data output.

The default configuration results in an output of SXGA, 15 fps, YUV data format with ITU embedded codes requiring a external clock frequency of 12MHz.

In practice the user is likely to require to write some additional setup information prior to receive the required data output.

10 Host communication - I²C control interface

The interface used on the VL6624/VS6624 is a subset of the I²C standard. Higher level protocol adaptations have been made to allow for greater addressing flexibility. This extended interface is known as the V2W interface.

10.1 Protocol

A message contains two or more bytes of data preceded by a START (S) condition and followed by either a STOP (P) or a repeated START (Sr) condition followed by another message.

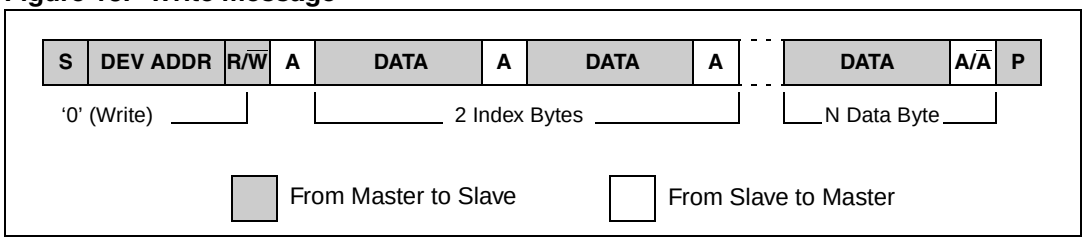
STOP and START conditions can only be generated by a V2W master.

After every byte transferred the receiving device must output an acknowledge bit which tells the transmitter if the data byte has been successfully received or not.

The first byte of the message is called the device address byte and contains the 7-bit address of the V2W slave to be addressed plus a read/write bit which defines the direction of the data flow between the master and the slave.

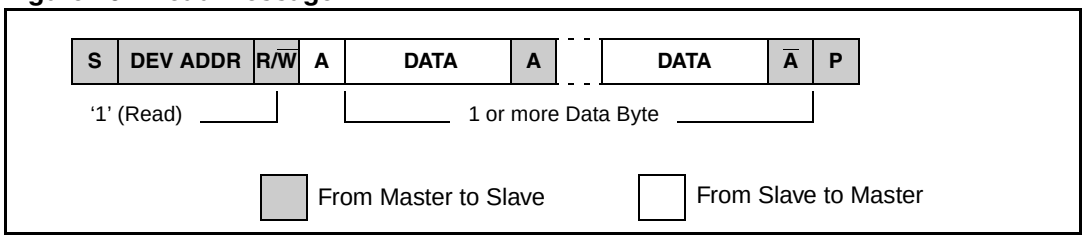
The meaning of the data bytes that follow device address changes depending whether the master is writing to or reading from the slave.

Figure 18. Write message



For the master writing to the slave the device address byte is followed by 2 bytes which specify the 16-bit internal location (index) for the data write. The next byte of data contains the value to be written to that register index. If multiple data bytes are written then the internal register index is automatically incremented after each byte of data transferred. The master can send data bytes continuously to the slave until the slave fails to provide an acknowledge or the master terminates the write communication with a STOP condition or sends a repeated START (Sr).

Figure 19. Read message



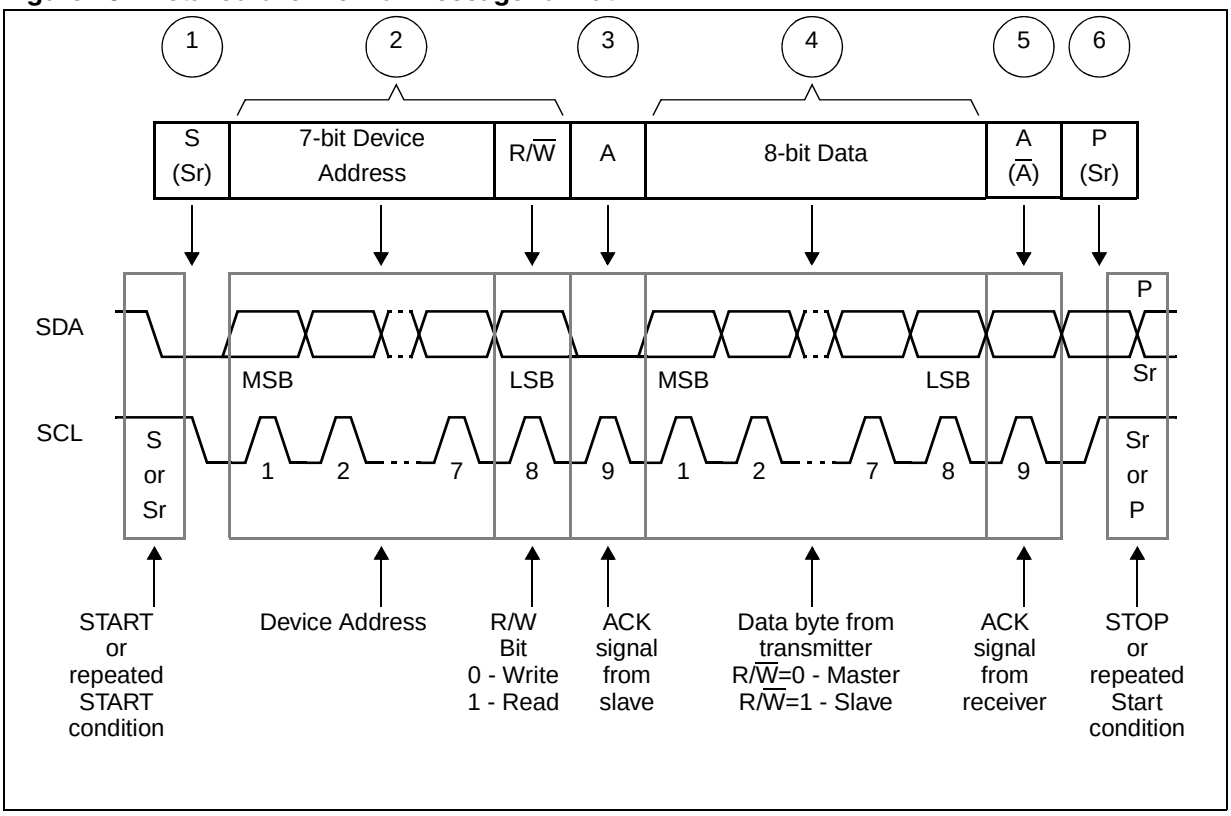
For the master reading from the slave the device address is followed by the contents of last register index that the previous read or write message accessed. If multiple data bytes are read then the internal register index is automatically incremented after each byte of data

read. A read message is terminated by the bus master generating a negative acknowledge after reading a final byte of data.

A message can only be terminated by the bus master, either by issuing a stop condition, a repeated start condition or by a negative acknowledge after reading a complete byte during a read operation.

10.2 Detailed overview of the message format

Figure 20. Detailed overview of message format



The V2W generic message format consists of the following sequence

1. Master generates a START condition to signal the start of new message.
2. Master outputs, MS bit first, a 7-bit device address of the slave the master is trying to communicate with followed by a R/$\overline{W}$ bit.
   a) R/$\overline{W}$ = 0 then the master (transmitter) is writing to the slave (receiver).
   b) R/$\overline{W}$ = 1 the master (receiver) is reading from the slave (transmitter).
3. The addressed slave acknowledges the device address.
4. Data transmitted on the bus
   a) When a write is performed then master outputs 8-bits of data on SDA (MS Bit first).
   b) When a read is performed then slave outputs 8-bits of data on SDA (MS Bit First).
5. Data receive acknowledge
   a) When a write is performed slave acknowledges data.
   b) When a read is performed master acknowledges data.

Repeat 4 and 5 until all the required data has been written or read.

Minimum number of data bytes for a read =1 (Shortest Message length is 2-bytes).

The master outputs a negative acknowledge for the data when reading the last byte of data. This causes the slave to stop the output of data and allows the master to generate a STOP condition.

6. Master generates a STOP condition or a repeated START.

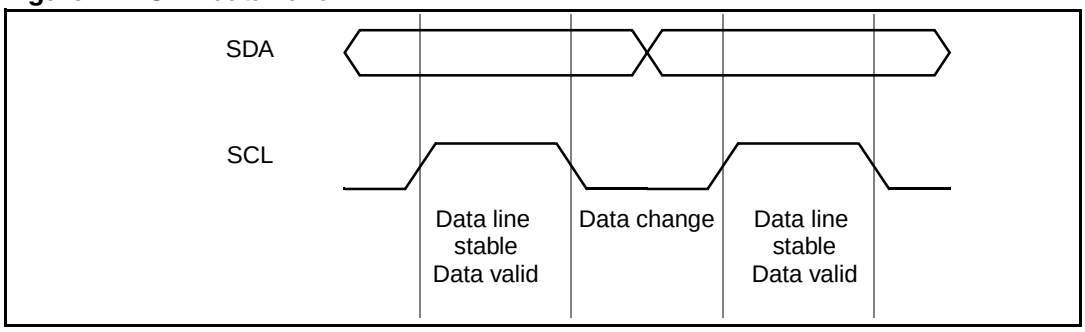
Figure 21. Device addresses

Sensor address	0	0	1	0	0	0	0	R/$\overline{W}$
Sensor write address 20_H	0	0	1	0	0	0	0	0
Sensor read address 21_H	0	0	1	0	0	0	0	1

10.3 Data valid

The data on SDA is stable during the high period of SCL. The state of SDA is changed during the low phase of SCL. The only exceptions to this are the start (S) and stop (P) conditions as defined below. (See *I²C slave interface* for full timing specification).

Figure 22. SDA data valid



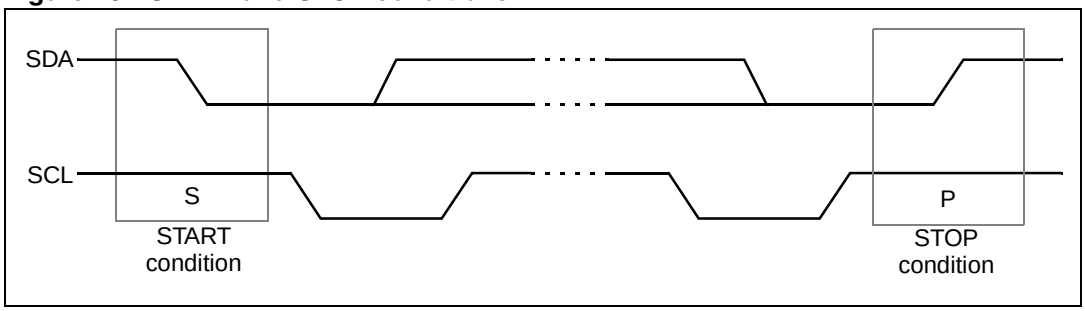
10.4 Start (S) and Stop (P) conditions

A START (S) condition defines the start of a V2W message. It consists of a high to low transition on SDA while SCL is high.

A STOP (P) condition defines the end of a V2W message. It consists of a low to high transition on SDA while SCL is high.

After STOP condition the bus is considered free for use by other devices. If a repeated START (Sr) is used instead of a stop then the bus stays busy. A START (S) and a repeated START (Sr) are considered to be functionally equivalent.

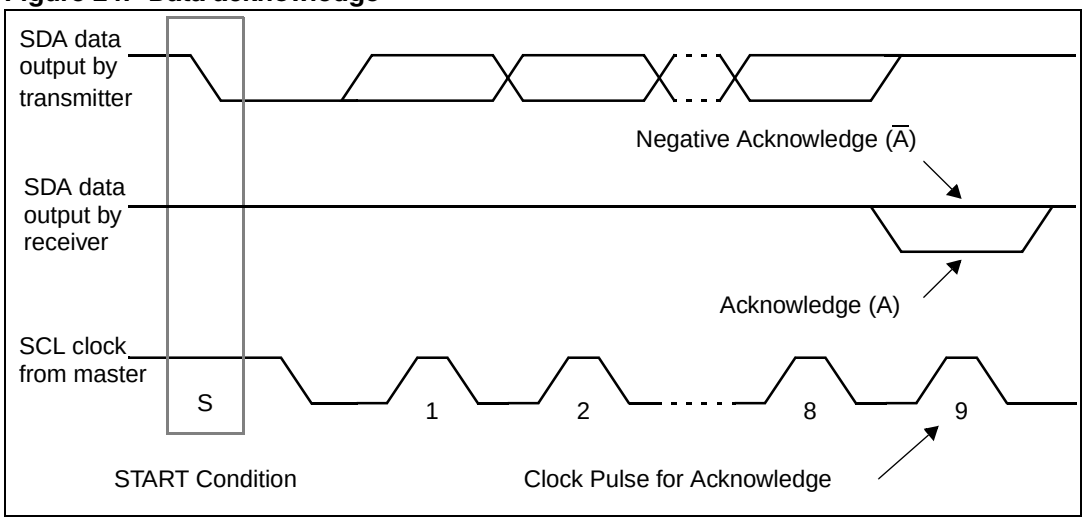
Figure 23. START and STOP conditions



10.5 Acknowledge

After every byte transferred the receiver must output an acknowledge bit. To acknowledge the data byte receiver pulls SDA during the 9th SCL clock cycle generated by the master. If SDA is not pulled low then the transmitter stops the output of data and releases control of the bus back to the master so that it can either generate a STOP or a repeated START condition.

Figure 24. Data acknowledge

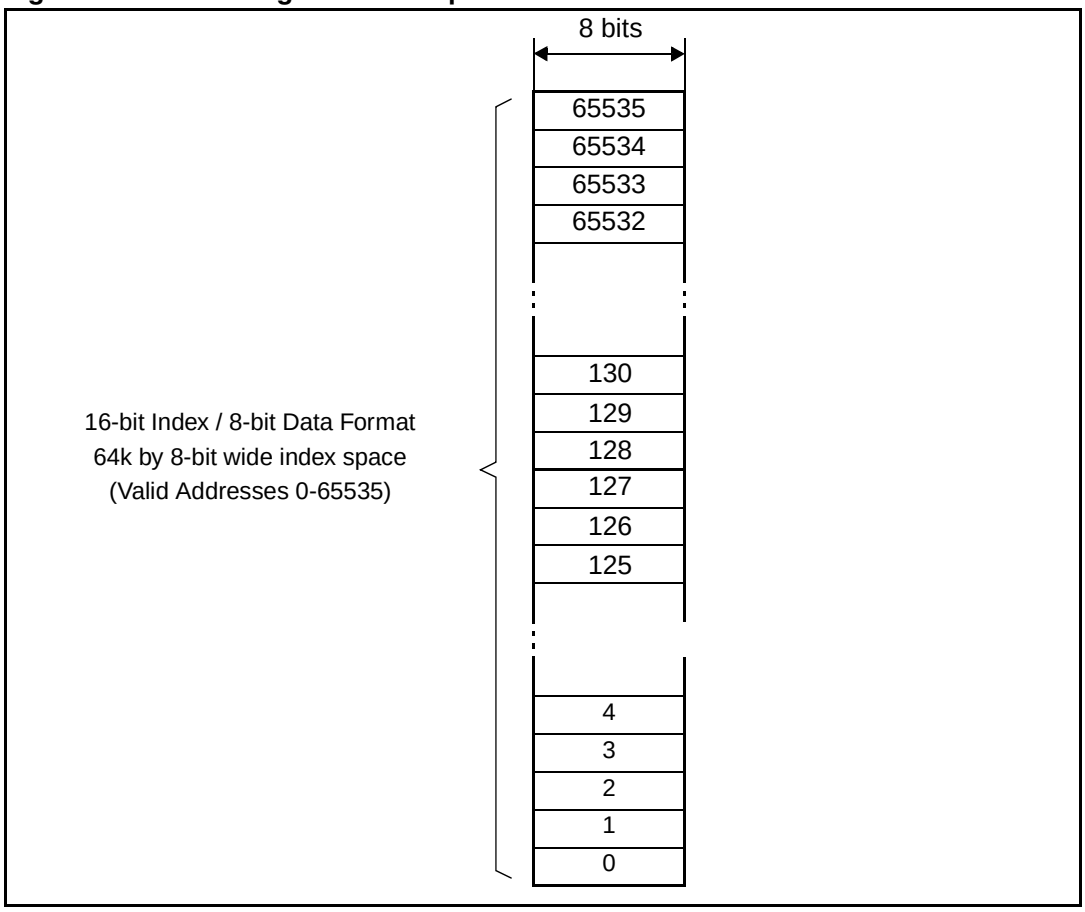


10.6 Index space

Communication using the serial bus centres around a number of registers internal to the either the sensor or the co-processor. These registers store sensor status, set-up, exposure and system information. Most of the registers are read/write allowing the receiving equipment to change their contents. Others (such as the chip id) are read only.

The internal register locations are organized in a 64k by 8-bit wide space. This space includes “real” registers, SRAM, ROM and/or micro controller values.

Figure 25. Internal register index space



10.7 Types of messages

This section gives guidelines on the basic operations to read data from and write data to VL6624/VS6624.

The serial interface supports variable length messages. A message contains no data bytes or one data byte or many data bytes. This data can be written to or read from common or different locations within the sensor. The range of instructions available are detailed below.

- Single location, single byte data read or write.
- Write no data byte. Only sets the index for a subsequent read message.
- Multiple location, multiple data read or write for fast information transfers.

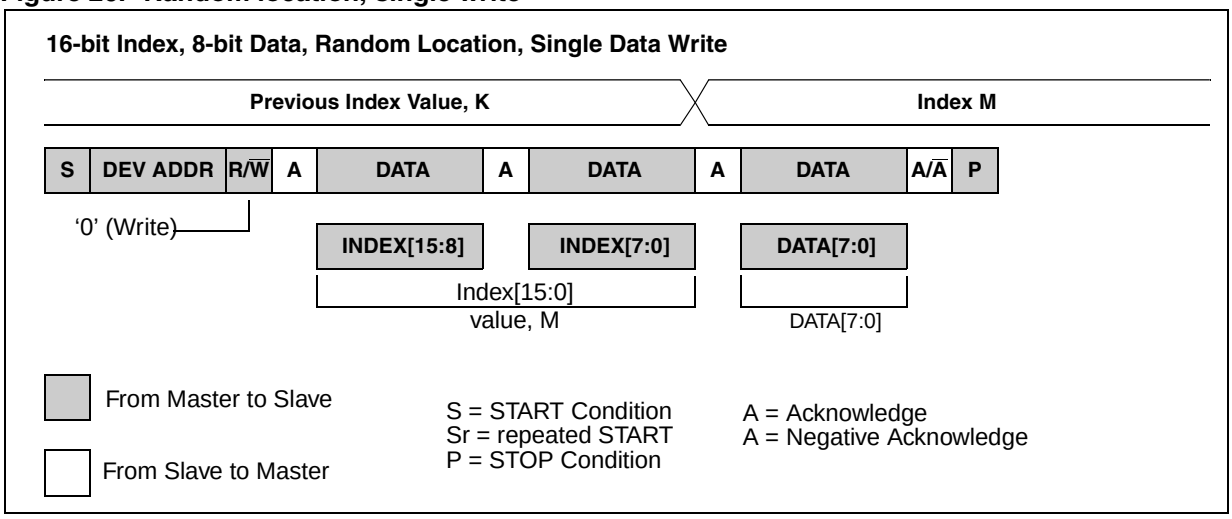
Any messages formats other than those specified in the following section should be considered illegal.

10.8 Random location, single data write

For the master writing to the slave the R/$\overline{W}$ bit is set to zero.

The register index value written is preserved and is used by a subsequent read. The write message is terminated with a stop condition from the master.

Figure 26. Random location, single write



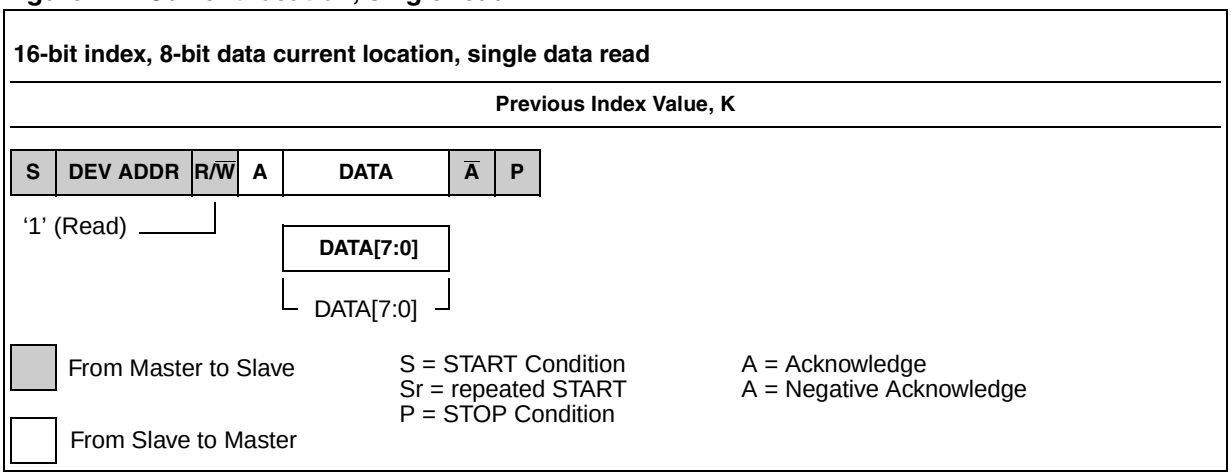
10.9 Current location, single data read

For the master reading from the slave the R/$\overline{W}$ bit is set to one. The register index of the data returned is that accessed by the previous read or write message.

The first data byte returned by a read message is the contents of the internal index value and NOT the index value. This was the case in older V2W implementations.

Note that the read message is terminated with a negative acknowledge ($\overline{A}$) from the master: it is not guaranteed that the master will be able to issue a stop condition at any other time during a read message. This is because if the data sent by the slave is all zeros, the SDA line cannot rise, which is part of the stop condition.

Figure 27. Current location, single read

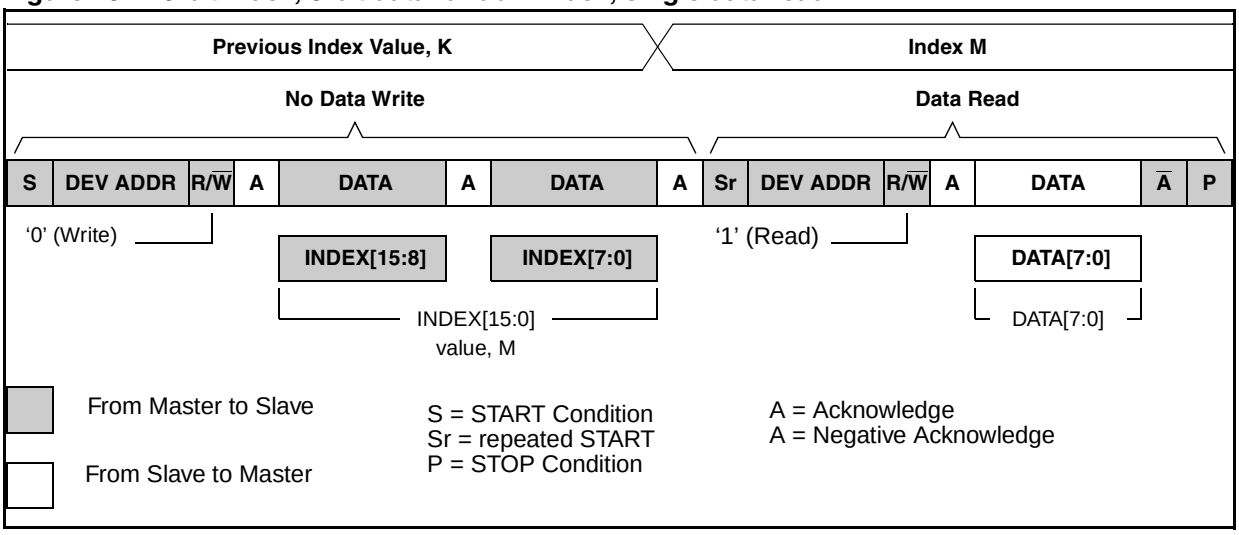


10.10 Random location, single data read

When a location is to be read, but the value of the stored index is not known, a write message with no data byte must be written first, specifying the index. The read message then completes the message sequence. To avoid relinquishing the serial to bus to another master a repeated start condition is asserted between the write and read messages.

As mentioned in the previous example, the read message is terminated with a negative acknowledge ($\overline{A}$) from the master.

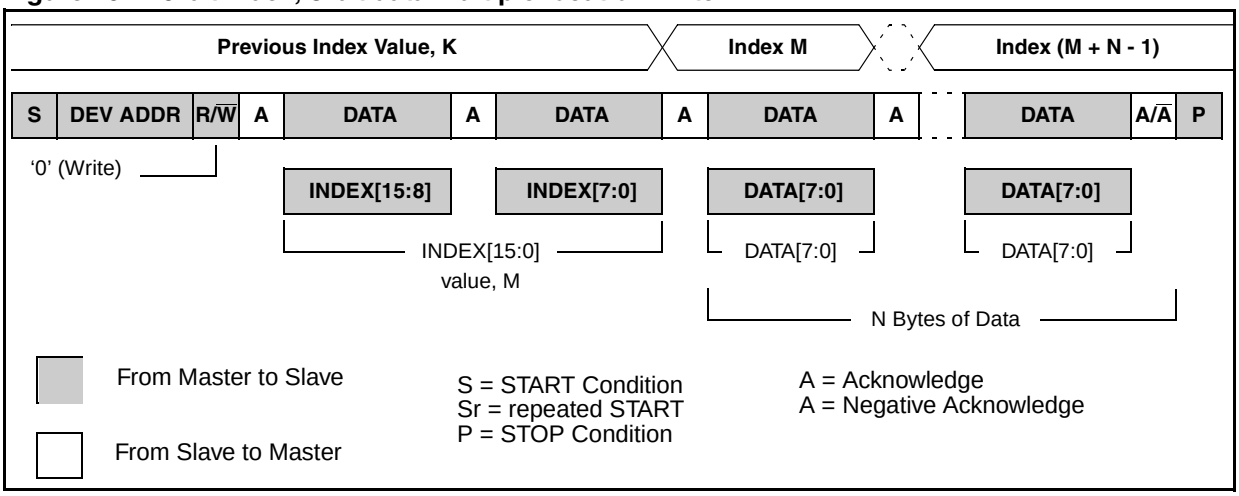
Figure 28. 16-bit index, 8-bit data random index, single data read



10.11 Multiple location write

For messages with more than 1 data byte the internal register index is automatically incremented for each byte of data output, making it possible to write data bytes to consecutive adjacent internal registers without having to send explicit indexes prior to sending each data byte.

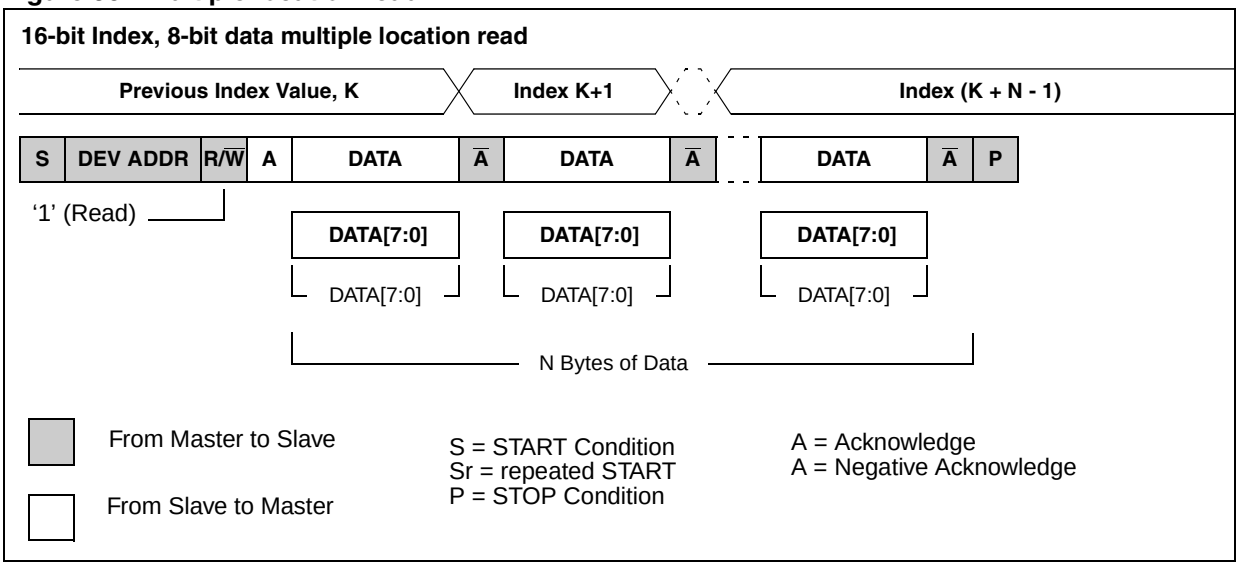
Figure 29. 16-bit index, 8-bit data multiple location write



10.12 Multiple location read stating from the current location

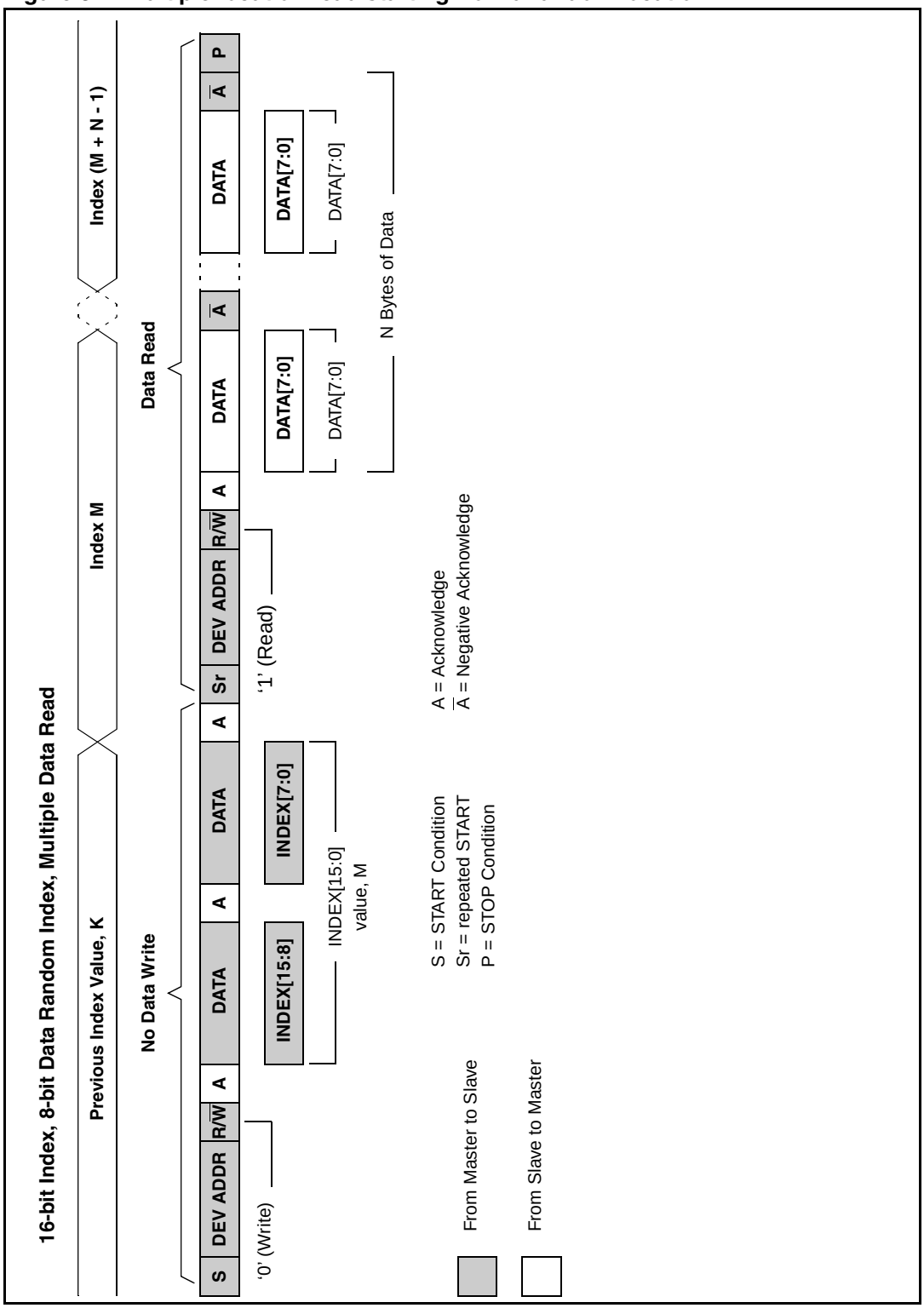
In the same manner to multiple location writes, multiple locations can be read with a single read message.

Figure 30. Multiple location read



10.13 Multiple location read starting from a random location

Figure 31. Multiple location read starting from a random location



11 Register map

The VL6624/VS6624 I²C write address is 0x20.

To read or write to registers other than those in *Low level control registers* section the device must be switched on, this is done by writing 0x02 to 0xC003. Information on initial power up for the device can be found in the *Section 9: Getting started*.

All I²C locations contain an 8-bit byte. However, certain parameters require 16 bits to represent them and are therefore stored in more than 1 location.

Note: For all 16 bit parameters the MSB register must be written before the LSB register.

The data stored in each location can be interpreted in different ways as shown below. Register contents represent different data types as described in *Table 6*.

Table 6. Data type

Data Type	Description
BYTE	Single field register 8 bit parameter
UINT_16	Multiple field registers - 16 bit parameter
FLAG_e	Bit 0 of register must be set/cleared
CODED	Coded register - function depends on value written
FLOAT	Float Value

Float number format

Float 900 is used in ST co-processors to represent floating point numbers in 2 bytes of data. It conforms to the following structure:

Bit[15] = Sign bit (1 represents negative)

Bit[14:9] = 6 bits of exponent, biased at decimal 31

Bit[8:0] = 9 bits of mantissa

To convert a floating point number to Float 900, use the following procedure:

- represent the number as a binary floating point number. Normalize the mantissa and calculate the exponent to give a binary scientific representation of 1.xxxxxxxxx * 2^y.
- The x symbols should represent 9 binary digits of the mantissa, round or pad with zeros to achieve 9 digits in total. Remove the leading 1 from the mantissa as it is redundant.
- To calculate the y value Bias the exponent by adding to 31 decimal then converting to binary.
- The data can then be placed in the structure above.

Example

Convert -0.41 to Float 900

Convert the fraction into binary by successive multiplication by 2 and removal of integer component

0.41 * 2 = 0.82	0
0.82 * 2 = 1.64	1
0.64 * 2 = 1.28	1
0.28 * 2 = 0.56	0
0.56 * 2 = 1.12	1
0.12 * 2 = 0.24	0
0.24 * 2 = 0.48	0
0.48 * 2 = 0.96	0
0.96 * 2 = 1.92	1
0.92 * 2 = 1.84	1
0.84 * 2 = 1.68	1
0.68 * 2 = 1.36	1
0.36 * 2 = 0.72	0

This gives us -0.0110100011110.

We then normalize by moving the decimal point to give - 1.10100011110 * 2^-2.

The mantissa is rounded and the leading zero removed to give 101001000.
We add the exponent to the bias of 31 that gives us 29 or 11101.
A leading zero is added to give 6 bits 011101.

The sign bit is set at 1 as the number is negative.

This gives us 1011 1011 0100 1000 as our Float 900 representation or BB48 in hex.

To convert the encoded representation back to a decimal floating point, we can use the following formula.

Real is = (-1)^sign * ((512+mantissae)>> 9) * 2^(exp-31)

Thus to convert BB48 back to decimal, the following procedure is followed:

Note that >>9 right shift is equal to division by 2^9.

Sign = 1

Exponent = 11101 (29 decimal)

Mantissa = 101001000 (328 decimal)

This gives us:

real = (-1)^1 * ((512+328)/2^9) * 2^(29-31)

real = -1 * (840/512) * 2^(-2)

real = -1 * 1.640625 * 0.25

real = -0.41015625

When compared to the original -0.41, we see that some rounding errors have been introduced.

Low level control registers

Table 7. Low-level control registers

Index	LowLevelControlRegisters[1]	
0xC003	**MicroEnable**	
	Default value	0x1c
	Purpose	Used to power up the device
	Type	CODED
	Possible values	<0x1c> initial state after low to high transition of CE pin <0x02> Power enable for all MCU Clock- start device
0xC044	**DIO_Enable**	
	Default value	0x00
	Purpose	Enables the digital I/O of the device
	Type	CODED
	Possible values	<0> IO pins in a high impedance state ‘Tri-state’ <1> IO pins enabled

1. Can be controlled in all stable states.

Note: The default values for the above registers are true when the device is powered on, Ext. Clk input is present and the CE pin is high. All other registers can be read when the MicroEnable register is set to 0x02.

User interface map

Device parameters [read only]

Table 8. Device parameters [read only]

Index	DeviceParameters [read only][1]	
0x0001 (MSByte) 0x0002 (LSByte)	**uwDeviceId**	
	Purpose	device id e.g. 624
	Type	UINT
0x0004	**bFirmwareVsnMajor**	
	Type	BYTE
0x0006	**bFirmwareVsnMinor**	
	Type	BYTE
0x0008	**bPatchVsnMajor**	
	Type	BYTE
0x000a	**bPatchVsnMinor**	
	Type	BYTE

1. Can be accessed in all stable state.

Host interface manager control

Table 9. Host interface manager control

Index	HostInterfaceManagerControl[1]	
0x0180	**bUserCommand**	
	Default value	<0> UNINITIALISED
	Purpose	User level control of operating states
	Type	CODED
	Possible values	<0> UNINITIALISED - powerup default <1> BOOT - the boot command will identify the sensor & setup low level handlers <2> RUN - stream video <3> PAUSE- stop video streaming <4> STOP - low power mode, analogue powered down <3> SNAPSHOT- grab one frame at correct exposure without flashgun <6> FLASHGUN - grab one frame at correct exposure for flashgun

1. Can be controlled in all stable states

Host interface manager status

Table 10. Host interface manager status [Read only]

Index	HostInterfaceManagerStatus [Read only][1]	
0x0202	**bState**	
	Default Value	<16>_RAW
	Purpose	The current state of the mode manager.
	Type	CODED
	Possible values	<16>_RAW - default powerup state. <33> WAITING_FOR_BOOT - Waiting for ModeManager to signal BOOT event. <34> PAUSED - Booted, the input pipe is idle. <38>WAITING_FOR_RUN - Waiting for ModeManager to complete RUN setup. <49> RUNNING - The pipe is active. <50> WAITING_FOR_PAUSE - The host has issued a PAUSE command. The HostInterfaceManager is waiting for the ModeManager to signal PAUSE processing complete. <64> FLASHGUN - Grabbing a single frame. <80> STOPPED - Low power

1. Can be accessed in all stable states

Run mode control

Table 11. Run mode control

Index	RunModeControl[1]	
0x0280	**fMeteringOn**	
	Default Value:	<1> TRUE
	Purpose	If metering is off the Auto Exposure (AE) and Auto White Balance (AWB) tasks are disabled
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE

1. Can be controlled in all stable states

Mode setup

Table 12. Mode setup

Index	ModeSetup	
0x0302	**bNonViewLive_ActivePipeSetupBank (Can be controlled in all stable states)**	
	Default Value:	<0> PipeSetupbank_0
	Purpose	Select the active bank for non view live mode
	Type	CODED
	Possible values	<0> PipeSetupbank_0 <1>PipeSetupbank_1
0x0308	**SensorMode (Must be configured in STOP mode)**	
	Default value	<0>SensorMode_SXGA
	Purpose	Select the different sensor mode
	Type	CODED
	Possible values	<0>SensorMode_SXGA <1>SensorMode_VGA <2>SensorMode_VGANormal

Pipe setup bank0

Table 13. Pipe setup bank0

Index	PipeSetupBank0[(1)]	
0x0380	**bImageSize0 #**	
	Default value	<1> ImageSize_SXGA
	Purpose	required output dimension.
	Type	CODED
	Possible values	<1> ImageSize_SXGA <2> ImageSize_VGA <3> ImageSize_CIF <4> ImageSize_QVGA <5> ImageSize_QCIF <6> ImageSize_QQVGA <7> ImageSize_QQCIF <8> ImageSize_Manual - to use ManualSubSample and ManualCrop controls select Manual mode.
0x0383(MSB) 0x0384(LSB)	**uwManualHSize0 #**	
	Default value	0x00
	Purpose	if ImageSize_Manual selected, input required manual H size
	Type	UINT16

Table 13. Pipe setup bank0

Index	PipeSetupBank0[1]	
0x0387(MSB) 0x0388(LSB)	**uwManualVSize0 #**	
	Default value	0x00
	Purpose	if ImageSize_Manual selected, input required manual V size
	Type	UINT16
0x038b(MSB) 0x038c(LSB)	**uwZoomStepHSize0**	
	Default value	0x01
	Purpose	Set the zoom H step
	Type	UINT16
0x038f(MSB) 0x0390(LSB)	**uwZoomStepVSize0**	
	Default value	0x01
	Purpose	Set the zoom V step
	Type	UINT16
0x0392	**bZoomControl0**	
	Default value	<0> ZoomStop
	Purpose	control zoom in, zoom out and zoom stop
	Type	C
	Possible values	<0> ZoomStop <1> ZoomStart_In <2> ZoomStart_Out
0x0395(MSB) 0x0396(LSB)	**uwPanStepIHSize0**	
	Default value	0x00
	Purpose	Set the pan H step
	Type	UINT16
0x0399(MSB) 0x039a(LSB)	**uwPanStepVSize0**	
	Default value	0x00
	Purpose	Set the PanV step
	Type	UINT16

Table 13. Pipe setup bank0

Index	PipeSetupBank0[1]	
0x039c	**bPanControl0**	
	Default value	<0> Pan_Disable
	Purpose	control pandisable, pan right, pan left, pan up, pan down
	Type	C
	Possible values	<0> Pan_Disable <1> Pan_Right <2> Pan_Left <3> Pan_Down <4> Pan_Up
0x039e	**bCropControl0**	
	Default value	<1> Crop_auto
	Purpose	Select cropping manual or auto
	Type	C
	Possible values	<0> Crop_manual <1> Crop_auto
0x03a1(MSB) 0x03a2(LSB)	**uwManualCropHorizontalStart0**	
	Default value	0x00
	Purpose	Set the cropping H start address
	Type	UINT16
0x03a5(MSB) 0x03a6(LSB)	**uwManualCropHorizontalSize0**	
	Default value	0x00
	Purpose	Set the cropping H size
	Type	UINT16
0x03a9(MSB) 0x03aa(LSB)	**uwManualCropVerticalStart0**	
	Default value	0x00
	Purpose	Set the cropping Vstart address
	Type	UINT16
0x03ad(MSB) 0x03ae(LSB)	**uwManualCropVerticalSize0**	
	Default value	0x00
	Purpose	Set the cropping Vsize
	Type	UINT16

Table 13. Pipe setup bank0

Index	PipeSetupBank0[1]	
0x03b0	**bImageFormat0 #[2]**	
	Default value	<0> ImageFormat_YCbCr_JFIF
	Purpose	select required output image format.
	Type	CODED
	Possible values	<0> ImageFormat_YCbCr_JFIF <1> ImageFormat_YCbCr_Rec601 <2> ImageFormat_YCbCr_Custom - to use custom output select required RgbToYuvOutputSignalRange from 'PipeSetupBank' page. <3> ImageFormat_YCbCr_400 <4> ImageFormat_RGB_565 <5> ImageFormat_RGB_565_Custom - to use custom output select required RgbToYuvOutputSignalRange from 'PipeSetupBank' page. <6> ImageFormat_RGB_444 <7> ImageFormat_RGB_444_Custom - to use custom output select required RgbToYuvOutputSignalRange from 'PipeSetupBank' page. <9> ImageFormat_Bayer10_ThroughVP <10> ImageFormat_Bayer8_CompThroughVP-- to compress bayer data to 8 bits data <11> ImageFormat_Bayer8_TranThroughVP-- to truncate bayer data to 8 bits data
0x03b2	**bBayerOutputAlignment0**	
	Default value	<4> BayerOutputAlignment_RightShifted
	Purpose	set bayer output alignment
	Type	CODED
	Possible values	<4> BayerOutputAlignment_RightShifted <5> BayerOutputAlignment_LeftShifted
0x03b4	**bContrast0**	
	Default value	0x87
	Purpose	contrast control for both YCbCr and RGB output.
	Type	BYTE
0x03b6	**bColourSaturation0**	
	Default value	0x78
	Purpose	colour saturation control for both YCbCr and RGB output.
	Type	BYTE
0x03b8	**bGamma0**	
	Default value	0x0f
	Purpose	gamma settings.
	Type	BYTE
	Possible values	0 to 31

Table 13. Pipe setup bank0

Index	PipeSetupBank0[1]	
0x03ba	**fHorizontalMirror0**	
	Default Value:	0x00
	Purpose	Horizontal image orientation flip
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x03bc	**fVerticalFlip0**	
	Default Value:	0x00
	Purpose	Vertical image orientation flip
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x03be	**bChannelID**	
	Default value	0x00
	Purpose	Logical DMA Channel Number
	Type	BYTE
	Possible values	0 to 6

1. Can be controlled in all stable state.
   # denotes registers where changes will only be consumed during the transition to a RUN state.
2. It is possible to switch between any YCrCb (422) mode, RGB mode and Bayer 10bit or move between YCrCb 400 and a bayer8 mode without a requiring a transition to STOP, it is not possible to move between these groups of modes without first a transition to STOP then a BOOT.

Pipe setup bank1

Table 14. Pipe setup bank1

Index	PipeSetupBank1[1]	
0x0400	**bImageSize1 #**	
	Default value	<1> ImageSize_SXGA
	Purpose	required output dimension.
	Type	CODED
	Possible values	<1> ImageSize_SXGA <2> ImageSize_VGA <3> ImageSize_CIF <4> ImageSize_QVGA <5> ImageSize_QCIF <6> ImageSize_QQVGA <7> ImageSize_QQCIF <8> ImageSize_Manual - to use ManualSubSample and ManualCrop controls select Manual mode.
0x0403(MSB) 0x0404(LSB)	**uwManualHSize1 #**	
	Default value	0x00
	Purpose	if ImageSize_Manual selected, input required manual H size
	Type	UINT16
0x0407(MSB) 0x0408(LSB)	**uwManualVSize1 #**	
	Default value	0x00
	Purpose	if ImageSize_Manual selected, input required manual V size
	Type	UINT16
0x040b(MSB) 0x040c(LSB)	**uwZoomStepHSize1**	
	Default value	0x01
	Purpose	Set the zoom H step
	Type	UINT16
0x040f(MSB) 0x0410(LSB)	**uwZoomStepVSize1**	
	Default value	0x01
	Purpose	Set the zoom V step
	Type	UINT16

Table 14. Pipe setup bank1

Index	PipeSetupBank1[1]	
0x0412	**bZoomControl1**	
	Default value	<0> ZoomStop
	Purpose	control zoom in, zoom out, zoom stop
	Type	CODED
	Possible values	<0> ZoomStop <1> ZoomStart_In <2> ZoomStart_Out
0x0415(MSB) 0x0416(LSB)	**uwPanStepIHSize1**	
	Default value	0x00
	Purpose	Set the pan H step
	Type	UINT16
0x0419(MSB) 0x041a(LSB)	**uwPanStepVSize1**	
	Default value	0x00
	Purpose	Set the PanV step
	Type	UINT16
0x041c	**bPanControl1**	
	Default value	<0> Pan_Disable
	Purpose	control pandisable, pan right, pan left, pan up, pan down
	Type	C
	Possible values	<0> Pan_Disable <1> Pan_Right <2> Pan_Left <3> Pan_Down <4> Pan_Up
0x041e	**bCropControl1**	
	Default value	<1> Crop_auto
	Purpose	Select cropping manual or auto
	Type	C
	Possible values	<0> Crop_manual <1> Crop_auto
0x0421(MSB) 0x0422(LSB)	**uwManualCropHorizontalStart1**	
	Default value	0x00
	Purpose	Set the cropping H start address
	Type	UINT16

Table 14. Pipe setup bank1

Index	PipeSetupBank1[1]	
0x0425(MSB) 0x0426(LSB)	**uwManualCropHorizontalSize1**	
	Default value	0x00
	Purpose	Set the cropping H size
	Type	UINT16
0x0429(MSB) 0x042a(LSB)	**uwManualCropVerticalStart1**	
	Default value	0x00
	Purpose	Set the cropping Vstart address
	Type	UINT16
0x042d(MSB) 0x042e(LSB)	**uwManualCropVerticalSize1**	
	Default value	0x00
	Purpose	Set the cropping Vsize
	Type	UINT16
0x0430	**bImageFormat1[2]**	
	Default value	<0> ImageFormat_YCbCr_JFIF
	Purpose	select required output image format.
	Type	CODED
	Possible values	<0> ImageFormat_YCbCr_JFIF <1> ImageFormat_YCbCr_Rec601 <2> ImageFormat_YCbCr_Custom - to use custom output select required RgbToYuvOutputSignalRange from 'PipeSetupBank' page. <3> ImageFormat_YCbCr_400 <4> ImageFormat_RGB_565 <5> ImageFormat_RGB_565_Custom - to use custom output select required RgbToYuvOutputSignalRange from 'PipeSetupBank' page. <6> ImageFormat_RGB_444 <7> ImageFormat_RGB_444_Custom - to use custom output select required RgbToYuvOutputSignalRange from 'PipeSetupBank' page. <9> ImageFormat_Bayer10ThroughVP <10> ImageFormat_Bayer8CompThroughVP-- to compress bayer data to 8 bits data <11> ImageFormat_Bayer8TranThroughVP-- to truncate bayer data to 8 bits data
0x0432	**bBayerOutputAlignment1**	
	Default value	<4> BayerOutputAlignment_RightShifted
	Purpose	set bayer output alignment
	Type	CODED
	Possible values	<4> BayerOutputAlignment_RightShifted <5> BayerOutputAlignment_LeftShifted

Table 14. Pipe setup bank1

Index	PipeSetupBank1[1]	
0x0434	**bContrast1**	
	Default value	0x87
	Purpose	contrast control for both YCbCr and RGB output.
	Type	BYTE
0x0436	**bColourSaturation1**	
	Default value	0x78
	Purpose	colour saturation control for both YCbCr and RGB output.
	Type	BYTE
0x0438	**bGamma1**	
	Default value	0x0f
	Purpose	gamma settings.
	Type	BYTE
	Possible values	0 to 31
0x043a	**fHorizontalMirror1**	
	Default value	0x00
	Purpose	Horizontal image orientation flip
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x043c	**fVerticalFlip1**	
	Default value	0x00
	Purpose	Vertical image orientation flip
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x043e	**bChannelD**	
	Default value	0x00
	Purpose	Logical DMA Channel Number
	Type	BYTE
	Possible values	0 to 6

1. Can be controlled in all stable state. # denotes registers where changes will only be consumed during the transition to a RUN state.
2. It is possible to switch between any YCrCb (422) mode, RGB mode and Bayer 10bit or move between YCrCb 400 and a bayer8 mode without a requiring a transition to STOP, it is not possible to move between these groups of modes without first a transition to STOP then a BOOT.

Viewlive control

Table 15. ViewLive control

Index	ViewLiveControl	
0x0480	**fEnable (Can be controlled in all stable states)**	
	Default value	<0> FALSE
	Purpose	set to enable the View Live mode.
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x0482	**bInitialPipeSetupBank (must be setup in PAUSE or STOP mode)**	
	Default value	<0> PipeSetupBank_0
	Purpose	First frame output will be from PipeSetupBank selected by 'bInitialPipeSetupBank'. if ViewLive is enabled the next frame will be from the other PipeSetupBank, otherwise only one PipeSetupBank will be used.
	Type	CODED
	Possible values	<0> PipeSetupBank_0 <1> PipeSetupBank_1

Viewlive status [read only]

Table 16. Viewlive status

Index	ViewLiveStatus [read only]	
0x0500	**CurrentPipeSetupBank**	
	Default value	<0> PipeSetupBank_0
	Purpose	indicates the PipeSetupBank which has most recently been applied to the pixel pipe hardware.
	Type	CODED
	Possible values	<0> PipeSetupBank_0 <1> PipeSetupBank_1

Power management

Table 17. Power management

Index	PowerManagement[1]	
0x0580	**bTimeToPowerdown**	
	Default value	0x0f
	Purpose	Time (mSecs) from entering Pause mode until the system automatically transitions stop mode. 0xff disables the automatic transition.
	Type	BYTE

1. Must be configured in STOP mode

Video timing parameter host inputs

Table 18. Video timing parameter host inputs

Index	VideoTimingParameterHostInputs[1]	
0x0605 (MSByte) 0x0606 (LSByte)	**uwExternalClockFrequencyMhzNumerator**	
	Default value	0x0c
	Purpose	specifies the External Clock Frequency... external clock frequency = uwExternalClockFrequencyMhzNumerator/bExternalClockFrequencyMhzDenominator
	Type	UINT16
0x0608	**bExternalClockFrequencyMhzDenominator**	
	Default value	0x01
	Type	BYTE

1. Should be configured in the RAW state

Video timing control

Table 19. Video timing control

Index	VideoTimingControl[1]	
0x0880	**bSysClkMode**	
	Default value	0x00
	Purpose	Decides system centre clock frequency
	Type	CODED
	Possible values	<0>12MHz Mode <1>13MHz Mode <2>13.5MHz Mode <3>Slave Mode

1. Should be configured in the RAW state

Frame dimension parameter host inputs

Table 20. Frame dimension parameter host inputs

Index	FrameDimensionParameterHostInputs[1]	
0x0c80	**bLightingFrequencyHz**	
	Default value	0x00
	Purpose	AC Frequency - used for flicker free time period calculations this mains frequency determines the flicker free time period.
	Type	BYTE
0x0c82	**fFlickerCompatibleFrameLength**	
	Default value	<0> FALSE
	Purpose	flicker_compatible_frame_length
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE

1. Can be controlled in all stable states

Static frame rate control

Table 21. Static frame rate control

Index	StaticFrameRateControl[1]	
0x0d81 (MSByte) 0x0d82 (LSByte)	**uwDesiredFrameRate_Num**	
	Default value	0x0f
	Purpose	Numerator for the Frame Rate
	Type	UINT16
0x0d84	**bDesiredFrameRate_Den**	
	Default value	0x01
	Purpose	Denominator for the Frame Rate
	Type	BYTE

1. Can be controlled in all stable states

Automatic Frame rate control

Table 22. Automatic Frame Rate Control

Index	AutomaticFrameRateControl[1]	
0x0e80	**bDisableFrameRateDamper**	
	Default value	0x00
	Purpose	Defines the mode in which the framerate of the system would work
	Type	
	Possible values	<0> Manual <1> Auto
0x0e8c (MSByte) 0x0e8a (LSByte)	**bMinimumDamperOutput**	
	Default value	0x00
	Purpose	Sets the minimum framerate employed when in automatic framerate mode.
	Type	UINT16

1. Can be controlled in all stable states

Exposure controls

Table 23. Exposure controls

Index	ExposureControls[1]	
0x1180	**bMode**	
	Default value	<0> AUTOMATIC_MODE
	Purpose	Sets the mode for the Exposure Algorithm
	Type	CODED
	possible values	<0> AUTOMATIC_MODE - Automatic Mode of Exposure which includes computation of Relative Step <1> COMPILED_MANUAL_MODE - Compiled Manual Mode in which the desired exposure is given and not calculated by algorithm <2> DIRECT_MANUAL_MODE - Mode in which the exposure parameters are input directly and not calculated by compiler <3> FLASHGUN_MODE - Flash Gun Mode in which the exposure parameters are set to fixed values

Table 23. Exposure controls

Index	ExposureControls[1]	
0x1182	**bMetering**	
	Default value	<0> ExposureMetering_flat
	Purpose	Weights to be associated with the zones for calculating the mean statistics Exposure Weight could Centered, Backlit or Flat
	Type	C
	possible values	<0> ExposureMetering_flat - Uniform gain associated with all pixels <1> ExposureMetering_backlit - more gain associated with centre pixels and bottom pixels <2> ExposureMetering_centred - more gain associated with centre pixels
0x1184	**bManualExposureTime_Num**	
	Default value	0x01
	Purpose	Exposure Time for Compiled Manual Mode in seconds. Num/Den gives required exposure time
	Type	BYTE
0x1186	**bManualExposureTime_Den**	
	Default value	0x1e
	Type	BYTE
0x1189 (MSByte) 0x118a (LSByte)	**fpManualFloatExposureTime**	
	Default value	0x59aa (15008)
	Purpose	Exposure Time for the Manual Mode. This value is in uSecs
	Type	FLOAT
0x1190	**iExposureCompensation**	
	Default value	0x00
	Purpose	Exposure Compensation - a user choice for setting the runtime target. A unit of exposure compensation corresponds to 1/6 EV. Default value according to the Nominal Target of 30 is 0. Coded Value of Exposure compensation can take values from -25 to 12.
	Type	INT8
0x1195 (MSByte) 0x1196 (LSByte)	**uwDirectModeCoarseIntegrationLines**	
	Default value	0x00
	Purpose	Coarse Integration Lines to be set for Direct Mode
	Type	UINT16

Table 23. Exposure controls

Index	ExposureControls[1]	
0x1199 (MSByte) 0x119a (LSByte)	**uwDirectModeFineIntegrationPixels**	
	Default value	0x00
	Purpose	Fine Integration Pixels to be set for Direct Mode
	Type	UINT16
0x119d (MSByte) 0x119e (LSByte)	**fpDirectModeAnalogGain**	
	Default value	0x00
	Purpose	Analog Gain to be set for Direct Mode
	Type	FLOAT
0x11a1 (MSByte) 0x11a2 (LSByte)	**fpDirectModeDigitalGain**	
	Default value	0x00
	Purpose	Digital Gain to be set for Direct Mode
	Type	FLOAT
0x11a5 (MSByte) 0x11a6 (LSByte)	**uwFlashGunModeCoarseIntLines**	
	Default value	0x00
	Purpose	Coarse Integration Lines to be set for Flash Gun Mode
	Type	UINT16
0x11a9 (MSByte) 0x11aa (LSByte)	**uwFlashGunModeFineIntPixels**	
	Default value	0x00
	Purpose	Fine Integration Pixels to be set for Flash Gun Mode
	Type	UINT16
0x11ad (MSByte) 0x11ae (LSByte)	**fpFlashGunModeAnalogGain**	
	Default value	0x00
	Purpose	Analog Gain to be set for Flash Gun Mode
	Type	FLOAT
0x11b1 (MSByte) 0x11b2 (LSByte)	**fpFlashGunModeDigitalGain**	
	Default value	0x00
	Purpose	Digital Gain to be set for Flash Gun Mode
	Type	FLOAT

Table 23. Exposure controls

Index	ExposureControls[1]	
0x11b4	**fFreezeAutoExposure**	
	Default value	<0> FALSE
	Purpose	Freeze auto exposure
	Type	Flag_e
	possible values	<0> FALSE <1> TRUE
0x11b7 (MSByte) 0x11b8 (LSByte)	**fpUserMaximumIntegrationTime**	
	Default value	0x647f (654336)
	Purpose	User Maximum Integration Time in microseconds. This control takes in the maximum integration time that host would like to support. This would in turn give an idea of the degree of “wobbly pencil effect” acceptable to Host.
	Type	FLOAT
0x11bb (MSByte) 0x11bc (LSByte)	**fpRecommendFlashGunAnalogGainThreshold**	
	Default value	0x4200 (4)
	Purpose	Recommend flash gun analog gain threshold value
	Type	FLOAT
0x11c0	**bAntiFlickerMode**	
	Default value	<0> AntiFlickerMode_Inhibit
	Purpose	Anti flicker mode
	Type	CODED
	Possible values	<0> AntiFlickerMode_Inhibit <1> AntiFlickerMode_ManualEnable <2>AntiFlickerMode_AutomaticEnable

1. Can be controlled in all stable states

White balance control

Table 24. White balance control parameters

Index	WBControlParameters(1)	
0x1480	**bMode**	
	Default value	<1> AUTOMATIC
	Purpose	For setting Mode of the white balance
	Type	CODED
	possible values	<0> OFF - No White balance, all gains will be unity in this mode <1> AUTOMATIC - Automatic mode, relative step is computed here <3> MANUAL_RGB - User manual mode, gains are applied manually <4> DAYLIGHT_PRESET - DAYLIGHT and all the modes below, fixed value of gains are applied here. <5> TUNGSTEN_PRESET <6> FLUORESCENT_PRESET <7> HORIZON_PRESET <8> MANUAL_COLOUR_TEMP <9> FLASHGUN_PRESET
0x1482	**bManualRedGain**	
	Default value	0x00
	Purpose	User setting for Red Channel gain
	Type	BYTE
0x1484	**bManualGreenGain**	
	Default value	0x00
	Purpose	User setting for Green Channel gain
	Type	BYTE
0x1486	**bManualBlueGain**	
	Default value	0x00
	Purpose	User setting for Blue Channel gain
	Type	BYTE
0x148b (MSByte) 0x148c (LSByte)	**fpFlashRedGain**	
	Default value	0x3e80 (1.250)
	Purpose	RedGain For FlashGun
	Type	FLOAT
0x148f (MSByte) 0x1490 (LSByte)	**fpFlashGreenGain**	
	Default value	0x3e00 (1.000)
	Purpose	Green Gain For FlashGun
	Type	FLOAT

Table 24. White balance control parameters

Index	WBControlParameters[1]	
0x1493 (MSByte) 0x1494 (LSByte)	**fpFlashBlueGain**	
	Default value	0x3e8a (1.269531)
	Purpose	BlueGain For FlashGun
	Type	FLOAT

1. Can be controlled in all stable states

Sensor setup

Table 25. Sensor setup

Index	SensorSetup[1]	
0x1990	**bBlackCorrectionOffset**	
	Default value	0x00
	Purpose	Black Correction Offset which would be added to the sensor pedestal to get the RE Offset. This is to improve the black level.
	Type	BYTE

1. Can be controlled in all stable states

Image Stability [read only]

Table 26. Image stability [read only]

Index	Image stability [read only]	
0x1900	**fWhiteBalanceStable**	
	Default value	0x00
	Purpose	Specifies that white balance system is stable/unstable
	Type	CODED
	Possible values	<0> Unstable <1>Stable
0x1902	**fExposureStable**	
	Default value	0x00
	Purpose	Specifies that white balance system is stable/unstable
	Type	CODED
	Possible values	<0> Unstable <1>Stable

Table 26. Image stability [read only]

Index	Image stability [read only]	
0x1906	**fStable**	
	Default value	0x00
	Purpose	Consolidated flag to indicate whether the system is stable/unstable
	Type	CODED
	Possible values	<0> Unstable <1>Stable

Flash control

Table 27. Flash control

Index	FlashControl(1)	
0x1a80	**bFlashMode**	
	Default value	<0> FLASH_OFF
	Purpose	Select the flash type and on/off
	Type	CODED
	Possible values	<0> FLASH_OFF <1>FLASH_TORCH <2>FLASH_PULSE
0x1a83(MSB) 0x1a84(LSB)	**uwFlashOffLine**	
	Default value	0x021c (540)
	Purpose	At flash_pulse mode, used to control off line
	Type	UINT16

1. Can be controlled in all stable states

Flash status [read only]

Table 28. Flash status

Index	FlashStatus [read only]	
0x1b00	**fFlashRecommend**	
	Default value	<0> FALSE
	Purpose	This flag is set if the Exposure Control system reports that the image is underexposed and so the flashgun is recommended to the Host. It is at the discretion of Host to use it or not for the following still grab.
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x1b02	**fFlashGrabComplete**	
	Default value	<0> FALSE
	Purpose	This flag indicates that the FlashGun Image has been grabbed.
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE

Scythe filter controls

Table 29. Scythe filter controls

Index	ScytheFilterControls(1)	
0x1d80	**fDisableFilter**	
	Default value	<0> FALSE
	Purpose	Disable Scythe Defect Correction
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE

1. Can be controlled in all stable state

Jack filter controls

Table 30. Jack filter controls

Index	JackFilterControls(1)	
0x1e00	**fDisableFilter**	
	Default value	<0> FALSE
	Purpose	Disable Jack Defect Correction
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE

1. Can be controlled in all stable state

Demosaic control

Table 31. Demosaic control

Index	DemosaicControl[1]	
0x1e80	**bAntiAliasFilterSuppress**	
	Default value	0x08
	Purpose	Anti alias filter suppress
	Type	BYTE

1. Can be controlled in all stable state

Colour matrix dampers

Table 32. Colour matrix dampers

Index	ColourMatrixDamper[1]	
0x1f00	**fDisable**	
	Default value	<0> FALSE
	Purpose	set to disable colour matrix damper and therefore ensure that all the Colour matrix coefficients remain constant under all conditions.
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x1f03 (MSByte) 0x1f04 (LSByte)	**fpLowThreshold**	
	Default value	0x67d1 (2000896)
	Purpose	Low Threshold for exposure for calculating the damper slope
	Type	FLOAT
0x1f07 (MSByte) 0x1f08 (LSByte)	**fpHighThreshold**	
	Default value	0x6862 (2498560)
	Purpose	High Threshold for exposure for calculating the damper slope
	Type	FLOAT
0x1f0b (MSByte) 0x1f0c (LSByte)	**fpMinimumOutput**	
	Default value	0x3acd (0.350098)
	Purpose	Minimum possible damper output for the ColourMatrix
	Type	FLOAT

1. Can be controlled in all stable state

Peaking control

Table 33. Peaking control

Index	Peaking control[1]	
0x2000	**bUserPeakGain**	
	Default value	0x0e
	Purpose	controls peaking gain / sharpness applied to the image
	Type	BYTE
0x2002	**fDisableGainDamping**	
	Default value	<0> FALSE
	Purpose	set to disable damping and therefore ensure that the peaking gain applied remains constant under all conditions
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x2005 (MSByte) 0x2006 (LSByte)	**fpDamperLowThreshold_Gain**	
	Default value	0x62ac (350208)
	Purpose	Low Threshold for exposure for calculating the damper slope - for gain
	Type	FLOAT
0x2009 (MSByte) 0x200a (LSByte)	**fpDamperHighThreshold_Gain**	
	Default value	0x65d1 (10004488)
	Purpose	High Threshold for exposure for calculating the damper slope - for gain
	Type	FLOAT
0x200d (MSByte) 0x200e (LSByte)	**fpMinimumDamperOutput_Gain**	
	Default value	0x3d33 (0.799805)
	Purpose	Minimum possible damper output for the gain.
	Type	FLOAT
0x2010	**bUserPeakLoThresh**	
	Default value	0x1e
	Purpose	Adjust degree of coring. range: 0 - 63
	Type	BYTE
0x2012	**fDisableCoringDamping**	
	Default value	<0> FALSE
	Purpose	set to ensure that bUserPeakLoThresh is applied to gain block
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE

Table 33. Peaking control

Index	Peaking control[1]	
0x2014	**bUserPeakHiThresh**	
	Default value	0x30
	Purpose	adjust maximum gain that can be applied. range: 0 - 63
	Type	BYTE
0x2017 (MSByte) 0x2018 (LSByte)	**fpDamperLowThreshold_Coring**	
	Default value	0x624a (300032)
	Purpose	Low Threshold for exposure for calculating the damper slope - for coring
	Type	FLOAT
0x201b (MSByte) 0x201c (LSByte)	**fpDamperHighThreshold_Coring**	
	Default value	0x656f (900096)
	Purpose	High Threshold for exposure for calculating the damper slope - for coring
	Type	FLOAT
0x201f (MSByte) 0x2020 (LSByte)	**fpMinimumDamperOutput_Coring**	
	Default value	0x3a00 (0.2500)
	Purpose	Minimum possible damper output for the Coring.
	Type	FLOAT

1. Can be controlled in all stable states

Pipe 0 RGB to YUV matrix manual control

Table 34. Pipe0 RGB to YUV matrix manual control

Index	Pipe0RGB to YUV matrix [1]	
0x2180	**fRgbToYuvManuCtrl**	
	Default value	<0> FALSE
	Purpose	Enables manual RGB to YUV matrix for PipeSetupBank0
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x2183 (MSByte) 0x2184(LSByte)	**w0_0**	
	Default value	0x00
	Purpose	Row 0 Column 0 of YUV matrix
	Type	UINT_16
0x2187 (MSByte) 0x2188 (LSByte)	**w0_1**	
	Default value	0x00
	Purpose	Row 0 Column 1 of YUV matrix
	Type	UINT_16
0x218c (MSByte) 0x218d (LSByte)	**w0_2**	
	Default value	0x00
	Purpose	Row 0 Column 2 of YUV matrix
	Type	UINT_16
0x2190 (MSByte) 0x218f (LSByte)	**w1_0**	
	Default value	0x00
	Purpose	Row 1 Column 0 of YUV matrix
	Type	UINT_16
0x2193 (MSByte) 0x2194 (LSByte)	**w1_1**	
	Default value	0x00
	Purpose	Row 1 Column 1 of YUV matrix
	Type	UINT_16
0x2197 (MSByte) 0x2198 (LSByte)	**w1_2**	
	Default value	0x00
	Purpose	Row 1 Column 2 of YUV matrix
	Type	UINT_16

Table 34. Pipe0 RGB to YUV matrix manual control

Index	Pipe0RGB to YUV matrix [1]	
0x219b (MSByte) 0x219c (LSByte)	**w2_0**	
	Default value	0x00
	Purpose	Row 2 Column 0 of YUV matrix
	Type	UINT_16
0x21a0 (MSByte) 0x219f (LSByte)	**w2_1**	
	Default value	0x00
	Purpose	Row 2 Column 1 of YUV matrix
	Type	UINT_16
0x21a3 (MSByte) 0x21a4 (LSByte)	**w2_2**	
	Default value	0x00
	Purpose	Row 2 Column 2 of YUV matrix
	Type	UINT_16
0x21a7 (MSByte) 0x21a8 (LSByte)	**YinY**	
	Default value	0x00
	Purpose	Y in Y
	Type	UINT_16
0x21ab (MSByte) 0x21ac (LSByte)	**YinCb**	
	Default value	0x00
	Purpose	Y in Cb
	Type	UINT_16
0x21b0 (MSByte) 0x21af (LSByte)	**YinCr**	
	Default value	0x00
	Purpose	Y in Cr
	Type	UINT_16

1. Can be controlled in all stable states

Pipe 1 RGB to YUV matrix manual control

Table 35. Pipe1 RGB To YUV matrix manual control

Index	Pipe1RgbToYuv(1)	
0x2200	**fRgbToYuvManuCtrl**	
	Default value	<0> FALSE
	Purpose	Enables manual RGB to YUV matrix for PipeSetupBank1
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x2203 (MSByte) 0x2204(LSByte)	**w0_0**	
	Default value	0x00
	Purpose	Row 0 Column 0 of YUV matrix
	Type	UINT_16
0x2207 (MSByte) 0x2208 (LSByte)	**w0_1**	
	Default value	0x00
	Purpose	Row 0 Column 1 of YUV matrix
	Type	UINT_16
0x220c (MSByte) 0x220d (LSByte)	**w0_2**	
	Default value	0x00
	Purpose	Row 0 Column 2 of YUV matrix
	Type	UINT_16
0x2210 (MSByte) 0x220f (LSByte)	**w1_0**	
	Default value	0x00
	Purpose	Row 1 Column 0 of YUV matrix
	Type	UINT_16
0x2213 (MSByte) 0x2214 (LSByte)	**w1_1**	
	Default value	0x00
	Purpose	Row 1 Column 1 of YUV matrix
	Type	UINT_16
0x2217 (MSByte) 0x2218 (LSByte)	**w1_2**	
	Default value	0x00
	Purpose	Row 1 Column 2 of YUV matrix
	Type	UINT_16

Table 35. Pipe1 RGB To YUV matrix manual control

Index	Pipe1RgbToYuv[1]	
0x221b (MSByte) 0x221c (LSByte)	**w2_0**	
	Default value	0x00
	Purpose	Row 2 Column 0 of YUV matrix
	Type	UINT_16
0x2220 (MSByte) 0x221f (LSByte)	**w2_1**	
	Default value	0x00
	Purpose	Row 2 Column 1 of YUV matrix
	Type	UINT_16
0x2223 (MSByte) 0x2224 (LSByte)	**w2_2**	
	Default value	0x00
	Purpose	Row 2 Column 2 of YUV matrix
	Type	UINT_16
0x2227 (MSByte) 0x2228 (LSByte)	**YinY**	
	Default value	0x00
	Purpose	Y in Y
	Type	UINT_16
0x222b (MSByte) 0x222c (LSByte)	**YinCb**	
	Default value	0x00
	Purpose	Y in Cb
	Type	UINT_16
0x2220 (MSByte) 0x222f (LSByte)	**YinCr**	
	Default value	0x00
	Purpose	Y in Cr
	Type	UINT_16

1. Can be controlled in all stable states

Pipe 0 gamma manual control

Table 36. Pipe 0 gamma manual control

Index	Pipe0 GammaManuControl[1]	
0x2280	**fGammaManuCtrl**	
	Default value	<0> FALSE
	Purpose	Enables manual Gamma Setup for PipeSetupBank0
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x2282	**bRPeakGamma**	
	Default value	0x00
	Purpose	Peaked Red channel gamma value
	Type	BYTE
0x2284	**bGPeakGamma**	
	Default value	0x00
	Purpose	Peaked Green channel gamma value
	Type	BYTE
0x2286	**bBPeakGamma**	
	Default value	0x00
	Purpose	Peaked Blue channel gamma value
	Type	BYTE
0x2288	**bRUnPeakGamma**	
	Default value	0x00
	Purpose	Unpeaked Red channel gamma value
	Type	BYTE
0x228a	**bGUnPeakGamma**	
	Default value	0x00
	Purpose	Unpeaked Green channel gamma value
	Type	BYTE
0x228c	**bBUnPeakGamma**	
	Default value	0x00
	Purpose	Unpeaked Blue channel gamma value
	Type	BYTE

1. Can be controlled in all stable states

Pipe 1 Gamma manual control

Table 37. Pipe 1 Gamma manual control

Index	Pipe1GammaManuControl[1]	
0x2300	**fGammaManuCtrl**	
	Default value	<0> FALSE
	Purpose	Enables manual Gamma Setup for PipeSetupBank1
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x2302	**bRPeakGamma**	
	Default value	0x00
	Purpose	Peaked Red channel gamma value
	Type	BYTE
0x2304	**bGPeakGamma**	
	Default value	0x00
	Purpose	Peaked Green channel gamma value
	Type	BYTE
0x2306	**bBPeakGamma**	
	Default value	0x00
	Purpose	Peaked Blue channel gamma value
	Type	BYTE
0x2308	**bRUnPeakGamma**	
	Default value	0x00
	Purpose	Unpeaked Red channel gamma value
	Type	BYTE
0x230a	**bGUnPeakGamma**	
	Default value	0x00
	Purpose	Unpeaked Green channel gamma value
	Type	BYTE
0x230c	**bBUnPeakGamma**	
	Default value	0x00
	Purpose	Unpeaked Blue channel gamma value
	Type	BYTE

1. Can be controlled in all stable states

Fade to black

Table 38. Fade to black

Index	FadeToBlack[1]	
0x2480	**fDisable**	
	Default value	<0> FALSE
	Purpose	Flag_e
	Type	<0> FALSE <1> TRUE
0x2483 (MSByte) 0x2484(LSByte)	**fpBlackValue**	
	Default value	0x0000 (0.000)
	Purpose	Black value
	Type	FLOAT
0x2487 (MSByte) 0x2488 (LSByte)	**fpDamperLowThreshold**	
	Default value	0x6d56 (6995968)
	Purpose	Low Threshold for exposure for calculating the damper slope
	Type	FLOAT
0x248b (MSByte) 0x248c (LSByte)	**fpDamperHighThreshold**	
	Default value	0x6cdc (11993088)
	Purpose	High Threshold for exposure for calculating the damper slope
	Type	FLOAT
0x248f (MSByte) 0x2490 (LSByte)	**fpDamperOutput**	
	Default value	0x0 (0.0000)
	Purpose	Minimum possible damper output.
	Type	FLOAT

1. Can be controlled in all stable states

Output formatter control

Table 39. Output formatter control

Index	OutputFormatterControl[1]	
0x2580	**bCodeCheckEn**	
	Default value	0x07
	Type	BYTE
0x2582	**bBlankFormat**	
	Default value	0x00
	Type	BYTE
0x2584	**bSyncCodeSetup**	
	Default value	0x01
	Type	CODED
	flag bits	[0] SyncCodeSetup_ins_code_en - set for embedded sync codes. [1] SyncCodeSetup_frame_mode - 0 for ITU. 1 for mode2 [2] SyncCodeSetup_field_bit [3] SyncCodeSetup_field_tag [4] SyncCodeSetup_field_load
0x2586	**bHSyncSetup**	
	Default value	0x0b
	Type	CODED
	flag bits	[0] HSyncSetup_sync_en [1] HSyncSetup_sync_pol [2] HSyncSetup_only_activelines [3] HSyncSetup_track_henv
0x2588	**bVSyncSetup**	
	Default value	0x07
	Type	CODED
	flag bits	[0] VSyncSetup_sync_en [1] VSyncSetup_pol [2] VSyncSetup_2_sel

Table 39. Output formatter control

Index	OutputFormatterControl[1]	
0x258a	**bPClkSetup**	
	Default value	0x05
	Type	CODED
	flag bits	[0] PClkSetup_prog_lo [1] PClkSetup_prog_hi [2] PClkSetup_sync_en [3] PClkSetup_hsync_en_n [4] PClkSetup_hsync_en_n_track_internal [5] PClkSetup_vsync_n [6] PClkSetup_vsync_n_track_internal [7] PClkSetup_freer
0x258c	**fPclkEn**	
	Default value	<1> TRUE
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x258e	**bOpfSpSetup**	
	Default value	0x00
	type	BYTE
0x2590	**bBlankData_MSB**	
	Default value	0x10
	Type	CODED
	Possible values	<16> BlankingMSB_Default
0x2592	**bBlankData_LSB**	
	Default value	0x80
	Type	CODED
	Possible values	<128> BlankingLSB_Default
0x2594	**bRgbSetup**	
	Default value	0x00
	Type	CODED
	flag bits	[0] RgbSetup_rgb444_itu_zp [1] RgbSetup_rb_swap [2] RgbSetup_bit_reverse [3] RgbSetup_softreset

Table 39. Output formatter control

Index	OutputFormatterControl[1]	
0x2596	**bYuvSetup**	
	Default value	0x00
	Type	CODED
	flag bits	[0] YuvSetup_u_first [1] YuvSetup_y_first
0x2598	**bVsyncRisingCoarseH**	
	Default value	0x00
	Type	BYTE
0x259a	**bVsyncRisingCoarseL**	
	Default value	0x00
	Type	BYTE
0x259c	**bVsyncRisingFineH**	
	Default value	0x00
	Type	BYTE
0x259e	**bVsyncRisingFineL**	
	Default value	0x01
	Type	BYTE
0x25a0	**bVsyncFallingCoarseH**	
	Default value	0x01
	Type	BYTE
0x25a2	**bVsyncFallingCoarseL**	
	Default value	0xf2
	Type	BYTE
0x25a4	**bVsyncFallingFineH**	
	Default value	0x00
	Type	BYTE
0x25a6	**bVsyncFallingFineL**	
	Default value	0x01
	Type	BYTE
0x25a8	**bHsyncRisingH**	
	Default value	0x00
	Type	BYTE

Table 39. Output formatter control

Index	OutputFormatterControl[1]	
0x25aa	**bHsyncRisingL**	
	Default value	0x03
	Type	BYTE
0x25ac	**bHsyncFallingH**	
	Default value	0x00
	Type	BYTE
0x25ae	**bHsyncFallingL**	
	Default value	0x07
	type	BYTE
0x25b0	**bOutputInterface**	
	Default value	[0] OutputInterface_ITU
	Type	CODED
	flag bits	[0] OutputInterface_ITU [1] OutputInterface_CCP_DataStrobe [2] OutputInterface_CCP_DataClock
0x25b2	**bCCPExtraData**	
	Default value	0x08
	Type	BYTE

1. Can be controlled in all stable states

NoRA controls

Table 40. NoRA controls

Index	NoRAControls[1]	
0x2600	**fDisable**	
	Default value	<0> NoraCtrl_auto
	Type	Flag_e
	Possible values	<0> NoraCtrl_auto - switches off NoRA for scaled outputs <1> NoraCtrl_ManuDisable - Always off <2> NoraCtrl_ManuEnable - Always on
0x2602	**bUsage**	
	Default value	0x04
	Purpose	
	Type	BYTE
0x2604	**bSplit_Kn**	
	Default value	0x01
	Purpose	
	Type	BYTE
0x2606	**bSplit_NI**	
	Default value	0x01
	Purpose	
	Type	BYTE
0x2608	**bTight_Green**	
	Default value	0x01
	Purpose	
	Type	BYTE
0x260a	**fDisableNoroPromoting**	
	Default value	<0> FALSE
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x260d (MSByte) 0x260e (LSByte)	**fpDamperLowThreshold**	
	Default value	0x6862 (2498560)
	Purpose	Low Threshold for exposure for calculating the damper slope
	Type	FLOAT

Table 40. NoRA controls

Index	NoRAControls[1]	
0x2611 (MSByte) 0x2612 (LSByte)	**fpDamperHighThreshold**	
	Default value	0x6a62 (4997120)
	Purpose	High Threshold for exposure for calculating the damper slope
	Type	FLOAT
0x2615 (MSByte) 0x2616 (LSByte)	**MinimumDamperOutput**	
	Default value	0x3a00 (0.2500)
	Purpose	Minimum possible damper output.
	Type	FLOAT

1. Can be controlled in all stable states

12 Optical specifications

Table 41. Optical specifications(1)

Parameter	Min.	Typ.	Max.	Unit
Optical format		1/3		inch
Effective focal length				mm
Aperture (F number)		3.2		
Horizontal field of view		52		deg.
Depth of field	60		infinity	cm
TV distortion			1	%

1. All measurements made at 23°C ± 2°C

12.1 Average sensitivity

The average sensitivity is a measure of the image sensor response to a given light stimulus. The optical stimulus is a white light source with a color temperature of 3200K, producing uniform illumination at the surface of the sensor package. An IR blocking filter is added to the light source. The analog gain of the sensor is set to x1. The exposure time, Δt, is set as 50% of maximum. The illuminance, I, is adjusted so the average sensor output code, Xlight, is roughly mid-range equivalent to a saturation level of 50%. Once Xlight has been recorded the experiment is repeated with no illumination to give a value Xdark.

The sensitivity is then calculated as $\frac{Xlight - Xdark}{\Delta t \cdot I}$ .The result is expressed in volts per lux-second.

The sensitivity of the VS6624 is given in *Table 42.*

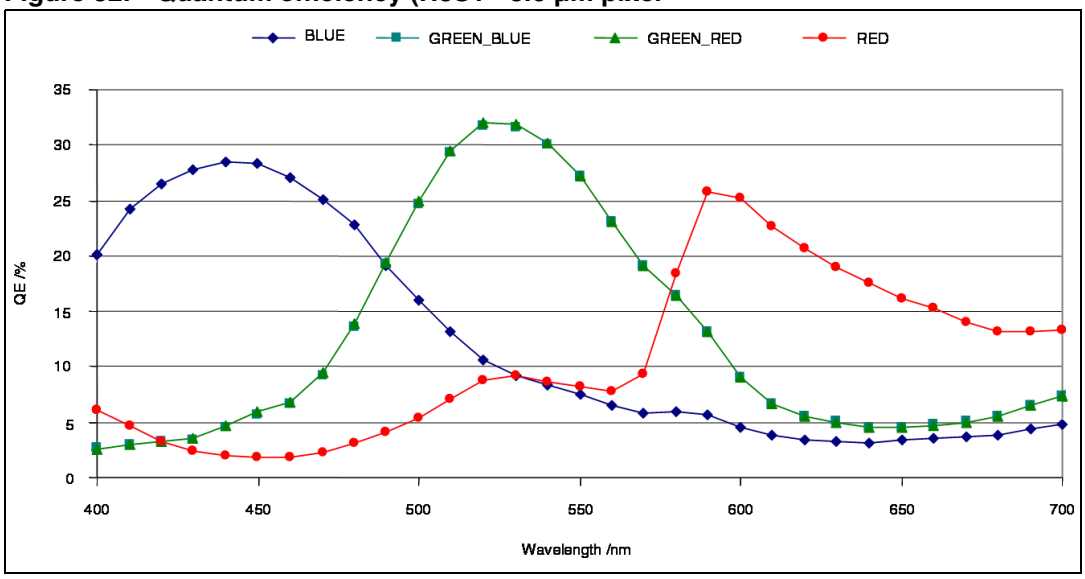
Table 42. VS6624 average sensitivity

Optical parameter	VS6624	Unit
Average sensitivity	0.49	V/lux.s

12.2 Spectral response

The spectral response for the VS6524 sensor is shown in *Figure 32*

Figure 32. Quantum efficiency (H8S1 - 3.0 µm pixel



13 Electrical characteristics

13.1 Absolute maximum ratings

Table 43. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STO}	Storage temperature	-40	85	°C
V_{DD}	Digital power supplies	-0.5	3.3	V
AVDD	Analog power supplies	-0.5	3.3	V

Caution: Stress above those listed under “Absolute Maximum Ratings” can cause permanent damage to the device. This is a stress rating only and functional operations of the device at these or other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

13.2 Operating conditions

Table 44. Supply specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{AF}	Operating temperature, functional (Camera is electrically functional)	-30	25	70	°C
T_{AN}	Operating temperature, nominal (Camera produces acceptable images)	-25	25	55	°C
T_{AO}	Operating temperature, optimal (Camera produces optimal optical performance)	5	25	30	°C
V_{DD}	Digital power supplies operating range (@ module pin(1))	1.7	1.8	2.0	V
		2.4	2.8	3.0	V
AVDD	Analog power supplies operating range (@ module pin(1))	2.4	2.8	3.0	V

1. Module can contain routing resistance up to 5 Ω

13.3 DC electrical characteristics

Note: Over operating conditions unless otherwise specified.

Table 45. DC electrical characteristics

Symbol	Description	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage	VDD 1.7~ 2.0V	-0.3		0.25 V_{DD}	V
		VDD 2.4 ~ 3.0V	-0.3		0.3 V_{DD}	V
V_{IH}	Input high voltage		0.7 V_{DD}		V_{DD} + 0.3	V
V_{OL}	Output low voltage	I_{OL} < 2 mA I_{OL} < 4 mA			0.2 V_{DD} 0.4 V_{DD}	V
V_{OH}	Output high voltage	I_{OH}< 4 mA	0.8 V_{DD}			V
I_{IL}	Input leakage current Input pins I/O pins	0 < V_{IN} < V_{DD}			+/- 10 +/- 1	µA µA
C_{IN}	Input capacitance, SCL	T_A = 25 °C, freq = 1 MHz			6	pF
C_{OUT}	Output capacitance	T_A = 25 °C, freq = 1 MHz			6	pF
$C_{I/O}$	I/O capacitance, SDA	T_A = 25 °C, freq = 1 MHz			8	pF

Table 46. Typical current consumption - Sensor mode VGA 30 fps

Symbol	Description	Test conditions	I_{AVDD}	I_{VDD}		Units
			V_{DD} = 2.8V	V_{DD} = 1.8V	V_{DD} = 2.8V	
I_{PD}	supply current in power down mode	CE=0, CLK = 12 MHz	1.4	0.05	0.07	µA
I_{stanby}	supply current in Standby mode	CE=1, CLK = 12 MHz	0.0014	1.3	8	mA
I_{Stop}	supply current in Stop mode	CE=1, CLK = 12 MHz	0.0014	4.1	4.2	mA
I_{Pause}	supply current in Pause mode	CE=1, CLK = 12 MHz	0.00175	43.8	43.3	mA
I_{run}	supply current in active streaming run mode	CE=1, CLK = 12 MHz streaming VGA @30 fps	11.3	55.1	54.8	mA

Table 47. Typical current consumption - Sensor mode SXGA 15 fps

Symbol	Description	Test conditions	I_{AVDD}	I_{VDD}		Units
			V_{DD} = 2.8V	V_{DD} = 1.8V	V_{DD} = 2.8V	
I_{PD}	supply current in power down mode	CE=0, CLK = 12 MHz	1.4	0.05	0.07	µA
I_{stanby}	supply current in Standby mode	CE=1, CLK = 12 MHz	0.0014	1.3	8	mA
I_{Stop}	supply current in Stop mode	CE=1, CLK = 12 MHz	0.0014	4.1	4	mA
I_{Pause}	supply current in Pause mode	CE=1, CLK = 12 MHz	0.0195	63.4	64.7	mA
I_{run}	supply current in active streaming run mode	CE=1, CLK = 12 MHz streaming VGA @30 fps	11.5	84.5	87	mA

13.4 External clock

The VL6624/VS6624 requires an external clock. This clock is a CMOS digital input. The clock input is fail-safe in power down mode.

Table 48. External clock

CLK	Range			Unit
	Min.	Typ.	Max.	
DC coupled square wave		VDD		V
Clock frequency (normal operation)	6.50	6.50, 8.40, 9.60, 9.72, 12.00, 13.00, 16.80, 19.20, 19.44	54	MHz

13.5 Chip enable

CE is a CMOS digital input. The module is powered down when a logic 0 is applied to CE. See *Power up sequence* for further information.

13.6 I²C slave interface

VL6624/VS6624 contains an I²C-type interface using two signals: a bidirectional serial data line (SDA) and an input-only serial clock line (SCL). See *Host communication - I²C control interface* for detailed description of protocol.

Table 49. Serial interface voltage levels(1)

Symbol	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
V_{HYS}	Hysteresis of Schmitt Trigger Inputs V_{DD} > 2 V V_{DD} < 2V	 N/A N/A	 N/A N/A	 0.05 V_{DD} 0.1 V_{DD}	 - -	 V V
V_{OL1} V_{OL3}	LOW level output voltage (open drain) at 3mA sink current V_{DD} > 2 V V_{DD} < 2V	 0 N/A	 0.4 N/A	 0 0	 0.4 0.2 V_{DD}	 V V
V_{OH}	HIGH level output voltage	N/A	N/A	0.8 V_{DD}		V
t_{OF}	Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance from 10 pF to 400 pF	-	250	20+0.1C_b(2)	250	ns
t_{SP}	Pulse width of spikes which must be suppressed by the input filter	N/A	N/A	0	50	ns

1. Maximum $V_{IH} = V_{DDmax} + 0.5$ V
2. C_b = capacitance of one bus line in pF

Figure 33. Voltage level specification

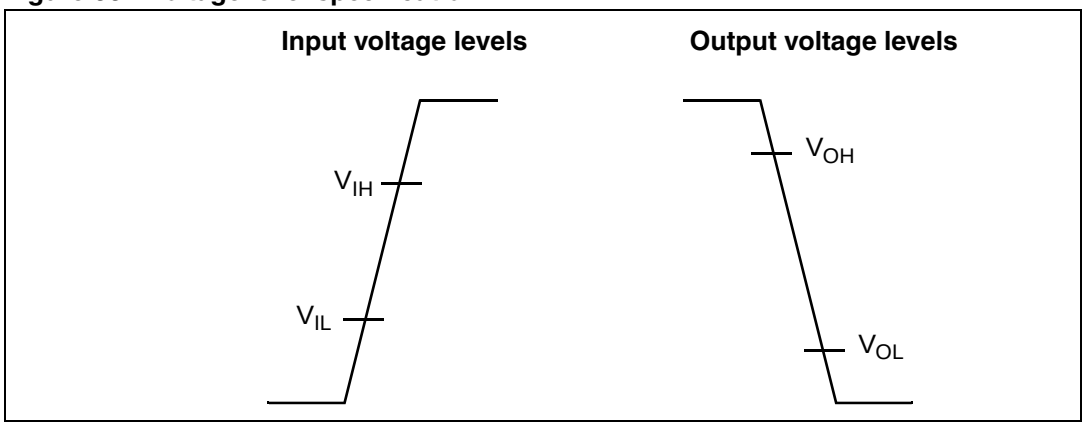


Table 50. Timing specification(1)

Symbol	Parameter	Standard mode		Fast mode		Unit
		Min.	Max.	Min.	Max.	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{HD;STA}$	Hold time for a repeated ***start***	4.0	-	0.6	-	µs
t_{LOW}	LOW period of SCL	4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of SCL	4.0	-	0.6	-	µs
$t_{SU;STA}$	Set-up time for a repeated ***start***	4.7	-	0.6	-	µs
$t_{HD;DAT}$	Data hold time (1)	300	-	300	-	ns
$t_{SU;DAT}$	Data Set-up time (1)	250	-	100	-	ns
t_r	Rise time of SCL, SDA	-	1000	$20+0.1C_b$(2)	300	ns
t_f	Fall time of SCL, SDA	-	300	$20+0.1C_b$(2)	300	ns
$t_{SU;STO}$	Set-up time for a ***stop***	4.0	-	0.6	-	µs
t_{BUF}	Bus free time between a ***stop*** and a ***start***	4.7	-	1.3	-	µs
C_b	Capacitive Load for each bus line	-	400	-	400	pF
V_{nL}	Noise Margin at the LOW level for each connected device (including hysteresis)	0.1 V_{DD}	-	0.1 V_{DD}	-	V
V_{nH}	Noise Margin at the HIGH level for each connected device (including hysteresis)	0.2 V_{DD}	-	0.2 V_{DD}	-	V

1. All values are referred to a V_{IHmin} = 0.9 V_{DD} and V_{ILmax} = 0.1 V_{DD}
2. C_b = capacitance of one bus line in pF

Figure 34. Timing specification

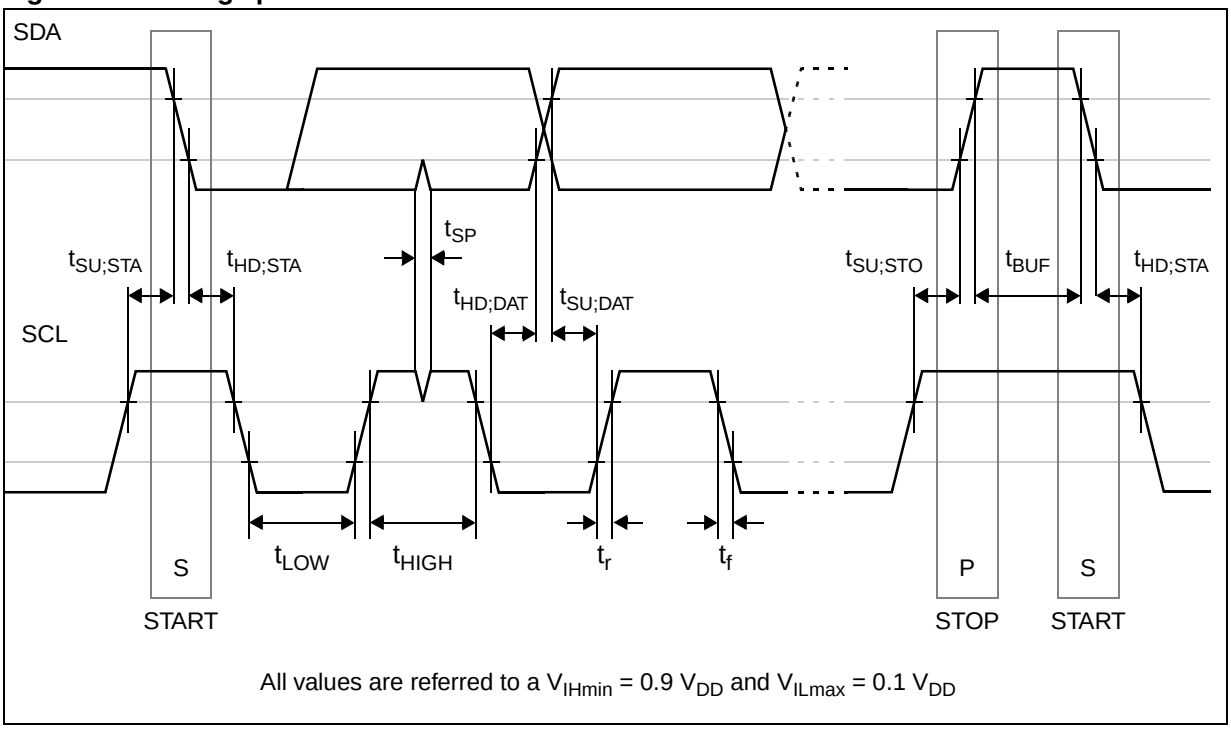
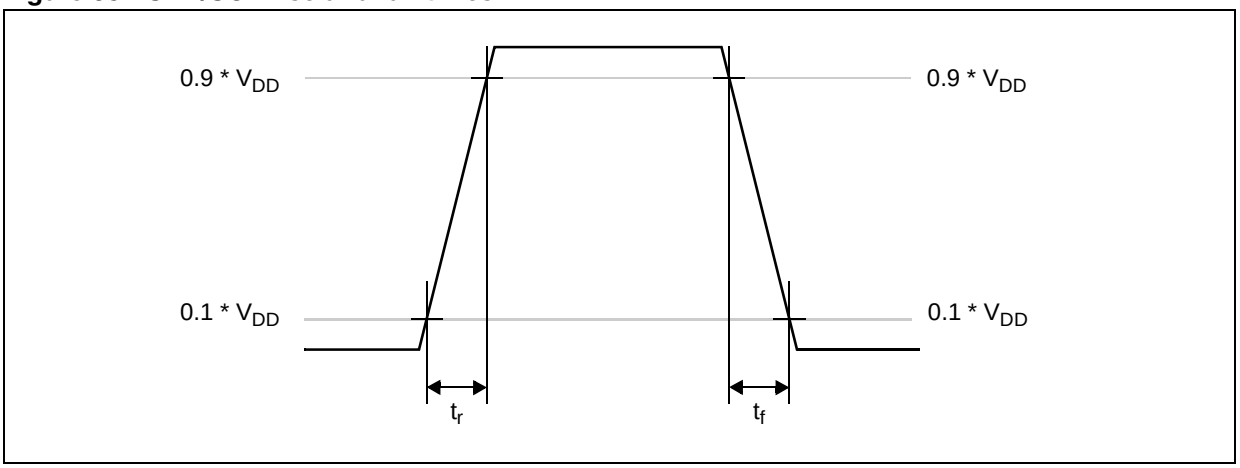


Figure 35. SDA/SCL rise and fall times



13.7 Parallel data interface timing

VL6624/VS6624 contains a parallel data output port (D[7:0]) and associated qualification signals (HSYNC, VSYNC, PCLK and FSO).

This port can be enabled and disabled (tri-stated) to facilitate multiple camera systems or bit-serial output configurations. The port is disabled (high impedance) upon reset.

Figure 36. Parallel data output video timing

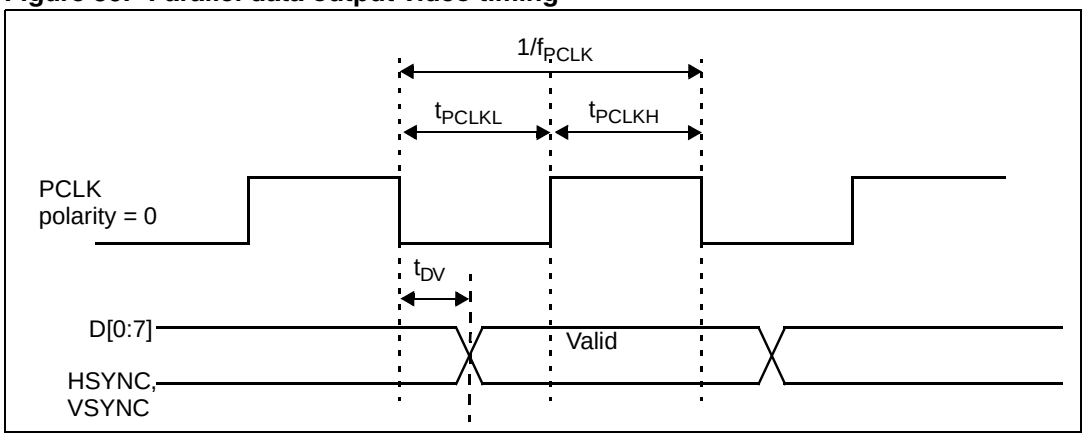


Table 51. Parallel data interface timings

Symbol	Description	Min.	Max.	Unit
f_{PCLK}	PCLK frequency		54	MHz
t_{PCLKL}	PCLK low width	$[1/2*(1/f_{PCLK})] - 3.9$	$[1/2*(1/f_{PCLK})] + 3.9$	ns
t_{PCLKH}	PCLK high width	$[1/2*(1/f_{PCLK})] - 3.9$	$[1/2*(1/f_{PCLK})] + 3.9$	ns
t_{DV}	PCLK to output valid	-5.15	1.62	ns

14 User precaution

As is common with many CMOS imagers the camera should not be pointed at bright static objects for long periods of time as permanent damage to the sensor may occur.

15 Package mechanical data

15.1 SmOP

Figure 37 and *Figure 38* present the package outline socket module VS6624Q0KP.

Figure 39 and *Figure 40* present the package outline FPC module VS6624P0LP.

Figure 37. Package outline socket module VS6624Q0KP

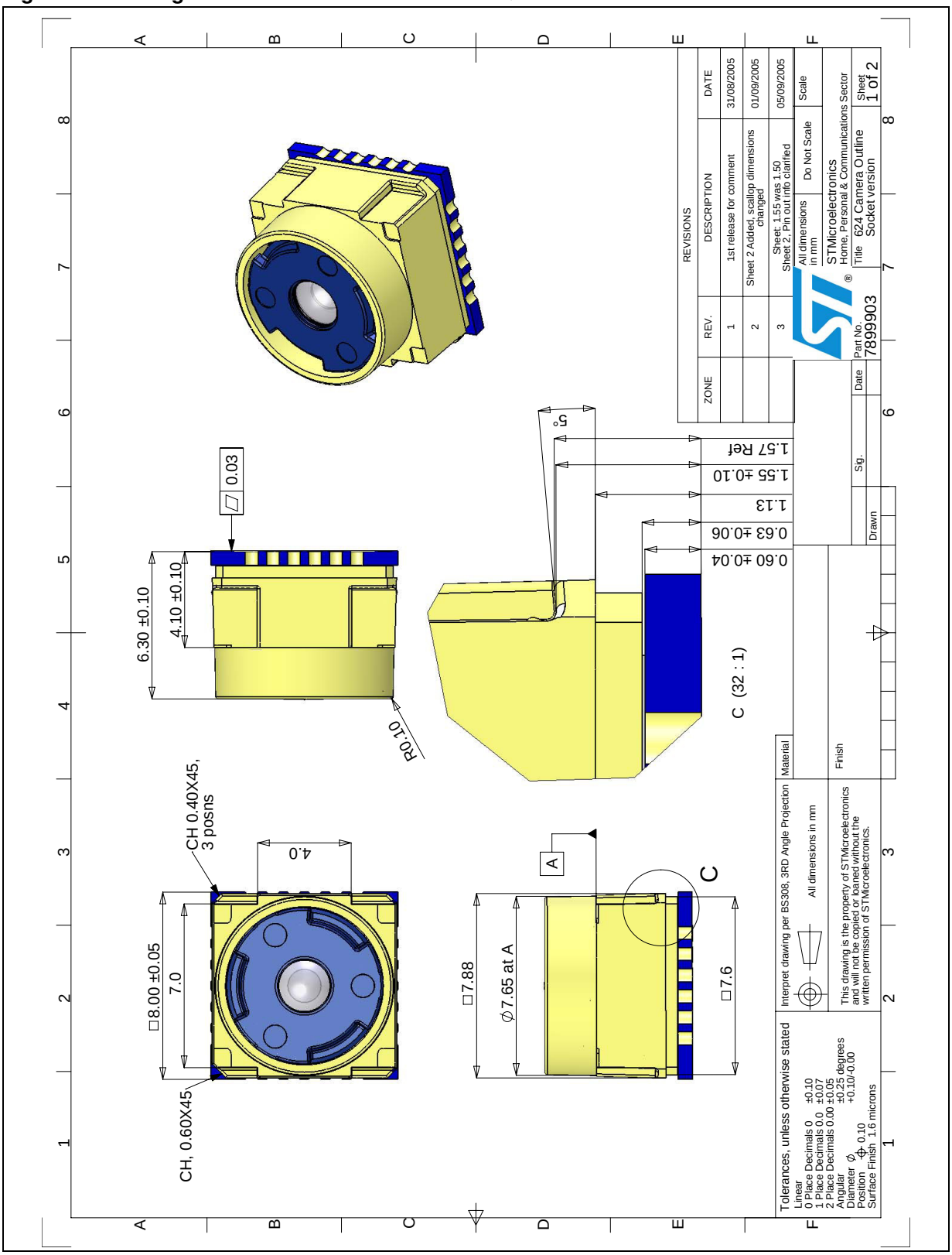


Figure 38. Package outline socket module VS6624Q0KP

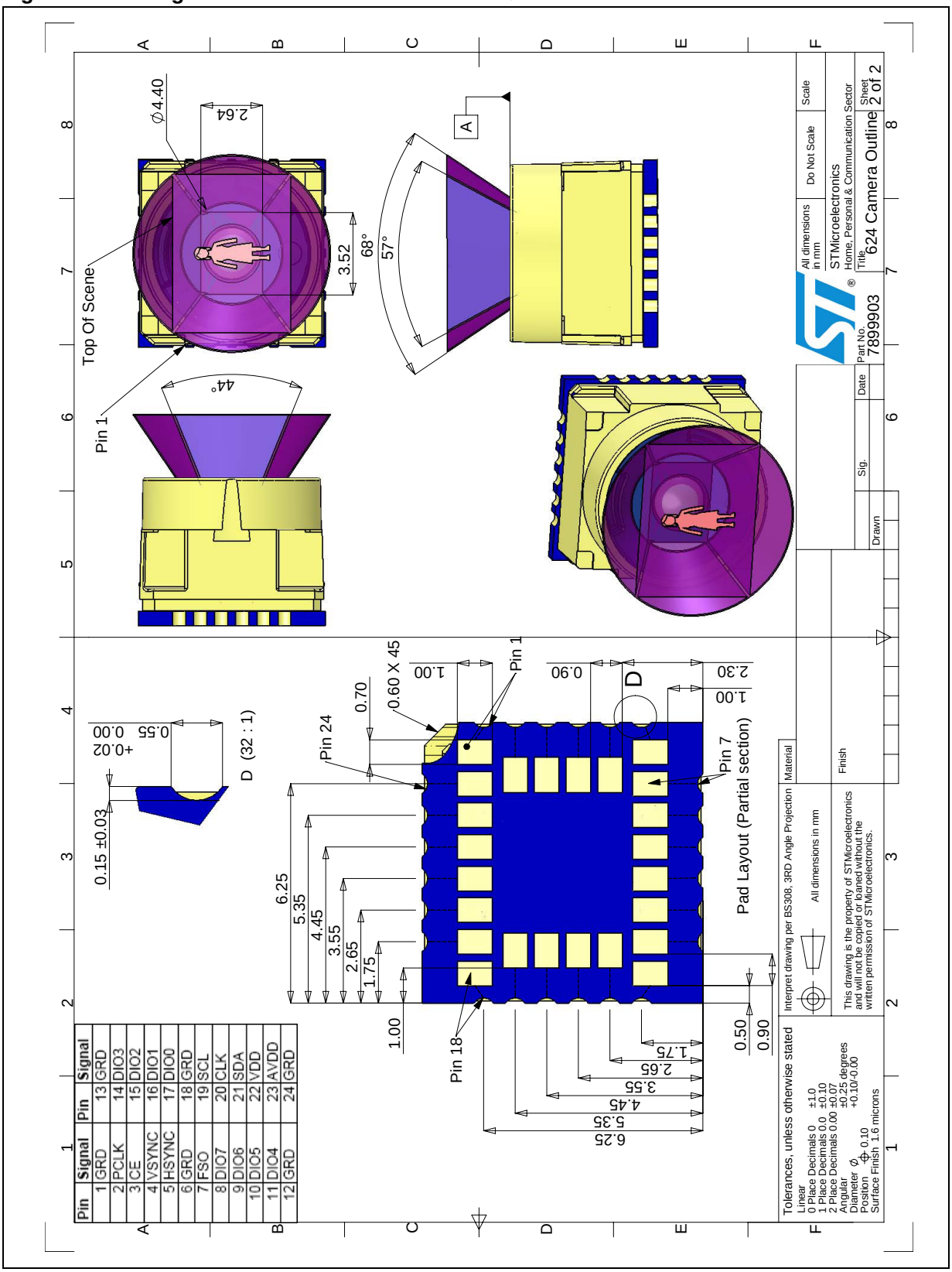


Figure 39. Package outline FPC module VS6624P0LP

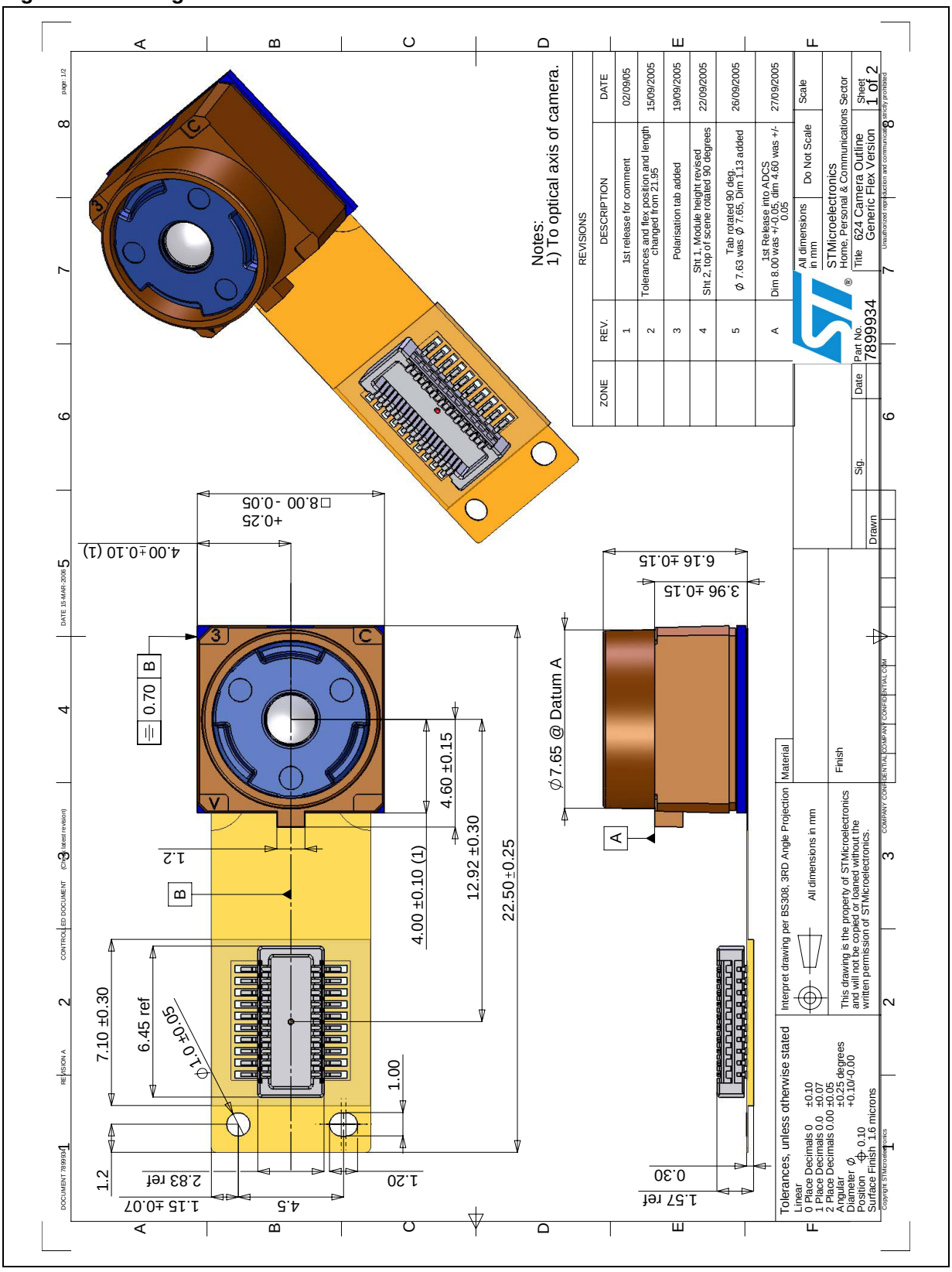
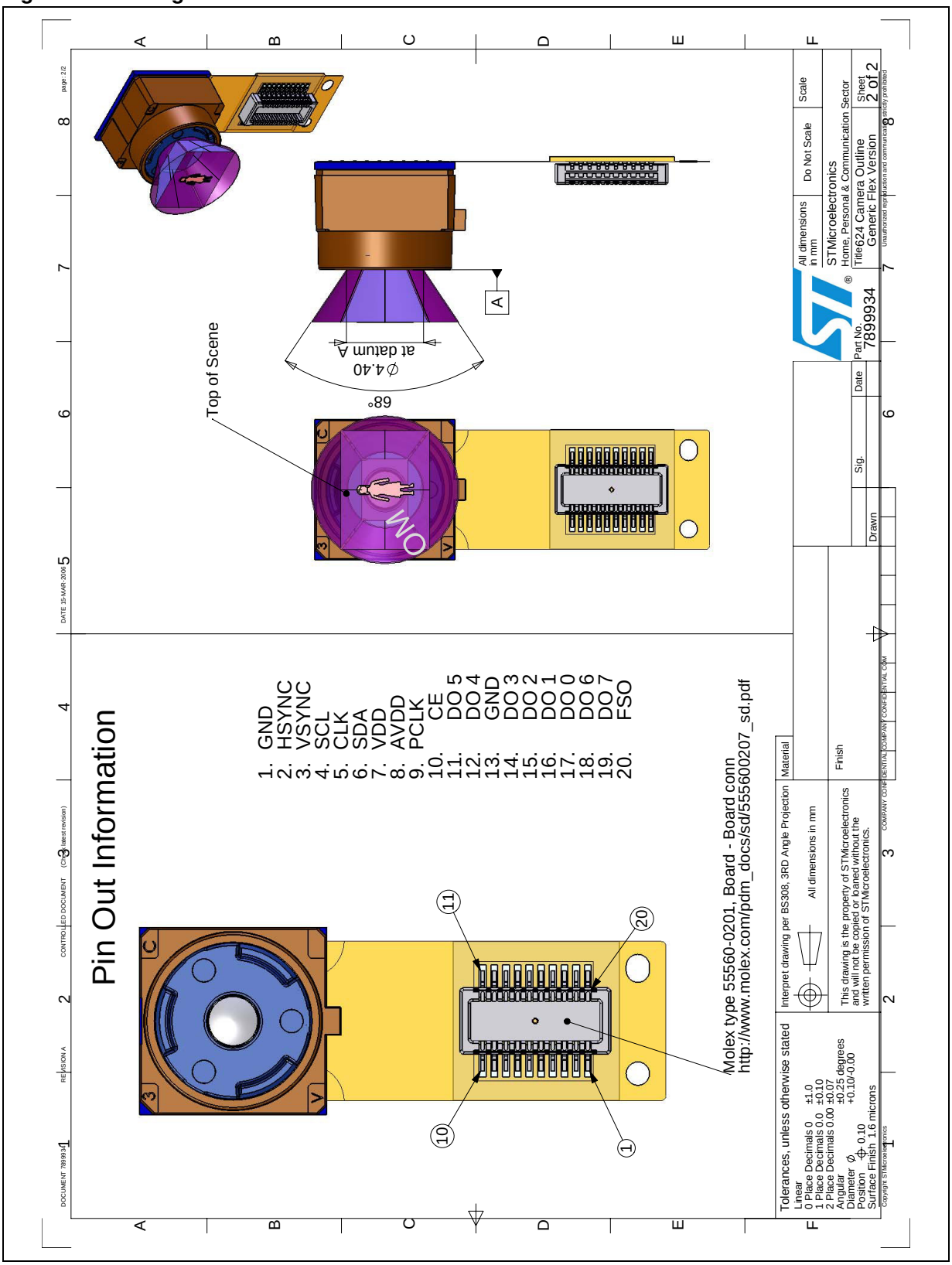


Figure 40. Package outline FPC module VS6624P0LP



15.2 LGA

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 52. LGA package mechanical data

Data book (mm)			
Symbol	**Min.**	**Typ.**	**Max.**
A	1.80	1.90	2.00
A4	0.35	0.4	0.45
A5	0.7	0.8	0.9
B1		2.0	
B2		3.5	
B3		0.55	
b	0.25	0.30	0.35
D	9.90	10.00	10.10
D1	9.60	9.70	9.80
D2		5	
D4		5.4	
e		0.8	
E	9.90	10.00	10.10
E1	9.60	9.70	9.80
E2		5	
E4		4.5	
G	1.0	1.1	1.2
G1		1	
G2	0.3	0.4	0.5
G3	0.8	0.9	1.0
G4		0.8	
H	0.8	0.9	1.0
H1		0.8	
H2	0.3	0.4	0.5
I	3.95	4.05	4.15
J		4.1	
K		0.3	

Table 52. LGA package mechanical data (continued)

Data book (mm)			
Symbol	**Min.**	**Typ.**	**Max.**
PHI	4°	5°	6°
z		1.65	
L	0.7	0.8	0.9
bbb		0.01	
ccc		0.1	
ddd		0.08	
eee		0.08	
nD		9	
nE		9	
n		36	

Figure 41. VL6524QOMH outline drawing

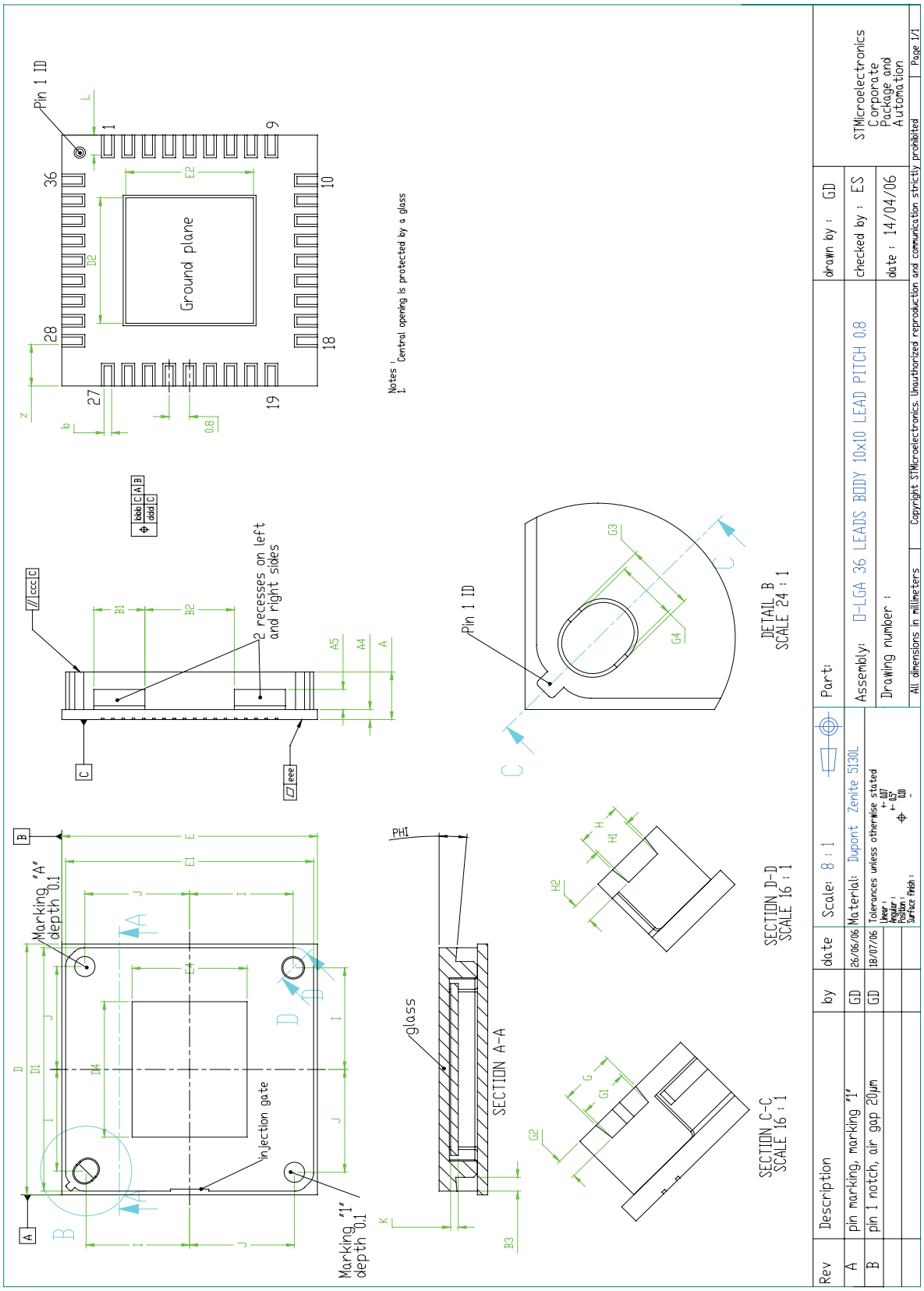


Table 53. VL6524 pin assignment

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	AVDD	10	GND	19	DIO7	28	GND
2	GND	11	NC	20	DIO6	29	PCLK
3	SDA	12	NC	21	DIO5	30	VDD
4	SCL	13	NC	22	DIO4	31	NC
5	CE	14	NC	23	VDD	32	NC
6	VDD	15	AVDD	24	DIO3	33	NC
7	CLK	16	HSYNC	25	DIO2	34	NC
8	GND	17	VSYNC	26	DIO1	35	NC
9	FSO	18	GND	27	DIO0	36	GND

16 Ordering information

Table 54. Order codes

Part number	Package
VS6624P0LP	SMOP2 VGA 8x8, flex
VS6624Q0KP	SMOP2 VGA 8x8, socket
VL6624QOMH	LGA 10x10x1.90 mm

17 Revision history

Table 55. Document revision history

Date	Revision	Changes
1-Feb-2006	1	Initial release.
14-Apr-2006	2	Updated *Table 51: Parallel data interface timings*. Updated module outline drawing s *Figure 39* and *Figure 40*
15-Jun-2006	3	Updated V_{IL} values in *Figure 45: DC electrical characteristics*. Updated *Figure 33: Voltage level specification*. Added *Average sensitivity* and *Spectral response* sections in *Section 12: Optical specifications*. Updated the applications and the document title on cover page. Moved order codes to *Chapter 16: Ordering information*.
06-Nov-2006	4	Added VL6624 reference and LGA outline drawings and dimensions.
06-Dec-2006	5	Corrected the part number for LGA plug-in in *Table 54*.
08-Jan-2007	6	Corrected the optical format in *Table 41: Optical specifications*
02-Jul-2007	7	Updated the list of applications on the cover page. Updated the *Table 16: Ordering information*. Added *Chapter 14: User precaution*.

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