FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-28203-4E

ASSP Image Processing

BIPOLAR

A/D Converter

(1-channel, 8-bit low-power model with built-in clamp circuit)

MB40568

■ DESCRIPTION

The MB40568 is an all-parallel (flash type) A/D converter for 8-bit video applications, and uses high-speed bipolar process technology for low-power consumption and high-speed conversion.

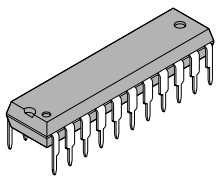
This A/D converter is capable of converting analog signals into digital signals at a rate of DC to 20 MSPS (megasamples per second). Additional circuitry including a clamp circuit and reference voltage generator circuits are build in, to make the MB40568 ideally suited for video signal processing.

■ FEATURES

- Resolution: 8 bits
- Linearity error: ±0.15 % typ.
- Maximum conversion rate: 20 MSPS min.
- Analog input voltage: 0 to 3 V in 2 V_{P-P} (clamp circuit)
  3 to 5 V (without clamp circuit)
- Digital input/output level: TTL Levels
- Power supply voltage: +5 V single power supply
- Power dissipation: 200 mW typ.

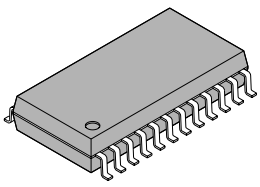
■ PACKAGES

22-pin Plastic SK-DIP



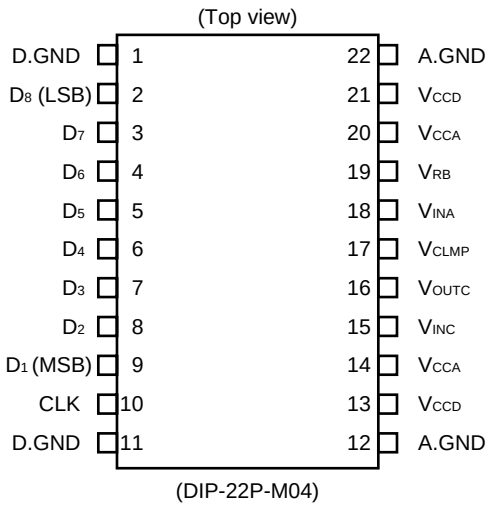
(DIP-22P-M04)

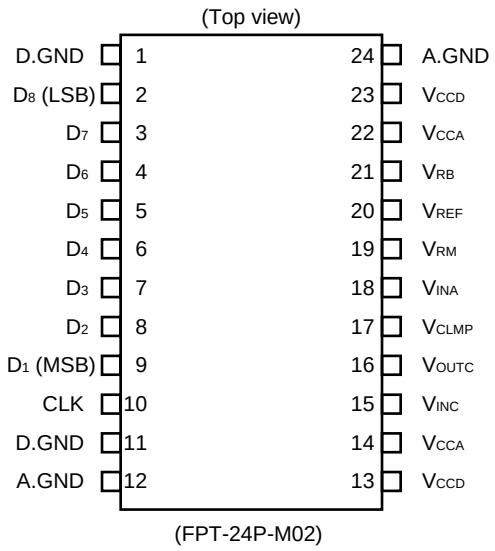
24-pin Plastic SOP



(FPT-24P-M02)

■ PIN ASSIGNMENTS





■ PIN DESCRIPTIONS

Pin no.		Symbol	Function
DIP	SOP		
1, 11	1, 11	D.GND	Ground pin Should be connected to the analog system ground.
2 to 9	2 to 9	D_8 to D_1	Digital signal output pin
10	10	CLK	Clock input pin
12, 22	12, 24	A.GND	Ground pin Should be connected to the analog system ground.
13, 21	13, 23	V_{CCD}	Power supply voltage input pin Also functions as V_{CCA} power supply, and should be in the same voltage level as V_{CCA} pin.
14, 20	14, 22	V_{CCA}	Power supply voltage input pin Also functions as V_{CCD} power supply, and should be in the same voltage level as V_{CCD} pin.
15	15	V_{INC}	Clamp circuit input pin The clamp circuit is a diode-clamp type sync chip clamp circuit. Should be shorted to ground if the clamp circuit is not used.
16	16	V_{OUTC}	Clamp circuit output pin A capacitor of at least 1 μF should be connected between this pin and the V_{CLMP} pin. Should be left open if the clamp circuit is not used.

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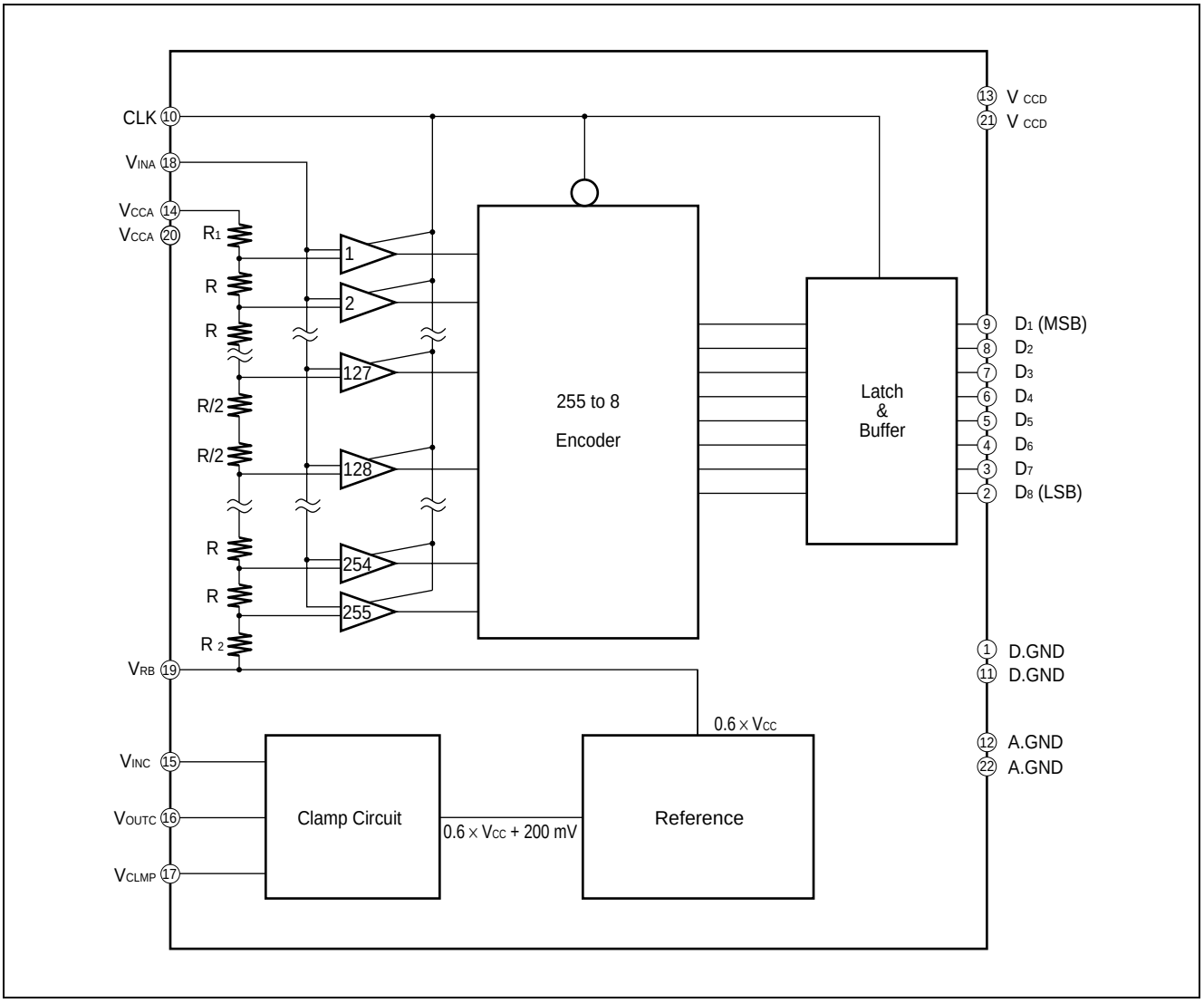
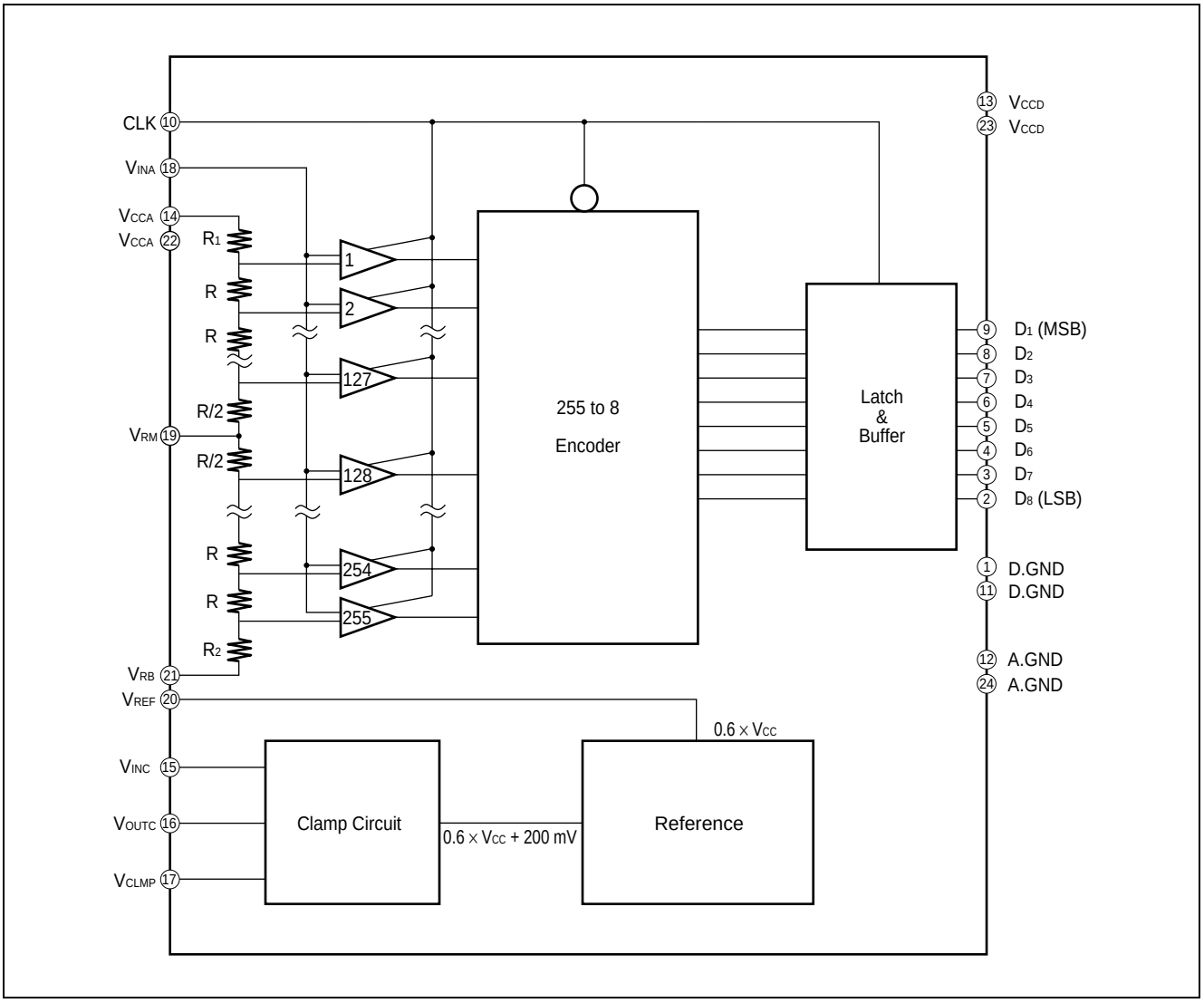
Pin no.		Symbol	Function
DIP	SOP		
17	17	V_{CLMP}	Clamp voltage output pin A capacitor of at least 1 µF should be connected between this pin and the V_{OUTC} pin. Should be left open if the clamp circuit is not used.
18	18	V_{INA}	Analog signal input pin
19	—	V_{RB}	Analog reference voltage pin In the DIP model, this pin is internally connected to the reference circuit. Always be sure that a capacitor is connected immediately next to the IC, between this pin and the ground. The capacitor must be at least 1 µF with excellent frequency characteristics.
—	19	V_{RM}	Reference voltage monitor pin Set to the midpoint of resistance between V_{CCA} and V_{RB}. Should be left open in normal use.
—	20	V_{REF}	Reference voltage output pin Should be left open when no reference voltage source is used.
—	21	V_{RB}	Analog reference voltage input pin When an internal reference voltage source is used, this pin should be shorted to the V_{REF} pin. In this case, always be sure that a capacitor is connected immediately next to the IC, between this pin and the ground. The capacitor must be at least 1 µF with excellent frequency characteristics. When an external reference voltage source is used, this pin will carry a current of up to 8.5 mA, therefore it is necessary to use a voltage source with sufficient sync capacity. A capacitor connection should also be used similar to that used with internal reference voltage sources.

■ BLOCK DIAGRAMS

1. SK-DIP



2. SOP


CLK 10
VINA 18
VCCA 14
VCCA 22
VRM 19
VRB 21
VREF 20
VINC 15
VOUTC 16
VCLMP 17
R1
R
R
R/2
R/2
R
R
R2
1
2
127
128
254
255
255 to 8
Encoder
Latch
&
Buffer
13 VCCD
23 VCCD
9 D1 (MSB)
8 D2
7 D3
6 D4
5 D5
4 D6
3 D7
2 D8 (LSB)
1 D.GND
11 D.GND
12 A.GND
24 A.GND
0.6 × VCC
Clamp Circuit
0.6 × VCC + 200 mV
Reference

■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{CCA}, V_{CCD}	–0.5 to +7.0	V
Digital input voltage	V_{IND}	–0.5 to +7.0	V
Analog input voltage	V_{INA}	–0.5 to V_{CC} + 0.5	V
Analog reference voltage*	V_{RB}	–0.5 to V_{CC} + 0.5	V
Clamp circuit input voltage	V_{INC}	–0.5 to V_{CC} + 0.5	V
Storage temperature	Tstg	–55 to +125	°C

* : Package : SOP
V_{CCA} = 2.0 ± 0.1 V, V_{RB} = 2.0 ± 0.1 V

WARNING: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power supply voltage*1	V_{CCA}, V_{CCD}	4.75	5.00	5.25	V
Analog input voltage	V_{INA}	V_{RB}	—	V_{CCA}	V
Analog reference voltage*2	V_{RB}	2.75	3	3.25	V
Clamp circuit input voltage*3	V_{INC}	0	—	3	V
Clamp capacitance	C_{CLMP}	1	—	—	µF
Digital high-level output voltage	I_{OH}	–400	—	—	µA
Digital low-level output voltage	I_{OL}	—	—	1.6	mA
Clock pulse width at high-level	t_{W^+}	22.5	—	—	ns
Clock pulse width at low-level	t_{W^-}	22.5	—	—	ns
Operating temperature	Top	0	—	70	°C

*1: V_{CCA} and V_{CCD} must be used in the same voltage level.
*2: Package : SOP
V_{CCA} = 2.0 ± 0.1 V, V_{RB} = 2.0 ± 0.1 V
*3: V_{INC} must have an amplitude of V_{CCA} – V_{CLMP}.

■ ELECTRIC CHARACTERISTICS

1. DC Characteristics

(1) Analog DC Characteristics

(V_{CCA} = V_{CCD} = 4.75 to 5.25 V, Ta = 0°C to +70°C)

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Resolution	—	—	—	8	bits	
Linearity error*	LE	—	±0.15	±0.3	%	DC Accuracy
Equivalent analog input resistance	R_{INA}	300	—	—	kΩ	$R_{INA} = \frac{V_{CCA} - V_{RB}}{I_{IHA} - I_{ILA}}$
Analog input capacitance	C_{INA}	—	40	50	pF	f_{INA} = 1MHz
Analog high-level input current	I_{IHA}	—	—	45	µA	$V_{INA} = V_{CCA}$
Analog low-level input current	I_{ILA}	—	—	40	µA	$V_{INA} = V_{RB}$
Clamp circuit input current	I_{INC}	–600	–200	—	µA	V_{INC} = 0 V
Reference voltage	V_{RB}	$0.6 \times V_{CC}$ –0.1	$0.6 \times V_{CC}$	$0.6 \times V_{CC}$ +0.1	V	SK-DIP22P package
	V_{REF}					SOP24P package Short between V_{REF} and V_{RB}
Clamp voltage	V_{CLMP}	—	V_{RB} + 0.2	—	V	
Reference current	I_{RB}	–8.5	–5.5	–3.0	mA	SOP24P package

* : V_{CCA} = V_{CCD} = 5.00 V, Ta = +25°C

(2) Digital DC Characteristics

(V_{CCA} = V_{CCD} = 4.75 to 5.25 V, Ta = 0°C to +70°C)

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Digital high-level output voltage	V_{OH}	2.7	—	—	V	I_{OH} = –400 µA
Digital low-level output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
Digital high-level input voltage	V_{IHD}	2.0	—	—	V	
Digital low-level input voltage	V_{ILD}	—	—	0.8	V	
Maximum input current	I_{ID}	—	—	100	µA	V_{ID} = 7 V
High-level input current	I_{IHD}	—	0	20	µA	V_{IHD} = 2.7 V
Digital low-level input current	I_{ILD}	–100	–10	—	µA	V_{ILD} = 0.4 V
Power supply current	I_{CC}	—	40*	85	mA	

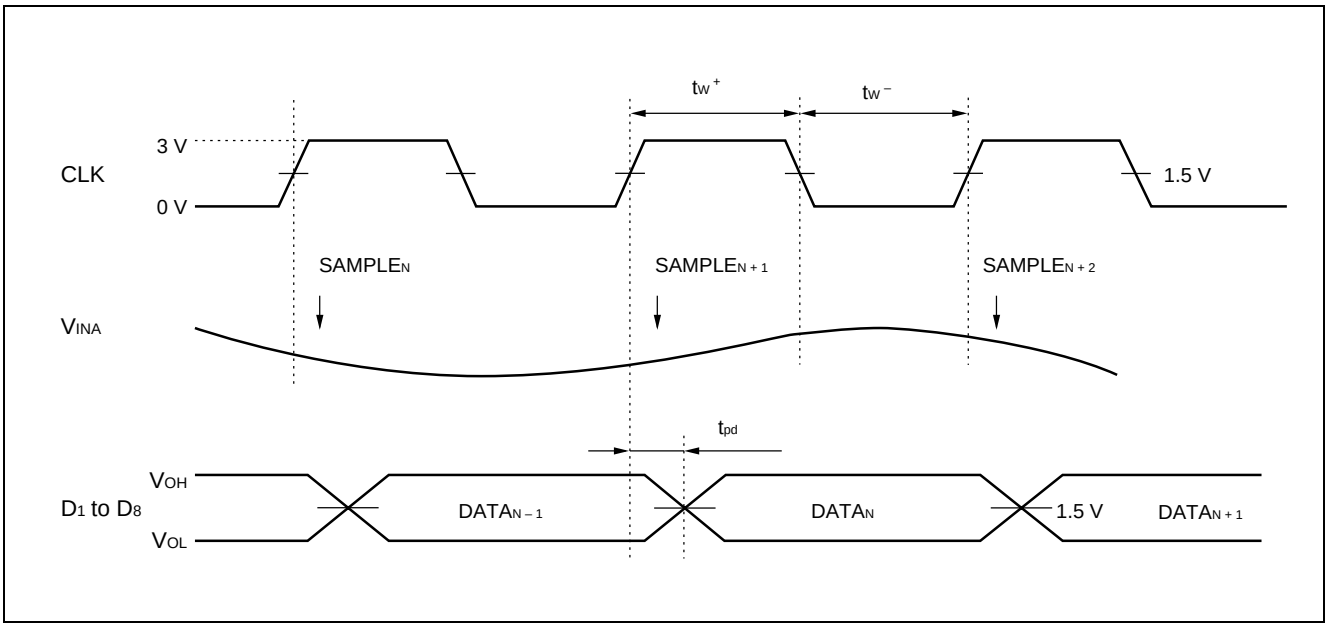
* : V_{CCA} = V_{CCD} = 5.00 V, Ta = +25°C

2. Switching Characteristics

(V_{CCA} = V_{CCD} = 4.75 to 5.25 V, Ta = 0°C to +70°C)

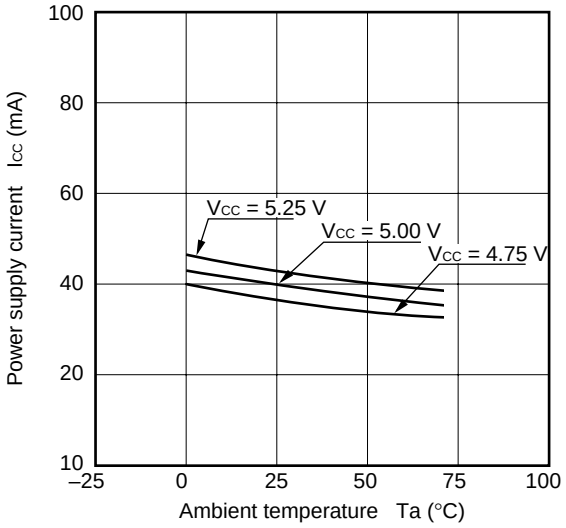
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Maximum conversion rate	f_S	20	—	—	MSPS
Digital output delay time	t_{pd}	8	15	30	ns

■ TIMING DIAGRAM

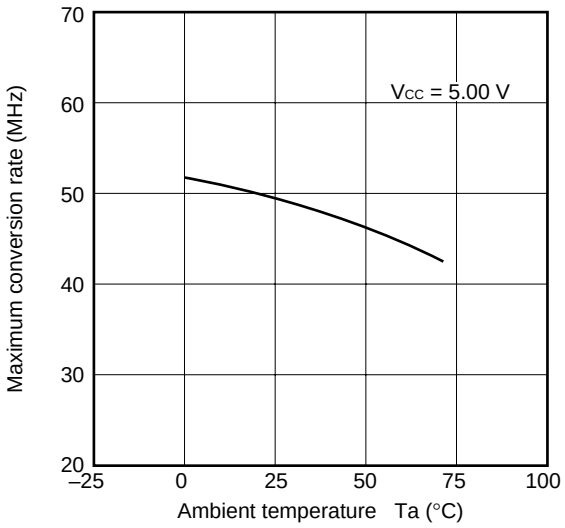


■ TYPICAL CHARACTERISTIC CURVES

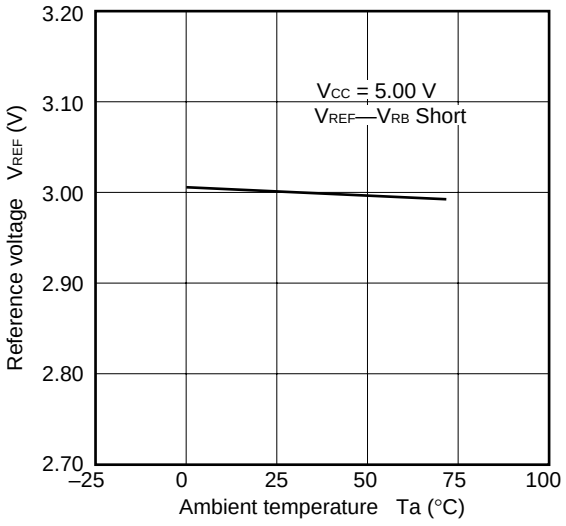
Power supply current vs. Temperature



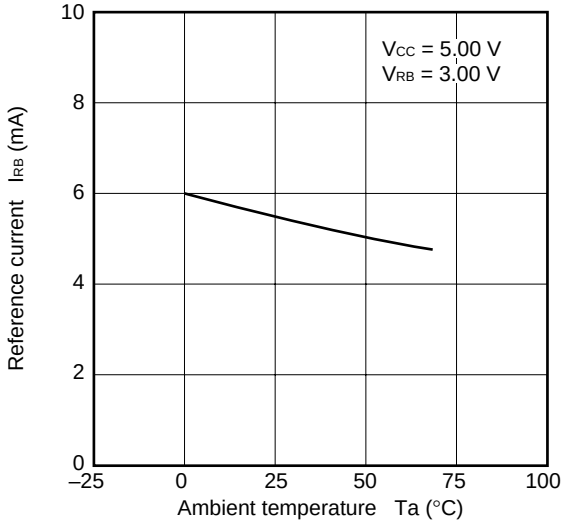
Maximum conversion rate vs. Temperature



Reference voltage vs. Temperature



Reference current vs. Temperature



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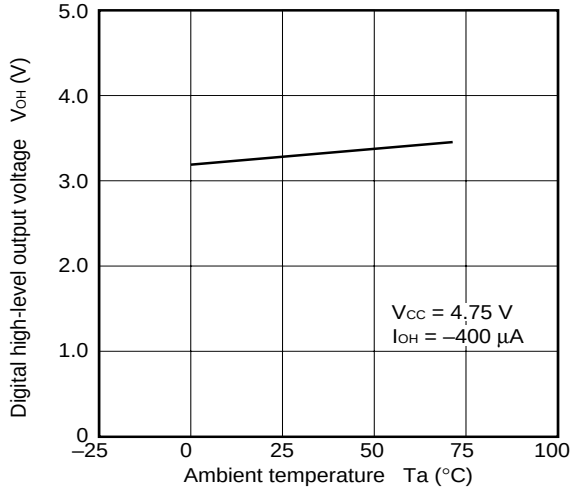
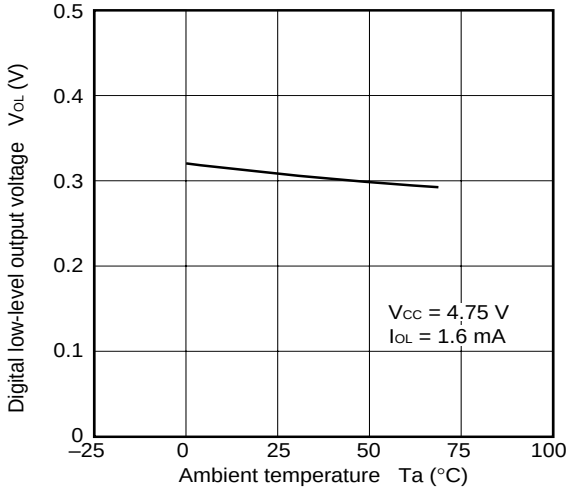
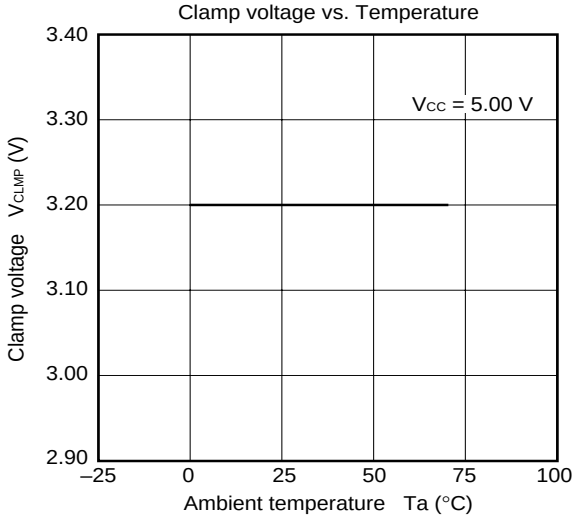
Digital high-level output voltage vs. Temperature



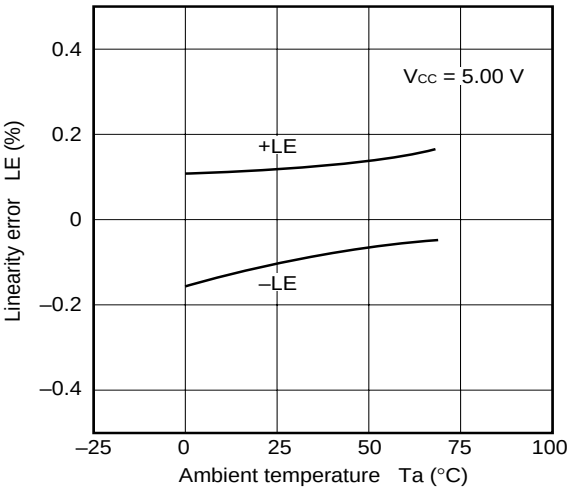
Digital low-level output voltage vs. Temperature



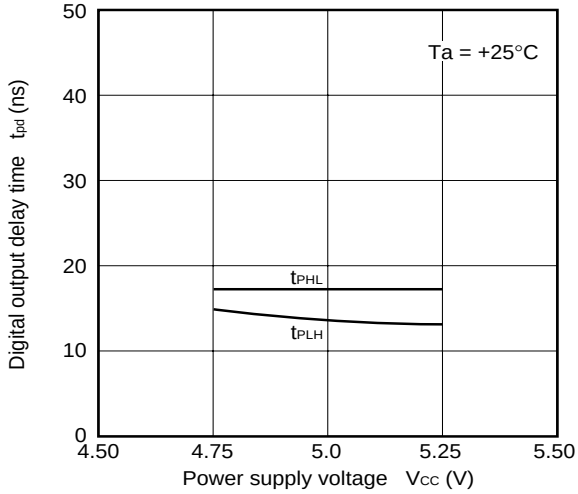
Clamp voltage vs. Temperature



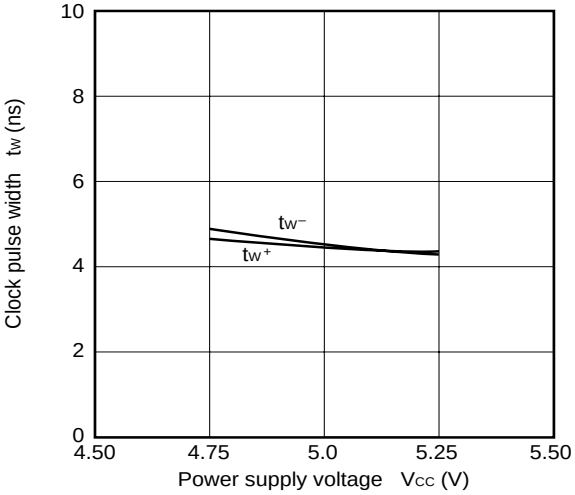
Linerity error vs. Temperature



Digital output delay time vs. Power supply voltage



Clock pulse width vs. Power supply voltage



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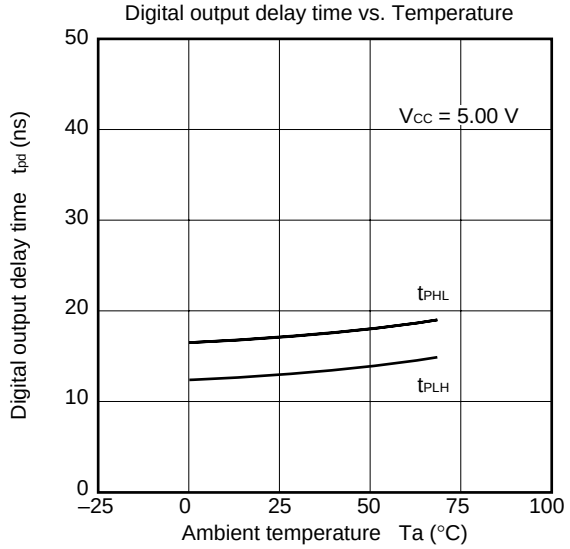
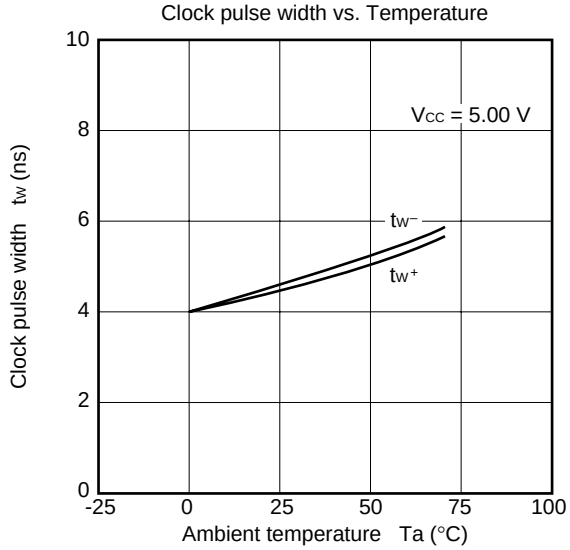
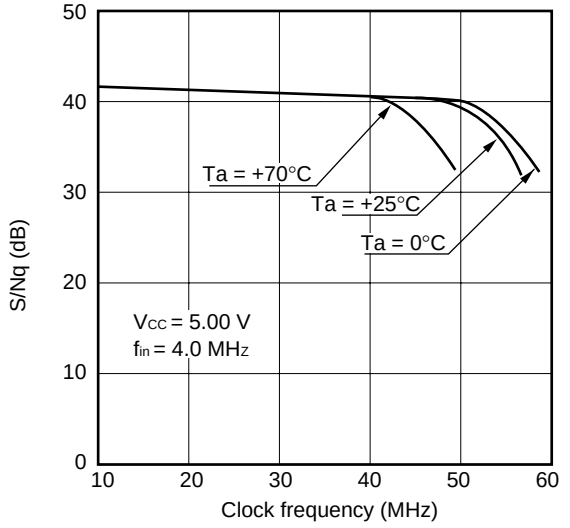
Digital output delay time vs. Temperature



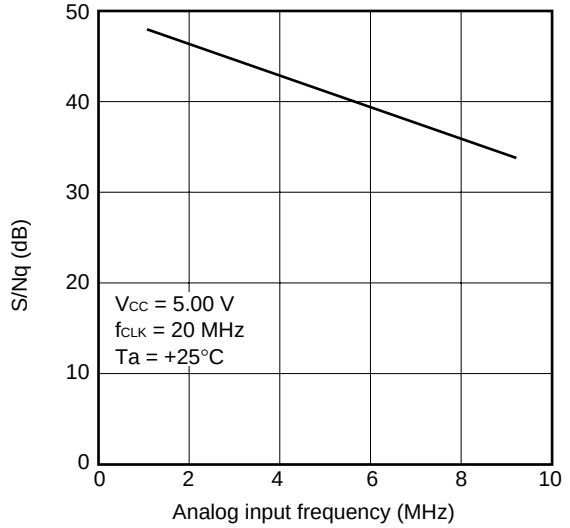
Clock pulse width vs. Temperature



S/Nq (RMS Signal/RMS Noise) vs. Clock frequency

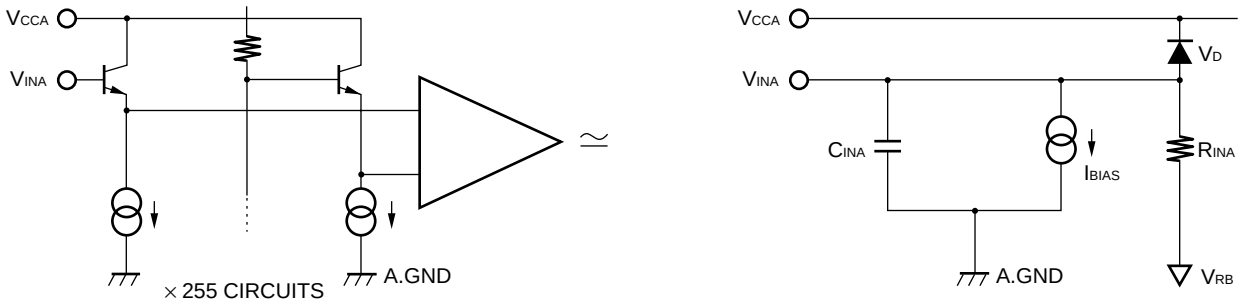


S/Nq (RMS Signal/RMS Noise) vs. Analog input frequency



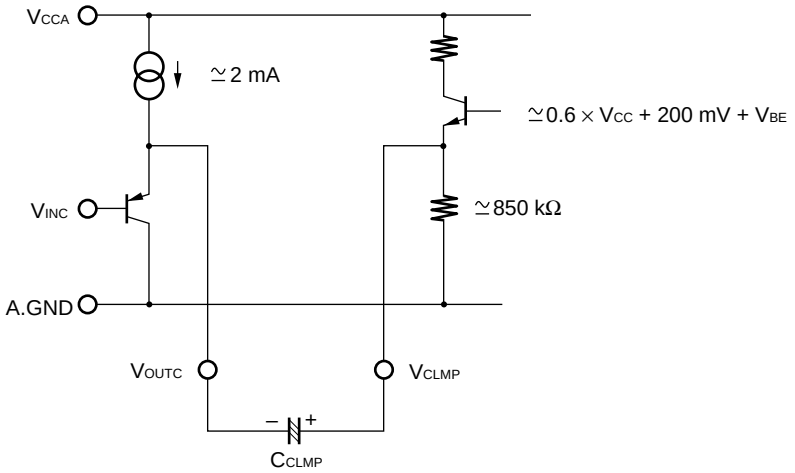
■ EQUIVALENT CIRCUIT

1. Analog Input Equivalent Circuit

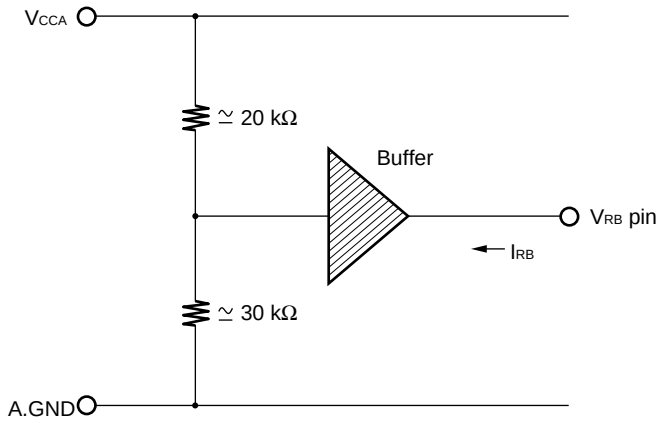


C_{INA} : Non-linear Emitter-Follower Junction Capacitance
R_{INA} : Linear Resistance Model for Input Current Transition by Comparator Switching
Infinite value for $V_{INA} < V_{RB}$ or when CLK + High
V_{RB} : Voltage at V_{RB} terminal.
I_{BIAS} : Constant Input Bias Current
V_D : The base-collector junction diode of emitter-follower transistor

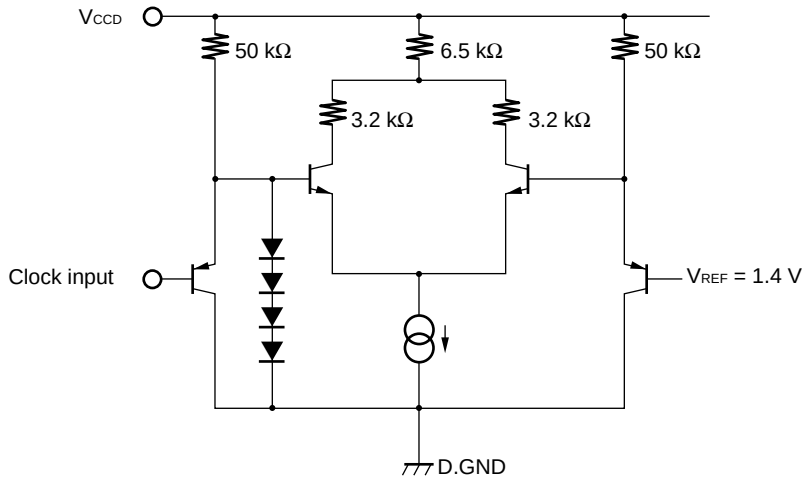
2. Equivalent Circuit of Clamp Circuit Block



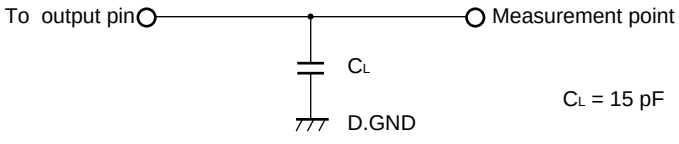
3. Equivalent Circuit of Reference Circuit Block



4. Digital Input Equivalent Circuit



5. Load Circuit for Output Buffer

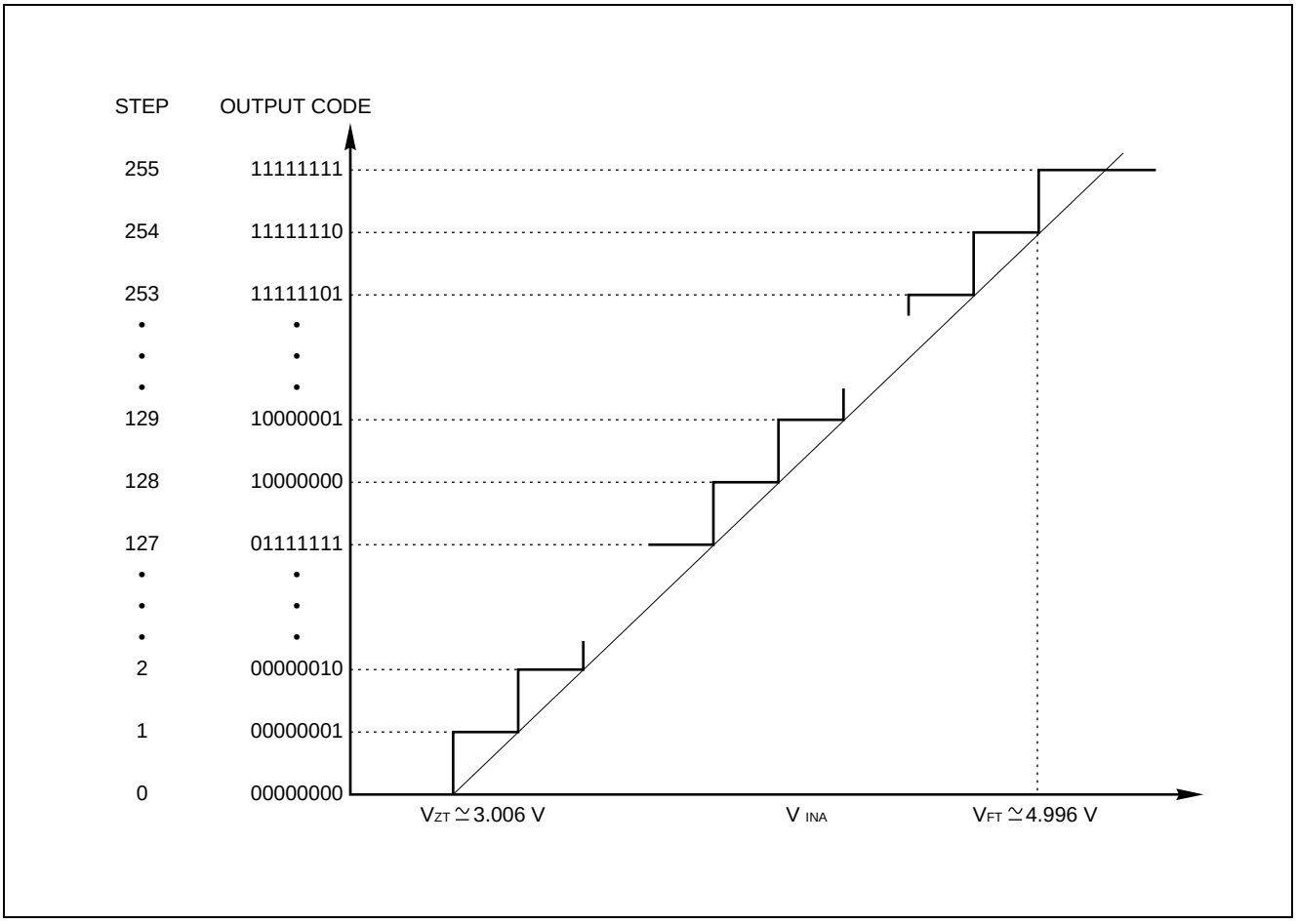


C_L = 15 pF

Note: CL = 15 pF including scope and jig capacitance

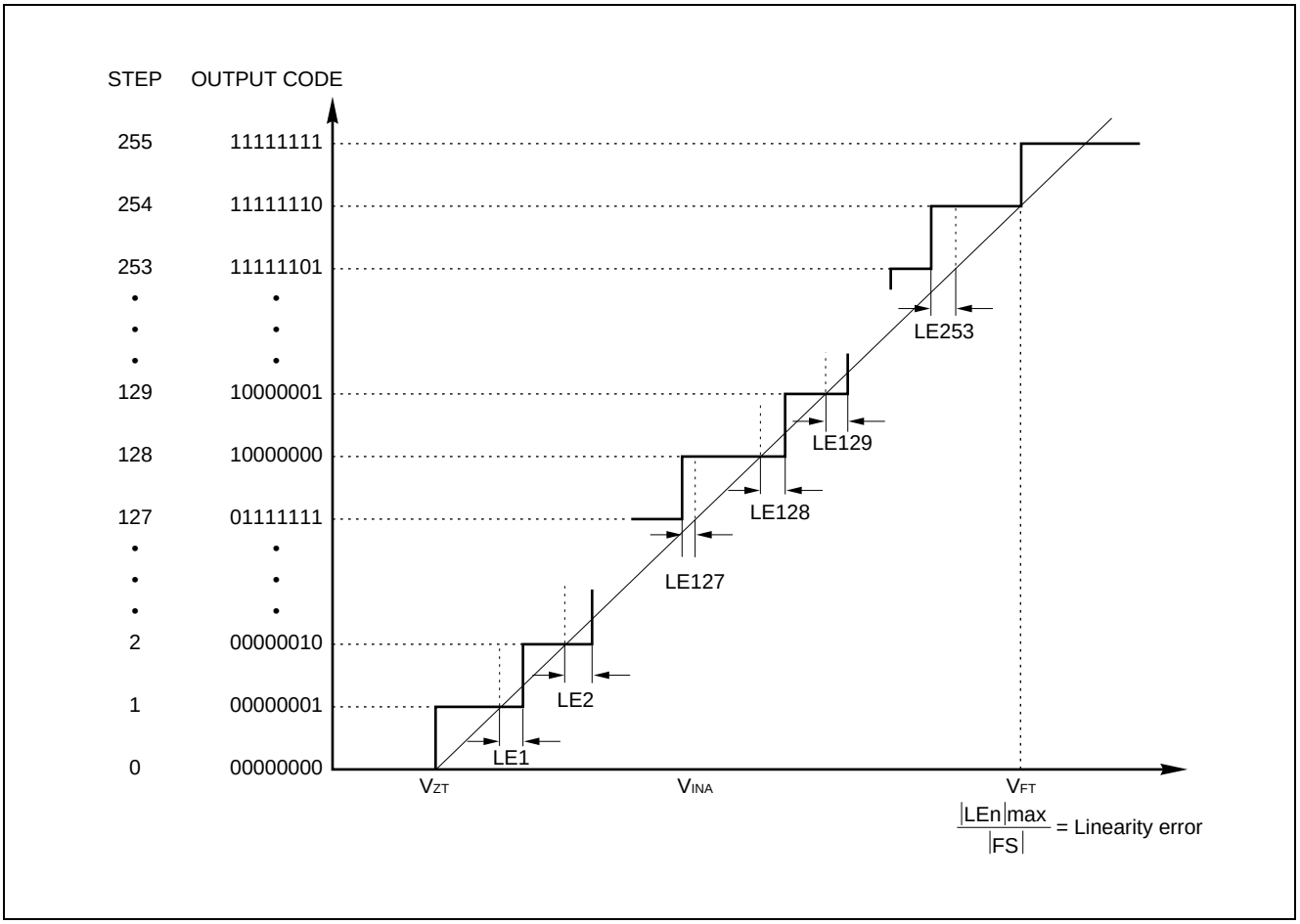
■ LINEARITY ERROR

1. Ideal Conversion Characteristics



The values for V_{ZT} and V_{FT} are typical values under conditions that $V_{CCA} = V_{CCD} = 5.000$ V and $V_{RB} = 3.000$ V.

2. Actual Conversion Characteristics



■ CLAMP CIRCUIT OPERATION

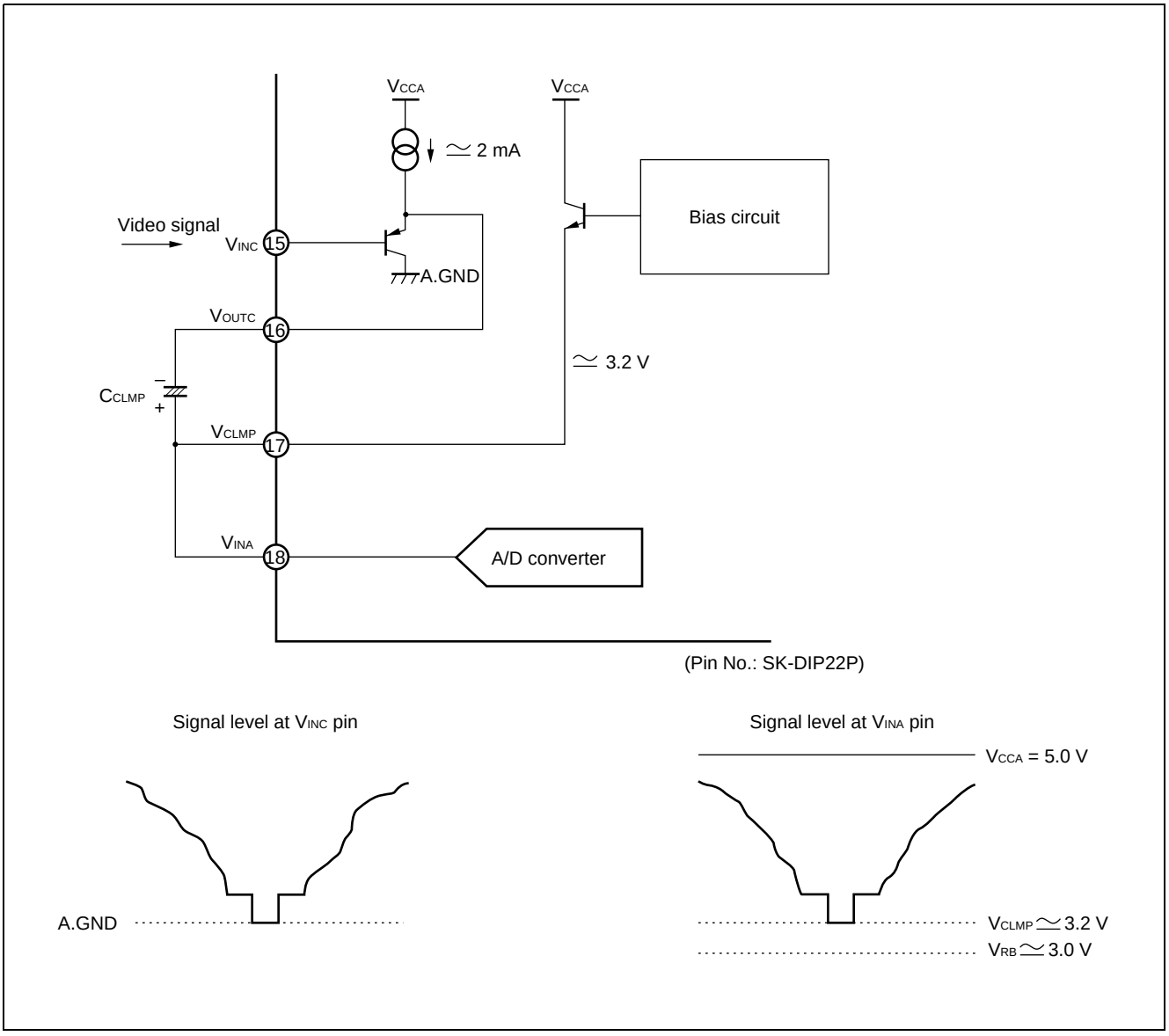
The MB40568's internal clamp circuit is a peak-detection type circuit, which clamps compound synchronized signals using the lowest sync point as clamp voltage (V_{CLMP}) (see illustration below).

The clamp voltage is set at $0.6 \times V_{CC} + 0.2$ V (typical).

If the clamp circuit is not used, the signal pins should be handled as follows:

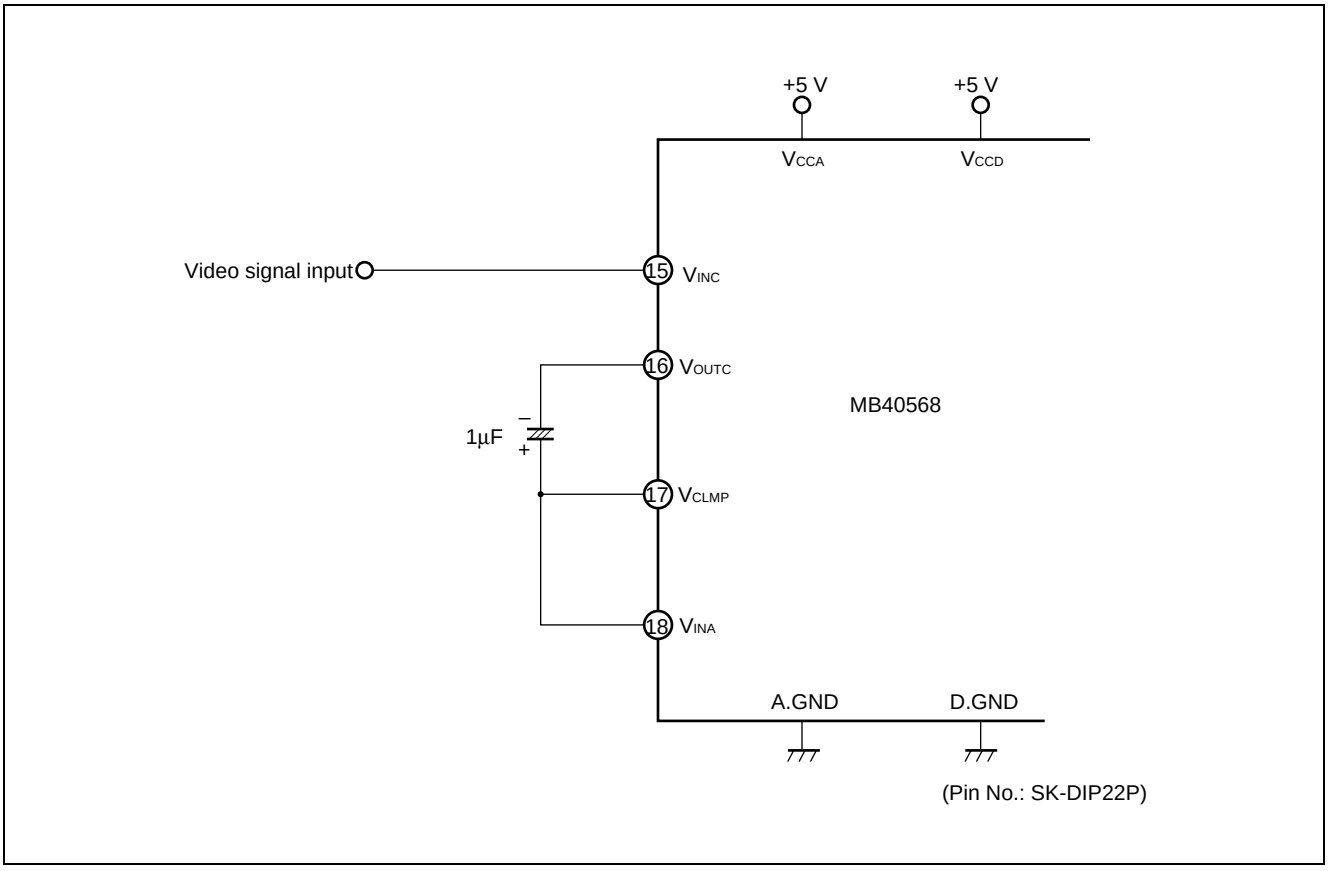
Pin name	Description
V_{INC}	Connect to GND
V_{OUTC}	Leave open
V_{CLMP}	Leave open

- **Clamp Circuit**

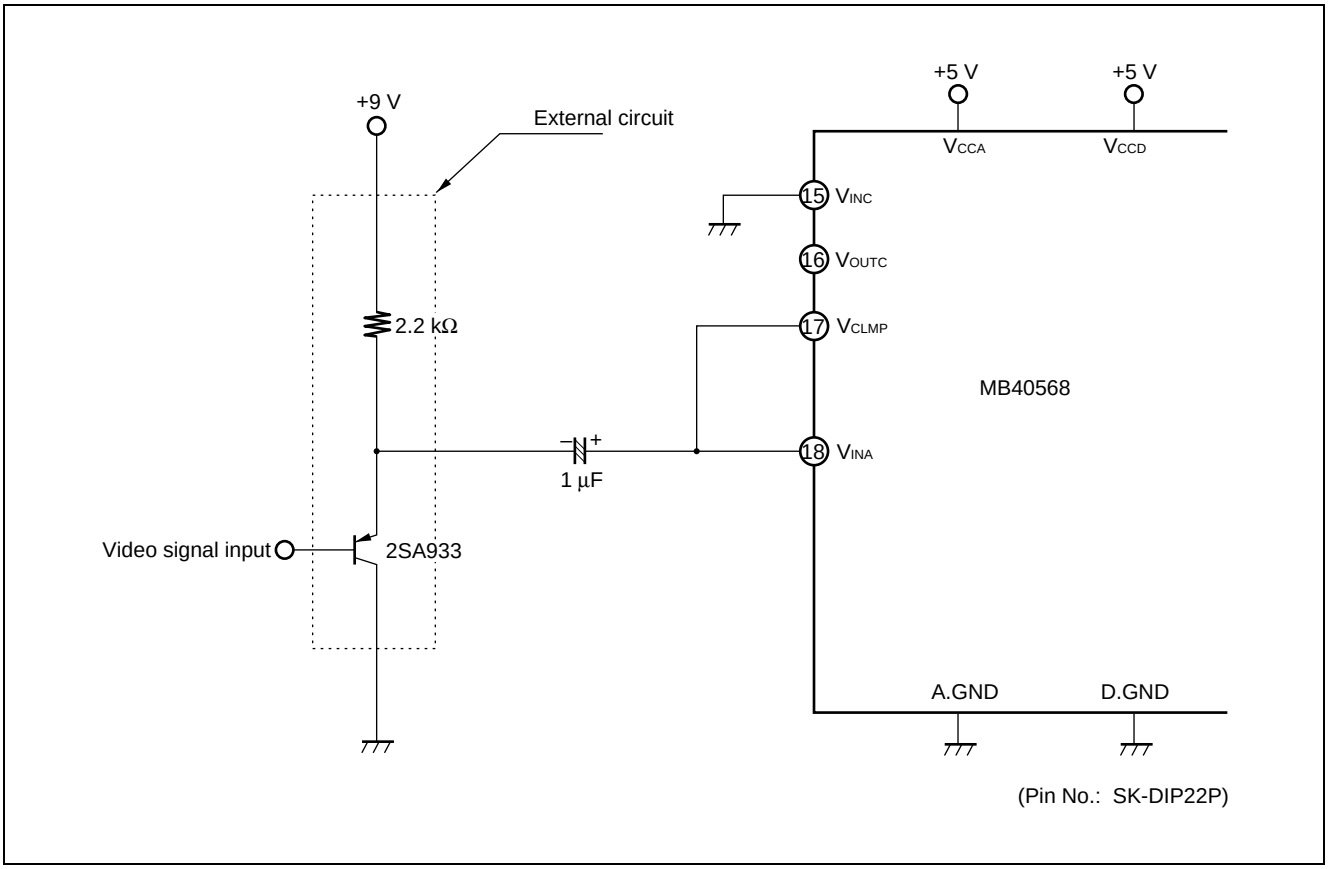


■ TYPICAL CONNECTION EXAMPLES

1. On-Chip Input PNP Transistor Utilized



2. Input PNP Transistor of Clamp Circuit is Put Externally

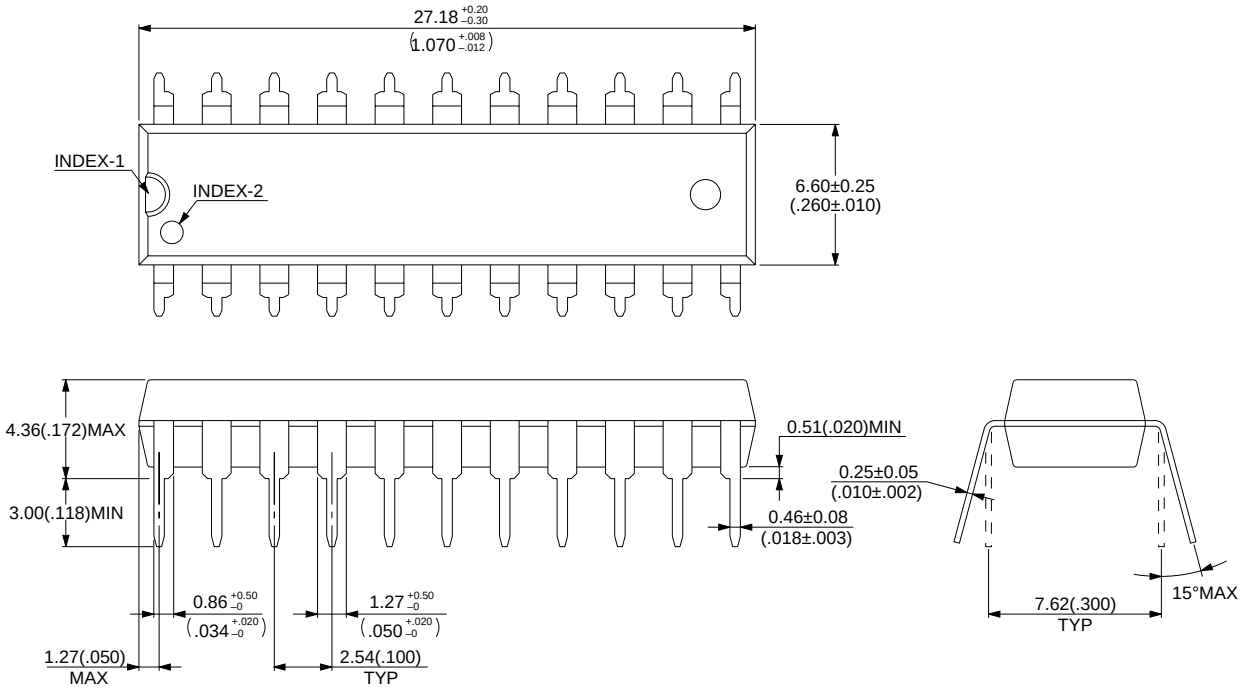


■ ORDERING INFORMATION

Part number	Package	Remarks
MB40568P-SK	20 pin Plastic SK-DIP (DIP-20P-M04)	
MB40568PF	24 pin Plastic SOP (FPT-24P-M02)	

■ PACKAGE DIMENSIONS

20-pin Plastic SK-DIP
(DIP-22P-M04)



Dimensions in mm (inches)

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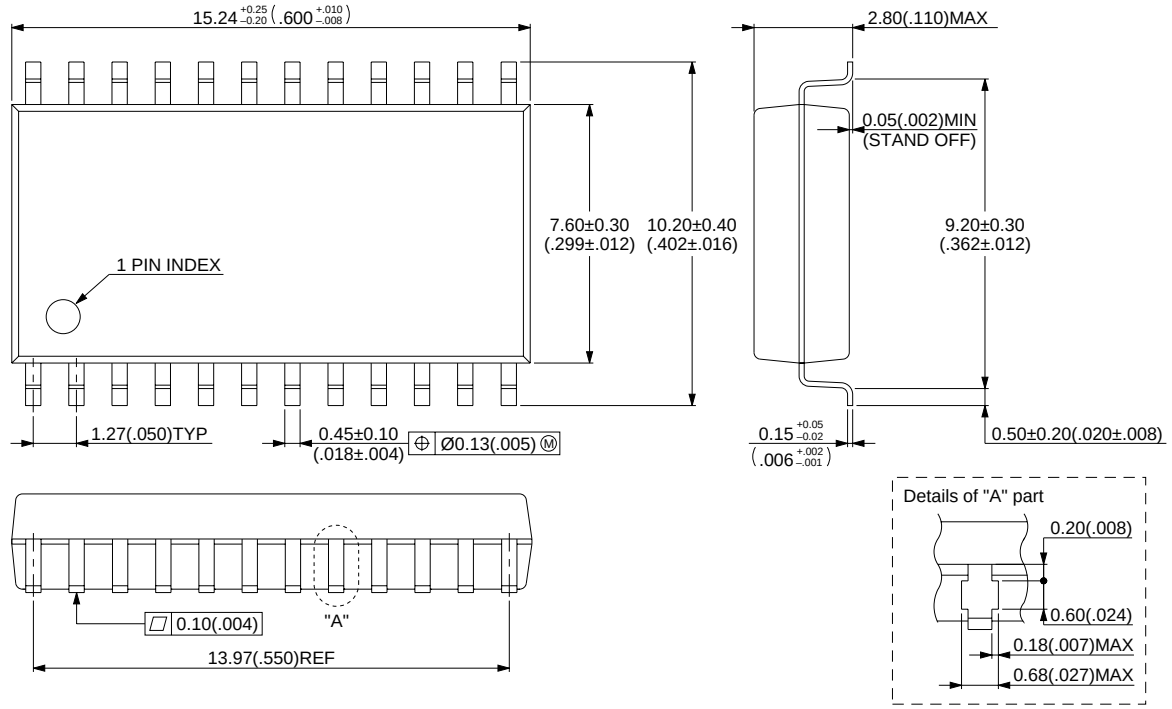
24-pin Plastic SOP
(FPT-24P-M02)



Dimensions in mm (inches)

MEMO

MEMO

FUJITSU LIMITED

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