



## TPS25925x/6x 简易的 5V/12V 电子熔丝保护开关

### 1 特性

- 12V 电子熔丝 – TPS25926x
- 5V 电子熔丝 – TPS25925x
- 集成 30mΩ 导通金属氧化物半导体场效应晶体管 (MOSFET)
- 固定过压钳位:
  - 6.1V 钳位 - TPS25925x
  - 15V 钳位 - TPS25926x
- 2A 至 5A 可调电流  $I_{LIMIT}$  (精度为  $\pm 15\%$ )
- 可编程  $V_{OUT}$  转换率, 欠压锁定 (UVLO)
- 内置热关断
- UL2367 认证正在处理中
- 单点故障测试期间安全 (UL60950)
- 小型封装 - 10L (3mm x 3mm) 超薄小外形尺寸无引线封装 (VSON)

### 2 应用

- 硬盘 (HDD) 和固态硬盘 (SSD)
- 机顶盒
- 服务器/辅助 (AUX) 电源
- PCI/PCIe 卡
- 适配器供电器件

### 3 说明

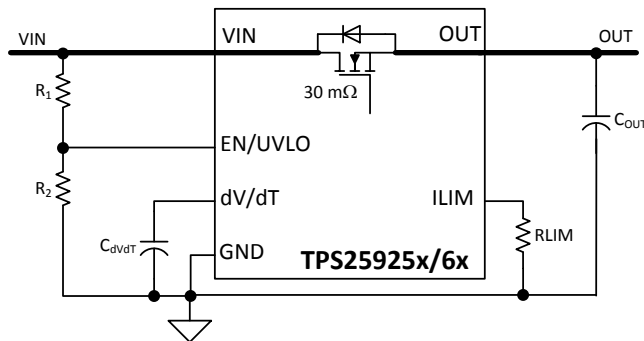
TPS25925x/6x 系列电子熔丝是采用小型封装的高度集成电路保护和电源管理解决方案。该器件使用极少的外部组件并可提供多重保护模式。它们能够有效地防止过载、短路、电压浪涌、过高浪涌电流和反向电流。电流限制水平可通过单个外部电阻进行设置, 设定电流限值的精度典型值为  $\pm 15\%$ 。内部钳位电路可将过电压限制在一个安全的固定最大值, 无需使用外部组件。TPS25926x 器件为 12V 系统提供过压保护 (OVP), 而 TPS25925x 器件为 5V 系统提供过压保护。在有特定电压斜坡要求的情况下, 可使用单个电容对提供的 dV/dT 引脚进行编程, 以确保适当的输出斜率。

#### 器件信息<sup>(1)</sup>

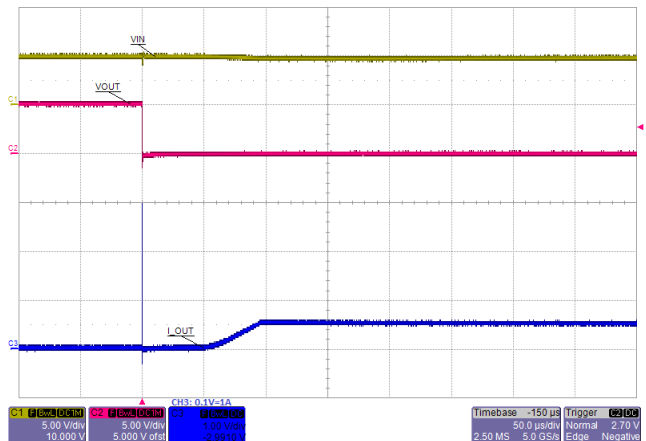
| 器件型号                 | 封装        | 封装尺寸 (标称值)      |
|----------------------|-----------|-----------------|
| TPS259250, TPS259251 | VSON (10) | 3.00mm × 3.00mm |
| TPS259260, TPS259261 |           |                 |

(1) 要了解所有可用封装, 请见数据表末尾的可订购产品附录。

应用电路原理图



瞬态: 输出短路



## 目录

|          |                                        |           |           |                                       |           |
|----------|----------------------------------------|-----------|-----------|---------------------------------------|-----------|
| <b>1</b> | <b>特性</b>                              | <b>1</b>  | <b>9</b>  | <b>Application and Implementation</b> | <b>18</b> |
| <b>2</b> | <b>应用</b>                              | <b>1</b>  | 9.1       | Application Information               | 18        |
| <b>3</b> | <b>说明</b>                              | <b>1</b>  | 9.2       | Typical Application                   | 18        |
| <b>4</b> | <b>修订历史记录</b>                          | <b>2</b>  | <b>10</b> | <b>Power Supply Recommendations</b>   | <b>23</b> |
| <b>5</b> | <b>Device Comparison Table</b>         | <b>3</b>  | 10.1      | Transient Protection                  | 23        |
| <b>6</b> | <b>Pin Configuration and Functions</b> | <b>3</b>  | 10.2      | Output Short-Circuit Measurements     | 24        |
| <b>7</b> | <b>Specifications</b>                  | <b>4</b>  | <b>11</b> | <b>Layout</b>                         | <b>24</b> |
| 7.1      | Absolute Maximum Ratings               | 4         | 11.1      | Layout Guidelines                     | 24        |
| 7.2      | ESD Ratings                            | 4         | 11.2      | Layout Example                        | 25        |
| 7.3      | Recommended Operating Conditions       | 4         | <b>12</b> | <b>器件和文档支持</b>                        | <b>26</b> |
| 7.4      | Thermal Information                    | 5         | 12.1      | 器件支持                                  | 26        |
| 7.5      | Electrical Characteristics             | 5         | 12.2      | 文档支持                                  | 26        |
| 7.6      | Timing Requirements                    | 6         | 12.3      | 相关链接                                  | 26        |
| 7.7      | Typical Characteristics                | 7         | 12.4      | 社区资源                                  | 26        |
| <b>8</b> | <b>Detailed Description</b>            | <b>14</b> | 12.5      | 商标                                    | 26        |
| 8.1      | Overview                               | 14        | 12.6      | 静电放电警告                                | 26        |
| 8.2      | Functional Block Diagram               | 14        | 12.7      | Glossary                              | 26        |
| 8.3      | Feature Description                    | 14        | <b>13</b> | <b>机械、封装和可订购信息</b>                    | <b>26</b> |
| 8.4      | Device Functional Modes                | 17        |           |                                       |           |

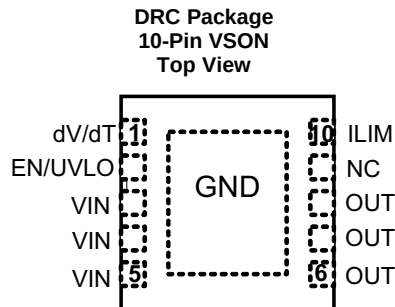
## 4 修订历史记录

| Changes from Original (August 2015) to Revision A               | Page |
|-----------------------------------------------------------------|------|
| <ul style="list-style-type: none"> <li>已更改 产品预览至量产数据</li> </ul> | 1    |

## 5 Device Comparison Table

| PART NUMBER | UV    | OV CLAMP | FAULT RESPONSE | STATUS |
|-------------|-------|----------|----------------|--------|
| TPS259250   | 4.3 V | 6.1 V    | Latched        | Active |
| TPS259251   | 4.3 V | 6.1 V    | Auto Retry     | Active |
| TPS259260   | 4.3 V | 15 V     | Latched        | Active |
| TPS259261   | 4.3 V | 15 V     | Auto Retry     | Active |

## 6 Pin Configuration and Functions



### Pin Functions

| PIN     |             | DESCRIPTION                                                                                                                                                                                                                                                            |
|---------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME    | NUMBER      |                                                                                                                                                                                                                                                                        |
| dV/dT   | 1           | Connect a capacitor from this pin to GND to control the ramp rate of OUT voltage at device turn-on.                                                                                                                                                                    |
| EN/UVLO | 2           | This is a dual function control pin. When used as an ENABLE pin and pulled down, it shuts off the internal pass MOSFET. When pulled high, it enables the device.<br>As an UVLO pin, it can be used to program different UVLO trip point via external resistor divider. |
| GND     | Thermal Pad | GND                                                                                                                                                                                                                                                                    |
| ILIM    | 10          | A resistor from this pin to GND will set the overload and short circuit limit.                                                                                                                                                                                         |
| NC      | 9           | Not Connected Internally. Can be left floating or grounded.                                                                                                                                                                                                            |
| OUT     | 6-8         | Output of the device                                                                                                                                                                                                                                                   |
| VIN     | 3-5         | Input supply voltage                                                                                                                                                                                                                                                   |

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted) <sup>(1)</sup> <sup>(2)</sup>

|                                       |                        | MIN  | MAX                 | UNIT |
|---------------------------------------|------------------------|------|---------------------|------|
| Supply voltage <sup>(1)</sup>         | VIN                    | −0.3 | 20                  | V    |
|                                       | VIN (Transient < 1 ms) |      | 22                  |      |
| Output voltage                        | OUT                    | −0.3 | VIN + 0.3           | V    |
|                                       | OUT (Transient < 1 μs) |      | −1.2                | V    |
| Voltage                               | ILIM                   | −0.3 | 7                   | V    |
| Continuous output current             |                        |      | 6.25 <sup>(3)</sup> | A    |
| Voltage                               | EN/UVLO                | −0.3 | 7                   | V    |
| Voltage                               | dV/dT                  | −0.3 | 7                   | V    |
| Storage temperature, T <sub>stg</sub> |                        | −65  | 150                 | °C   |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential voltages, are with respect to network ground terminal.

(3) Device supports high peak current during short circuit conditions until current is internally limited.

### 7.2 ESD Ratings

|                    |                         |                                                                                | VALUE | UNIT |
|--------------------|-------------------------|--------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 | V    |
|                    |                         | Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±500  |      |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                                                      |                  | MIN | TYP | MAX  | UNIT |
|------------------------------------------------------|------------------|-----|-----|------|------|
| Input voltage                                        | VIN (TPS25926x)  | 4.5 | 12  | 13.8 | V    |
|                                                      | VIN (TPS25925x)  | 4.5 | 5   | 5.5  |      |
|                                                      | dV/dT, EN/UVLO   | 0   |     | 6    |      |
|                                                      | ILIM             | 0   |     | 3    |      |
| Continuous output current                            | I <sub>OUT</sub> | 0   |     | 5    | A    |
| Resistance                                           | ILIM             | 10  | 100 | 162  | kΩ   |
| External capacitance                                 | OUT              | 0.1 | 1   | 1000 | μF   |
|                                                      | dV/dT            |     | 1   | 1000 | nF   |
| Operating junction temperature range, T <sub>J</sub> |                  | −40 | 25  | 125  | °C   |
| Operating Ambient temperature range, T <sub>A</sub>  |                  | −40 | 25  | 85   | °C   |

## 7.4 Thermal Information<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

| THERMAL METRIC       |                                              | TPS25925x/6x | UNIT |
|----------------------|----------------------------------------------|--------------|------|
|                      |                                              | DRC (VSON)   |      |
|                      |                                              | 10 PINS      |      |
| R <sub>θJA</sub>     | Junction-to-ambient thermal resistance       | 45.9         | °C/W |
| R <sub>θJCTop</sub>  | Junction-to-case (top) thermal resistance    | 53           |      |
| R <sub>θJB</sub>     | Junction-to-board thermal resistance         | 21.2         |      |
| Ψ <sub>JT</sub>      | Junction-to-top characterization parameter   | 1.2          |      |
| Ψ <sub>JB</sub>      | Junction-to-board characterization parameter | 21.4         |      |
| R <sub>θJCbott</sub> | Junction-to-case (bottom) thermal resistance | 5.9          |      |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

–40°C ≤ T<sub>J</sub> ≤ 125°C, V<sub>IN</sub> = 12 V for TPS25926x, V<sub>IN</sub> = 5 V for TPS25925x, V<sub>EN /UVLO</sub> = 2 V, R<sub>ILIM</sub> = 100 kΩ, C<sub>dVdT</sub> = OPEN. All voltages referenced to GND (unless otherwise noted).

| PARAMETER                        |                                            | TEST CONDITIONS                                                                                             | MIN  | TYP  | MAX   | UNIT |
|----------------------------------|--------------------------------------------|-------------------------------------------------------------------------------------------------------------|------|------|-------|------|
| VIN (INPUT SUPPLY)               |                                            |                                                                                                             |      |      |       |      |
| V <sub>UVR</sub>                 | UVLO threshold, rising                     |                                                                                                             | 4.15 | 4.3  | 4.45  | V    |
| V <sub>UVhyst</sub>              | UVLO hysteresis <sup>(1)</sup>             |                                                                                                             | 5%   |      |       |      |
| I <sub>QON</sub>                 | Supply current                             | Enabled: EN/UVLO = 2 V, TPS25926x                                                                           | 0.3  | 0.47 | 0.55  | mA   |
|                                  |                                            | Enabled: EN/UVLO = 2 V, TPS25925x                                                                           | 0.35 | 0.42 | 0.6   | mA   |
| I <sub>QOFF</sub>                |                                            | EN/UVLO = 0 V                                                                                               |      | 0.13 | 0.225 | mA   |
| V <sub>OVC</sub>                 | Over-voltage clamp                         | VIN > 16.5 V, I <sub>OUT</sub> = 10 mA, TPS25926x                                                           | 13.8 | 15   | 16.5  | V    |
|                                  |                                            | VIN > 6.75 V, I <sub>OUT</sub> = 10 mA,<br>–40°C ≤ T <sub>J</sub> ≤ 85°C, TPS25925x                         | 5.5  | 6.1  | 6.75  |      |
|                                  |                                            | VIN > 6.75 V, I <sub>OUT</sub> = 10 mA,<br>–40°C ≤ T <sub>J</sub> ≤ 125°C, TPS25925x                        | 5.25 | 6.1  | 6.75  |      |
| EN/UVLO (ENABLE/UVLO INPUT)      |                                            |                                                                                                             |      |      |       |      |
| V <sub>ENR</sub>                 | EN Threshold voltage, rising               |                                                                                                             | 1.37 | 1.4  | 1.44  | V    |
| V <sub>ENF</sub>                 | EN Threshold voltage, falling              |                                                                                                             | 1.32 | 1.35 | 1.39  | V    |
| I <sub>EN</sub>                  | EN Input leakage current                   | 0 V ≤ V <sub>EN</sub> ≤ 5 V                                                                                 | –100 | 0    | 100   | nA   |
| dV/dT (OUTPUT RAMP CONTROL)      |                                            |                                                                                                             |      |      |       |      |
| I <sub>dVdT</sub>                | dV/dT Charging current <sup>(1)</sup>      | V <sub>dVdT</sub> = 0 V                                                                                     | 220  |      |       | nA   |
| R <sub>dVdT_disch</sub>          | dV/dT Discharging resistance               | EN/UVLO = 0 V, I <sub>dVdT</sub> = 10 mA sinking                                                            | 50   | 73   | 100   | Ω    |
| V <sub>dVdTmax</sub>             | dV/dT Max capacitor voltage <sup>(1)</sup> |                                                                                                             | 5.5  |      |       | V    |
| GAIN <sub>dVdT</sub>             | dV/dT to OUT gain <sup>(1)</sup>           | ΔV <sub>dVdT</sub>                                                                                          | 4.85 |      |       | V/V  |
| ILIM (CURRENT LIMIT PROGRAMMING) |                                            |                                                                                                             |      |      |       |      |
| I <sub>ILIM</sub>                | ILIM Bias current <sup>(1)</sup>           |                                                                                                             | 10   |      |       | μA   |
| I <sub>OL</sub>                  | Overload current limit <sup>(2)</sup>      | R <sub>ILIM</sub> = 45.3 kΩ, V <sub>VIN-OUT</sub> = 1 V                                                     | 1.75 | 2.1  | 2.45  | A    |
|                                  |                                            | R <sub>ILIM</sub> = 100 kΩ, V <sub>VIN-OUT</sub> = 1 V                                                      | 3.4  | 3.75 | 4.05  |      |
|                                  |                                            | R <sub>ILIM</sub> = 150 kΩ, V <sub>VIN-OUT</sub> = 1 V                                                      | 4.5  | 5.1  | 5.7   |      |
| I <sub>OL-R-Short</sub>          |                                            | R <sub>ILIM</sub> = 0 Ω, Shorted Resistor Current Limit (Single Point Failure Test: UL60950) <sup>(1)</sup> | 0.84 |      |       | A    |
| I <sub>OL-R-Open</sub>           |                                            | R <sub>ILIM</sub> = OPEN, Open Resistor Current Limit (Single Point Failure Test: UL60950) <sup>(1)</sup>   | 0.73 |      |       | A    |

(1) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

(2) Pulsed testing techniques used during this test maintain junction temperature approximately equal to ambient temperature.

## Electrical Characteristics (continued)

–40°C ≤ T<sub>J</sub> ≤ 125°C, V<sub>IN</sub> = 12 V for TPS25926x, V<sub>IN</sub> = 5 V for TPS25925x, V<sub>EN /UVLO</sub> = 2 V, R<sub>ILIM</sub> = 100 kΩ, C<sub>dVdT</sub> = OPEN.  
All voltages referenced to GND (unless otherwise noted).

| PARAMETER                 |                                                                         | TEST CONDITIONS                                                     | MIN        | TYP  | MAX  | UNIT |
|---------------------------|-------------------------------------------------------------------------|---------------------------------------------------------------------|------------|------|------|------|
| I <sub>SCL</sub>          | Short-circuit current limit <sup>(2)</sup>                              | R <sub>ILIM</sub> = 45.3 kΩ, V <sub>VIN-OUT</sub> = 5 V, TPS25925x  | 1.72       | 2.05 | 2.42 | A    |
|                           |                                                                         | R <sub>ILIM</sub> = 45.3 kΩ, V <sub>VIN-OUT</sub> = 12 V, TPS25926x | 1.62       | 1.98 | 2.37 |      |
|                           |                                                                         | R <sub>ILIM</sub> = 100 kΩ, V <sub>VIN-OUT</sub> = 5 V, TPS25925x   | 3.1        | 3.56 | 4.0  |      |
|                           |                                                                         | R <sub>ILIM</sub> = 100 kΩ, V <sub>VIN-OUT</sub> = 12 V, TPS25926x  | 2.9        | 3.32 | 3.85 |      |
|                           |                                                                         | R <sub>ILIM</sub> = 150 kΩ, V <sub>VIN-OUT</sub> = 5 V, TPS25925x   | 4.22       | 4.95 | 5.69 |      |
|                           |                                                                         | R <sub>ILIM</sub> = 150 kΩ, V <sub>VIN-OUT</sub> = 12 V, TPS25926x  | 3.7        | 4.5  | 5.5  |      |
| RATIO <sub>FASTTRIP</sub> | Fast-Trip comparator level w.r.t. overload current limit <sup>(1)</sup> | I <sub>FASTTRIP</sub> : I <sub>OL</sub>                             | 160%       |      |      |      |
| V <sub>OpenILIM</sub>     | ILIM Open resistor detect threshold <sup>(1)</sup>                      | V <sub>ILIM</sub> Rising, R <sub>ILIM</sub> = OPEN                  | 3.1        |      |      | V    |
| OUT (PASS FET OUTPUT)     |                                                                         |                                                                     |            |      |      |      |
| T <sub>ON</sub>           | Turn-on delay <sup>(1)</sup>                                            | EN/UVLO → H to I <sub>VIN</sub> = 100 mA, 1-A resistive load at OUT | 220        |      |      | μs   |
| R <sub>DS(on)</sub>       | FET ON resistance                                                       | T <sub>J</sub> = 25°C                                               | 21         | 30   | 39   | mΩ   |
|                           |                                                                         | T <sub>J</sub> = 125°C                                              | 40 50      |      |      |      |
| I <sub>OUT-OFF-LKG</sub>  | OUT Bias current in off state                                           | V <sub>EN/UVLO</sub> = 0 V, V <sub>OUT</sub> = 0 V (Sourcing)       | –5         | 0    | 1.2  | μA   |
| I <sub>OUT-OFF-SINK</sub> |                                                                         | V <sub>EN/UVLO</sub> = 0V, V <sub>OUT</sub> = 300 mV (Sinking)      | 10         | 15   | 20   |      |
| THERMAL SHUT DOWN (TSD)   |                                                                         |                                                                     |            |      |      |      |
| T <sub>SHDN</sub>         | TSD Threshold, rising <sup>(1)</sup>                                    |                                                                     | 150        |      |      | °C   |
| T <sub>SHDNhyst</sub>     | TSD Hysteresis <sup>(1)</sup>                                           |                                                                     | 10         |      |      | °C   |
|                           | Thermal fault: latched or autoretry                                     | TPS259250, TPS259260                                                | LATCHED    |      |      |      |
|                           |                                                                         | TPS259251, TPS259261                                                | AUTO-RETRY |      |      |      |

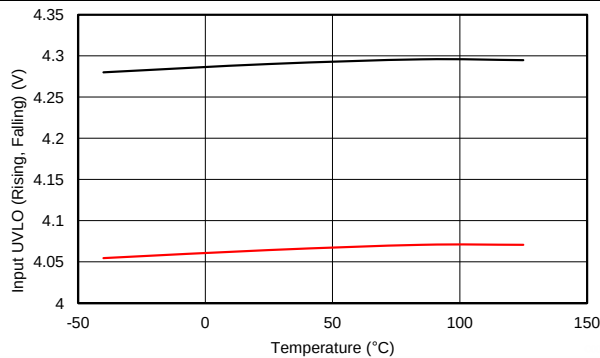
## 7.6 Timing Requirements

| PARAMETER                        |                                                                                            | TEST CONDITIONS                                                                 | MIN  | TYP | MAX  | UNIT |
|----------------------------------|--------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------|------|-----|------|------|
| t <sub>OFFdly</sub>              | Turn Off delay <sup>(1)</sup>                                                              | EN↓                                                                             | 0.4  |     |      | μs   |
| dV/dT (OUTPUT RAMP CONTROL)      |                                                                                            |                                                                                 |      |     |      |      |
| t <sub>dVdT</sub>                | Output ramp time                                                                           | TPS25926x, EN/UVLO → H to OUT = 11.7 V, C <sub>dVdT</sub> = 0                   | 0.7  | 1   | 1.3  | ms   |
|                                  |                                                                                            | TPS25925x, EN/UVLO → H to OUT = 4.9 V, C <sub>dVdT</sub> = 0                    | 0.28 | 0.4 | 0.52 |      |
|                                  |                                                                                            | TPS25926x, EN/UVLO → H to OUT = 11.7 V, C <sub>dVdT</sub> = 1 nF <sup>(1)</sup> | 12   |     |      |      |
|                                  |                                                                                            | TPS25925x, EN/UVLO → H to OUT = 4.9 V, C <sub>dVdT</sub> = 1 nF <sup>(1)</sup>  | 5    |     |      |      |
| ILIM (CURRENT LIMIT PROGRAMMING) |                                                                                            |                                                                                 |      |     |      |      |
| t <sub>FastOffDly</sub>          | Fast-Trip comparator delay <sup>(1)</sup>                                                  | I <sub>OUT</sub> > I <sub>FASTTRIP</sub> to I <sub>OUT</sub> = 0 (Switch Off)   | 300  |     |      | ns   |
| THERMAL SHUTDOWN (TSD)           |                                                                                            |                                                                                 |      |     |      |      |
| t <sub>TSDdly</sub>              | Retry Delay after TSD Recovery, T <sub>J</sub> < [T <sub>SHDN</sub> - 10°C] <sup>(1)</sup> | At VIN = 5 V, TPS259251 and TPS259261                                           | 110  |     |      | ms   |
|                                  |                                                                                            | At VIN = 12 V, TPS259251 and TPS259261                                          | 145  |     |      |      |

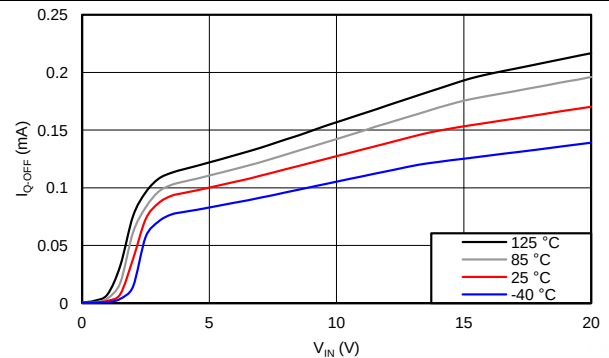
(1) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

## 7.7 Typical Characteristics

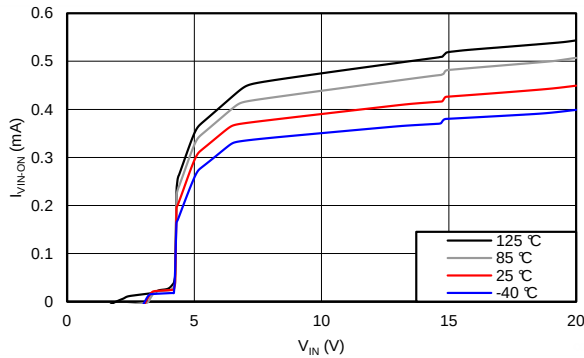
$T_J = 25^\circ\text{C}$ ,  $V_{VIN} = 12\text{ V}$  for TPS25926x,  $V_{VIN} = 5\text{ V}$  for TPS25925x,  $V_{EN/UVLO} = 2\text{ V}$ ,  $R_{ILIM} = 100\text{ k}\Omega$ ,  $C_{VIN} = 0.1\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ ,  $C_{dVdT} = \text{OPEN}$  (unless stated otherwise)



**Figure 1. Input UVLO vs Temperature**

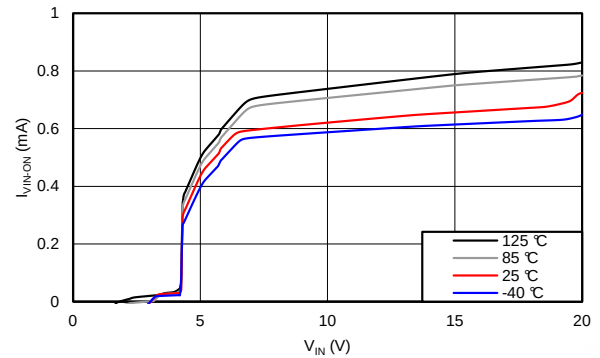


**Figure 2.  $I_{Q-OFF}$  vs  $V_{IN}$**



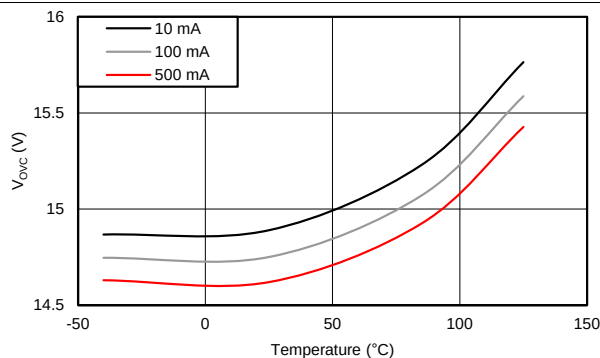
TPS25926x

**Figure 3.  $I_{VIN-ON}$  vs  $V_{IN}$**



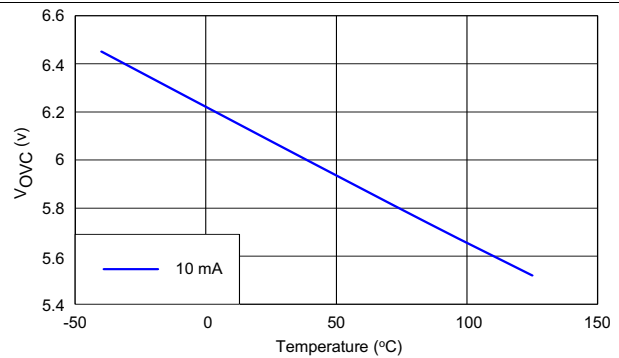
TPS25925x

**Figure 4.  $I_{VIN-ON}$  vs  $V_{IN}$**



TPS25926x

**Figure 5.  $V_{OVC}$  vs Temperature Across  $I_{OUT}$**

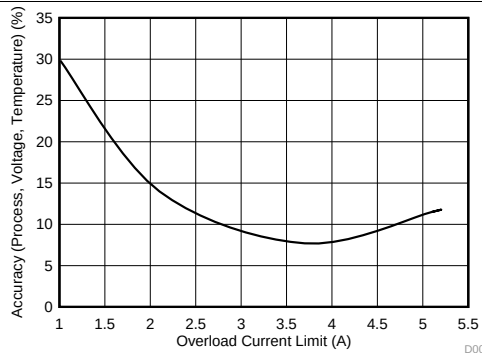


TPS25925x

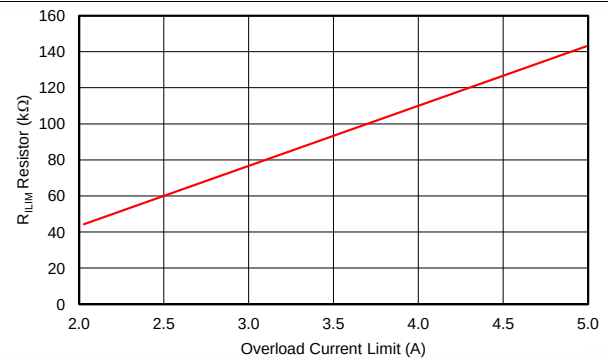
**Figure 6.  $V_{OVC}$  vs Temperature**

## Typical Characteristics (continued)

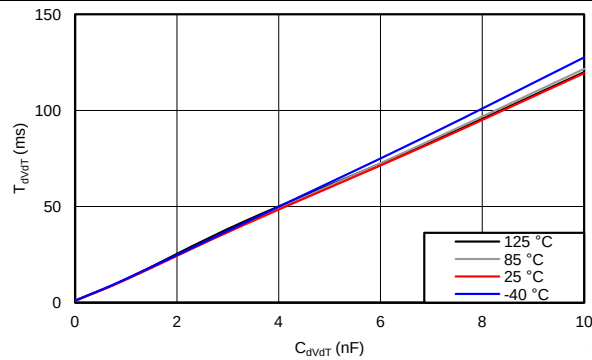
$T_J = 25^\circ\text{C}$ ,  $V_{VIN} = 12\text{ V}$  for TPS25926x,  $V_{VIN} = 5\text{ V}$  for TPS25925x,  $V_{EN/UVLO} = 2\text{ V}$ ,  $R_{ILIM} = 100\text{ k}\Omega$ ,  $C_{VIN} = 0.1\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ ,  $C_{dVdT} = \text{OPEN}$  (unless stated otherwise)



**Figure 7. Accuracy vs Overload Current Limit**

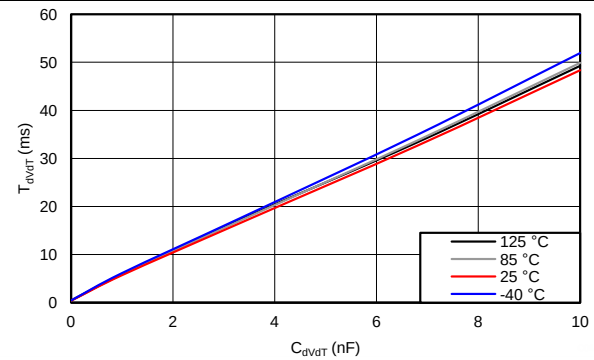


**Figure 8.  $R_{ILIM}$  Resistor vs Overload Current Limit**



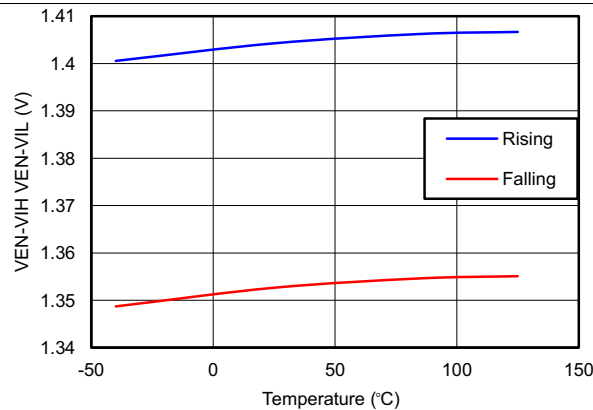
TPS25926x

**Figure 9.  $T_{dVdT}$  vs  $C_{dVdT}$**

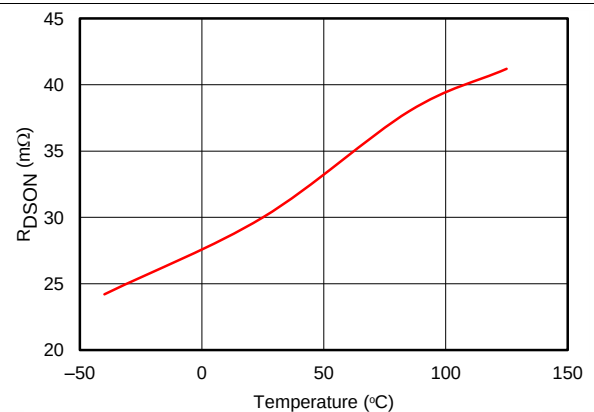


TPS25925x

**Figure 10.  $T_{dVdT}$  vs  $C_{dVdT}$**



**Figure 11.  $V_{EN-VIH}$ ,  $V_{EN-VIL}$  vs Temperature**



**Figure 12.  $R_{DS(on)}$  vs Temperature**



## Typical Characteristics (continued)

$T_J = 25^\circ\text{C}$ ,  $V_{VIN} = 12\text{ V}$  for TPS25926x,  $V_{VIN} = 5\text{ V}$  for TPS25925x,  $V_{EN/UVLO} = 2\text{ V}$ ,  $R_{ILIM} = 100\text{ k}\Omega$ ,  $C_{VIN} = 0.1\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ ,  $C_{dVdT} = \text{OPEN}$  (unless stated otherwise)

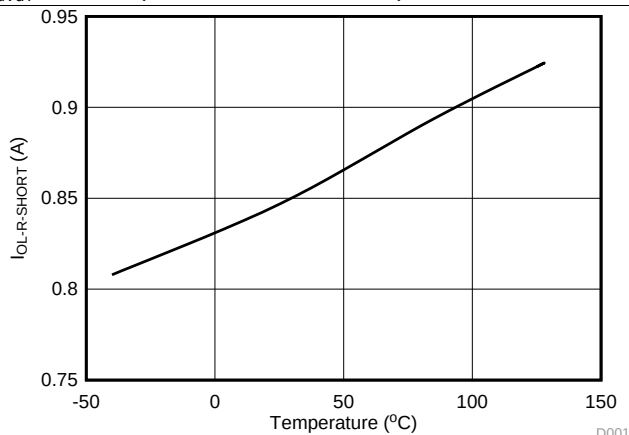


Figure 13.  $I_{OL-R-Short}$  vs Temperature

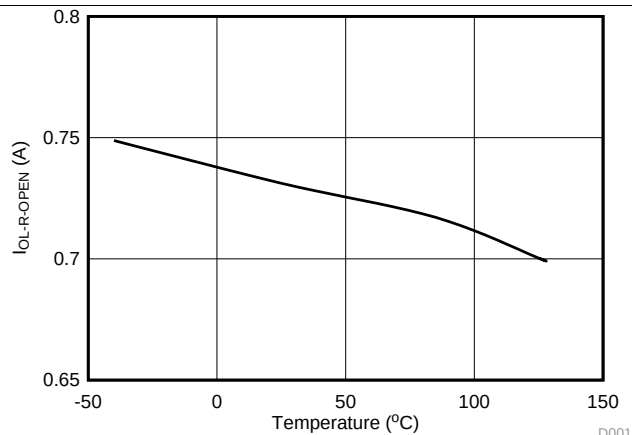


Figure 14.  $I_{OL-R-Open}$  vs Temperature

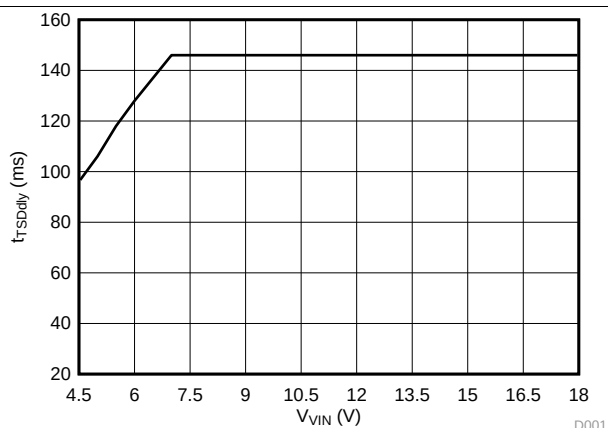


Figure 15. Retry Delay vs  $V_{VIN}$

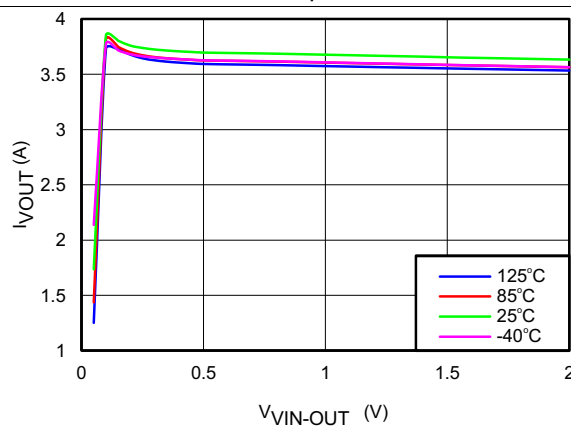


Figure 16.  $I_{OUT}$  vs  $V_{VIN-OUT}$

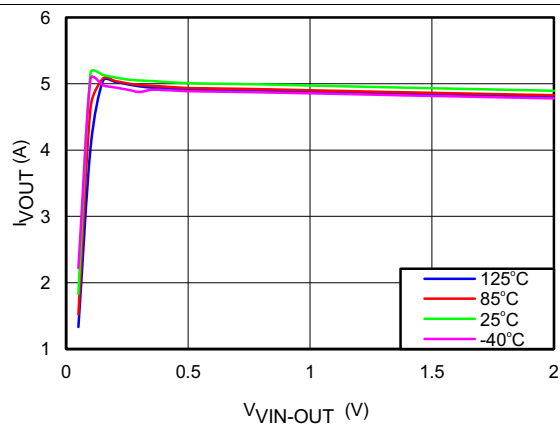


Figure 17.  $I_{OUT}$  vs  $V_{VIN-OUT}$

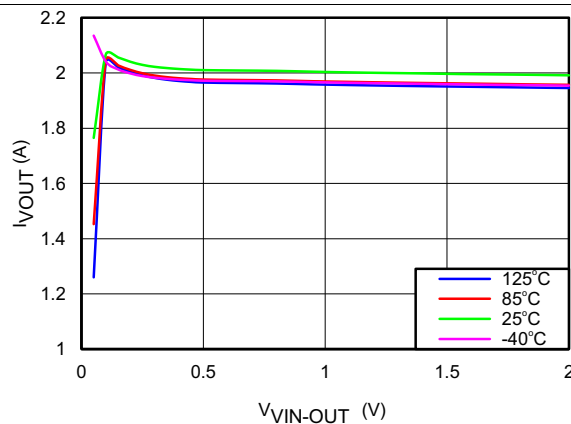
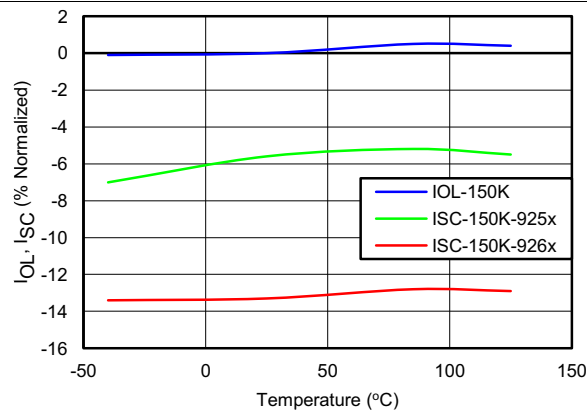


Figure 18.  $I_{OUT}$  vs  $V_{VIN-OUT}$

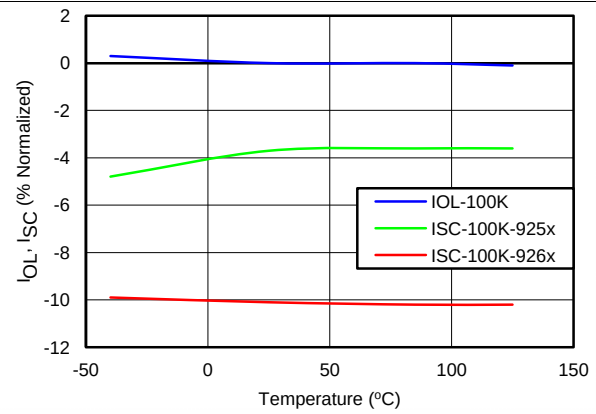
## Typical Characteristics (continued)

$T_J = 25^\circ\text{C}$ ,  $V_{VIN} = 12\text{ V}$  for TPS25926x,  $V_{VIN} = 5\text{ V}$  for TPS25925x,  $V_{EN/UVLO} = 2\text{ V}$ ,  $R_{ILIM} = 100\text{ k}\Omega$ ,  $C_{VIN} = 0.1\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ ,  $C_{dVdT} = \text{OPEN}$  (unless stated otherwise)



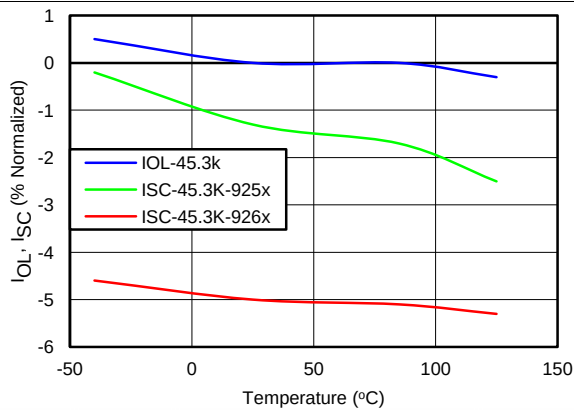
$R_{ILIM} = 150\text{ k}\Omega$

Figure 19.  $I_{OL}$ ,  $I_{SC}$  vs Temperature



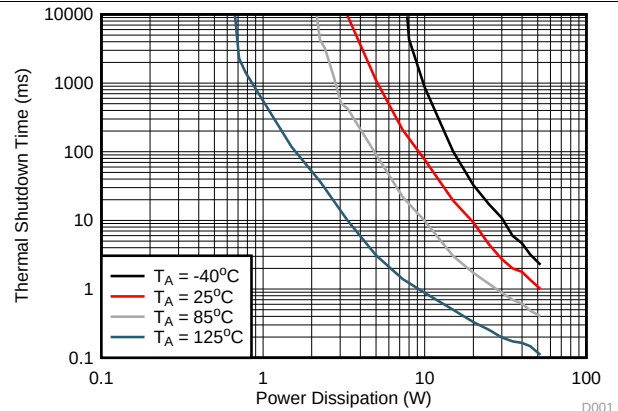
$R_{ILIM} = 100\text{ k}\Omega$

Figure 20.  $I_{OL}$ ,  $I_{SC}$  vs Temperature



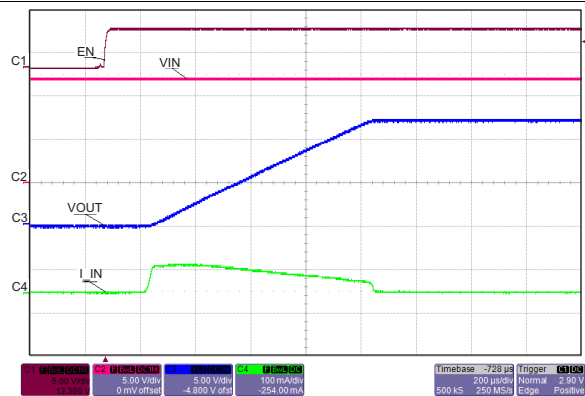
$R_{ILIM} = 45.3\text{ k}\Omega$

Figure 21.  $I_{OL}$ ,  $I_{SC}$  vs Temperature



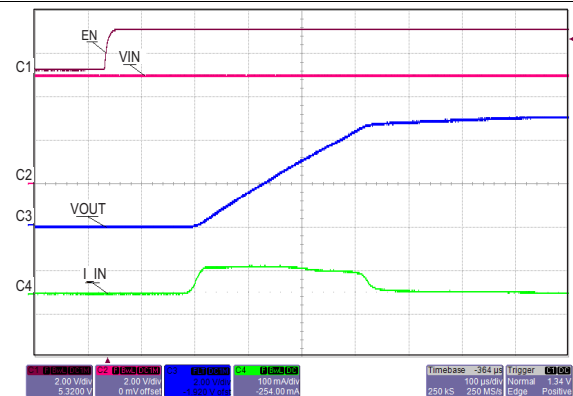
D001

Figure 22. Thermal Shutdown Time vs Power Dissipation



TPS25926x,  $C_{dVdT} = \text{OPEN}$ ,  $C_{OUT} = 4.7\text{ }\mu\text{F}$

Figure 23. Transient: Output Ramp



TPS25925x,  $C_{dVdT} = \text{OPEN}$ ,  $C_{OUT} = 4.7\text{ }\mu\text{F}$

Figure 24. Transient: Output Ramp

## Typical Characteristics (continued)

$T_J = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{ V}$  for TPS25926x,  $V_{IN} = 5\text{ V}$  for TPS25925x,  $V_{EN/UVLO} = 2\text{ V}$ ,  $R_{ILIM} = 100\text{ k}\Omega$ ,  $C_{VIN} = 0.1\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ ,  $C_{dVdT} = \text{OPEN}$  (unless stated otherwise)

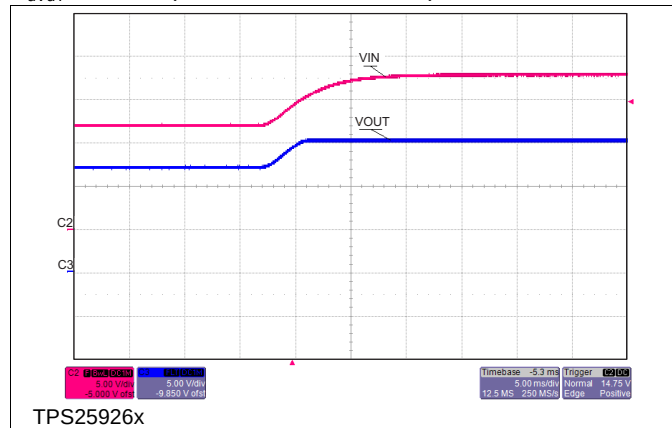


Figure 25. Transient: Over-Voltage Clamp

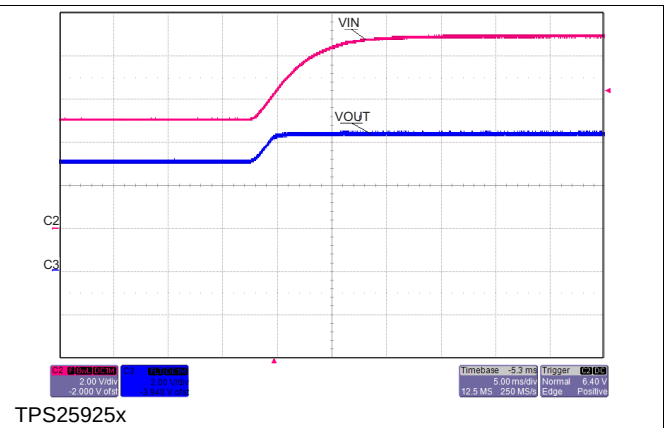


Figure 26. Transient: Over-Voltage Clamp

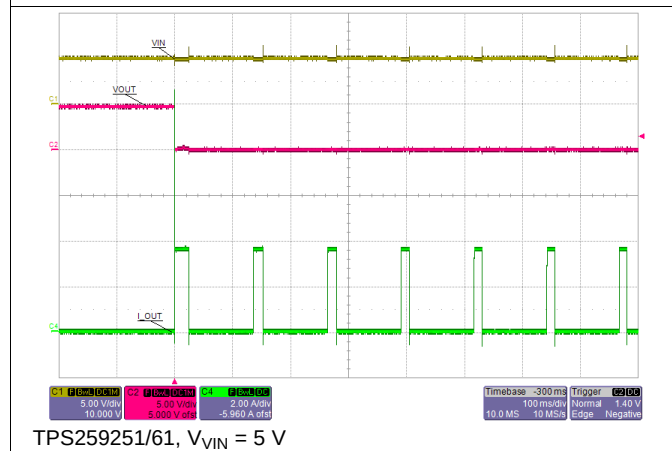


Figure 27. Transient: Thermal Fault Auto-Retry

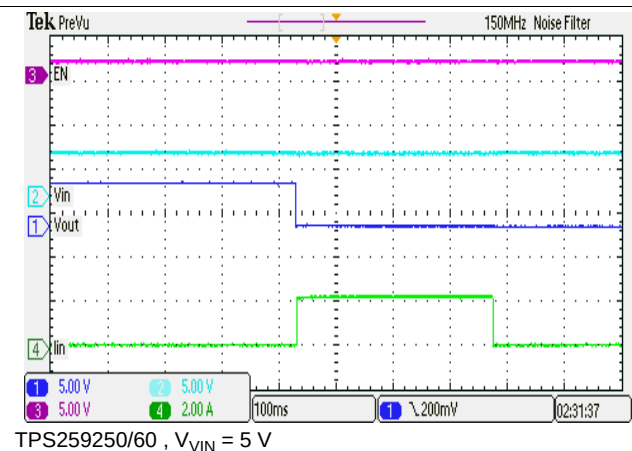


Figure 28. Transient: Thermal Fault Latched

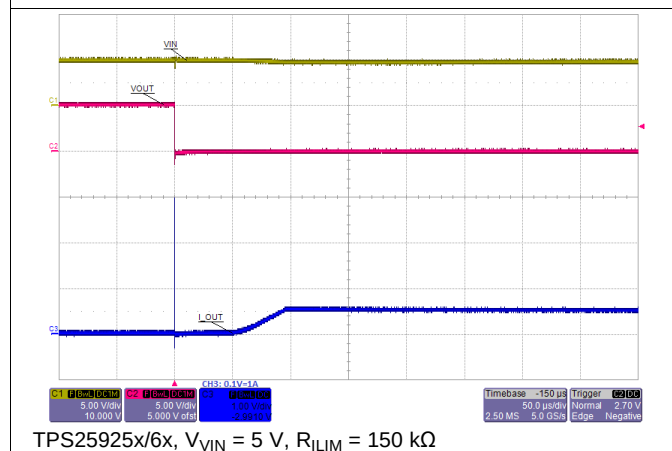


Figure 29. Transient: Output Short Circuit

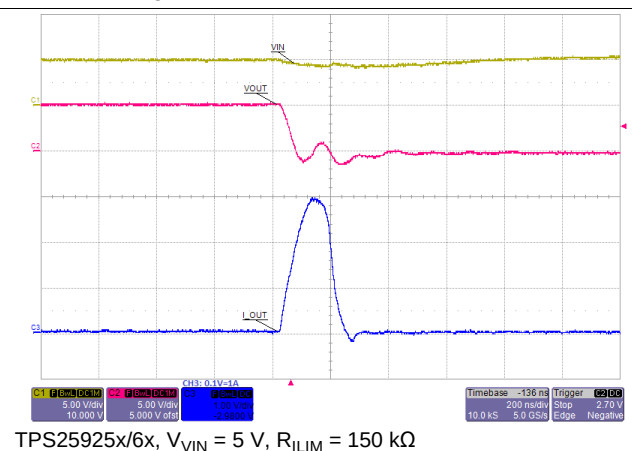
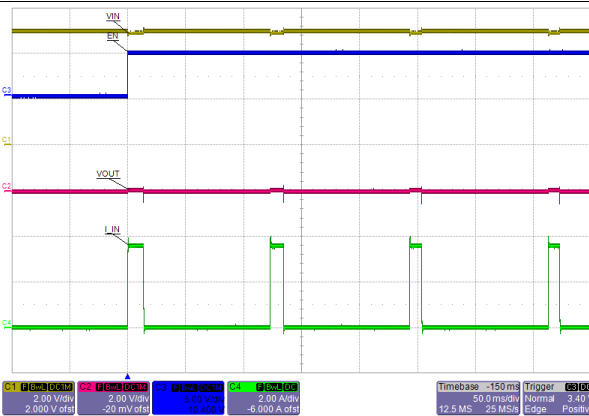


Figure 30. Short Circuit (Zoom): Fast-Trip Comparator

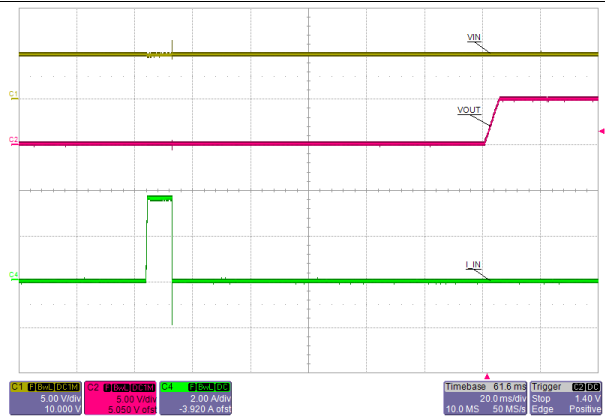
## Typical Characteristics (continued)

$T_J = 25^\circ\text{C}$ ,  $V_{\text{VIN}} = 12\text{ V}$  for TPS25926x,  $V_{\text{VIN}} = 5\text{ V}$  for TPS25925x,  $V_{\text{EN/UVLO}} = 2\text{ V}$ ,  $R_{\text{ILIM}} = 100\text{ k}\Omega$ ,  $C_{\text{VIN}} = 0.1\text{ }\mu\text{F}$ ,  $C_{\text{OUT}} = 1\text{ }\mu\text{F}$ ,  $C_{\text{dVdT}} = \text{OPEN}$  (unless stated otherwise)



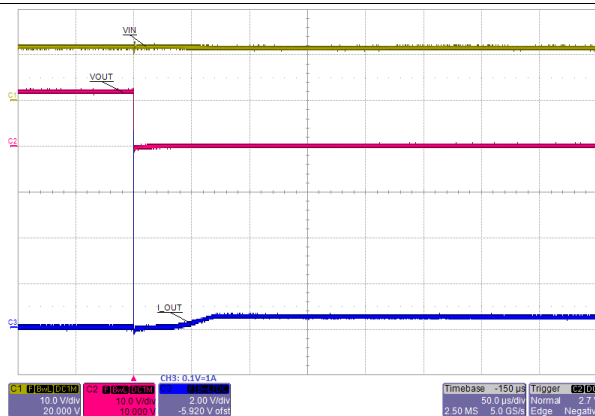
TPS259251/61,  $V_{\text{VIN}} = 5\text{ V}$

**Figure 31. Transient: Wake Up to Short Circuit**



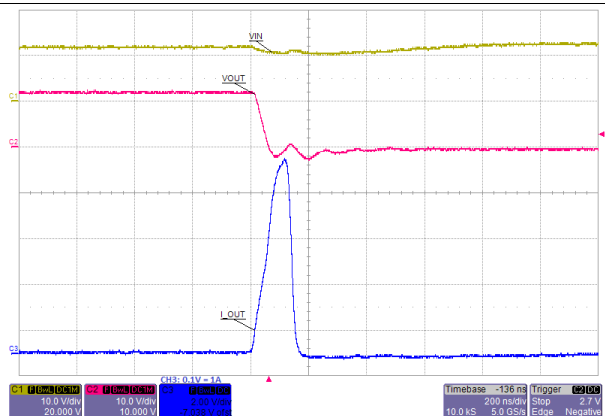
TPS259251/61,  $V_{\text{VIN}} = 5\text{ V}$ ,  $C_{\text{dVdT}} = 1\text{ nF}$

**Figure 32. Transient: Recovery from Short Circuit**



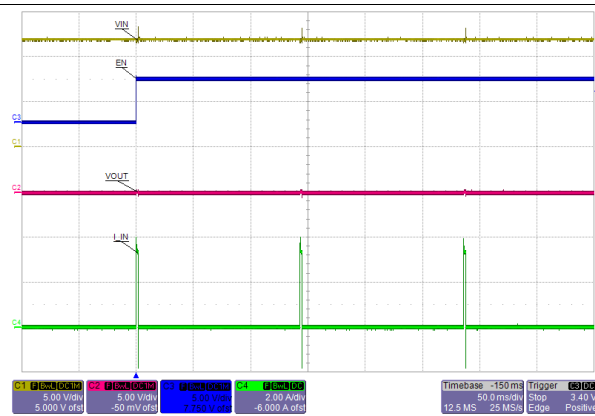
TPS25926x,  $V_{\text{VIN}} = 12\text{ V}$ ,  $R_{\text{ILIM}} = 150\text{ k}\Omega$

**Figure 33. Transient: Output Short Circuit**



TPS25926x,  $V_{\text{VIN}} = 12\text{ V}$ ,  $R_{\text{ILIM}} = 150\text{ k}\Omega$

**Figure 34. Short Circuit (Zoom): Fast-Trip Comparator**



TPS25926x,  $V_{\text{VIN}} = 12\text{ V}$

**Figure 35. Transient: Wake Up to Short Circuit**

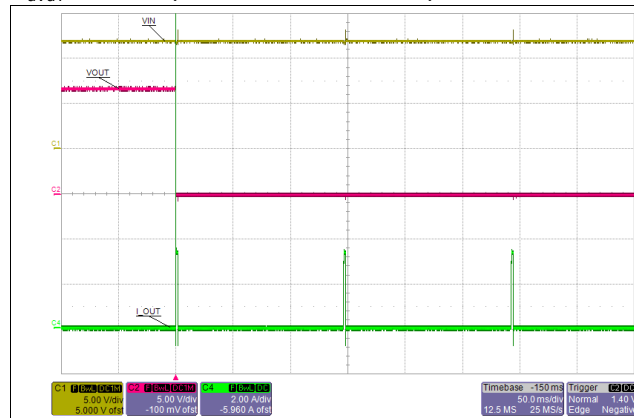


TPS25926x,  $V_{\text{VIN}} = 12\text{ V}$ ,  $C_{\text{dVdT}} = 1\text{ nF}$

**Figure 36. Transient: Recovery from Short Circuit**

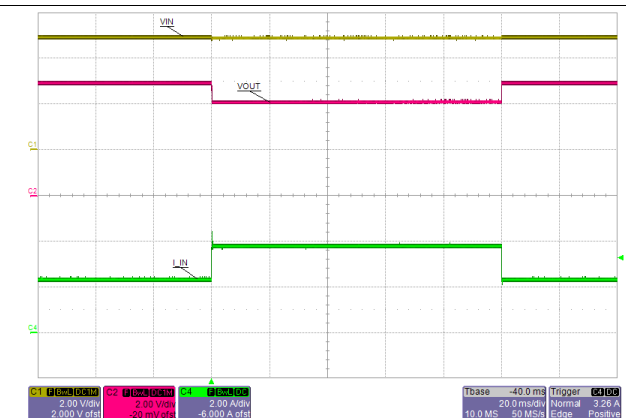
## Typical Characteristics (continued)

$T_J = 25^\circ\text{C}$ ,  $V_{VIN} = 12\text{ V}$  for TPS25926x,  $V_{VIN} = 5\text{ V}$  for TPS25925x,  $V_{EN/UVLO} = 2\text{ V}$ ,  $R_{ILIM} = 100\text{ k}\Omega$ ,  $C_{VIN} = 0.1\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ ,  $C_{dVdT} = \text{OPEN}$  (unless stated otherwise)



TPS25926x,  $V_{VIN} = 12\text{ V}$

**Figure 37. Transient: Thermal Fault Auto-Retry**



$I_{LOAD}$  stepped From 65% to 125%, back to 65%

**Figure 38. Transient: Overload Current Limit**

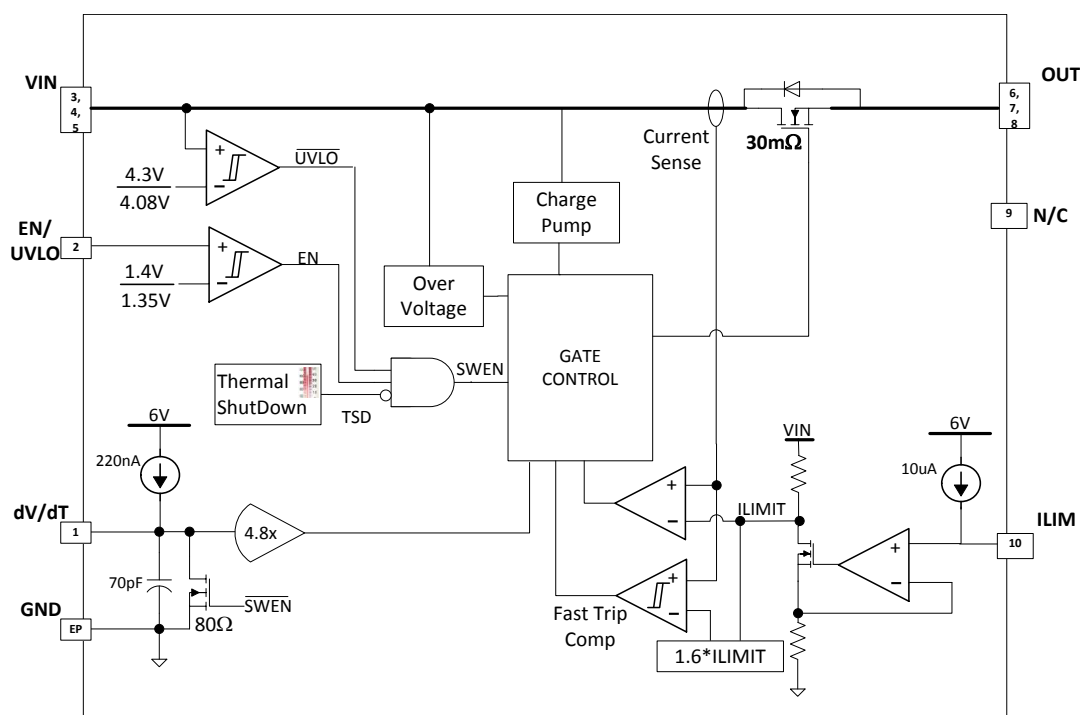
## 8 Detailed Description

### 8.1 Overview

The TPS25925x/6x is an e-fuse with integrated power switch that is used to manage current/voltage/start-up voltage ramp to a connected load. The device starts its operation by monitoring the VIN bus. When VIN exceeds the undervoltage-lockout threshold ( $V_{UVLO}$ ), the device samples the EN/UVLO pin. A high level on this pin enables the internal MOSFET. As VIN rises, the internal MOSFET of the device will start conducting and allow current to flow from VIN to OUT. When EN/UVLO is held low (below  $V_{ENF}$ ), internal MOSFET is turned off. User also has the ability to modify the output voltage ramp time by connecting a capacitor between dV/dT pin and GND.

After a successful start-up sequence, the device now actively monitors its load current and input voltage, ensuring that the adjustable overload current limit IOL is not exceeded and input voltage spikes are safely clamped to VOVC level at the output. This keeps the output device safe from harmful voltage and current transients. The device also has built-in thermal sensor. In the event device temperature ( $T_J$ ) exceeds TSHDN, typically 150°C, the thermal shutdown circuitry will shut down the internal MOSFET thereby disconnecting the load from the supply. In TPS259250/60, the output will remain disconnected (MOSFET open) until power to device is recycled or EN/UVLO is toggled (pulled low and then high). The TPS259251/61 device will remain off and commences an auto-retry cycle of 145 ms after device temperature falls below  $T_{SHDN} - 10^\circ\text{C}$ . This auto-retry cycle will continue until the fault is cleared.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 GND

This is the most negative voltage in the circuit and is used as a reference for all voltage measurements unless otherwise specified.

## Feature Description (continued)

### 8.3.2 VIN

Input voltage to the TPS25925x/6x. A ceramic bypass capacitor close to the device from VIN to GND is recommended to alleviate bus transients. The recommended operating voltage range is 4.5 V – 13.8 V for TPS25926x and 4.5 V – 5.5 V for TPS25925x. The device can continuously sustain a voltage of 20 V on VIN pin. However, above the recommended maximum bus voltage, the device is in over-voltage protection (OVP) mode, limiting the output voltage to  $V_{OVC}$ . The power dissipation in OVP mode is  $P_{D\_OVP} = (V_{VIN} - V_{OVC}) \times I_{OUT}$ , which can potentially heat up the device and cause thermal shutdown.

### 8.3.3 dV/dT

Connect a capacitor from this pin to GND to control the slew rate of the output voltage at power-on. This pin can be left floating to obtain a predetermined slew rate (minimum  $T_{dVdT}$ ) on the output. Governing slew rate at start-up is shown in [Equation 1](#).

$$\frac{dV_{OUT}}{dt} = \frac{I_{dVdT} \times GAIN_{dVdT}}{C_{dVdT} + C_{INT}} \quad (1)$$

Where:

$$I_{dVdT} = 220 \text{ nA (TYP)}$$

$$C_{INT} = 70 \text{ pF (TYP)}$$

$$GAIN_{dVdT} = 4.85$$

$$\frac{dV_{OUT}}{dT} = \text{Desired output slew rate}$$

The total ramp time ( $T_{dVdT}$ ) for 0 to VIN can be calculated using the following equation:

$$T_{dVdT} = 10^6 \times V_{IN} \times (C_{dVdT} + 70 \text{ pF}) \quad (2)$$

For details on how to select an appropriate charging time/rate, refer to the applications section [Setting Output Voltage Ramp Time \( \$T\_{dVdT}\$ \)](#).

### 8.3.4 EN/UVLO

As an input pin, it controls both the ON/OFF state of the internal MOSFET and that of the external blocking FET. In its high state, the internal MOSFET is enabled and charging begins for the gate of external FET. A low on this pin turns off the internal MOSFET and pull the gate of the external FET to GND via the built-in discharge resistor. High and Low levels are specified in the parametric table of the datasheet. The EN/UVLO pin is also used to clear a thermal shutdown latch in the TPS259250/60 by toggling this pin (H→L).

The internal de-glitch delay on EN/UVLO falling edge is intentionally kept low (1  $\mu$ s typical) for quick detection of power failure. For applications where a higher de-glitch delay on EN/UVLO is desired, or when the supply is particularly noisy, it is recommended to use an external bypass capacitor from EN/UVLO to GND.

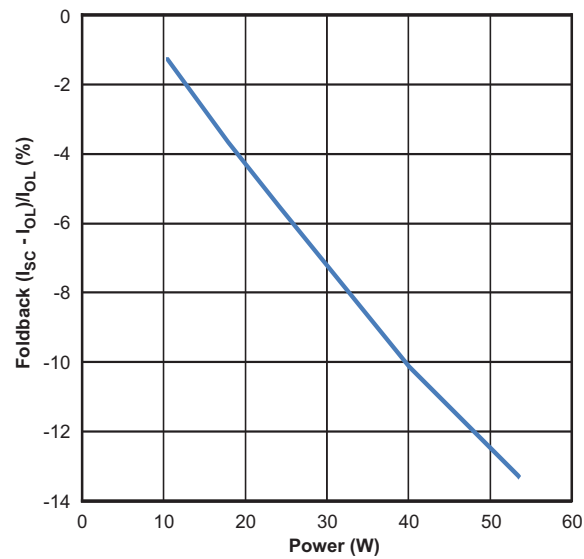
### 8.3.5 ILIM

The device continuously monitors the load current and keeps it limited to the value programmed by  $R_{ILIM}$ . After start-up event and during normal operation, current limit is set to  $I_{OL}$  (over-load current limit).

$$I_{OL} = (0.7 + 3 \times 10^{-5} \times R_{ILIM}) \quad (3)$$

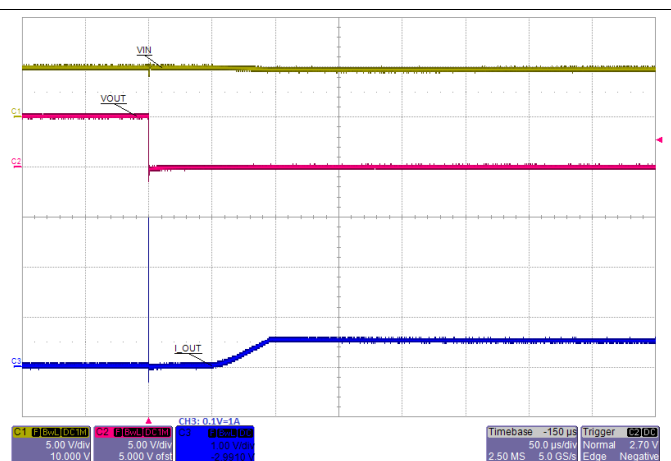
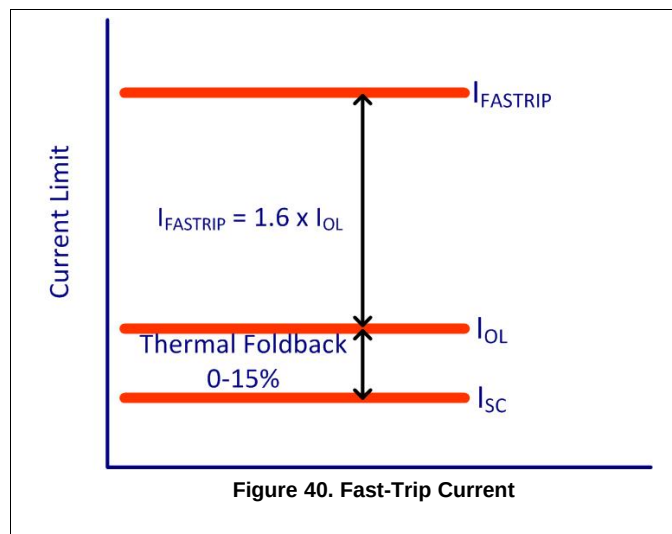
When power dissipation in the internal MOSFET [ $P_D = (V_{VIN} - V_{OUT}) \times I_{OUT}$ ] exceeds 10 W, there is a 2% – 12% thermal foldback in the current limit value so that  $I_{OL}$  drops to  $I_{SC}$ . In each of the two modes, MOSFET gate voltage is regulated to throttle short-circuit and overload current flowing to the load. Eventually, the device shuts down due to over temperature.

## Feature Description (continued)



**Figure 39. Thermal Foldback in Current Limit**

During a transient short circuit event, the current through the device increases very rapidly. The current-limit amplifier cannot respond to this event due to its limited bandwidth. Therefore, the TPS25925/6 incorporates a fast-trip comparator, which shuts down the pass device when  $I_{OUT} > I_{FASTrip}$ , and terminates the rapid short-circuit peak current. The trip threshold is set to 60% higher than the programmed over-load current limit ( $I_{FASTrip} = 1.6 \times I_{OL}$ ). After the transient short-circuit peak current has been terminated by the fast-trip comparator, the current limit amplifier smoothly regulates the output current to  $I_{OL}$  (see Figure 40).





## 8.4 Device Functional Modes

The TPS25925x/6x is a hot-swap controller with integrated power switch that is used to manage current/voltage/start-up voltage ramp to a connected load. The device starts its operation by monitoring the VIN bus. When  $V_{VIN}$  exceeds the undervoltage-lockout threshold ( $V_{UVL}$ ), the device samples the EN/UVLO pin. A high level on this pin enables the internal MOSFET. As VIN rises, the internal MOSFET of the device and external FET (if connected) starts conducting and allows current to flow from VIN to OUT. When EN/UVLO is held low (that is, below  $V_{ENF}$ ), the internal MOSFET is turned off; thereby, blocking the flow of current from VIN to OUT. The user can modify the output voltage ramp time by connecting a capacitor between dV/dT pin and GND.

Having successfully completed its start-up sequence, the device now actively monitors the load current and input voltage, ensuring that the adjustable overload current limit  $I_{OL}$  is not exceeded and input voltage spikes are safely clamped to  $V_{OVC}$  level at the output. This keeps the output device safe from harmful voltage and current transients. The device also has built-in thermal sensor. If the device temperature ( $T_J$ ) exceeds  $T_{SHDN}$ , typically 150°C, the thermal shutdown circuitry shuts down the internal MOSFET; thereby, disconnecting the load from the supply. In the TPS259250/60, the output remains disconnected (MOSFET open) until power to device is recycled or EN/UVLO is toggled (pulled low and then high). The TPS259251/61 device will remain off and commences an auto-retry cycle of 145 ms after device temperature falls below  $T_{SHDN} - 10^\circ\text{C}$ . This auto-retry cycle will continue until the fault is cleared.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TPA25925x/6x is a smart eFuse. It is typically used for Hot-Swap and Power rail protection applications. It operates from 4.5 V to 18 V with programmable current limit and undervoltage protection. The device aids in controlling the in-rush current and provides precise current limiting during overload conditions for systems such as Set-Top-Box, DTVs, Gaming Consoles, SSDs/HDDs and Smart Meters. The device also provides robust protection for multiple faults on the sub-system rail.

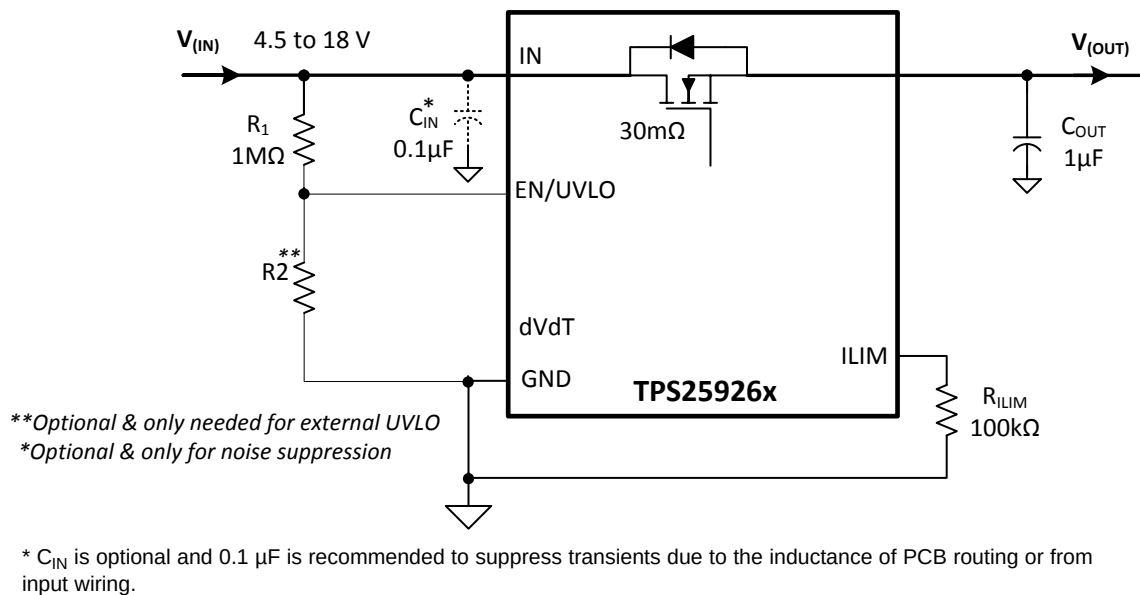
The following design procedure can be used to select component values for the device.

Alternatively, the WEBENCH® software may be used to generate a complete design. The WEBENCH® software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. Additionally, a spreadsheet design tool *TPS2592xx Design Calculator* ([SLUC570](#)) is available on web folder.

This section presents a simplified discussion of the design process.

### 9.2 Typical Application

#### 9.2.1 Simple eFuse Protection for Set Top Boxes



**Figure 42. Typical Application Schematic: Simple e-Fuse for STBs**

#### 9.2.1.1 Design Requirements

**Table 1. Design Parameters**

| DESIGN PARAMETER                             | EXAMPLE VALUE              |
|----------------------------------------------|----------------------------|
| Input voltage range, $V_{IN}$                | 12 V                       |
| Undervoltage lockout set point, $V_{(UV)}$   | Default: $V_{UVR} = 4.3$ V |
| Overvoltage protection set point, $V_{(OV)}$ | Default: $V_{OVC} = 15$ V  |

## Typical Application (continued)

**Table 1. Design Parameters (continued)**

| DESIGN PARAMETER                    | EXAMPLE VALUE |
|-------------------------------------|---------------|
| Load at start-up, $R_{L(SU)}$       | 4 $\Omega$    |
| Current limit, $I_{OL}$             | 3.7 A         |
| Load capacitance, $C_{OUT}$         | 1 $\mu$ F     |
| Maximum ambient temperatures, $T_A$ | 85°C          |

### 9.2.1.2 Detailed Design Procedure

The following design procedure can be used to select component values for the TPS25926x.

#### 9.2.1.2.1 Step by Step Design Procedure

To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- Normal input operation voltage
- Maximum output capacitance
- Maximum current Limit
- Load during start-up
- Maximum ambient temperature of operation

This design procedure below seeks to control the junction temperature of device under both static and transient conditions by proper selection of output ramp-up time and associated support components. The designer can adjust this procedure to fit the application and design criteria.

#### 9.2.1.2.2 Programming the Current-Limit Threshold: $R_{ILIM}$ Selection

The  $R_{ILIM}$  resistor at the ILIM pin sets the over load current limit, this can be set using [Equation 4](#).

$$R_{ILIM} = \frac{I_{ILIM} - 0.7}{3 \times 10^{-5}} \quad (4)$$

For  $I_{ILIM} = 3.7$  A, from [Equation 4](#),  $R_{ILIM}$  is 100 k $\Omega$ , choose closest standard value resistor with 1% tolerance.

#### 9.2.1.2.3 Undervoltage Lockout Set Point

The undervoltage lockout (UVLO) trip point is adjusted using the external voltage divider network of  $R_1$  and  $R_2$  as connected between IN, EN/UVLO and GND pins of the device. The values required for setting the undervoltage are calculated solving [Equation 5](#).

$$V_{(UV)} = \frac{R_1 + R_2}{R_2} \times V_{ENR} \quad (5)$$

Where  $V_{ENR}$  is enable voltage rising threshold (1.4 V). Since  $R_1$  and  $R_2$  will leak the current from input supply ( $V_{in}$ ), these resistors should be selected based on the acceptable leakage current from input power supply ( $V_{in}$ ).

The current drawn by  $R_1$  and  $R_2$  from the power supply  $\{I_{(R12)} = V_{(IN)}/(R_1 + R_2)\}$ .

However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current,  $I_{(R12)}$  must be chosen to be 20x greater than the leakage current expected.

For default UVLO of  $V_{UVR} = 4.3$  V, select  $R_2 = \text{OPEN}$ , and  $R_1 = 1$  M $\Omega$ . Since EN/UVLO pin is rated only to 7 V, it cannot be connected directly to  $V_{IN} = 12$  V. It has to be connected through  $R_1 = 1$  M $\Omega$  only, so that the pull-up current for EN/UVLO pin is limited to < 20  $\mu$ A.

The power failure threshold is detected on the falling edge of supply. This threshold voltage is 4% lower than the rising threshold,  $V_{UVR}$ . This is calculated using [Equation 6](#).

$$V_{(PFAIL)} = 0.96 \times V_{UVR} \quad (6)$$

Where  $V_{UVR}$  is 4.3 V, Power fail threshold set is : 4.1 V.

#### 9.2.1.2.4 Setting Output Voltage Ramp Time ( $T_{dVdT}$ )

For a successful design, the junction temperature of device should be kept below the absolute-maximum rating during both dynamic (start-up) and steady state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and in-rush current limit required with system capacitance to avoid thermal shutdown during start-up with and without load.

The ramp-up capacitor  $C_{dVdT}$  needed is calculated considering the two possible cases.

##### 9.2.1.2.4.1 Case 1: Start-Up without Load: Only Output Capacitance $C_{OUT}$ Draws Current During Start-Up

During start-up, as the output capacitor charges, the voltage difference as well as the power dissipated across the internal FET decreases. The average power dissipated in the device during start-up is calculated using [Equation 8](#).

For TPS25926x device, the inrush current is determined as,

$$I_{(INRUSH)} = C_{(OUT)} \times \frac{V_{(IN)}}{T_{dVdT}} \quad (7)$$

Power dissipation during start-up is:

$$P_{D(INRUSH)} = 0.5 \times V_{(IN)} \times I_{(INRUSH)} \quad (8)$$

[Equation 8](#) assumes that load does not draw any current until the output voltage has reached its final value.

##### 9.2.1.2.4.2 Case 2: Start-Up with Load: Output Capacitance $C_{OUT}$ and Load Draws Current During Start-Up

When load draws current during the turn-on sequence, there will be additional power dissipated. Considering a resistive load during start-up ( $R_{L(SU)}$ ), load current ramps up proportionally with increase in output voltage during  $T_{dVdT}$  time. The average power dissipation in the internal FET during charging time due to resistive load is given by:

$$P_{D(LOAD)} = \left( \frac{1}{6} \right) \times \frac{V_{(IN)}^2}{R_{L(SU)}} \quad (9)$$

Total power dissipated in the device during startup is:

$$P_{D(STARTUP)} = P_{D(INRUSH)} + P_{D(LOAD)} \quad (10)$$

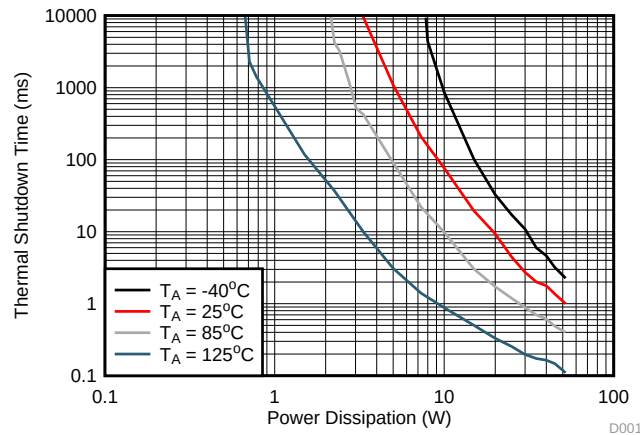
Total current during startup is given by:

$$I_{(STARTUP)} = I_{(INRUSH)} + I_L(t) \quad (11)$$

If  $I_{(STARTUP)} > I_{OL}$ , the device limits the current to  $I_{OL}$  and the current limited charging time is determined by:

$$T_{dVdT(Current-Limited)} = C_{OUT} \times R_{L(SU)} \times \left[ \frac{I_{OL}}{I_{(INRUSH)}} - 1 + \ln \left( \frac{I_{(INRUSH)}}{I_{OL} - \frac{V_{(IN)}}{R_{L(SU)}}} \right) \right] \quad (12)$$

The power dissipation, with and without load, for selected start-up time should not exceed the shutdown limits as shown in [Figure 43](#):



**Figure 43. Thermal Shutdown Limit Plot**

For the design example under discussion, select ramp-up capacitor  $C_{dVdT}$  = OPEN. Then, using Equation 2:

$$T_{dVdT} = 10^6 \times 12 \times (0 + 70 \text{ pF}) = 840 \text{ } \mu\text{s} \quad (13)$$

The inrush current drawn by the load capacitance ( $C_{OUT}$ ) during ramp-up using Equation 14:

$$I_{(INRUSH)} = 1 \text{ } \mu\text{F} \times \frac{12}{840 \text{ } \mu\text{s}} = 15 \text{ mA} \quad (14)$$

The inrush power dissipation is calculated using Equation 15:

$$P_{D(INRUSH)} = 0.5 \times 12 \times 15 \text{ m} = 90 \text{ mW} \quad (15)$$

For 90 mW of power loss, the thermal shut down time of the device should not be less than the ramp-up time  $T_{dVdT}$  to avoid the false trip at maximum operating temperature. From thermal shutdown limit graph Figure 43 at  $T_A = 85^\circ\text{C}$ , for 90 mW of power, the shutdown time is infinite. So it is safe to use 0.79 ms as start-up time without any load on output.

Considering the start-up with load  $4 \text{ } \Omega$ , the additional power dissipation, when load is present during start up is calculated using Equation 9:

$$P_{D(LOAD)} = \frac{12 \times 12}{6 \times 4} = 6 \text{ W} \quad (16)$$

The total device power dissipation during start up is:

$$P_{D(STARTUP)} = 6 + 90 \text{ m} = 6.09 \text{ W} \quad (17)$$

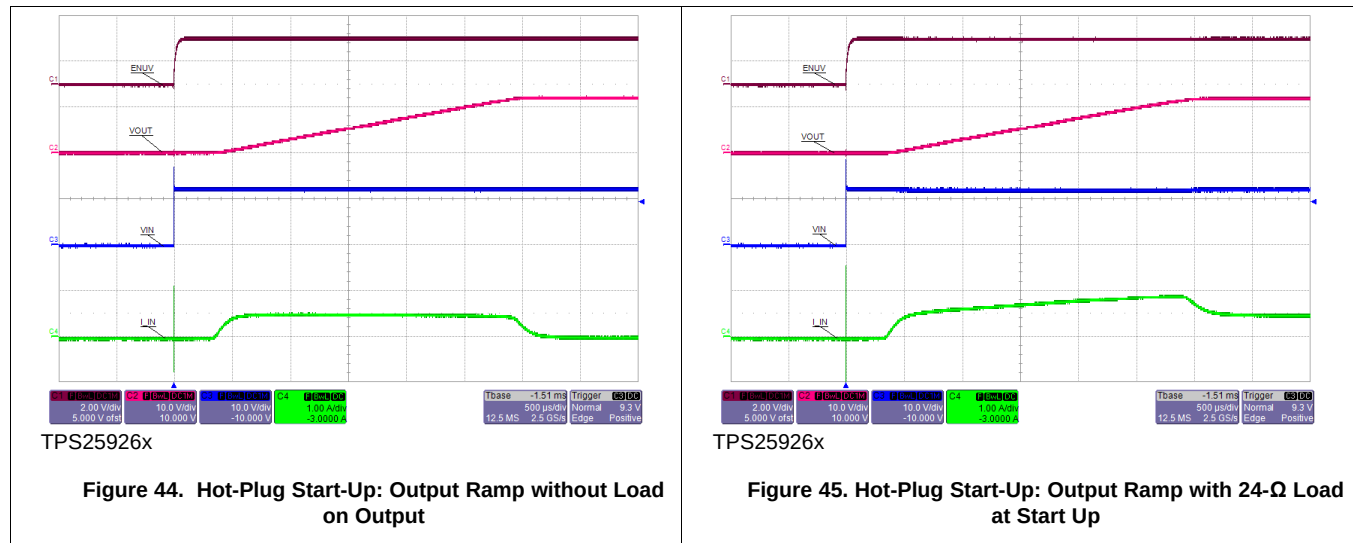
From thermal shutdown limit graph at  $T_A = 85^\circ\text{C}$ , the thermal shutdown time for 6.09 W is more than 10 ms. So it is well within acceptable limits to use no external capacitor ( $C_{dVdT}$ ) with start-up load of  $4 \text{ } \Omega$ .

If, due to large  $C_{OUT}$ , there is a need to decrease the power loss during start-up, it can be done with increase of  $C_{dVdT}$  capacitor.

#### 9.2.1.2.5 Support Component Selection - $C_{VIN}$

$C_{VIN}$  is a bypass capacitor to help control transient voltages, unit emissions, and local supply noise. Where acceptable, a value in the range of  $0.001 \text{ } \mu\text{F}$  to  $0.1 \text{ } \mu\text{F}$  is recommended for  $C_{VIN}$ .

### 9.2.1.3 Application Curves



## 10 Power Supply Recommendations

The device is designed for supply voltage range of  $4.5\text{ V} \leq V_{\text{IN}} \leq 18\text{ V}$ . If the input supply is located more than a few inches from the device an input ceramic bypass capacitor higher than  $0.1\text{ }\mu\text{F}$  is recommended. Power supply should be rated higher than the current limit set to avoid voltage droops during over current and short-circuit conditions.

### 10.1 Transient Protection

In case of short circuit and over load current limit, when the device interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on value of inductance in series to the input or output of the device. Such transients can exceed the [Absolute Maximum Ratings](#) of the device if steps are not taken to address the issue.

Typical methods for addressing transients include:

- Minimizing lead length and inductance into and out of the device
- Using large PCB GND plane
- Schottky diode across the output to absorb negative spikes
- A low value ceramic capacitor ( $C_{\text{IN}} = 0.001\text{ }\mu\text{F}$  to  $0.1\text{ }\mu\text{F}$ ) to absorb the energy and dampen the transients. The approximate value of input capacitance can be estimated with [Equation 18](#):

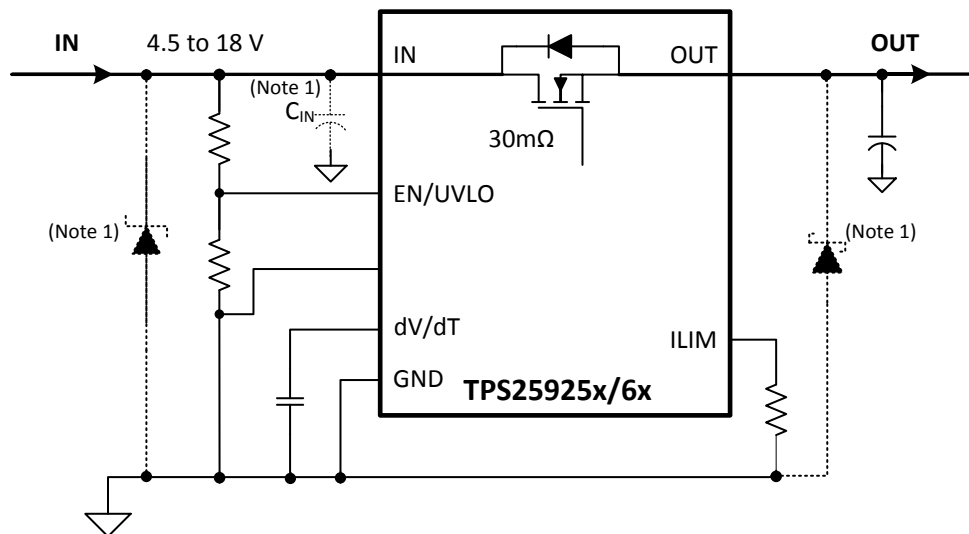
$$V_{\text{SPIKE(Absolute)}} = V_{\text{(IN)}} + I_{\text{(LOAD)}} \times \sqrt{\frac{L_{\text{(IN)}}}{C_{\text{(IN)}}}} \quad (18)$$

Where:

- $V_{\text{(IN)}}$  is the nominal supply voltage
- $I_{\text{(LOAD)}}$  is the load current
- $L_{\text{(IN)}}$  equals the effective inductance seen looking into the source
- $C_{\text{(IN)}}$  is the capacitance present at the input

Some applications may require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the [Absolute Maximum Ratings](#) of the device.

The circuit implementation with optional protection components (a ceramic capacitor, TVS and schottky diode) is shown in [Figure 46](#).



(1) Optional components needed for suppression of transients

**Figure 46. Circuit Implementation with Optional Protection Components**

## 10.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. Source bypassing, input leads, circuit layout and component selection, output shorting method, relative location of the short, and instrumentation all contribute to variation in results. The actual short itself exhibits a certain degree of randomness as it microscopically bounces and arcs. Care in configuration and methods must be used to obtain realistic results. Do not expect to see waveforms exactly like those in the data sheet; every setup differs.

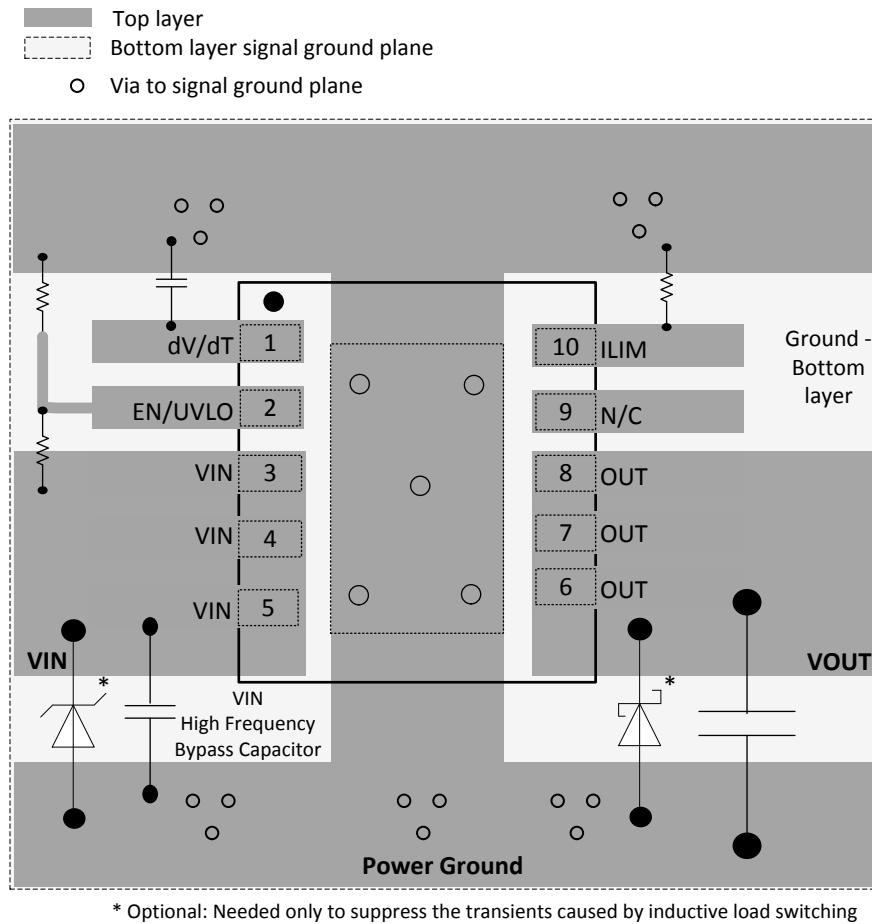
## 11 Layout

### 11.1 Layout Guidelines

- For all applications, a 0.01- $\mu$ F or greater ceramic decoupling capacitor is recommended between IN terminal and GND. For hot-plug applications, where input power path inductance is negligible, this capacitor can be eliminated/minimized.
- The optimum placement of decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC. See [Figure 47](#) for a PCB layout example.
- High current carrying power path connections should be as short as possible and should be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC. The PCB ground should be a copper plane or island on the board.
- Locate all TPS25925x/6x support components:  $R_{ILIM}$ ,  $C_{dVdT}$  and resistors for ENUV, close to their connection pin. Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the  $R_{ILIM}$  and  $C_{dVdT}$  components to the device should be as short as possible to reduce parasitic effects on the current limit and soft start timing. These traces should not have any coupling to switching signals on the board.
- Protection devices such as TVS, snubbers, capacitors, or diodes should be placed physically close to the device they are intended to protect, and routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it should be physically close to the OUT pins.
- Obtaining acceptable performance with alternate layout schemes is possible; however this layout has been shown to produce good results and is intended as a guideline.



## 11.2 Layout Example



**Figure 47. Layout Example**

## 12 器件和文档支持

### 12.1 器件支持

#### 12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

### 12.2 文档支持

#### 12.2.1 相关文档

《TPS2592xx 设计计算器》（文献编号：SLUC570）

### 12.3 相关链接

以下表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 2. 相关链接

| 器件        | 产品文件夹                 | 样片与购买                 | 技术文档                  | 工具与软件                 | 支持与社区                 |
|-----------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| TPS259250 | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> |
| TPS259251 | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> |
| TPS259260 | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> |
| TPS259261 | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> |

### 12.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.5 商标

E2E is a trademark of Texas Instruments.

### 12.6 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS259250DRCR    | ACTIVE        | VSON         | DRC                | 10   | 3000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | 259250                  | <a href="#">Samples</a> |
| TPS259250DRCT    | ACTIVE        | VSON         | DRC                | 10   | 250            | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | 259250                  | <a href="#">Samples</a> |
| TPS259251DRCR    | ACTIVE        | VSON         | DRC                | 10   | 3000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | 259251                  | <a href="#">Samples</a> |
| TPS259251DRCT    | ACTIVE        | VSON         | DRC                | 10   | 250            | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | 259251                  | <a href="#">Samples</a> |
| TPS259260DRCR    | ACTIVE        | VSON         | DRC                | 10   | 3000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | 259260                  | <a href="#">Samples</a> |
| TPS259260DRCT    | ACTIVE        | VSON         | DRC                | 10   | 250            | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | 259260                  | <a href="#">Samples</a> |
| TPS259261DRCR    | ACTIVE        | VSON         | DRC                | 10   | 3000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | 259261                  | <a href="#">Samples</a> |
| TPS259261DRCT    | ACTIVE        | VSON         | DRC                | 10   | 250            | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | 259261                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

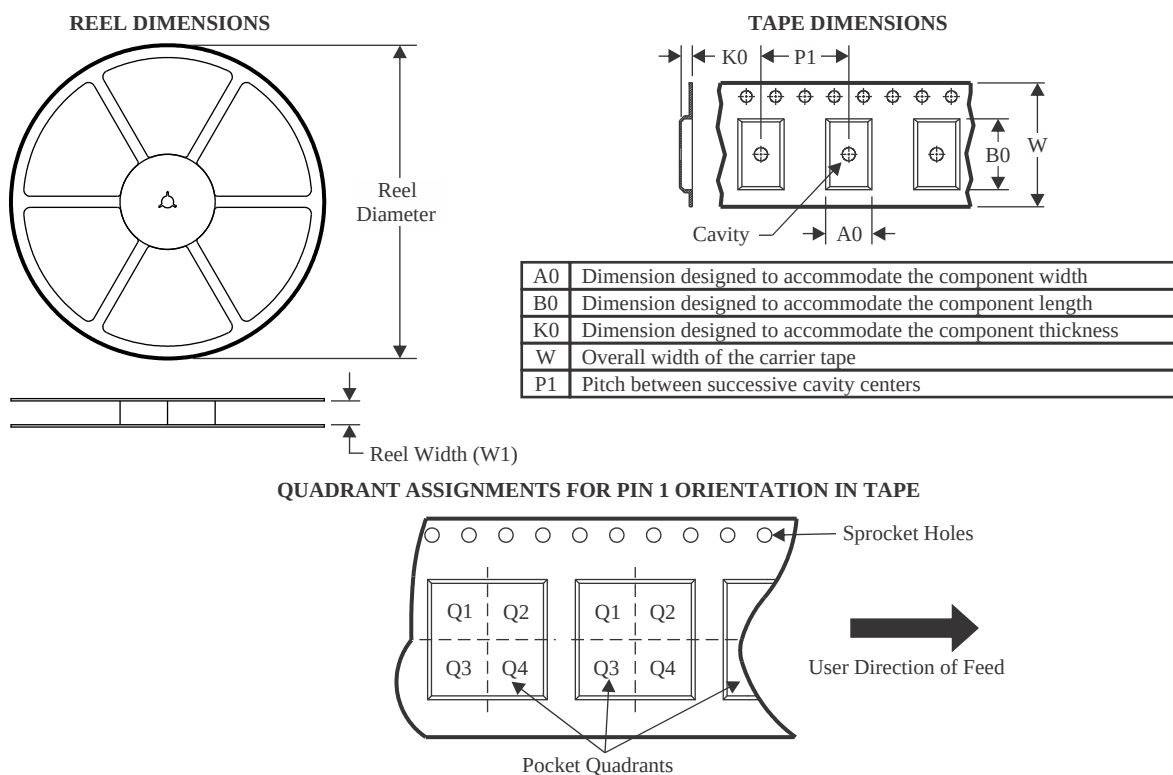
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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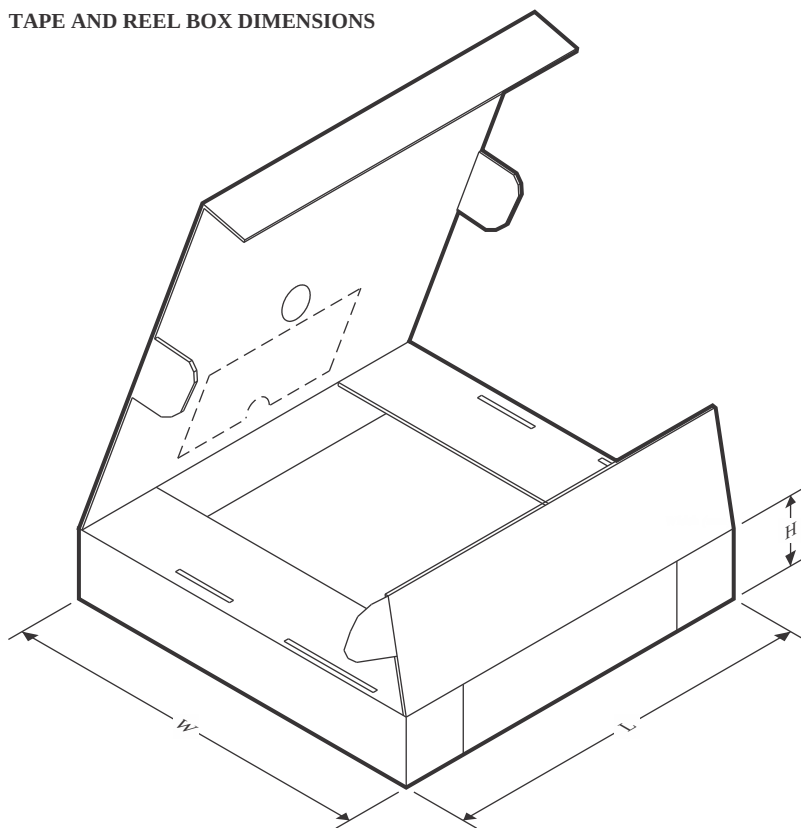
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS259250DRCR | VSON         | DRC             | 10   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPS259250DRCT | VSON         | DRC             | 10   | 250  | 180.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPS259251DRCR | VSON         | DRC             | 10   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPS259251DRCR | VSON         | DRC             | 10   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPS259251DRCT | VSON         | DRC             | 10   | 250  | 180.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPS259251DRCT | VSON         | DRC             | 10   | 250  | 180.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPS259260DRCR | VSON         | DRC             | 10   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPS259260DRCT | VSON         | DRC             | 10   | 250  | 180.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPS259261DRCR | VSON         | DRC             | 10   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPS259261DRCR | VSON         | DRC             | 10   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPS259261DRCT | VSON         | DRC             | 10   | 250  | 180.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPS259261DRCT | VSON         | DRC             | 10   | 250  | 180.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS259250DRCR | VSON         | DRC             | 10   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS259250DRCT | VSON         | DRC             | 10   | 250  | 210.0       | 185.0      | 35.0        |
| TPS259251DRCR | VSON         | DRC             | 10   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS259251DRCR | VSON         | DRC             | 10   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS259251DRCT | VSON         | DRC             | 10   | 250  | 210.0       | 185.0      | 35.0        |
| TPS259251DRCT | VSON         | DRC             | 10   | 250  | 210.0       | 185.0      | 35.0        |
| TPS259260DRCR | VSON         | DRC             | 10   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS259260DRCT | VSON         | DRC             | 10   | 250  | 210.0       | 185.0      | 35.0        |
| TPS259261DRCR | VSON         | DRC             | 10   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS259261DRCR | VSON         | DRC             | 10   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS259261DRCT | VSON         | DRC             | 10   | 250  | 210.0       | 185.0      | 35.0        |
| TPS259261DRCT | VSON         | DRC             | 10   | 250  | 210.0       | 185.0      | 35.0        |

## GENERIC PACKAGE VIEW

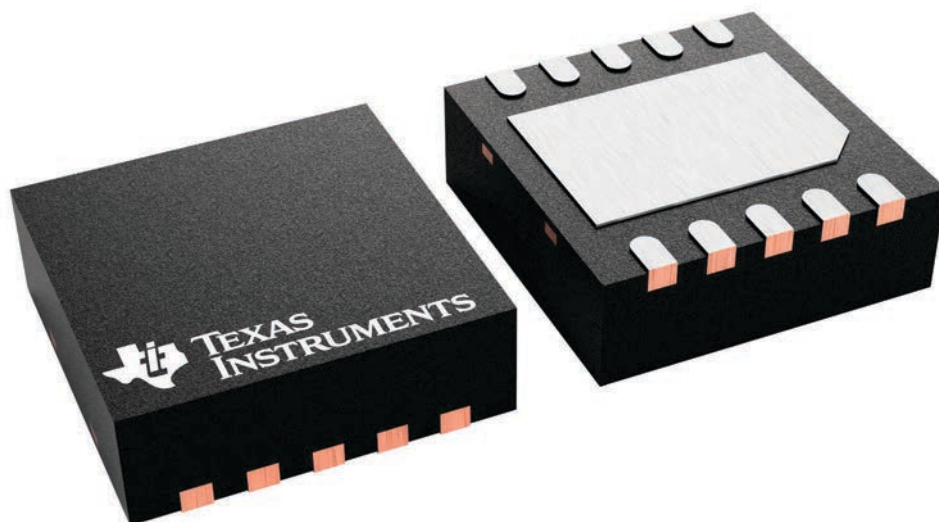
**DRC 10**

**VSON - 1 mm max height**

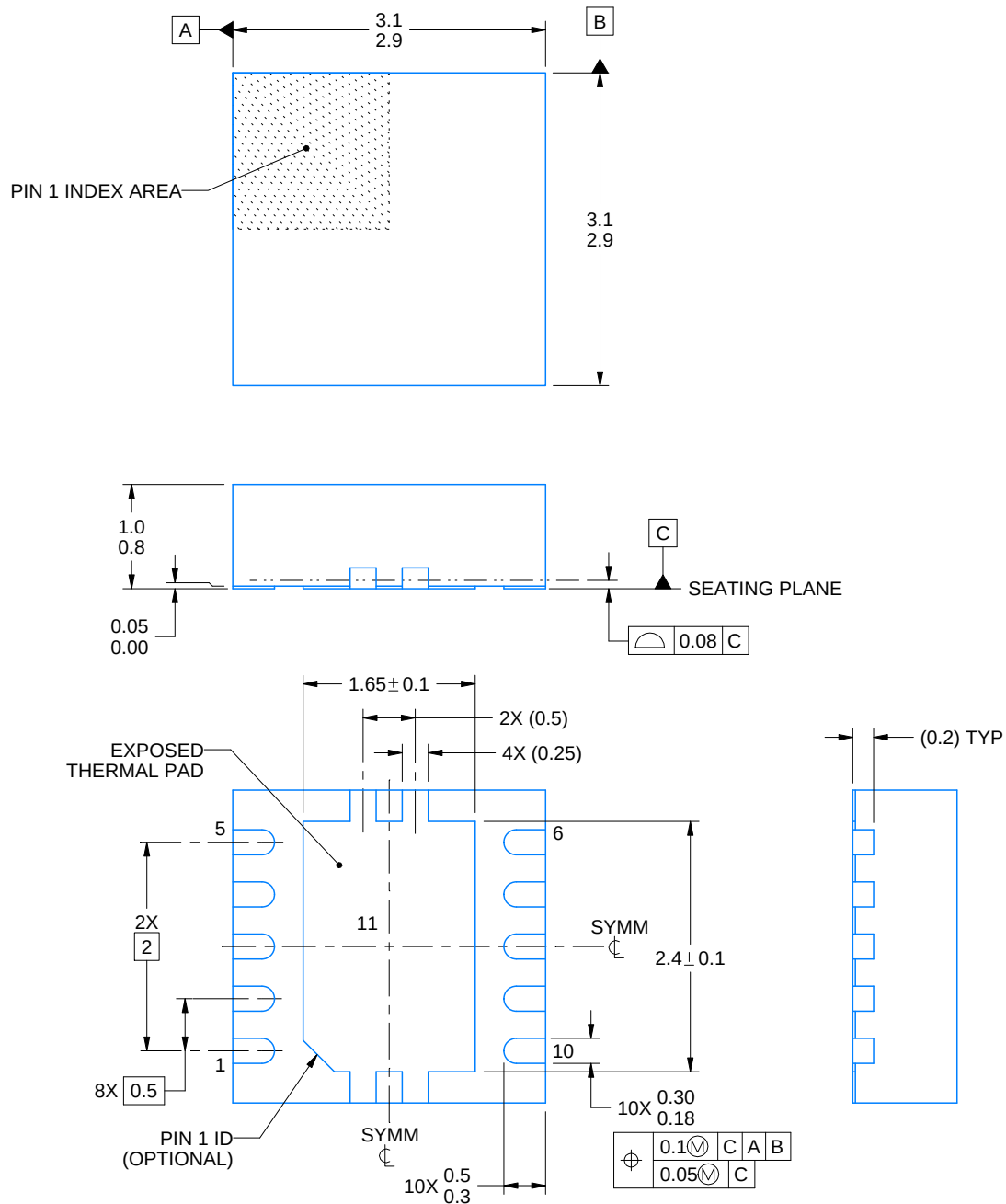
3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



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## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

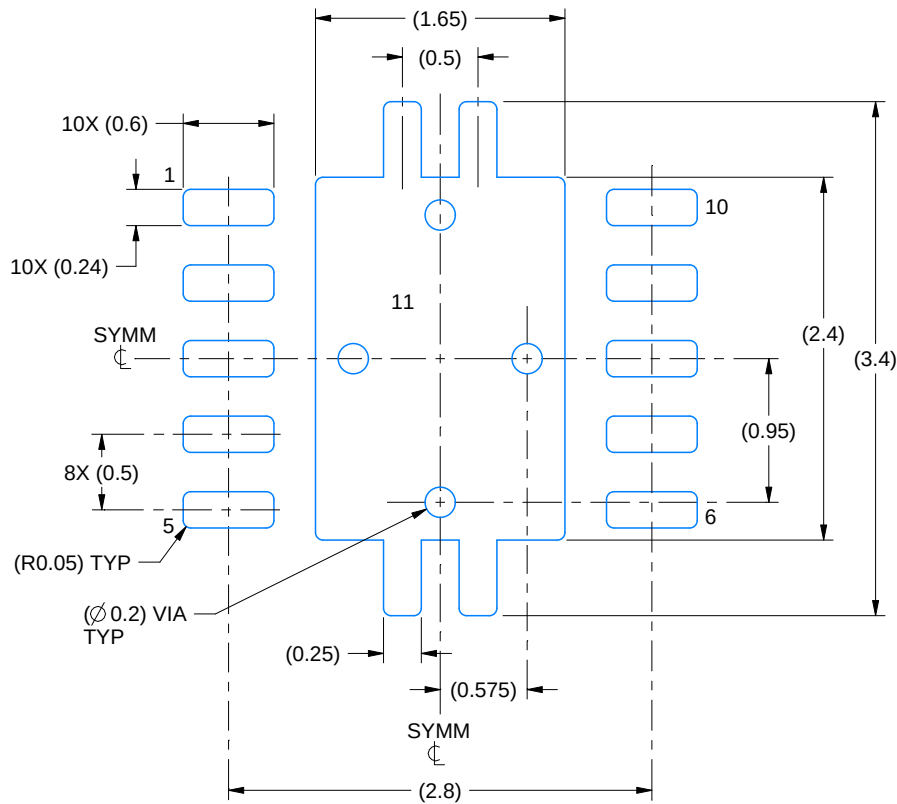


# EXAMPLE BOARD LAYOUT

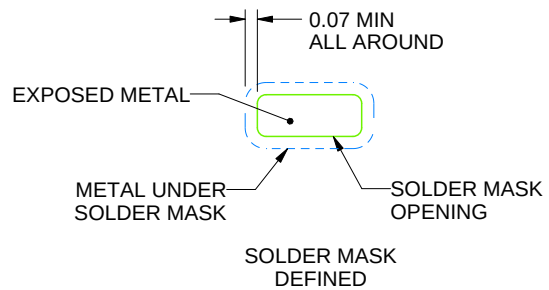
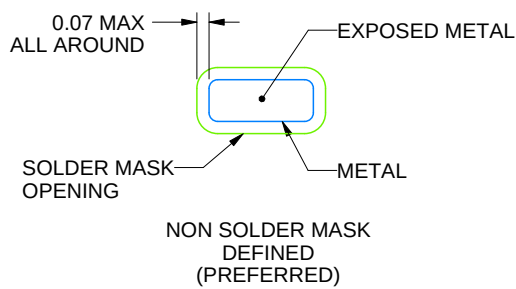
DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



**LAND PATTERN EXAMPLE**  
EXPOSED METAL SHOWN  
SCALE:20X



**SOLDER MASK DETAILS**

4218878/B 07/2018

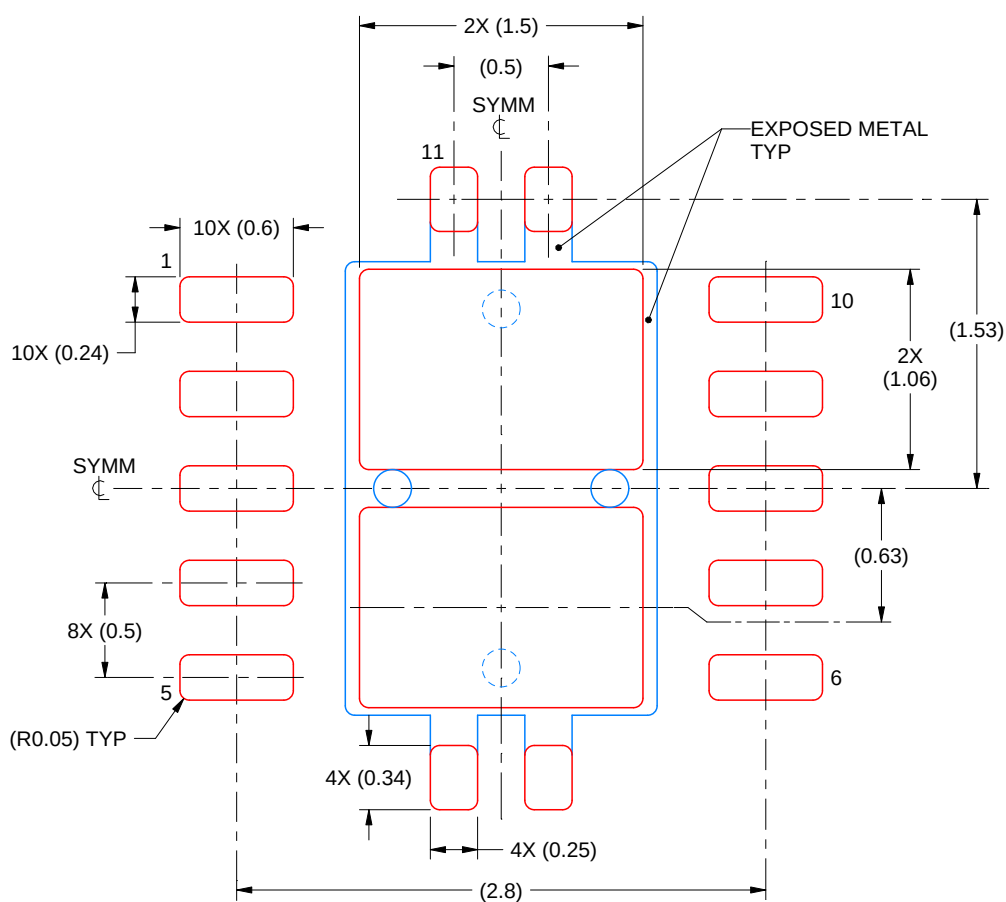
NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

**DRC0010J**

**VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



## SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:  
80% PRINTED SOLDER COVERAGE BY AREA  
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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