

**ANALOG
DEVICES**

± 15 kV ESD Protected, 3.3 V Single-Channel RS-232 Line Driver/Receiver

ADM3101E

FEATURES

460 kbps data rate
1 Tx and 1 Rx
Meets EIA/TIA-232E specifications
0.1 μ F charge pump capacitors
Contact discharge: ± 8 kV
Air gap discharge: ± 15 kV

APPLICATIONS

General-purpose RS-232 data links
Industrial/telecommunications diagnostics ports

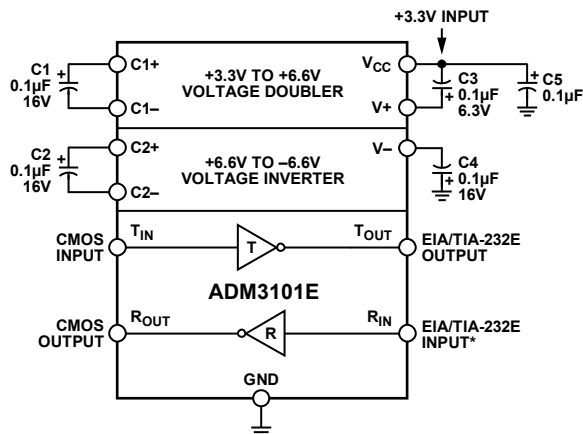
GENERAL DESCRIPTION

The ADM3101E is a high speed, single-channel, RS-232/ITU-T V.28 transceiver interface device that operates from a single 3.3 V power supply. Low power consumption makes it ideal for battery-powered portable instruments.

The ADM3101E conforms to the EIA/TIA-232E and ITU-T V.28 specifications and operates at data rates of up to 460 kbps.

All RS-232 (T_{OUT} and R_{IN}) and CMOS (T_{IN} and R_{OUT}) inputs and outputs are protected against electrostatic discharges (up to ± 15 kV ESD protection).

FUNCTIONAL BLOCK DIAGRAM



*INTERNAL 5k Ω PULL-DOWN
RESISTOR ON THE RS-232 INPUT.

Figure 1.

Because of the ± 15 kV ESD protection of the ADM3101E input/output pins, this device is ideally suited for operation in electrically harsh environments or where RS-232 cables are frequently plugged and unplugged.

Four external 0.1 μ F charge pump capacitors are used for the voltage doubler/inverter permitting operation from a single 3.3 V supply.

The ADM3101E is available in both a 12-lead LFCSP and 16-lead QSOP, specified over the -40°C to $+85^{\circ}\text{C}$ temperature range.

Rev. C

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
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REVISION HISTORY

7/08—Rev. B to Rev. C

Changes to General Description Section	1
Reformatted Table 1	4
Change to T_{IN} Rating, Table 2	4
Changes to Figure 2	5
Moved High Baud Rate Section	8
Added Exposed Pad Notation to Outline Dimensions	9

12/07—Rev. A to Rev. B

Added 16-lead QSOP Package (Universal)	1
Updated Outline Dimensions	10
Changes to Ordering Guide	10

10/07—Rev. 0 to Rev. A

Changes to Figure 1	1
Changes to Table 1, RS-232 Receiver Section	3
Changes to Table 3	5
Changes to Figure 11	8

5/07—Revision 0: Initial Version

SPECIFICATIONS

$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $C1$ to $C4 = 0.1 \text{ }\mu\text{F}$, $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DC CHARACTERISTICS					
Operating Voltage Range	No load R _L = 3 kΩ to GND	3.0	3.3	5.5	V
Power Supply Current, V _{CC}			1.5	2.6	mA
			5	7	mA
LOGIC					
Input Logic Threshold Low, V _{INL}	T _{IN}			0.6	V
Input Logic Threshold High, V _{INH}	T _{IN}	1.4			V
Input Logic Threshold Low, V _{INL}	T _{IN} , V _{CC} = 5.0 V ± 0.5 V			0.8	V
Input Logic Threshold High, V _{INH}	T _{IN} , V _{CC} = 5.0 V ± 0.5 V	2.0			V
CMOS Output Voltage Low, V _{OL}	I _{OUT} = 1.6 mA			0.4	V
CMOS Output Voltage High, V _{OH}	I _{OUT} = −1 mA	V _{CC} − 0.6			V
Logic Pull-Up Current	T _{IN} = GND to V _{CC}		5	12	μA
RS-232 RECEIVER					
EIA/TIA-232E Input Voltage Range ¹	V _{CC} = 3.0 V to 5.5 V	−30		+30	V
EIA/TIA-232E Input Threshold Low		0.6	1.3		V
EIA/TIA-232E Input Threshold High			1.6	2.4	V
EIA/TIA-232E Input Hysteresis			0.4		V
EIA/TIA-232E Input Resistance		3	5	7	kΩ
TRANSMITTER					
Output Voltage Swing	V _{CC} = 3.3 V to 5.5 V; transmitter output loaded with 3 kΩ to ground V _{CC} = 3.0 V V _{CC} = 0 V, V _{OUT} = ±2 V ¹	±5.0	±5.7		V
RS-232					
RS-562		±4.5			V
Transmitter Output Resistance		300			Ω
RS-232 Output Short-Circuit Current				±15	mA
TIMING CHARACTERISTICS					
Maximum Data Rate	V _{CC} = 3.3 V, R _L = 3 kΩ to 7 kΩ, C _L = 50 pF to 1000 pF	460			kbps
Receiver Propagation Delay					
t _{PHL}			0.4		μs
t _{PLH}	R _L = 3 kΩ, C _L = 1000 pF		0.4		μs
Transmitter Propagation Delay			600		ns
Transmitter Skew			80		ns
Receiver Skew			70		ns
Transition Region Slew Rate		+3 V to −3 V or −3 V to +3 V, V _{CC} = +3.3 V, R _L = 3 kΩ, C _L = 1000 pF, T _A = 25°C ¹	5.5	10	30
ESD PROTECTION					
RS-232 and CMOS I/O Pins	Human body model air discharge		±15		kV
	Human body model contact discharge		±8		kV

¹ Guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Rating
V_{CC}	−0.3 V to +6 V
V_+	$(V_{CC} - 0.3 \text{ V})$ to +13 V
V_-	+0.3 V to −13 V
Input Voltages	
T_{IN}	−0.3 V to $(V_{CC} + 0.3 \text{ V})$
R_{IN}	±30 V
Output Voltages	
T_{OUT}	±15 V
R_{OUT}	−0.3 V to $(V_{CC} + 0.3 \text{ V})$
Short-Circuit Duration	
T_{OUT}	Continuous
Package Information	
θ_{JA} , Thermal Impedance (LFCSP)	61.1°C/W
θ_{JA} , Thermal Impedance (QSOP)	149.97°C/W
Operating Temperature Range	
Industrial (A Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Pb-Free Temperature (Soldering, 10 sec)	260°C

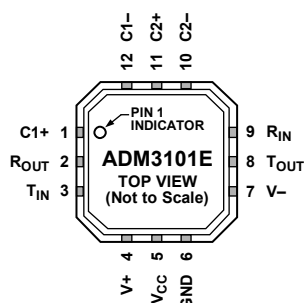
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

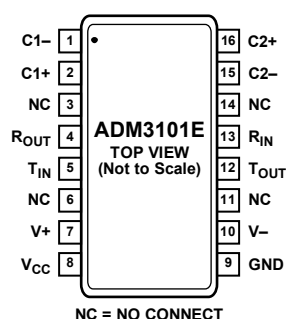
PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. PADDLE CONNECTED TO GND. THIS CONNECTION IS NOT REQUIRED TO MEET THE ELECTRICAL PERFORMANCES.

06766-002

Figure 2. LFCSP Pin Configuration



NC = NO CONNECT

06766-014

Figure 3. QSOP Pin Configuration

Table 3. Pin Function Descriptions

Pin No.		Mnemonic	Description
LFCSP	QSOP		
1, 12	2, 1	C1+, C1–	Positive and Negative Connections for Charge Pump Capacitor. External Capacitor C1 is connected between these pins; a 0.1 μF capacitor is recommended, but larger capacitors up to 10 μF can be used.
2	4	R _{OUT}	Receiver Output. This pin outputs CMOS output logic levels.
3	5	T _{IN}	Transmitter (Driver) Input. This input accepts TTL/CMOS levels.
4	7	V+	Internally Generated Positive Supply (+6 V Nominal).
5	8	V _{CC}	Power Supply Input, 3.0 V to 5.5 V.
6	9	GND	Ground. Must be connected to 0 V.
7	10	V–	Internally Generated Negative Supply (–6 V Nominal).
8	12	T _{OUT}	Transmitter (Driver) Output. This pin outputs RS-232 signal levels (typically $\pm 6\text{ V}$).
9	13	R _{IN}	Receiver Input. This input accepts RS-232 signal levels. An internal 5 k Ω pull-down resistor to GND is connected on the input.
10, 11	15, 16	C2–, C2+	Positive and Negative Connections for Charge Pump Capacitor. External Capacitor C2 is connected between these pins; a 0.1 μF capacitor is recommended, but larger capacitors up to 10 μF can be used.
N/A	3, 6, 11, 14	NC	No Connect. These pins should always remain unconnected.

TYPICAL PERFORMANCE CHARACTERISTICS

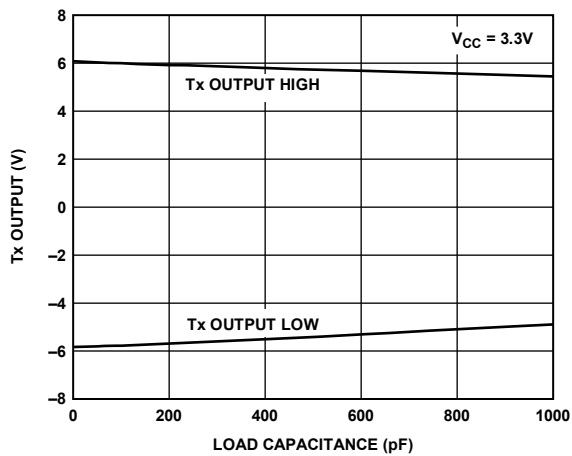


Figure 4. Transmitter Output Voltage High/Low vs. Load Capacitance @ 460 kbps

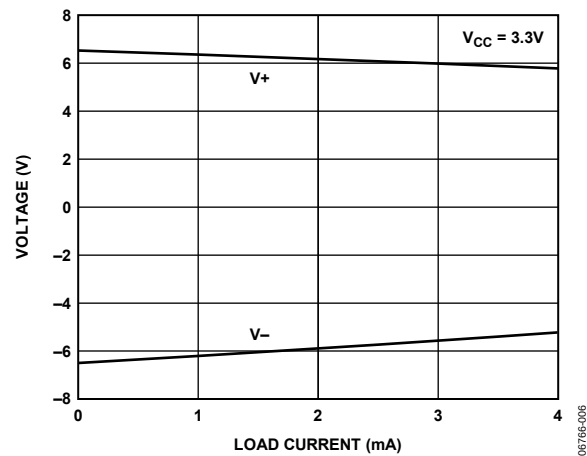


Figure 7. Charge Pump V+, V- vs. Load Current

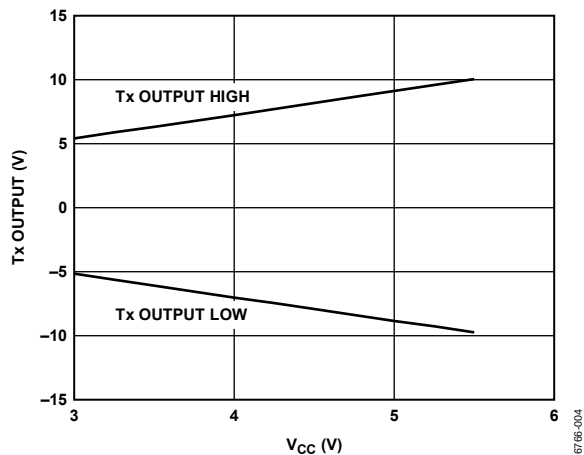


Figure 5. Transmitter Output Voltage High/Low vs. V_{CC} , $R_L = 3\text{ k}\Omega$

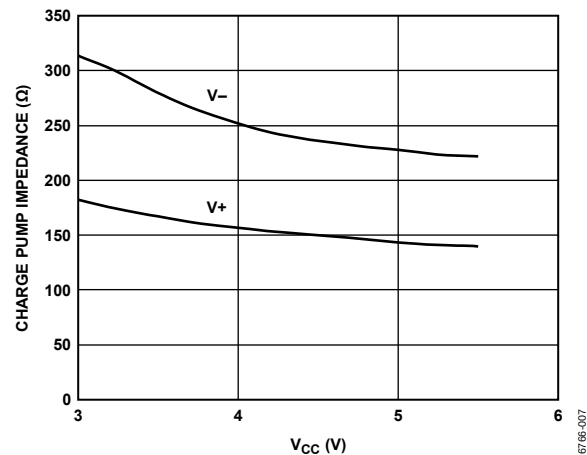


Figure 8. Charge Pump Impedance vs. V_{CC}

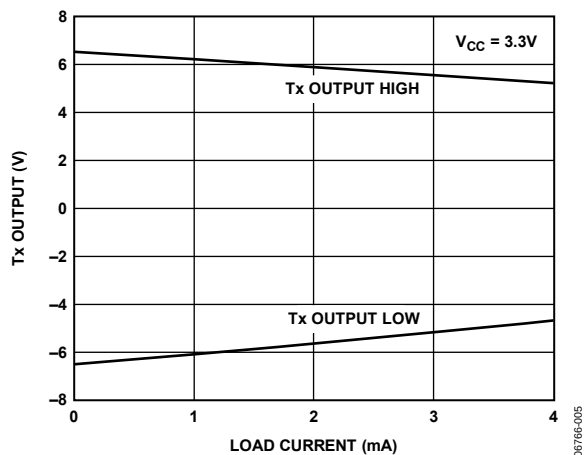


Figure 6. Transmitter Output Voltage High/Low vs. Load Current

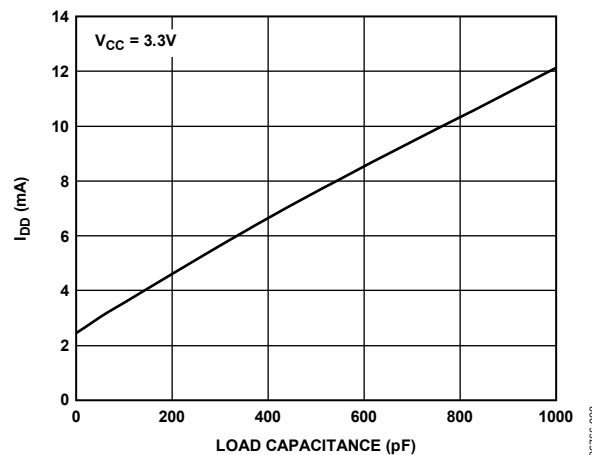


Figure 9. Power Supply Current vs. Load Capacitance

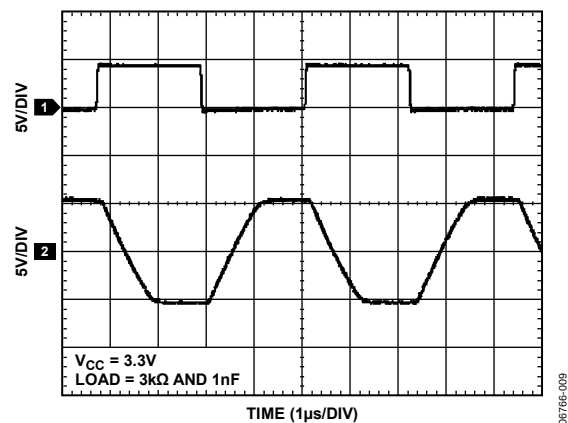


Figure 10. 460 kbps Data Transmission

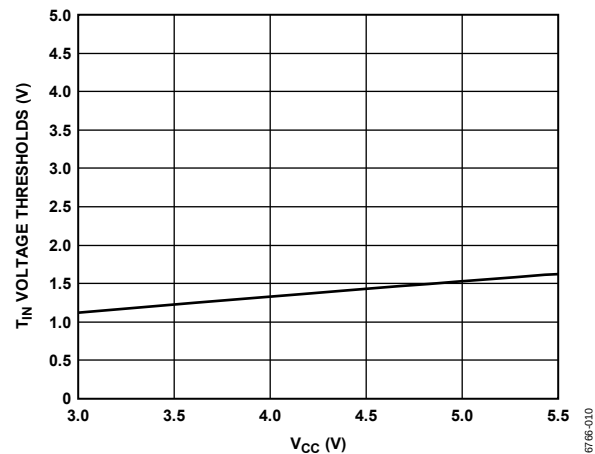


Figure 11. T_{IN} Voltage Threshold vs. V_{CC}

OUTLINE DIMENSIONS

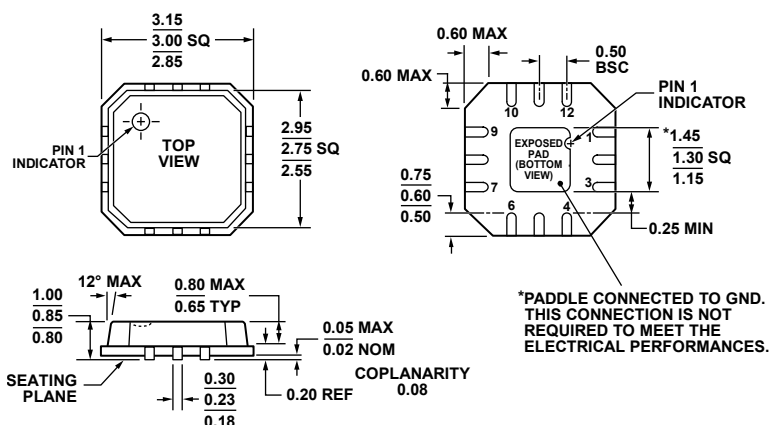


Figure 15. 12-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
3 mm × 3 mm Body, Very Thin Quad
(CP-12-1)
Dimensions shown in millimeters

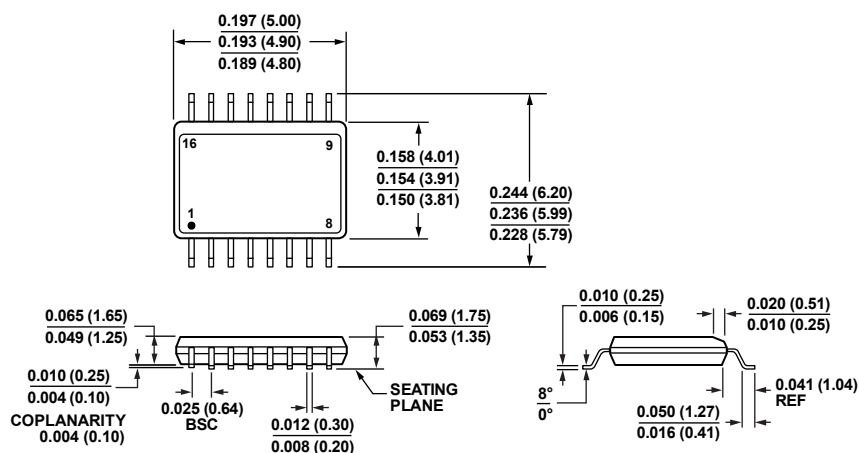


Figure 16. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in inches

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADM3101EACPZ-REEL ¹	−40°C to +85°C	12-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-12-1	MA6
ADM3101EACPZ-250R7 ¹	−40°C to +85°C	12-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-12-1	MA6
ADM3101EARQZ ¹	−40°C to +85°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16	
ADM3101EARQZ-REEL ¹	−40°C to +85°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16	

¹ Z = RoHS Compliant Part.

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