



W83194BR-S

200MHZ 2-DIMM CLOCK FOR SOLANO CHIPSET

1.0 GENERAL DESCRIPTION

The W83194BR-S is a Clock Synthesizer for Intel 815 Solano chipset. W83194BR-S provides all clocks required for high-speed RISC or CISC microprocessor and also provides 64 different frequencies of CPU, SDRAM, PCI, 3V66, IOAPIC clocks frequency setting. All clocks are externally selectable with smooth transitions.

The W83194BR-S provides I²C serial bus interface to program the registers to enable or disable each clock outputs and provides 0.25% and 0.5% center type spread spectrum to reduce EMI.

The W83194BR-S provides stepless frequency programming by controlling the VCO freq. and the clock output divisor ratio. Also the skew of CPU, SDRAM and 3V66 clock outputs are programmable. A watch dog timer is quipped and when time out, the RESET# pin will output 4ms pulse signal.

The W83194BR-S accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. High drive PCI and SDRAM CLOCK outputs typically provide greater than 1 V /ns slew rate into 30 pF loads. CPU CLOCK outputs typically provide better than 1 V /ns slew rate into 20 pF loads as maintaining 50±5% duty cycle. The fixed frequency outputs as REF, 24MHz, and 48 MHz provide better than 0.5V /ns slew rate.

2.0 PRODUCT FEATURES

- 2 CPU clocks
- 3 3V66 for chipset and AGP clocks
- 9 SDRAM clocks for 2 DIMMs
- 7 PCI synchronous clocks.
- Optional single or mixed supply:
(VddR = VddP=VddS = Vdd48 = Vdd3 = 3.3V, VddLAPIC=VddLPCPU=2.5V)
- Skew form CPU to PCI clock -1 to 4 ns, center 2.6 ns
- Smooth frequency switch with selections from 66.8 to 200 MHz
- I²C 2-Wire serial interface and I²C read back
- 0.25% and 0.5% center type spread spectrum
- Programmable registers to enable/stop each output and select modes
- Two 48 MHz pins for USB
- 24 MHz for super I/O
- 48-pin SSOP package

3.0 PIN CONFIGURATION

REFX2/*FS3	<input type="checkbox"/>	1 ●	48	<input type="checkbox"/>	VddLAPIC
VddR	<input type="checkbox"/>	2	47	<input type="checkbox"/>	IOAPIC
Xin	<input type="checkbox"/>	3	46	<input type="checkbox"/>	VddLCPU
Xout	<input type="checkbox"/>	4	45	<input type="checkbox"/>	CPUCLK0
Vss	<input type="checkbox"/>	5	44	<input type="checkbox"/>	CPUCLK1
Vdd3	<input type="checkbox"/>	6	43	<input type="checkbox"/>	VssC
3V66-0	<input type="checkbox"/>	7	42	<input type="checkbox"/>	VddS
3V66-1	<input type="checkbox"/>	8	41	<input type="checkbox"/>	SDRAM 0
3V66-2	<input type="checkbox"/>	9	40	<input type="checkbox"/>	SDRAM 1
Vss	<input type="checkbox"/>	10	39	<input type="checkbox"/>	SDRAM 2
PCICLK0^/ *FS0	<input type="checkbox"/>	11	38	<input type="checkbox"/>	VssS
PCICLK1^/ FS1#	<input type="checkbox"/>	12	37	<input type="checkbox"/>	SDRAM 3
PCICLK2^/ *FS2	<input type="checkbox"/>	13	36	<input type="checkbox"/>	SDRAM 4
VssP	<input type="checkbox"/>	14	35	<input type="checkbox"/>	SDRAM 5
PCICLK3/MODE1*	<input type="checkbox"/>	15	34	<input type="checkbox"/>	VddS
PCICLK4^	<input type="checkbox"/>	16	33	<input type="checkbox"/>	SDRAM 6
VddP	<input type="checkbox"/>	17	32	<input type="checkbox"/>	SDRAM 7
PCICLK5^	<input type="checkbox"/>	18	31	<input type="checkbox"/>	SDRAM 8
PCICLK6	<input type="checkbox"/>	19	30	<input type="checkbox"/>	VssS
Vss48	<input type="checkbox"/>	20	29	<input type="checkbox"/>	PD#/RESET\$
48MHz_0	<input type="checkbox"/>	21	28	<input type="checkbox"/>	SDCLK*
48MHz_1/ FS4#	<input type="checkbox"/>	22	27	<input type="checkbox"/>	VddA
*SIO_SEL/24_48MHz	<input type="checkbox"/>	23	26	<input type="checkbox"/>	VssA
Vdd48	<input type="checkbox"/>	24	25	<input type="checkbox"/>	SDATA*

*: internal pull-up
 #: active low
 \$: ope drain

4.0 PIN DESCRIPTION

IN - Input

OUT - Output

I/O - Bi-directional Pin

- Active Low

● - Internal 250kΩ pull-up

4.1 Crystal I/O

SYMBOL	PIN	I/O	FUNCTION
Xin	3	IN	Crystal input with internal loading capacitors(36pF) and feedback resistors.
Xout	4	OUT	Crystal output at 14.318MHz nominally with internal loading capacitors(36pF).

4.2 CPU, SDRAM, PCI, IOAPIC Clock Outputs

SYMBOL	PIN	I/O	FUNCTION
CPUCLK [0:1]	45,44	OUT	Low skew (< 250ps) clock outputs for host frequencies such as CPU and Chipset.
PD#/RESET\$	29	IN	Pin16 *Mode1=1, Power Down mode when driven low. Pin16 *Mode1=0, RESET# output (4ms low active pulse when Watch Dog time out)
IOAPIC	47	OUT	Clock outputs synchronous with PCI clock and powered by VddA.
SDRAM [0:8]	41,40, 39,37,36,35,33 ,32,31	OUT	SDRAM clock outputs.
PCICLK0/ *FS0	11	I/O	3.3V 33MHz PCI clock during normal operation. Latched input for FS0 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks(Default=1).
PCICLK1/ FS1#	12	I/O	Low skew (< 250ps) PCI clock outputs. Latched input for FS1 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks(Default=0).
PCICLK2/ *FS2	13	I/O	Low skew (< 250ps) PCI clock outputs. Latched input for FS2 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks(Default=1).
PCICLK3/MODE1*	15	I/O	PCI clock during normal operation. Latched Input. *Mode1=1, Pin 29 is PD#; *Mode1=0, Pin 29 is RESET\$
PCICLK [4:6]	16,18,19	OUT	Low skew (< 250ps) PCI clock outputs.
3V66 [0:2]	7,8,9	OUT	3.3V output clocks for the chipset.

4.3 I²C Control Interface

SYMBOL	PIN	I/O	FUNCTION
SDATA	25	I/O	Serial data of I ² C 2-wire control interface
SDCLK	28	IN	Serial clock of I ² C 2-wire control interface

4.4 Fixed Frequency Outputs

SYMBOL	PIN	I/O	FUNCTION
REFX2 / *FS3	3	I/O	14.318MHz reference clock. This REF output is the stronger buffer for ISA bus loads. Latched input for FS3 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks (Default=1).
*SIO_SEL/24_48MHz	23	I/O	24MHz or 48MHz output clock. Latched input for SIO_SEL at initial power up for the output frequency of 24MHz(HIGH) and 48MHz(LOW) clocks.
48MHz_0	21	O	48MHz output for USB during normal operation.
48MHz_1/ FS4#	22	I/O	48MHz / Latched input for FS4 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks (Default=0).

4.5 Power Pins

SYMBOL	PIN	FUNCTION
VddL	48	Power supply for CPU & IOAPIC, 2.5V or 3.3V.
Vdd48	24	Power supply for 48MHz output, 3.3V.
Vdd3	6	Power supply for 3V_66 output, 3.3V.
VddP	16	Power supply for PCICLK, 3.3V.
VddR	2	Power supply for REFX2, 3.3V.
VddS	42,34	Power supply for SDRAM[0:8], nominal 3.3V.
VddA	27	Power for I2C CLK and DATA.
Vss	5,10,14,20,26,30,38,43	Circuit Ground.



PRELIMINARY

5.0 FREQUENCY SELECTION BY HARDWARE

FS4	FS3	FS2	FS1	FS0	CPU(MHz)	SDRAM (MHz)	3V66(MHz)	PCI(MHz)	IOAPIC (MHz)
0	0	0	0	0	75.30	112.95	75.30	37.65	18.83
0	0	0	0	1	95.00	95.00	63.33	31.67	15.83
0	0	0	1	0	129.00	129.00	86.00	43.00	21.50
0	0	0	1	1	150.00	113.00	75.33	37.67	18.83
0	0	1	0	0	150.00	150.00	75.00	37.50	18.75
0	0	1	0	1	110.00	110.00	73.33	36.67	18.33
0	0	1	1	0	140.00	140.00	70.00	35.00	17.50
0	0	1	1	1	144.00	108.00	72.00	36.00	18.00
0	1	0	0	0	68.30	102.45	68.30	34.15	17.08
0	1	0	0	1	105.00	105.00	70.00	35.00	17.50
0	1	0	1	0	138.00	138.00	69.00	34.50	17.25
0	1	0	1	1	140.00	105.00	70.00	35.00	17.50
0	1	1	0	0	66.80	100.20	66.80	33.40	16.70
0	1	1	0	1	100.20	100.20	66.80	33.40	16.70
0	1	1	1	0	133.60	133.60	66.80	33.40	16.70
0	1	1	1	1	133.60	100.20	66.80	33.40	16.70
1	0	0	0	0	157.30	118.00	78.67	39.33	19.67
1	0	0	0	1	160.00	120.00	80.00	40.00	20.00
1	0	0	1	0	146.00	110.00	73.33	36.67	18.33
1	0	0	1	1	122.00	91.50	61.00	30.50	15.25
1	0	1	0	0	127.00	127.00	84.67	42.33	21.17
1	0	1	0	1	122.00	122.00	81.33	40.67	20.33
1	0	1	1	0	117.00	117.00	78.00	39.00	19.50
1	0	1	1	1	114.00	114.00	76.00	38.00	19.00
1	1	0	0	0	80.00	120.00	80.00	40.00	20.00
1	1	0	0	1	78.00	117.00	78.00	39.00	19.50
1	1	0	1	0	166.00	166.00	83.00	41.50	20.75
1	1	0	1	1	160.00	160.00	80.00	40.00	20.00
1	1	1	0	0	66.60	100.00	66.67	33.33	16.67
1	1	1	0	1	100.00	100.00	66.67	33.33	16.67
1	1	1	1	0	133.30	133.30	66.65	33.33	16.66
1	1	1	1	1	133.30	100.00	66.67	33.33	16.67



PRELIMINARY

6.0 SERIAL CONTROL REGISTERS

The Pin column lists the affected pin number and the @PowerUp column gives the state at true power up. Registers are set to the values shown only on true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the below described sequence (Register 0, Register 1, Register 2,) will be valid and acknowledged.

Frequency Table Setting by I2C (SEL5 ~ SEL0)

SSEL5	SSEL4	SSEL3	SSEL2	SSEL1	SSEL0	CPU (MHz)	SDRAM (MHz)	3V66 (MHz)	PCI(MHz)	IOAPIC (MHz)
0	0	0	0	0	0	75.30	112.95	75.30	37.65	18.83
0	0	0	0	0	1	95.00	95.00	63.33	31.67	15.83
0	0	0	0	1	0	129.00	129.00	86.00	43.00	21.50
0	0	0	0	1	1	150.00	113.00	75.33	37.67	18.83
0	0	0	1	0	0	150.00	150.00	75.00	37.50	18.75
0	0	0	1	0	1	110.00	110.00	73.33	36.67	18.33
0	0	0	1	1	0	140.00	140.00	70.00	35.00	17.50
0	0	0	1	1	1	144.00	108.00	72.00	36.00	18.00
0	0	1	0	0	0	68.30	102.45	68.30	34.15	17.08
0	0	1	0	0	1	105.00	105.00	70.00	35.00	17.50
0	0	1	0	1	0	138.00	138.00	69.00	34.50	17.25
0	0	1	0	1	1	140.00	105.00	70.00	35.00	17.50
0	0	1	1	0	0	66.80	100.20	66.80	33.40	16.70
0	0	1	1	0	1	100.20	100.20	66.80	33.40	16.70
0	0	1	1	1	0	133.60	133.60	66.80	33.40	16.70
0	0	1	1	1	1	133.60	100.20	66.80	33.40	16.70
0	1	0	0	0	0	157.30	118.00	78.67	39.33	19.67
0	1	0	0	0	1	160.00	120.00	80.00	40.00	20.00
0	1	0	0	1	0	146.00	110.00	73.33	36.67	18.33
0	1	0	0	1	1	122.00	91.50	61.00	30.50	15.25
0	1	0	1	0	0	127.00	127.00	84.67	42.33	21.17
0	1	0	1	0	1	122.00	122.00	81.33	40.67	20.33
0	1	0	1	1	0	117.00	117.00	78.00	39.00	19.50
0	1	0	1	1	1	114.00	114.00	76.00	38.00	19.00
0	1	1	0	0	0	80.00	120.00	80.00	40.00	20.00
0	1	1	0	0	1	78.00	117.00	78.00	39.00	19.50
0	1	1	0	1	0	166.00	166.00	83.00	41.50	20.75
0	1	1	0	1	1	160.00	160.00	80.00	40.00	20.00
0	1	1	1	0	0	66.60	100.00	66.67	33.33	16.67



PRELIMINARY

0	1	1	1	0	1	100.00	100.00	66.67	33.33	16.67
0	1	1	1	1	0	133.30	133.30	66.65	33.33	16.66
0	1	1	1	1	1	133.30	100.00	66.67	33.33	16.67
SSEL5	SSEL4	SSEL3	SSEL2	SSEL1	SSEL0	CPU (MHz)	SDRAM (MHz)	3V66 (MHz)	PCI(MHz)	IOAPIC (MHz)
1	0	0	0	0	0	136.00	102.00	68.00	34.00	17.00
1	0	0	0	0	1	138.00	138.00	69.00	34.50	17.25
1	0	0	0	1	0	139.00	104.25	69.50	34.75	17.38
1	0	0	0	1	1	141.00	105.75	70.50	35.25	17.63
1	0	0	1	0	0	142.00	142.00	71.00	35.50	17.75
1	0	0	1	0	1	142.00	106.50	71.00	35.50	17.75
1	0	0	1	1	0	143.00	143.00	71.50	35.75	17.88
1	0	0	1	1	1	143.00	107.25	71.50	35.75	17.88
1	0	1	0	0	0	144.00	144.00	72.00	36.00	18.00
1	0	1	0	0	1	144.00	108.00	72.00	36.00	18.00
1	0	1	0	1	0	146.00	146.00	73.00	36.50	18.25
1	0	1	0	1	1	146.00	109.50	73.00	36.50	18.25
1	0	1	1	0	0	147.00	147.00	73.50	36.75	18.38
1	0	1	1	0	1	147.00	110.25	73.50	36.75	18.38
1	0	1	1	1	0	148.00	148.00	74.00	37.00	18.50
1	0	1	1	1	1	148.00	111.00	74.00	37.00	18.50
1	1	0	0	0	0	149.00	111.75	74.50	37.25	18.63
1	1	0	0	0	1	152.00	152.00	76.00	38.00	19.00
1	1	0	0	1	0	153.00	114.75	76.50	38.25	19.13
1	1	0	0	1	1	156.00	156.00	78.00	39.00	19.50
1	1	0	1	0	0	157.00	117.75	78.50	39.25	19.63
1	1	0	1	0	1	158.00	158.00	79.00	39.50	19.75
1	1	0	1	1	0	159.00	119.25	79.50	39.75	19.88
1	1	0	1	1	1	160.00	160.00	80.00	40.00	20.00
1	1	1	0	0	0	162.00	121.50	81.00	40.50	20.25
1	1	1	0	0	1	164.00	123.00	82.00	41.00	20.50
1	1	1	0	1	0	170.00	127.50	85.00	42.50	21.25
1	1	1	0	1	1	175.00	116.67	77.78	38.89	19.44
1	1	1	1	0	0	180.00	120.00	80.00	40.00	20.00
1	1	1	1	0	1	185.00	185.00	61.67	30.83	15.42
1	1	1	1	1	0	190.00	126.67	63.33	31.67	15.83
1	1	1	1	1	1	200.40	133.60	66.80	33.40	16.70

6.1 Register 0: Control Register

Bit	@PowerUp	Pin	Description
7	X	-	FS0#
6	X	-	FS1#
5	X	-	FS2#
4	X	-	FS3#
3	X	-	FS4#
2	1	-	If Reg0-bit7=1 0 = $\pm 0.5\%$ Center type Spread Spectrum Modulation 1 = $\pm 0.75\%$ Center type Spread Spectrum Modulation If Reg0-bit7=0 0 = -0.6% Down type Spread Spectrum Modulation 1 = -1.0% Down type Spread Spectrum Modulation
1	0	-	0 = Normal 1 = Spread Spectrum enabled
0	1	-	1=CENTER SPREAD 0=DOWN SPREAD

6.2 Register 1 : SDRAM Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	38	SDRAM7 (Active / Inactive)
6	1	41	SDRAM6 (Active / Inactive)
5	1	42	SDRAM5 (Active / Inactive)
4	1	43	SDRAM4 (Active / Inactive)
3	1	44	SDRAM3 (Active / Inactive)
2	1	47	SDRAM2 (Active / Inactive)
1	1	48	SDRAM1 (Active / Inactive)
0	1	49	SDRAM0 (Active / Inactive)

6.3 Register 2: PCI Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	20	PCICLK7 (Active / Inactive)
6	1	19	PCICLK6 (Active / Inactive)
5	1	18	PCICLK5 (Active / Inactive)
4	1	16	PCICLK4 (Active / Inactive)
3	1	15	PCICLK3 (Active / Inactive)
2	1	13	PCICLK2 (Active / Inactive)
1	1	12	PCICLK1 (Active / Inactive)
0	1	11	PCICLK0 (Active / Inactive)

6.4 Register 3: Control Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	9	3V66_2(Active/Inactive)
6	1	8	3V66_1(Active / Inactive)
5	1	7	3V66_0(Active / Inactive)
4	1	23	24_48MHz (Active / Inactive)
3	1	47	IOAPIC (Active / Inactive)
2	1	21	48MHz0 (Active / Inactive)
1	1	22	48MHz1 (Active / Inactive)
0	1	1	REF2X (Active / Inactive)

6.5 Register 4: Control Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	0	-	SSEL3 (Frequency table selection by software via I ² C)
6	0	-	SSEL2 (Frequency table selection by software via I ² C)
5	0	-	SSEL1 (Frequency table selection by software via I ² C)
4	0	-	SSEL0 (Frequency table selection by software via I ² C)
3	0	-	0 = Selection by hardware 1 = Selection by software I ² C - Bit (1,2, 4:6)
2	0	-	SSEL4 (Frequency table selection by software via I ² C)
1	0	-	SSEL5 (Frequency table selection by software via I ² C)
0	0	-	0 = Running 1 = Tristate all outputs

6.6 Register 5: Skew Register

Bit	@PowerUp	Pin	Description
7	1	-	CSkew2 (CPU to SDRAM skew program bit)
6	0	-	CSkew1 (CPU to SDRAM skew program bit)
5	0	-	CSkew0 (CPU to SDRAM skew program bit)
4	1	-	CASkew2 (CPU to 3V66 skew program bit)
3	0	-	CASkew1 (CPU to 3V66 skew program bit)
2	0	-	CASkew0 (CPU to 3V66 skew program bit)
1	1	51	CPUCLK1(Active/Inactive)
0	1	52	CPUCLK0(Active / Inactive)



PRELIMINARY

6.7 Register 6~10: Step-less M/N Mode Control Registers

6.12 Register 11: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	0	-	Winbond Chip ID
6	1	-	Winbond Chip ID
5	0	-	Winbond Chip ID
4	1	-	Winbond Chip ID
3	0	-	Winbond Chip ID
2	0	-	Winbond Chip ID
1	0	-	Winbond Chip ID
0	0	-	Winbond Chip ID

6.13 Register 12: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	0	-	Winbond Chip ID
6	1	-	Winbond Chip ID
5	0	-	Winbond Chip ID
4	0	-	Winbond Chip ID
3	0	-	Winbond Chip ID
2	0	-	Winbond Version ID
1	1	-	Winbond Version ID
0	0	-	Winbond Version ID

Register10 Bit3-6				Ratio		
Bit6	Bit 5	Bit 4	Bit 3	CPU	SDRAM	3V66
DS3	DS2	DS1	DS0			
0	0	0	0	4	4	6
0	0	0	1	3	3	6
0	0	1	0	2	3	6
0	0	1	1	2	2	6
0	1	0	0	6	4	6
0	1	0	1	3	4	6
0	1	1	0	6	3	6
0	1	1	1	4	3	6
1	0	x	x	2	2	4
1	1	x	x	2	4	6

7.0 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or Vdd).

Symbol	Parameter	Rating
Vdd , V _{IN}	Voltage on any pin with respect to GND	- 0.5 V to + 7.0 V
T _{STG}	Storage Temperature	- 65°C to + 150°C
T _B	Ambient Temperature	- 55°C to + 125°C
T _A	Operating Temperature	0°C to + 70°C

7.2 Electrical Characteristics---Input/Output

Vddq1=Vddq2 = Vddq3 = Vddq4 =3.3V, VddL1 =VddL2= 2.5V , T _A = 0° C to +70° C						
Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input Low Voltage	V _{IL}	Vss-0.3		0.8	V _{dc}	
Input High Voltage	V _{IH}	2.0		Vdd+0.3	V _{dc}	
Input Low Current	I _{IL}	-5			μA	No pull-up resistors
Input Low Current	I _{IL}	-200			μA	Pull-up resistors
Input High Current	I _{IH}	-5		5	μA	
Input Capacitance	C _{IN}			5	pF	Logic inputs
	C _{OUT}			6	pF	Output capacitance
	C _{INX}	27		45	pF	Xin and Xout
Operating Supply Current	I _{dd3}			100	mA	CPU = 66.6 MHz PCI = 33.3 Mhz with load
Power Down Supply Current	I _{dd2}			600	μA	
Settling Time	T _s			3	mS	From first crossing to 1% target freq.

PRELIMINARY

Delay	t_{PZH}, t_{PZH}	1		10	nS	Output enable delay
	t_{PLZ}, t_{PZH}	1		10	nS	Output enable delay

7.3 Electrical Characteristics of CPU Clock

Vdd=2.5V +/- 5%; C_L=10-20pF

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Output Impedance	R _{DSP}	13.5		40	Ohm	
Output Impedance	R _{DSN}	13.5		40	Ohm	
Output Low Voltage	V _{OL}			0.4	V	I _{OL} =1mA
Output High Voltage	V _{OH}	2.0			V	I _{OH} =-1mA
Output Low Current	I _{OL}	27		30	MA	
Output High Current	I _{OH}	-27		-27	MA	
Pull-Up Current Min	I _{OH(min)}	-27			MA	Vout = 1.0 V
Pull-Up Current Max	I _{OH(max)}			-27	MA	Vout = 2.0V
Rise/Fall Time Min Between 0.4 V and 2.0 V	T _{RF(min)}	0.4			ns	10pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	T _{RF(max)}			1.6	ns	20pF Load
Duty Cycle	Dt	45		55	%	V _T =1.25V
Skew	T _{SK}			175	ps	V _T =1.25V
Jitter	T _{SC-C}			250	ps	V _T =1.25V

7.4 Electrical Characteristics of 3V66 Clock

Vdd=3.3V +/- 5%; C_L=10-30pF

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Output Impedance	R _{DSP}	15		55	Ohm	
Output Impedance	R _{DSN}	15		55	Ohm	
Output Low Voltage	V _{OL}			0.55	V	I _{OL} =1mA
Output High Voltage	V _{OH}	2.4			V	I _{OH} =-1mA
Output Low Current	I _{OL}	30		38	MA	
Output High Current	I _{OH}	-33		-33	MA	
Rise/Fall Time Min Between 0.4 V and 2.0 V	T _{RF(min)}	0.4			ns	10pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	T _{RF(max)}			1.6	ns	20pF Load



PRELIMINARY

Duty Cycle	Dt	45		55	%	$V_T=1.5V$
Skew	T_{SK}			175	ps	$V_T=1.5V$
Jitter	T_{SC-C}			500	ps	$V_T=1.5V$

7.5 Electrical Characteristics of SDRAM Clock

$V_{dd}=3.3V \pm 5\%$; $C_L=20-30pF$

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Output Impedance	R_{DSP}	13.5		40	Ohm	
Output Impedance	R_{DSN}	13.5		40	Ohm	
Output Low Voltage	V_{OL}			0.45	V	$I_{OL}=1mA$
Output High Voltage	V_{OH}	2.4			V	$I_{OH}=-1mA$
Output Low Current	I_{OL}	54		54	MA	
Output High Current	I_{OH}	-54		-45	MA	
Rise/Fall Time Min Between 0.4 V and 2.0 V	$T_{RF(min)}$	0.4			ns	10pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	$T_{RF(max)}$			1.6	ns	20pF Load
Duty Cycle	Dt	45		55	%	$V_T=1.5V$
Skew	T_{SK}			250	ps	$V_T=1.5V$
Jitter	T_{SC-C}			250	ps	$V_T=1.5V$

7.6 Electrical Characteristics of PCI Clock

$V_{dd}=3.3V \pm 5\%$; $C_L=10-30pF$

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Output Impedance	R_{DSP}	15		55	Ohm	
Output Impedance	R_{DSN}	15		55	Ohm	
Output Low Voltage	V_{OL}			0.55	V	$I_{OL}=1mA$
Output High Voltage	V_{OH}	2.4			V	$I_{OH}=-1mA$
Output Low Current	I_{OL}	30		38	MA	
Output High Current	I_{OH}	-33		-33	MA	
Rise/Fall Time Min Between 0.4 V and 2.0 V	$T_{RF(min)}$	0.5			ns	10pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	$T_{RF(max)}$			2.0	ns	20pF Load



PRELIMINARY

Between 0.4 V and 2.0 V						
Duty Cycle	Dt	45		55	%	$V_T=1.5V$
Skew	T_{SK}			500	ps	$V_T=1.5V$
Jitter	Tsc-c			500	ps	$V_T=1.5V$

7.7 Electrical Characteristics of 48MHz, REF Clock

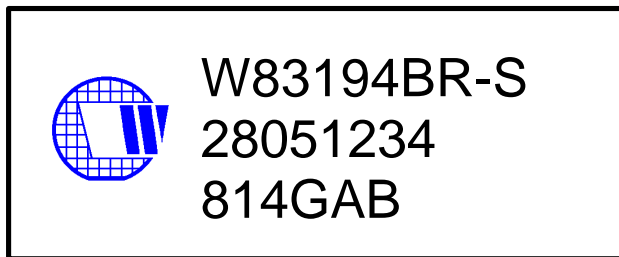
$V_{dd}=3.3V \pm 5\%$; $C_L=10-20pF$

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Output Impedance	R_{DSP}	20		55	Ohm	
Output Impedance	R_{DSN}	20		55	Ohm	
Output Low Voltage	V_{OL}			0.4	V	$I_{OL}=1mA$
Output High Voltage	V_{OH}	2.4			V	$I_{OH}=-1mA$
Output Low Current	I_{OL}	29		27	MA	
Output High Current	I_{OH}	-29		-23	MA	
Rise Time	T_R		1.8	4	ns	10pF Load
Fall Time	T_F		1.7	4	ns	20pF Load
Duty Cycle	Dt	45		55	%	$V_T=1.5V$
Skew	T_{SK}			500	ps	$V_T=1.5V$
Jitter	Tsc-c			1000	ps	$V_T=1.5V$

8.0 ORDERING INFORMATION

Part Number	Package Type	Production Flow
W83194BR-S	48 PIN SSOP	Commercial, 0°C to +70°C

9.0 HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83194BR-S

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 814 G B B

814: packages made in '98, week 14

G: assembly house ID; O means OSE, G means GR

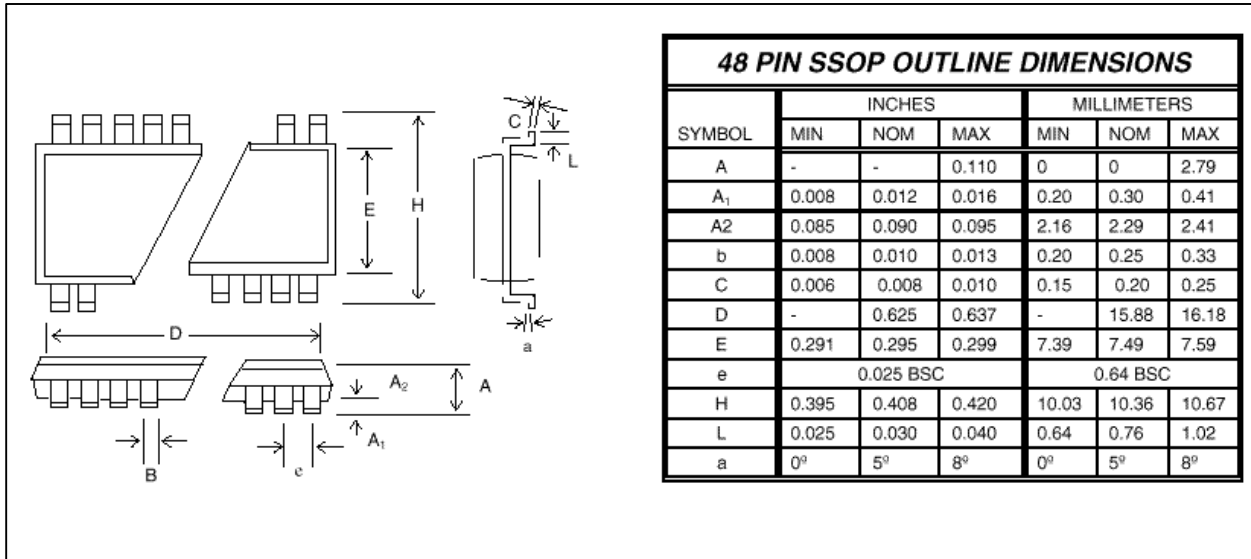
A: Internal use code

B: IC revision

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PRELIMINARY

10.0 PACKAGE DRAWING AND DIMENSIONS



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