WPMDH1152401 / 171012402

MagI³C Power Module

VDRM - Variable Step Down Regulator Module

6-42V / 1.5A / 5-24V Output

DESCRIPTION

The VDRM series of the MagI³C Power Module family provide a fully integrated DC-DC power supply including the buck switching regulator and inductor in a package.

The WPMDH1152401 offers high efficiency and delivers up to 1.5A of output current. It operates from 6V input voltage up to 42V. It is designed for fast transient response.

It is available in an innovative industrial high power density TO263-7EP (10.16 x 13.77 x 4.57mm) package that enhances thermal performance and allows for hand or machine soldering.

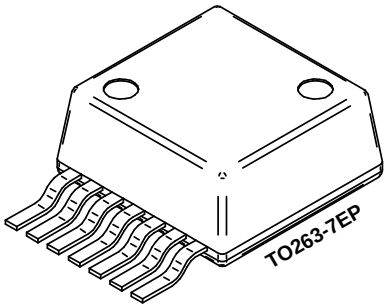
The VDRM regulators have an on-board protection circuitry to guard against thermal overstress and electrical damage featuring thermal shut-down, over-current, short-circuit, overvoltage and under-voltage protections.

FEATURES

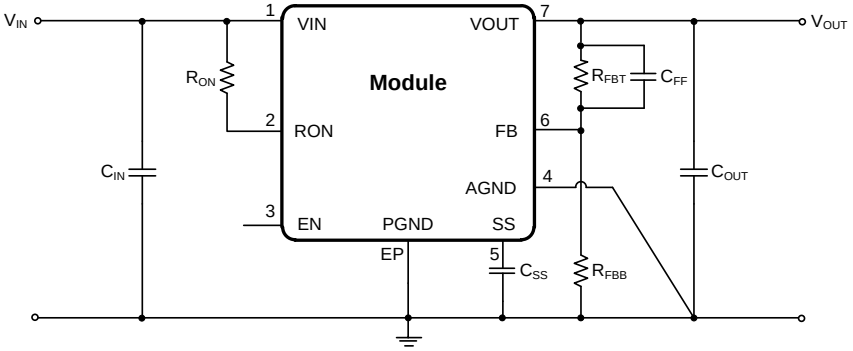
- Peak efficiency up to 97%
- Current capability up to 1.5A
- Wide input voltage range: 6V to 42V
- Output voltage range: 5V to 24V
- Maximum output power: 36W
- Integrated shielded inductor solution for quick time to market and ease of use
- Single exposed pad for best-in-class thermal performance
- Low output voltage ripple
- Under voltage lockout Protection (UVLO)
- Programmable soft-start
- Adjustable switching frequency
- Thermal shut down, inrush current and output short circuit protection
- Operating ambient temp. range up to 105°C
- Operating junction temp. range: -40 to 125°C
- RoHS & REACH compliant
- Mold compound UL 94 Class V0 (flammability testing) certified
- Complies with EN 55022 class B radiated and conducted emissions standard

TYPICAL APPLICATIONS

- Point-of-Load DC-DC applications from 12V and 24V industrial rails
- Industrial, Test & Measurement, Medical applications
- System power supplies
- DSPs, FPGAs, MCUs and MPUs supply
- I/O interface power supply



TYPICAL CIRCUIT DIAGRAM



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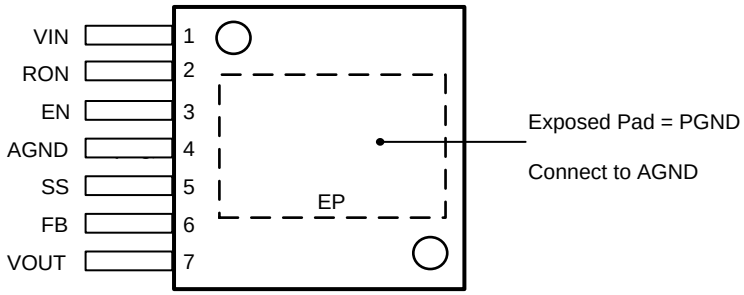
PACKAGE



PIN DESCRIPTION

PIN #	SYMBOL	TYPE	PIN DESCRIPTION
1	V_{IN}	Power	The supply input pin is a terminal for an unregulated input voltage source. It is required to place the input capacitor nearby the VIN pin and PGND.
2	R_{ON}	Input	An external resistor from R_{ON} to V_{IN} pin sets the on-time and frequency of the application. The value range of the resistor is from 25kΩ to 124kΩ.
3	EN	Input	The enable input pin is internally connected to the precision enable comparator and the rising threshold is at 1.18V. Maximum recommended input level is 6.5V.
4	AGND	Supply	The analog ground pin is the reference point for all stated voltages and must be connected to PGND.
5	SS	Input	For the soft-start function there is an internal 8µA current source which charges an external capacitor to generate the soft-start.
6	FB	Input	The feedback pin is internally connected to the regulation circuitry, the over-voltage and short-circuit comparators. The regulation reference point is 0.8V at this input pin. Connect the feedback resistor divider between the output and AGND to set the output voltage.
7	V_{OUT}	Power	The output voltage pin is connected to the internal inductor. For the best stability and operation connect the output capacitor between this pin and PGND.
EP	PGND	Power	Exposed Pad – Main node for switch current of internal LS-MOSFET. Used as heat sink for power dissipation during operation. Must be electrically connected to pin 4.

ORDERING INFORMATION

ORDER CODE	PART DESCRIPTION	PACKAGE	PACKING UNIT
171012402	WPMDH1152401JT	TO263-7EP	Tape and Reel with 250 Units
178012402	WPMDH1152401JEV	Eval Board	evaluation board 1 Unit

SALES INFORMATION

SALES CONTACTS
Würth Elektronik eiSos GmbH & Co. KG EMC & Inductive Solutions Max-Eyth-Str. 1 74638 Waldenburg Germany Tel. +49 (0) 79 42 945 - 0 www.we-online.com powermodules@we-online.com

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ABSOLUTE MAXIMUM RATINGS

Caution:
Exceeding the listed absolute maximum ratings may affect the device negatively and may cause permanent damage.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{IN}, R_{ON}	Input Voltage, On-time resistor	-0.3 to 43.5	V
EN, FB, SS	Enable, Feedback, Soft-start Input	-0.3 to 7.0	V
$V_{ESD-HBM}$	ESD, human body model (1)	-2000 to 2000	V
T_J	Junction temperature	150	°C
T_{ST}	Storage temperature	-65 to 150	°C
T_{SOLR}	Peak case/leads temperature during reflow soldering, max. 20sec (2) Maximum two cycles!	240 ±5°C	°C

OPERATING CONDITIONS

Operating conditions are conditions under which operation of the device is intended to be functional. All values are referenced to GND.

SYMBOL	PARAMETER	MIN (3)	TYP (4)	MAX (3)	UNIT
V_{IN}	Input voltage	6	-	42	V
V_{OUT}	Regulated output voltage	5		24	V
EN	Enable input	0	-	6.5	V
T_A	Ambient temperature range	-40	-	note (5)	°C
T_J	Junction temperature range	-40	-	125	°C

THERMAL SPECIFICATIONS

SYMBOL	PARAMETER	TYP	UNIT
θ_{JA}	Thermal resistance junction to ambient(6)	16	°C/W
θ_{JC}	Thermal resistance junction to case, no air flow	1.9	°C/W
T_{SD}	Thermal shut down, junction temperature, rising	165	°C
$T_{SD-HYST}$	Thermal shut down hysteresis, falling	15	°C

ELECTRICAL SPECIFICATIONS

MIN and MAX limits are valid for the recommended junction temperature range of **-40°C to 125°C**. Typical values represent statistically the utmost probability at following conditions: V_{IN}=24V, V_{OUT}=12V, R_{ON}=249KΩ T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN (3)	TYP (4)	MAX (3)	UNIT
I_{OCP}	Over current protection		2.4	3.2	3.95	A
V_{EN}	EN threshold trip point	V_{EN} rising	1.10	1.18	1.25	V
V_{EN-HYS}	EN threshold hysteresis	V_{EN} falling	-	90	-	mV
f_{SW}	Switching frequency	Continuous Conduction Mode (CCM)	0.2	-	0.8	MHz
t_{ON-MIN}	ON timer minimum pulse width		-	150	-	ns
t_{OFF}	OFF timer pulse width		-	260	-	ns
I_{SS}	SS pin source current	V_{SS} = 0V	8	10	15	µA
t_{SS}	Soft-start time	C_{SS} = 4.7nF		0.5		ms
I_{SS-DIS}	SS discharge current		-	-200	-	µA

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SYMBOL	PARAMETER	CONDITIONS	MIN (3)	TYP (4)	MAX (3)	UNIT
V_{FB}	In-regulation feedback voltage	V_{IN} = 24V, V_{OUT} = 12V V_{SS} >+ 0.8V T_J = -40°C to 125°C I_{OUT} = 10mA to 1.5A	0.784	0.804	0.825	V
V_{FB}	In-regulation feedback voltage	V_{IN} = 24V, V_{OUT} = 12V V_{SS} >+ 0.8V T_J = 25°C I_{OUT} = 10mA to 1.5A	0.786	0.803	0.818	V
V_{FB-OVP}	Feedback over-voltage protection threshold		-	0.92	-	V
I_{FB}	Feedback input bias current		-	5	-	nA
I_Q	Non switching input current	V_{FB}= 0.86V	-	1	-	mA
I_{SD}	Shut down quiescent current	V_{EN}= 0V	-	25	-	µA
ΔV_{OUT}	Output voltage ripple	V_{OUT}=5V C_{OUT}=100µF 6.3V X7R	-	8	-	mVpp
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	V_{IN} = 16V to 42V I_{OUT}=1.5A	-	0.01	-	%
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	V_{IN} = 24V I_{OUT} = 0A to 1A	-	1.5	-	mV/A
η	Efficiency	V_{IN}=24V V_{OUT}=12V I_{OUT}=1A	-	93	-	%
η	Efficiency	V_{IN} = 24V V_{OUT} = 12V I_{OUT} = 1.5A	-	92	-	%

NOTES

(1) The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD-22-114.

(2) JEDEC J-STD020

(3) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

(4) Typical numbers are valid at 25°C ambient temperature and represent statistically the utmost probability assuming the Gaussian distribution.

(5) Depending on heat sink design, number of PCB layers, copper thickness and air flow.

(6) 4 layer printed circuit board, 76.2mm x 76.2mm area, 35µm copper, no air flow.

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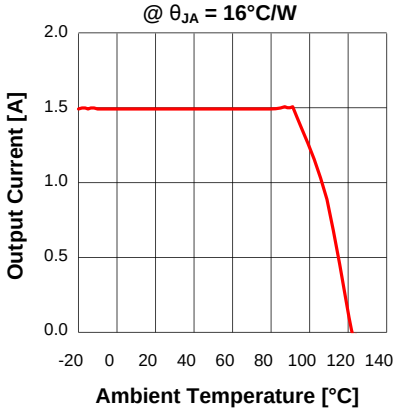
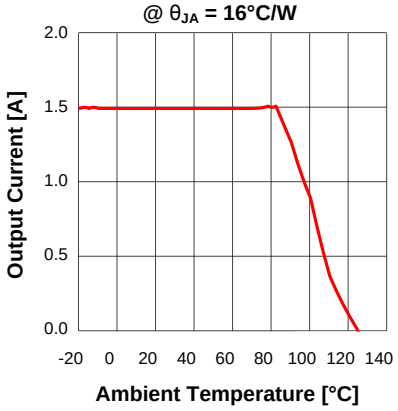
If not otherwise specified, the following conditions apply: V_{IN} = 24V; C_{IN} = 10µF X7R ceramic; C_O = 47µF X7R ceramic, T_{AMB} = 25°C

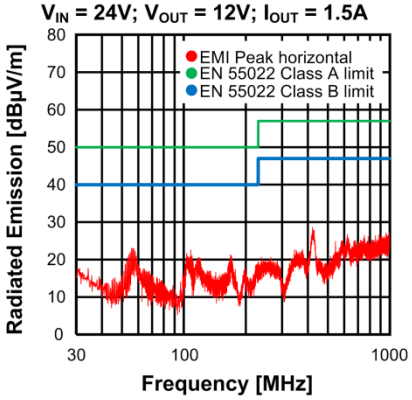
Thermal Derating: V_{IN} = 24V, V_{OUT} = 12V @ θ_{JA} = 16°C/W



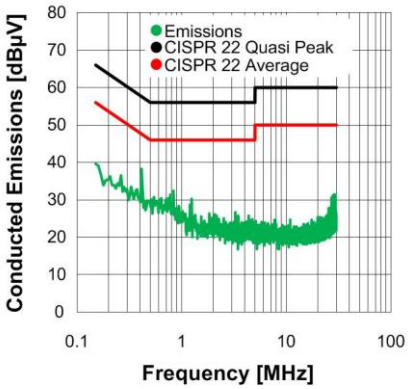
Thermal Derating: V_{IN} = 42V, V_{OUT} = 24V @ θ_{JA} = 16°C/W



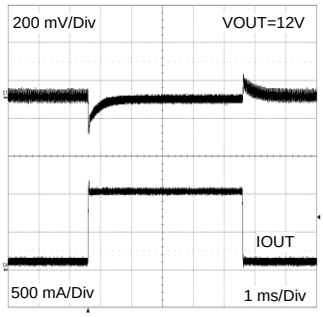
Radiated EMI according to EN55022 (CISPR-22); Measured on Evaluation Board at 3m antenna distance; V_{IN} = 24V; V_{OUT} = 12V; I_{OUT} = 1.5A



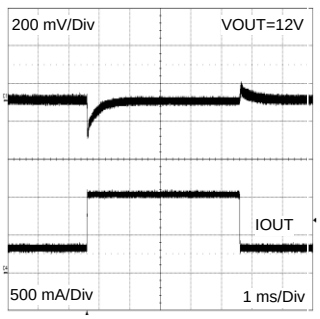
Conducted EMI V_{OUT} = 12V Evaluation Board BOM and 3.3 µH 2x10µF LC line filter



Load Transient Response VIN = 24V VOUT = 12V Load Step from 10% to 70%



Load Transient Response VIN = 24V VOUT = 12V Load Step from 30% to 70%



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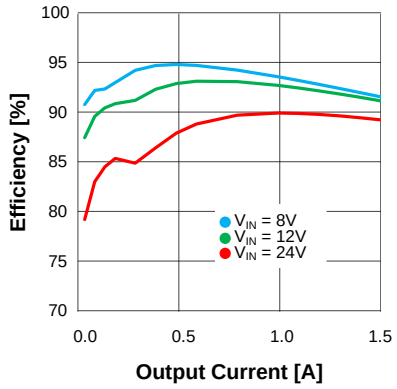
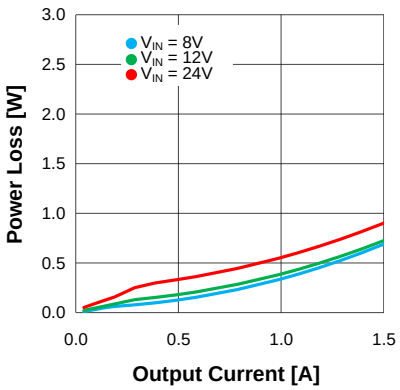
If not otherwise specified, the following conditions apply: V_{IN} = 24V; C_{IN} = 10µF X7R ceramic; C_O = 47µF X7R ceramic, T_{AMB} = 25°C

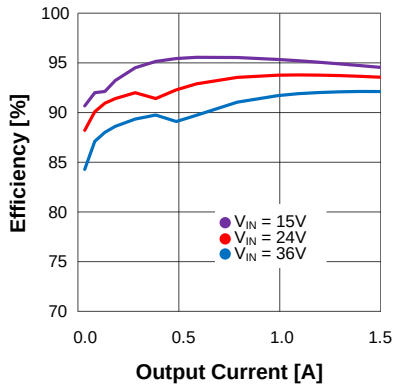
Efficiency: V_{OUT} = 5V @ T_{AMB} = 25°C



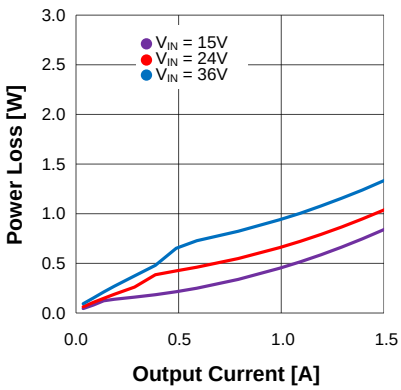
Power Loss: V_{OUT} = 5V @ T_{AMB} = 25°C



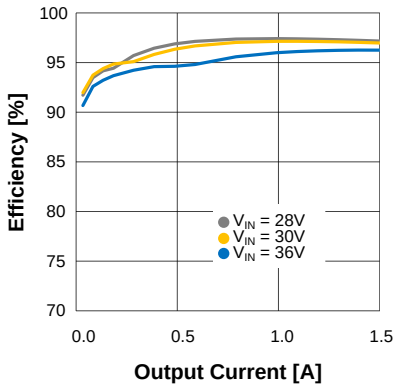
Efficiency: V_{OUT} = 12V @ T_{AMB} = 25°C



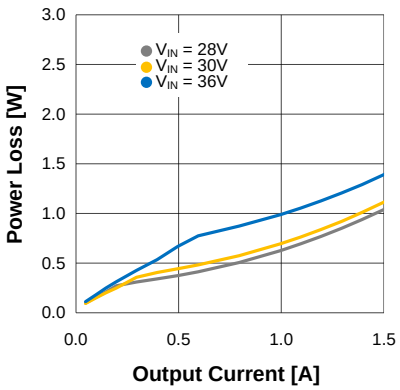
Power Loss: V_{OUT} = 12V @ T_{AMB} = 25°C



Efficiency: V_{OUT} = 24V @ T_{AMB} = 25°C



Power Loss: V_{OUT} = 24V @ T_{AMB} = 25°C



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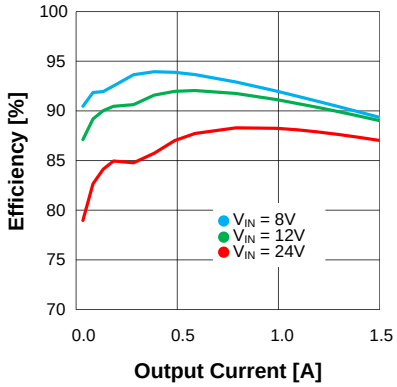
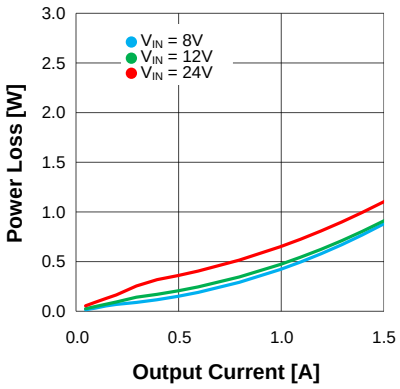
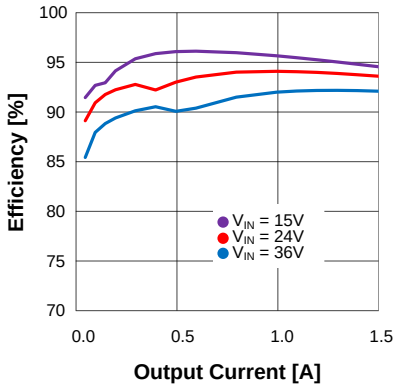
Efficiency: V_{OUT} = 5V @ T_{AMB} = 85°C



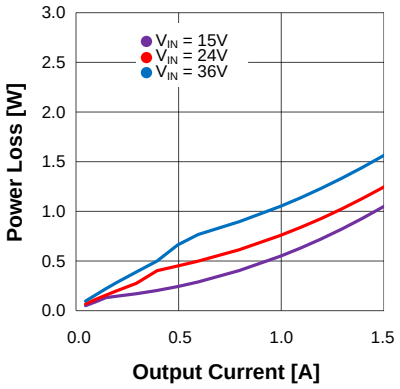
Power Loss: V_{OUT} = 5V @ T_{AMB} = 85°C



Efficiency: V_{OUT} = 12V @ T_{AMB} = 85°C



Power Loss: V_{OUT} = 12V @ T_{AMB} = 85°C



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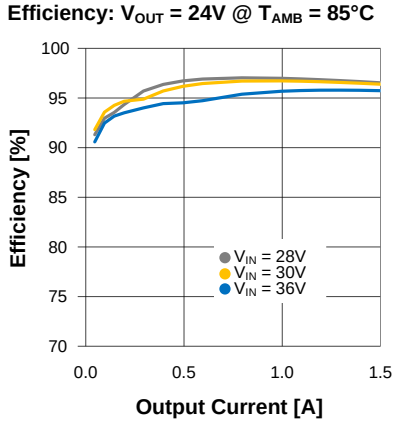
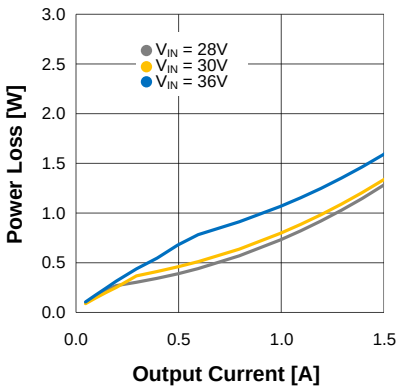


Power Loss: V_{OUT} = 24V @ T_{AMB} = 85°C



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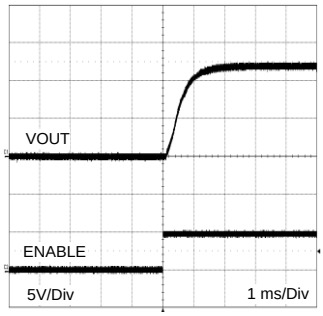
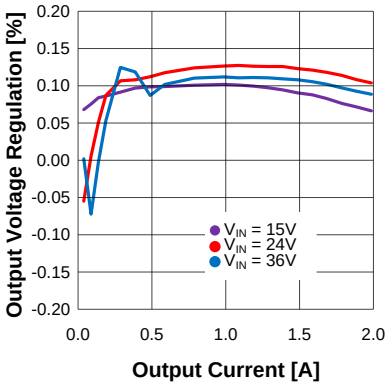
If not otherwise specified, the following conditions apply: V_{IN} = 24V; C_{IN} = 10µF X7R ceramic; C_O = 47µF X7R ceramic, T_{AMB} = 25°C

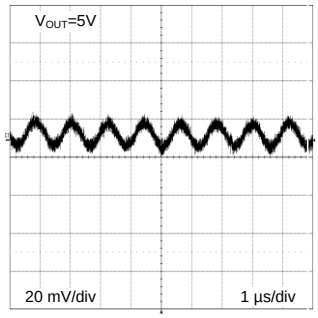
Startup V_{IN} = 24V, I_{OUT} = 1.5A



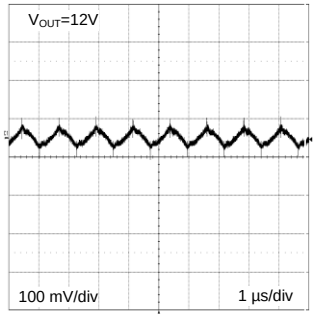
Line and Load Regulation T_{AMB} = 25°C



Output Rippel
V_{IN} = 12V, I_{OUT} = 1.5A, Ceramic C_{OUT}, BW = 200MHz



Output Rippel
V_{IN} = 24V, I_{OUT} = 1.5A, Polymer Electrolytic C_{OUT}, BW = 200MHz



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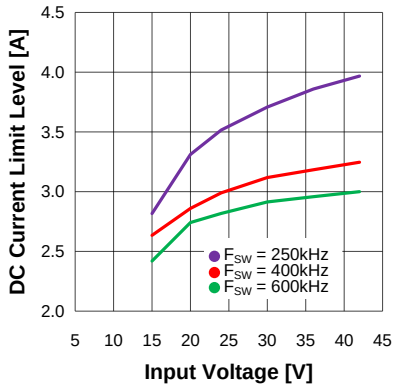
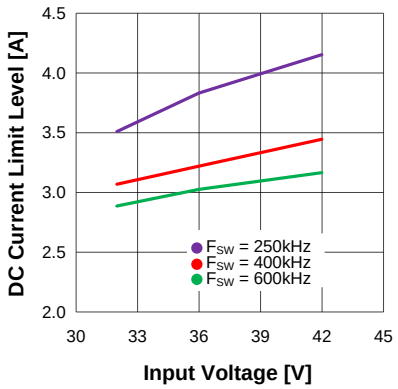
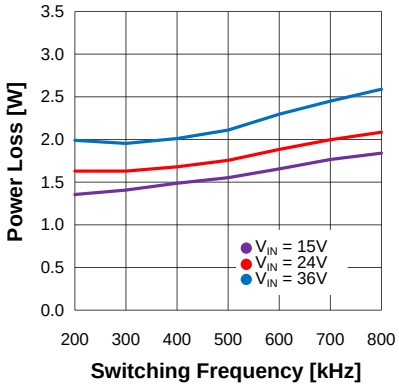
Current Limit vs. Input Voltage
V_{OUT} = 12V @ T_{AMB} = 25°C



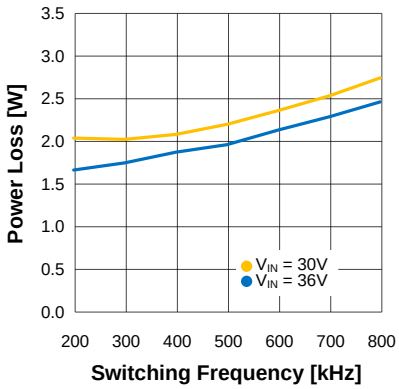
Current Limit vs. Input Voltage
V_{OUT} = 24V @ T_{AMB} = 25°C



Switching Frequency vs. Power Dissipation
V_{OUT} = 12V @ T_{AMB} = 25°C



Switching Frequency vs. Power Dissipation
V_{OUT} = 24V @ T_{AMB} = 25°C



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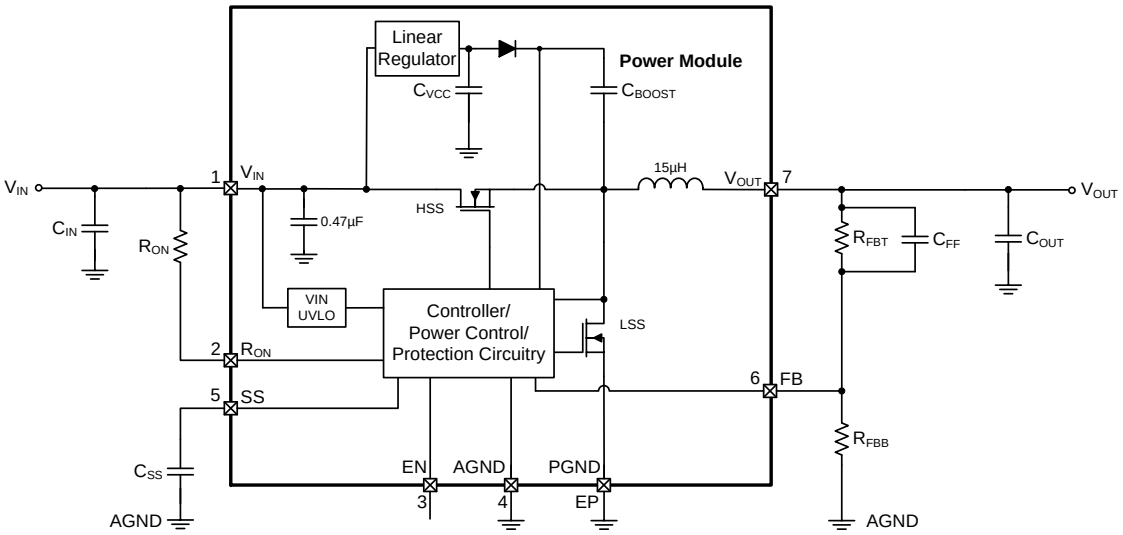
BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The MagI³C Power Module WPMDH1152401 is based on a synchronous step down regulator with integrated MOSFET and a power inductor. The control scheme uses a constant on-time (COT) low ripple hysteretic regulation loop.

The V_{OUT} of the regulator is divided with the feedback resistor network R_{FBT} and R_{FBB} and fed into the FB pin. The internal comparator compares this signal with the internal 0.8V reference. If the feedback voltage is below the reference, the High Side MOSFET is turned on for a fixed on-time.

To achieve a regulated output voltage the off-time is modulated. At stable V_{IN} to V_{OUT} condition the relation between on-time and off-time is constant. The on-time is fixed and preset by the value of the RON resistor. The switching frequency is directly proportional to this value.
The connection of the R_{ON} resistor to V_{IN} results into an additional compensation of varying V_{IN} values, (V_{IN} feed-forward) so the switching frequency will remain almost constant even during V_{IN} transients.

A load current transient (low to high current) allows the off-time to immediately transition to the minimum of 260 ns. This results in a short term higher switching frequency which ensures an extremely quick regulation response. As soon as the output capacitor is recharged to the nominal output voltage the switching frequency will return to the original value even though the load current is higher.

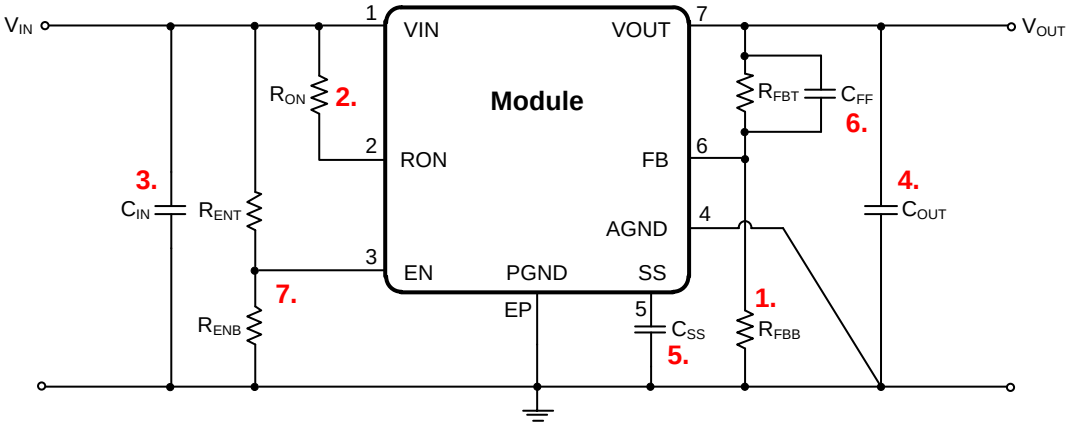
Constant on-time control scheme does not require compensation circuitry which makes the overall design very simple. Nevertheless it requires a certain minimum ripple at the feedback pin.
The MagI³C Power Module WPMDH1152401 generates this ripple internally and is supported by the C_{FF} capacitor which bypasses AC ripple directly to the feedback pin from the output. With this architecture very small output ripple values of 10ths of millivolts similar to current or voltage mode devices are achieved.

DESIGN FLOW

7 Steps to design the power application

The next 7 simple steps will show how to select the external components to design your power application:

1. **Program output voltage**
2. **Set operating frequency with R_{ON}**
3. **Select input capacitor**
4. **Select output capacitor**
5. **Select soft-start capacitor**
6. **Select feed forward capacitor**
7. **Optional: Program under voltage lockout divider**



Step 1. Select Output Voltage (V_{OUT})
Output voltage is determined by a divider of two resistors connected between V_{OUT} and ground. The midpoint of the divider is connected to the FB input. The voltage at FB is compared to a 0.8V internal reference. In normal operation an on-time cycle is initiated when the voltage on the FB pin falls below 0.8V. The high-side MOSFET on-time cycle causes the output voltage to rise and the voltage at the FB to exceed 0.8V. As long as the voltage at FB is above 0.8V, on time cycles will not occur.
The ratio of the feedback resistors for a desired output voltage is:

$$\frac{R_{FBT}}{R_{FBB}} = \left(\frac{V_{OUT}}{0.8V}\right) - 1 \qquad (1)$$

These resistors should be chosen from values in the range of 1kΩ to 50kΩ.

A table of values for R_{FBT}, R_{FBB}, and R_{ON} is included in the applications circuit.

Step 2. Select On-Time Resistor (R_{ON})
Many designs will begin with a desired switching frequency in mind. For that purpose the following equation can be used.

$$R_{ON} \approxeq \frac{V_{OUT}}{(1.3 * 10^{-10} * f_{SW(CCM)})} \qquad (2)$$

The selection of R_{ON} and $f_{SW(CCM)}$ must be confined by limitations in the on-time and off-time for the COT control section. The on-time of the MagI³C power module timer is determined by the resistor R_{ON} and the input voltage V_{IN}. It is calculated as follows:

$$t_{ON} = \frac{(1.3 * 10^{-10} * R_{ON})}{V_{IN}} \qquad (3)$$

DESIGN FLOW

The inverse relationship of t_{ON} and V_{IN} gives a nearly constant switching frequency as V_{IN} is varied. R_{ON} should be selected such that the on-time at maximum V_{IN} is greater than 150ns. The on-timer has a limiter to ensure a minimum of 150ns for t_{ON}. This limits the maximum operating frequency, which is governed by the following equation:

$$f_{SW(MAX)} = \frac{V_{OUT}}{(V_{IN(MAX)} * 150ns)} \quad (4)$$

This equation can be used to select R_{ON} if a certain operating frequency is desired as long as the minimum on-time of 150ns is observed. The limit for R_{ON} can be calculated as follows:

$$R_{ON} \geq \frac{V_{IN(MAX)} * 150nsec}{(1.3 * 10^{-10})} \quad (5)$$

If R_{ON} calculated in equation (2) is less than the minimum value determined in equation (5) a lower frequency should be selected. Alternatively, $V_{IN(MAX)}$ can also be limited in order to keep the frequency unchanged.
Additionally note, the minimum off-time of 260 ns limits the maximum duty ratio. Larger R_{ON} (lower F_{SW}) should be selected in any application requiring large duty ratio.

Discontinuous Conduction and Continuous Conduction Modes
At light load the regulator will operate in discontinuous conduction mode (DCM). With load currents above the critical conduction point, it will operate in continuous conduction mode (CCM). When operating in DCM the switching cycle begins at zero amps inductor current, increases up to a peak value, and then recedes back to zero before the end of the off-time. Note that during the period of time when the inductor current is zero, all load current is supplied by the output capacitor. The next on-time period starts when the voltage on the FB pin falls below the internal reference. The switching frequency is lower in DCM and varies more with load current as compared to CCM. Conversion efficiency in DCM is maintained since conduction and switching losses are reduced with the smaller load and lower switching frequency. Operating frequency in DCM can be calculated as follows:

$$f_{SW(DCM)} \cong \frac{V_{OUT} * (V_{IN} - 1) * 15\mu H * 1.18 * 10^{20} * I_{OUT}}{(V_{IN} - V_{OUT}) * (R_{ON})^2} \quad (6)$$

In CCM, current flows through the inductor through the entire switching cycle and never falls to zero during the off-time. The switching frequency remains relatively constant with load current and line voltage variations. The CCM operating frequency can be calculated using equation (4) above.

The approximate formula for determining the DCM/CCM boundary is as follows:

$$I_{DCB} \cong \frac{V_{OUT} * (V_{IN} - V_{OUT})}{2 * 15\mu H * f_{SW(CCM)} * V_{IN}} \quad (7)$$

The value of the inductor inside the module is 15µH. This was chosen as a good balance between low and high input voltage applications. The main parameter affected by the inductor is the amplitude of the inductor ripple current (I_{LR}).

I_{LR} peak to peak can be calculated with:

$$I_{LR\ P-P} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{15\mu H * f_{SW} * V_{IN}} \quad (8)$$

Where V_{IN} is the maximum input voltage and f_{SW} is the previously selected value in equation (2).
If the output current I_{OUT} is determined by assuming that $I_{OUT} = I_L$, the higher and lower peak of I_{LR} can be determined. Be aware that the lower peak of I_{LR} must be positive if CCM operation is required.

DESIGN FLOW

Step 3. Select Input Capacitor (C_{IN})

The MagI³C power module contains an internal 0.47µF input ceramic capacitor. Additional input capacitance is required external to the MagI³C power module to handle the input ripple current of the application. This input capacitance should be located as close as possible to the MagI³C power module. Input capacitor selection is generally directed to satisfy the input ripple current requirements rather than by capacitance value. Worst case input ripple current rating is dictated by the equation:

$$I(C_{IN(RMS)}) \approxeq \frac{1}{2} * I_{OUT} * \sqrt{D / (1 - D)} \qquad (9)$$

where $D \approxeq \frac{V_{OUT}}{V_{IN}}$

(As a point of reference, the worst case ripple current will occur when the module is presented with full load current and when $V_{IN} = 2 * V_{OUT}$).

Recommended minimum input capacitance is 10µF X7R ceramic with a voltage rating at least 25% higher than the maximum applied input voltage for the application. It is also recommended that attention be paid to the voltage and temperature deratings of the capacitor selected. It should be noted that ripple current rating of ceramic capacitors may be missing from the capacitor data sheet and you may have to contact the capacitor manufacturer for this rating.

If the system design requires a certain maximum value of input ripple voltage ΔV_{IN} to be maintained then the following equation may be used:

$$C_{IN} \geq \frac{I_{OUT} * D * (1 - D)}{f_{SW-CCM} * \Delta V_{IN}} \qquad (10)$$

If ΔV_{IN} is 1% of V_{IN} for a 24V input to 12V output application this equals 240 mV and f_{SW} = 400 kHz.

$$C_{IN} \geq \frac{1.5A * \frac{12V}{24V} * (1 - \frac{12V}{24V})}{400000 * 0.240V}$$

$$C_{IN} \geq 3.9\mu F$$

Additional bulk capacitance with higher ESR may be required to damp any resonant effects of the input capacitance and parasitic inductance of the incoming supply lines.

DESIGN FLOW

Step 4. Select Output Capacitor (C_{OUT})
None of the required output capacitance is integrated within the module. At a minimum, the output capacitor must meet the worst case RMS current rating of $0.5 * I_{LR\,P-P}$, as calculated in equation (8). Beyond that, additional capacitance will reduce output ripple so long as the ESR is low enough to permit it. A minimum value of 10µF is generally required. Please consider the derating of the nominal capacitance value dependent on the DC voltage applied across it. Experimentation will be required if attempting to operate with a minimum value. Low ESR capacitors, such as ceramic and polymer electrolytic capacitors are recommended.

Capacitance:
The following equation provides a good first pass approximation of C_{OUT} for load transient requirements:

$$C_{OUT} \geq \frac{I_{STEP} * V_{FB} * L * V_{IN}}{4 * V_{OUT} * (V_{IN} - V_{OUT}) * V_{OUT-TRAN}} \qquad (11)$$

For example:
$I_{STEP} = 1.5A, V_{IN} = 24V, V_{OUT} = 12V, V_{OUT-TRAN} = 50mV$

Solving:

$$C_{OUT} \geq \frac{1.5A * 0.8V * 15\mu H * 24V}{4 * 12V * (24V - 12V) * 0.05V}$$

$$C_{OUT} \geq 15\mu F$$

ESR:
The ESR of the output capacitor affects the output voltage ripple. High ESR will result in larger V_{OUT} peak-to-peak ripple voltage. Furthermore, high output voltage ripple caused by excessive ESR can trigger the over-voltage protection monitored at the FB pin. The ESR should be chosen to satisfy the maximum desired V_{OUT} peak-to-peak ripple voltage and to avoid over-voltage protection during normal operation. The following equations can be used:

$$ESR_{MAX-RIPPLE} \leq \frac{V_{OUT-RIPPLE}}{I_{LR\,P-P}} \qquad (12)$$

where $I_{LR\,P-P}$ (peak to peak inductor ripple current) is calculated using equation (8).

$$ESR_{MAX-OVP} < \frac{(V_{FB-OVP} - V_{FB})}{(I_{LR\,P-P} * A_{FB})} \qquad (13)$$

where A_{FB} is the gain of the feedback network from V_{OUT} to V_{FB} at the switching frequency.

As worst case, assume the gain of A_{FB} with the C_{FF} capacitor at the switching frequency is 1.
The selected output capacitor should have sufficient voltage and RMS current rating.
The RMS current is calculated as follows:

$$I(C_{OUT(RMS)}) = \frac{I_{LR\,P-P}}{\sqrt{12}} \qquad (14)$$

DESIGN FLOW

Step 5. Select Soft-Start Capacitor (C_{SS})

Programmable soft-start permits the regulator to slowly ramp to its steady state operating point after being enabled, thereby reducing current inrush from the input supply and slowing the output voltage rise-time to prevent overshoot. Upon turn-on, after all UVLO conditions have been passed, an internal 8µA current source begins charging the external soft-start capacitor. The soft-start capacitor can be calculated with:

$$C_{SS} = t_{SS} * \frac{8\mu A}{0.8V} \quad (15)$$

with t_{ss} = select soft-start time in (ms)

The use of a 4.7nF capacitor results in 0.5ms soft-start duration. This is a recommended minimum value.
As the soft-start input exceeds 0.8V the output of the power stage will be in regulation. The soft-start capacitor continues charging until it reaches approximately 3.8V on the SS pin. Voltage levels between 0.8V and 3.8V have no effect on other circuit operation.
Note that high values of the C_{SS} capacitance will cause more output voltage droop when a load transient goes across the DCM-CCM boundary. Use equation (7) to find the DCM-CCM boundary load current for the specific operating condition. If a fast load transient response is desired for steps between DCM and CCM mode the soft-start capacitor value should be less than 0.018µF. Note that the following conditions will reset the soft-start capacitor by discharging the SS input to ground with an internal 200µA current sink:

1. The enable input being “pulled low”
2. Thermal shutdown condition
3. Over-current fault
4. Internal VIN_{UVLO}

Step 6. Select Feed Forward Capacitor (C_{FF})

A feed-forward capacitor C_{FF} is placed in parallel with R_{FBT} which bypasses AC ripple directly to the feedback pin from the output to support the internal ripple generator. This capacitor also affects load step transient response. Its value is usually determined experimentally by load stepping between DCM and CCM conduction modes and adjusting for best transient response and minimum output ripple. A value of 22nF has been practically evaluated as best performing. The feed forward capacitor C_{FF}, should be located close to the FB pin.

Step 7. Optional: Select Enable Divider, R_{ENT}, R_{ENB}

The enable input provides a precise 1.18V reference threshold to allow direct logic drive or connection to a voltage divider from a higher enable voltage such as V_{IN}. The enable input also incorporates 90mV (typ) of hysteresis resulting in a falling threshold of 1.09V. The maximum recommended voltage into the EN pin is 6.5V. For applications where the midpoint of the enable divider exceeds 6.5V, a small zener diode can be added to limit this voltage.
The function of the R_{ENT} and R_{ENB} divider shown in the application block diagram is to allow the designer to choose an input voltage below which the circuit will be disabled. This implements the feature of programmable external under voltage lockout. This is often used in battery powered systems to prevent deep discharge of the system battery. It is also useful in system designs for sequencing of output rails or to prevent early turn-on of the supply as the main input voltage rail rises at power-up. Most systems will benefit by using the precision Enable threshold to establish a system under voltage lockout. The recommended approach is to choose an input UVLO level that is higher than the target regulated output voltage for the stage. Without an Enable divider, this series of devices will attempt to turn on around 3.5 Vin. This would not be useful for a stage that ultimately might be creating 5Vout. Operation of the module on input voltage conditions below the nominal output should be avoided. Systems that don't implement the Enable divider will turn in early during the rise of Vin and might not have monotonic rise in output voltage. Many systems need smooth rise in supply voltage. In the case of sequencing supplies, the divider is connected to a rail that becomes active earlier in the power-up cycle than the MagI³C power module output rail. The two resistors should be chosen based on the following ratio:

DESIGN FLOW

$$\frac{R_{ENT}}{R_{ENB}} = \frac{V_{UVLO\ (EXTERN)}}{1.18V} - 1 \qquad (16)$$

$V_{UVLO\ (EXTERN)}$ = User programmable voltage threshold to turn the module ON/OFF.

The EN pin is internally pulled up to V_{IN} and can be left floating for always-on operation. However, it is good practice to use the enable divider and turn on the regulator when V_{IN} is close to reaching its nominal value. This will guarantee smooth startup and will prevent overloading the input supply.

Determine power losses and thermal requirements of the board

For example:

$V_{IN} = 24V, V_{OUT} = 12V, I_{OUT} = 1.5A, T_{AMB(MAX)} = 85°C$ and $T_{J(MAX)} = 125°C$

$T_{AMB(MAX)}$ is the maximum air temperature surrounding the module.
$T_{J(MAX)}$ is the maximum value of the junction temperature according to the “OPERATING CONDITIONS” limit.

The goal of the calculation is to determine the characteristics of the required heat sink. In case of a surface mounted module this would be the PCB (number of layers, copper area and thickness). These characteristics are reflected in the value of the thermal resistance case to ambient: Θ_{CA}.

The basic formula for calculating the operating junction temperature T_J of a semiconductor device is as follows:

$$T_J = P_{IC-Loss} * \theta_{JA} + T_{AMB} \qquad (17)$$

$P_{IC-LOSS}$ are the total power losses within the module IC and are related to the operating conditions.
Θ_{JA} is the thermal resistance junction to ambient and calculated as:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \qquad (18)$$

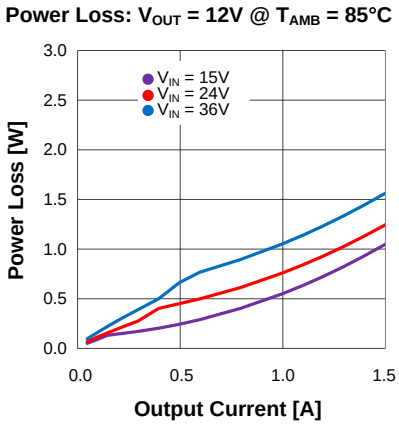
Θ_{JC} is the thermal resistance junction to case.

Combining equation (17) and (18) results in the maximum case-to-ambient thermal resistance:

$$\theta_{CA(MAX)} < \frac{T_{J-MAX} - T_{AMB(MAX)}}{P_{IC-Loss}} - \theta_{JC} \qquad (19)$$

From section ”THERMAL SPECIFICATIONS“ the typical thermal resistance from junction to case (Θ_{JC}) is defined as 1.9 °C/W. Use the 85°C power dissipation curves in the “TYPICAL PERFORMANCE CURVES“ section to estimate the $P_{IC-LOSS}$ for the application being designed.

DESIGN FLOW

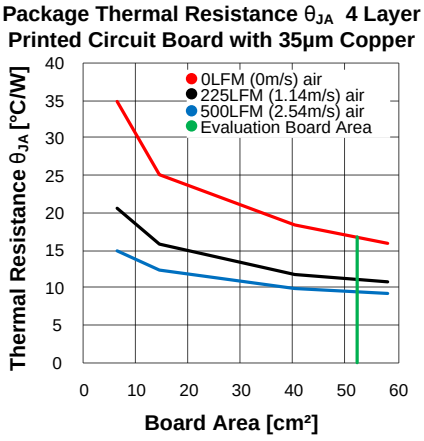


From the graph we read a power loss of 1.2W. Entering the values in formula (19) results in:

$$\theta_{CA(MAX)} < \frac{125°C - 85°C}{1.2W} - 1.9°C/W = 31.4°C/W$$

$$\theta_{JA(MAX)} = \theta_{JC} + \theta_{CA(MAX)} = 1.9°C/W + 15.2°C/W = 33.3°C/W$$

To achieve this thermal resistance the PCB is required to dissipate the heat effectively. The area of the PCB will have a direct effect on the overall junction-to-ambient thermal resistance. In order to estimate the necessary copper area we can refer to the following package thermal resistance graph. This graph is taken from the “TYPICAL PERFORMANCE CURVES“ section and shows how the θ_{JA} varies with the PCB area.



For $\theta_{JA} < 33.3°C/W$ and only natural convection (i.e. no air flow), the minimum PCB area can be smaller than 10cm^2. This corresponds to a square board with 5.5cm x 5.5cm copper area, 4 layers, and 35µm copper thickness. Higher copper thickness will further improve the overall thermal performance. Note that thermal vias should be placed under the IC package to easily transfer heat from the top layer of the PCB to the inner layers and the bottom layer.

Light Load Operation:

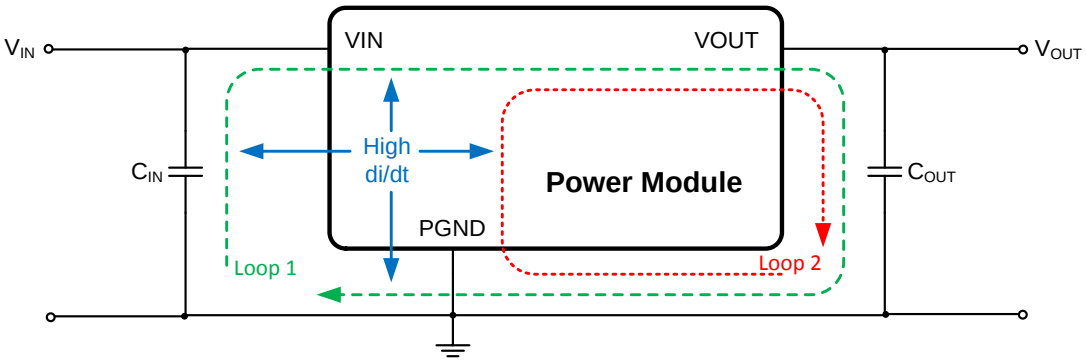
At light load the device continuously decreases the switching frequency and thereby maintains a high efficiency.
The ripple is slightly increasing in this mode of operation but still small due to no burst mode operation. See waveforms in section “TYPICAL PERFORMANCE CURVES”. No minimum load is required.

DESIGN FLOW

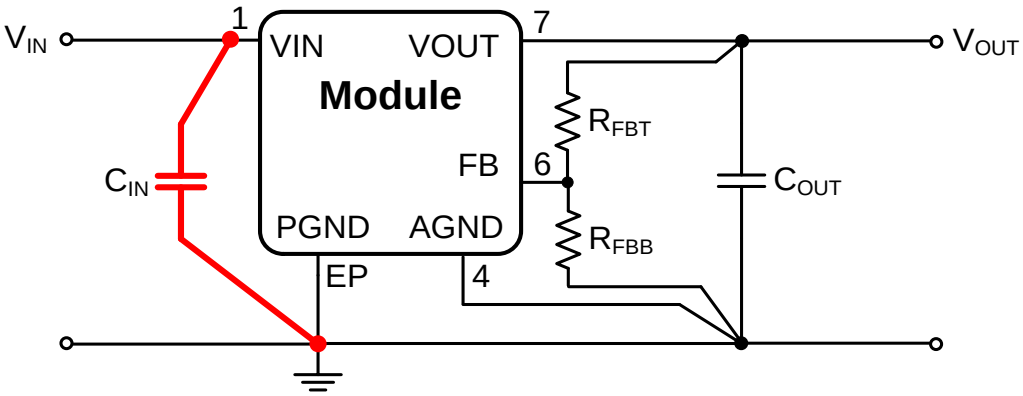
PCB Layout Instructions:

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce and resistive voltage drop in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following five simple design rules.

1: Minimize area of switched current loops.



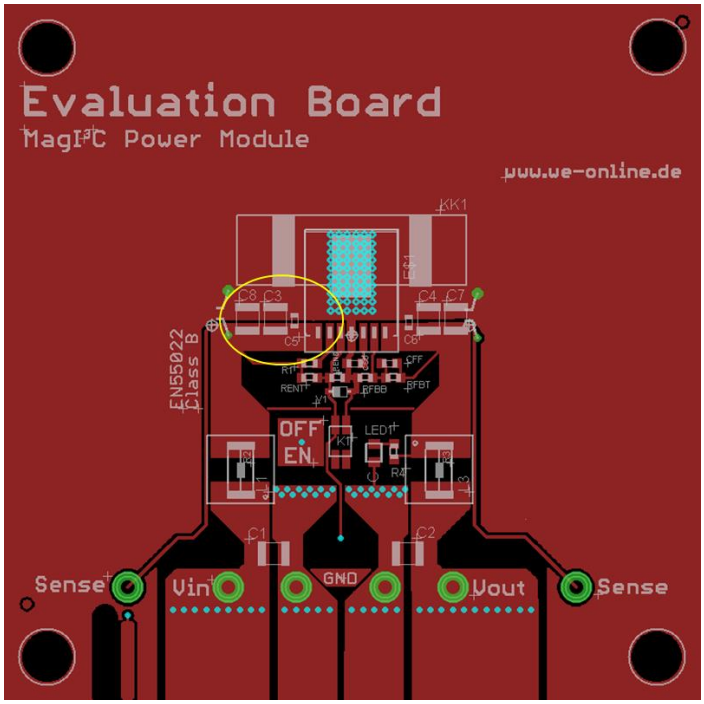
Target is to identify the paths in the system which have discontinuous current flow. They are the most critical ones because they act as an antenna and cause observable high frequency noise (EMI). The easiest approach to find the critical paths is to draw the high current loops during both switching cycles and identify the sections which do not overlap. They are the ones where no continuous current flows and high di/dt is observed. Loop1 is the current path during the ON-time of the High-Side Mosfet. Loop2 is the current path during the OFF-time of the High-Side Mosfet.



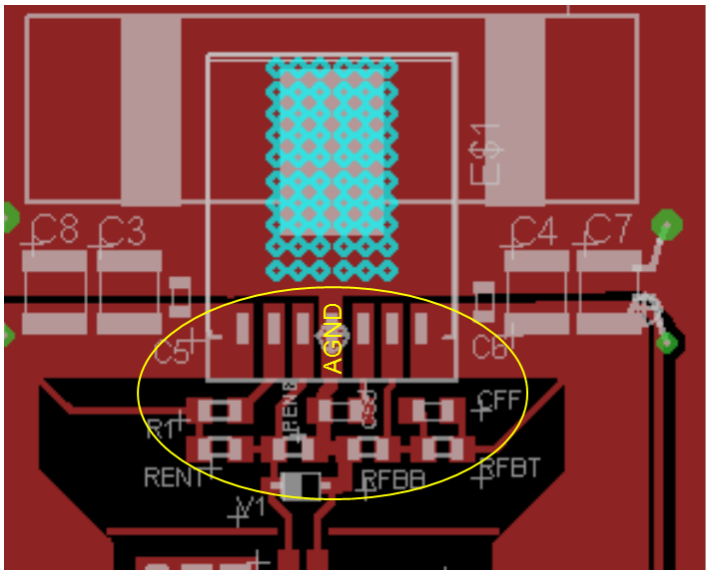
Based on those considerations, the path of the input capacitor C_{IN} is the most critical one to generate high frequency noise on Vin. Therefore place C_{IN} as close as possible to the MagI³C power module V_{IN} and PGND exposed pad EP. This will minimize the high di/dt area and reduce radiated EMI. Additionally, grounding for both the input and output capacitor should consist of a localized top side plane that connects to the PGND exposed pad.

DESIGN FLOW

The placement of the input capacitors is highlighted in the following picture of the evaluation board:

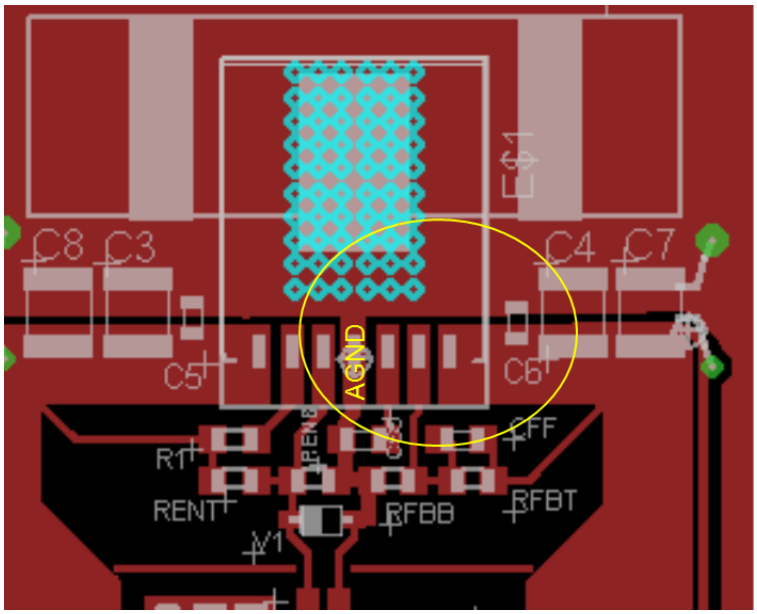


2: Have a single point ground.
The ground connections for the feedback, soft-start, and enable components should be routed to the AGND pin of the device. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior.

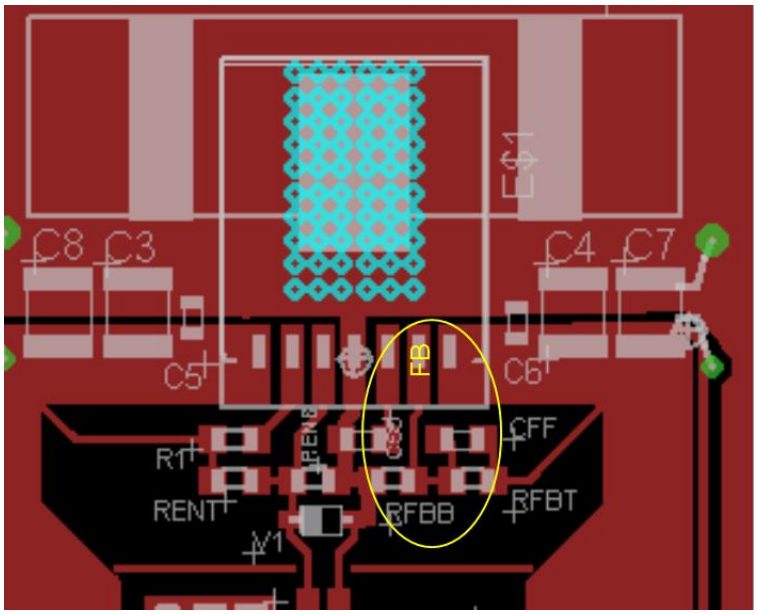


DESIGN FLOW

Provide the single point ground connection from AGND pin 4 to the GND terminal of the output capacitor. This is the point of lowest noise.



3: Minimize trace length to the FB pin.
The feedback resistors, R_{FBT} and R_{FBB}, and the feed forward capacitor C_{FF}, should be located close to the FB pin. Since the FB node is high impedance, maintain the copper area as small as possible. The traces from R_{FBT}, R_{FBB}, and C_{FF} should be routed away from the body of the MagI³C power module to minimize noise pickup.

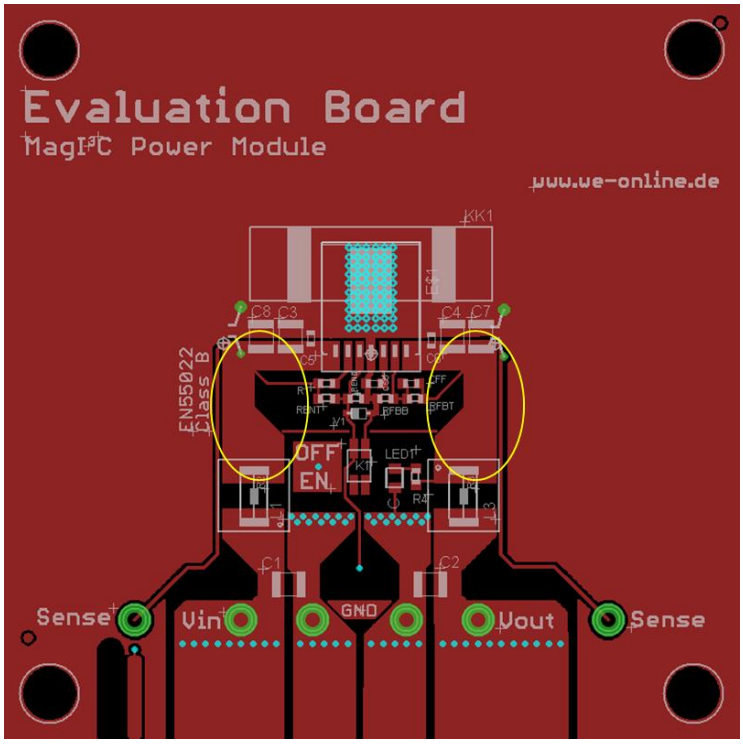


WPMDH1152401 / 171012402

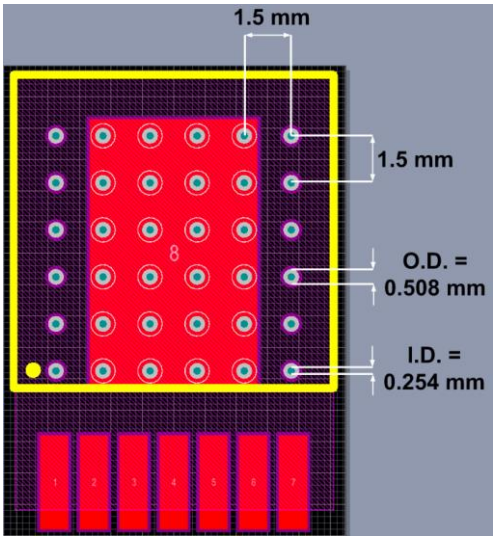
MagI³C Power Module
VDRM - Variable Step Down Regulator Module

DESIGN FLOW

4: Make input and output bus connections as wide as possible.
This reduces any voltage drops on the input or output of the converter and maximizes efficiency.



5: Provide adequate device heat-sinking.
Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has a plurality of copper layers, these thermal vias can also be used to make connection to inner layer heat-spreading ground planes. For best results use a 6 x 6 via array with minimum via diameter of 254µm thermal vias spaced 1.5mm. Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.



PROTECTIVE FEATURES

Output Over-voltage protection (OVP)

The voltage at FB is compared to a 0.8V internal reference. The over-voltage protection (OVP) has a threshold of 0.92V. If FB rises above this limit, the on-time is immediately terminated. It can occur if the input voltage is increased very suddenly or if the output load is decreased very suddenly. Once OVP is activated, the top MOSFET on-times will be inhibited until the condition clears. Additionally, the synchronous MOSFET will remain on until inductor current falls to zero.

Over current protection (OCP)

Current limit detection is carried out during the off-time by monitoring the current in the synchronous MOSFET. Referring to the Functional Block Diagram, when the top MOSFET is turned off, the inductor current flows through the load, the PGND pin and the internal synchronous MOSFET. If this current exceeds the I_{CL} value, the current limit comparator disables the start of the next on-time period. The next switching cycle will occur only if the FB input is less than 0.8V and the inductor current has decreased below I_{CL}. Inductor current is monitored during the period of time the synchronous MOSFET is conducting. As long as the inductor current exceeds I_{CL}, further on-time intervals for the top MOSFET will not occur. Switching frequency is lower during current limit due to the longer off-time. It should also be noted that DC current limit varies with duty cycle, switching frequency, and temperature.

The values of the current limits during short circuit are visualized in the graph in the “TYPICAL PERFORMANCE” section. The green curve with the reference “Max load current” represents the output current limit at which the output voltage is still in full regulation at nominal value. A further increase of the load current will cause a drop of the output voltage.

Over temperature protection (OTP)

The junction temperature of the MagI³C power module should not be allowed to exceed its maximum ratings. Thermal protection is implemented by an internal thermal shutdown circuit which activates at 165°C (typ.) causing the device to enter a low power standby state. In this state the main MOSFET remains off causing V_{OUT} to fall, and additionally the C_{SS} capacitor is discharged to ground. Thermal protection helps to prevent catastrophic failures in case of accidental device overheating. When the junction temperature falls back below 145°C (typical hysteresis = 20°C) the SS pin is released, V_{OUT} rises smoothly, and normal operation resumes.

Zero coil current detection (ZCCT)

The current of the lower (synchronous) MOSFET is monitored by a zero coil current detection circuit which inhibits the synchronous MOSFET when its current reaches zero until the next on-time. This circuit enables the DCM operating mode, which improves efficiency at light loads.

Output under-voltage protection (UVP)

The MagI³C power module will properly start up into a pre-biased output. This startup situation is common in multiple rail logic applications where current paths may exist between different power rails during the startup sequence. The pre-bias level of the output voltage must be less than the input UVLO set point. This will prevent the output pre-bias from enabling the regulator through the high side MOSFET body diode.

WPMDH1152401 / 171012402

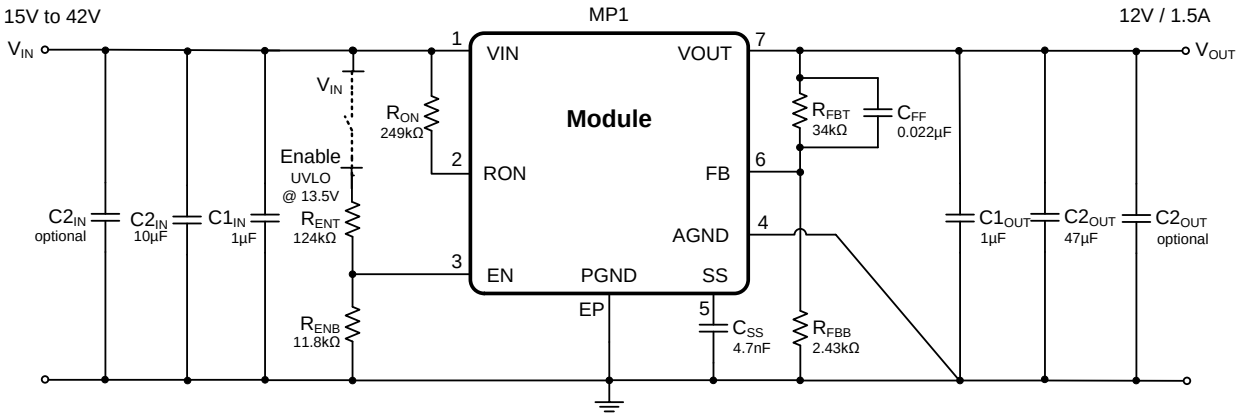
MagI³C Power Module

VDRM - Variable Step Down Regulator Module

APPLICATIONS

The MagI³C power module for high output voltage is an easy-to-use DC-DC solution capable of driving up to a 2A load with exceptional power conversion efficiency, output voltage accuracy, line and load regulation. It is available in an innovative package that enhances thermal performance and allows hand or machine soldering. Following application circuits show possible operating configurations.

Application Circuit



Bill of Materials for Design Example 1:

Recommended component values specified at T_A = 25°C

Ref Designator	Description	Case Size	Part
MP1	MagI³C Power Module	TO263-7EP	WE MagI³C Power Module
$C1_{IN}$, $C1_{OUT}$	1µF, 50V, X7R, ±10%	1206	Capacitor
$C2_{IN}$	10µF, 50V, X5R, ±20%	1210	Capacitor
$C2_{OUT}$	47µF, 35mΩ, 16V, ±20%	1210	Capacitor
C_{FF}	0.022µF, 100V, X7R, ±10%	0805	Capacitor
C_{SS}	4.7nF, 25V, X7R, ±10%	0805	Capacitor
R_{ENB}	11.8kΩ, ±1%	0805	Resistor
R_{ENT}	124kΩ, ±1%	0805	Resistor
R_{FBT}	34kΩ, ±1%	0805	Resistor
R_{FBB}	2.43kΩ, ±1%	0805	Resistor
R_{ON}	249kΩ, ±1%	0805	Resistor

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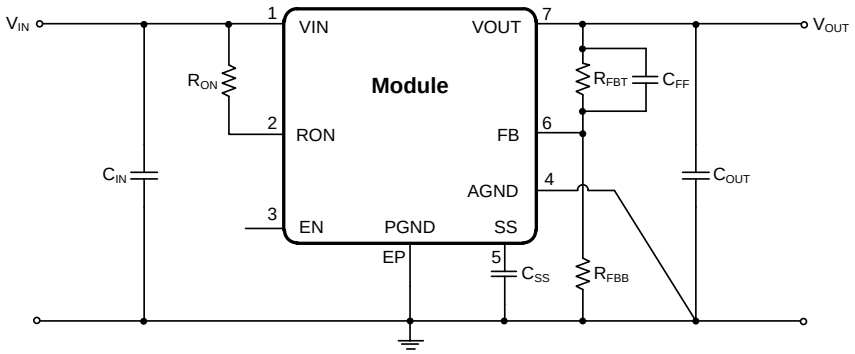
MagI³C Power Module

VDRM - Variable Step Down Regulator Module

Application Circuit



Bill of Materials for Design Example 2:

V_{out}	24V	18V	15V	12V	5V
R_{FBT}	34kΩ	34kΩ	34kΩ	34kΩ	34kΩ
R_{FBB}	1.18kΩ	1.58kΩ	1.91kΩ	2.43kΩ	6.49kΩ
R_{ON}	499kΩ	374kΩ	287kΩ	249kΩ	100kΩ
C_{IN}	10µF				
C_{OUT}	33µF	33µF	47µF	47µF	100µF
C_{SS}	4700pF				
C_{FF}	0.022µF				
$C_{OUT-ESR}$	1-75mΩ	1-60mΩ	1-65mΩ	1-75mΩ	1-145mΩ
V_{IN}	28-42V	22-42V	18-42V	15-42V	8-42V

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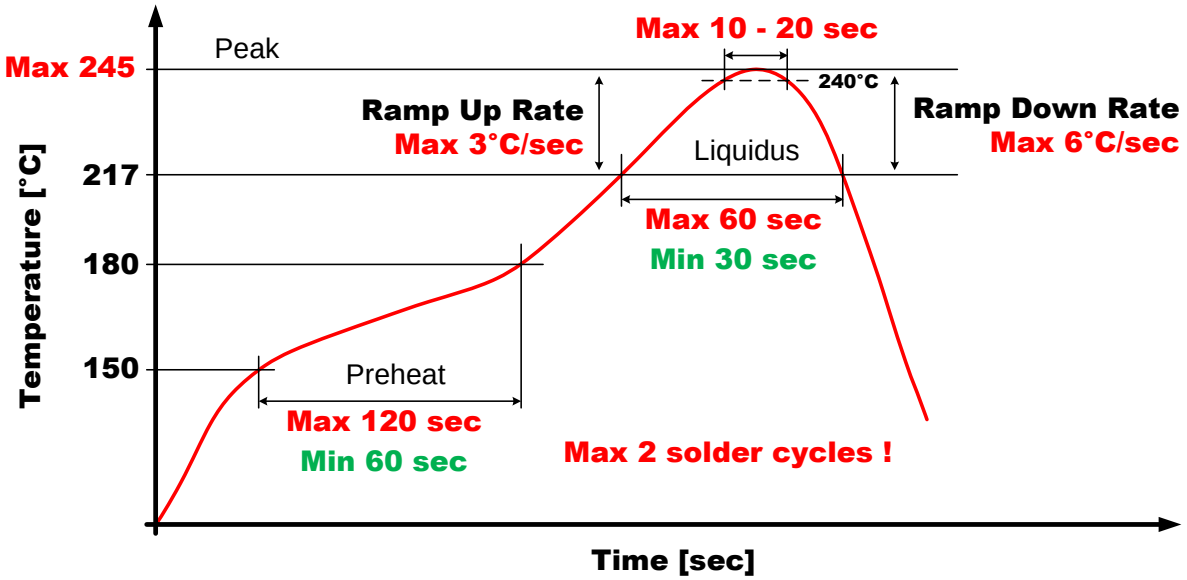
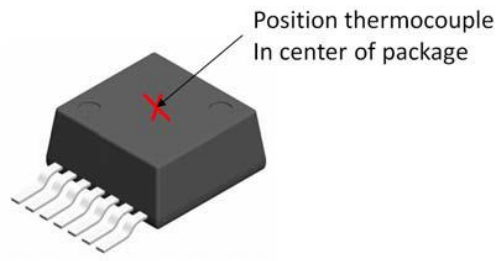
HANDLING RECOMMENDATIONS

1. The power module is classified as MSL3 (JEDEC Moisture Sensitivity Level 3) and requires special handling due to moisture sensitivity (JEDEC J-STD033).
2. The parts are delivered in a sealed bag (Moisture Barrier Bags = MBB) and should be processed within one year.
3. When opening the moisture barrier bag check the Humidity Indicator Card (HIC) for color status. Bake parts prior to soldering in case indicator color has changed according to the notes on the card .
4. Parts must be processed after 168 hour (7 days) of floor life. Once this time has been exceeded, bake parts prior to soldering per JEDEC J-STD033 recommendation.

SOLDER PROFILE

1. Only Pb-Free assembly is recommended according to JEDEC J-STD020.
2. Measure the peak reflow temperature of the MagI³C power module in the middle of the top view.
3. Ensure that the peak reflow temperature does not exceed 240°C ±5°C as per JEDEC J-STD020.
4. The reflow time period during peak temperature of 240°C ±5°C must not exceed 20 seconds.
5. Reflow time above liquidus (217°C) must not exceed 60 seconds.
6. Maximum ramp up is rate 3°C per second
7. Maximum ramp down rate is 6°C per second
8. Reflow time from room (25°C) to peak must not exceed 8 minutes as per JEDEC J-STD020.
9. **Maximum numbers of reflow cycles is two**.
10. **For minimum risk, solder the module in the last reflow cycle of the PCB production.**
11. For soldering process please consider lead material copper (Cu) and lead finish tin (Sn).
12. For solder paste use a standard SAC Alloy such as SAC 305, type 3 or higher.
13. Below profile is valid for convection reflow only
14. Other soldering methods (e.g.vapor phase) are not verified and have to be validated by the customer on his own risk





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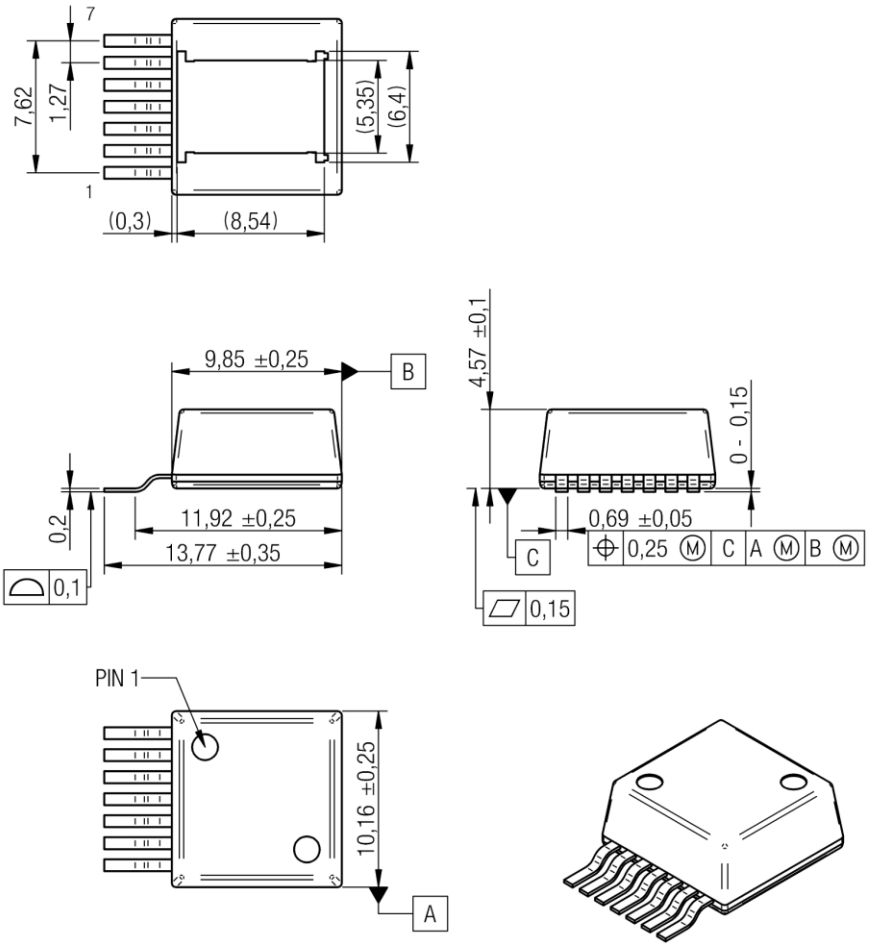
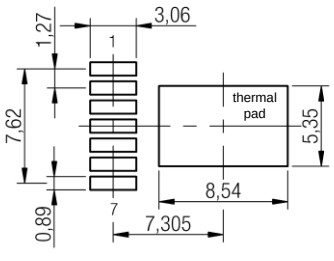
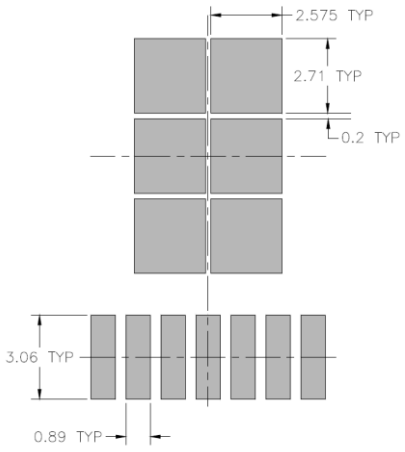
PHYSICAL DIMENSIONS (mm)

Package Type: TO263-7





recommended soldering pad



recommended stencil design
solder paste recommendation 150µm

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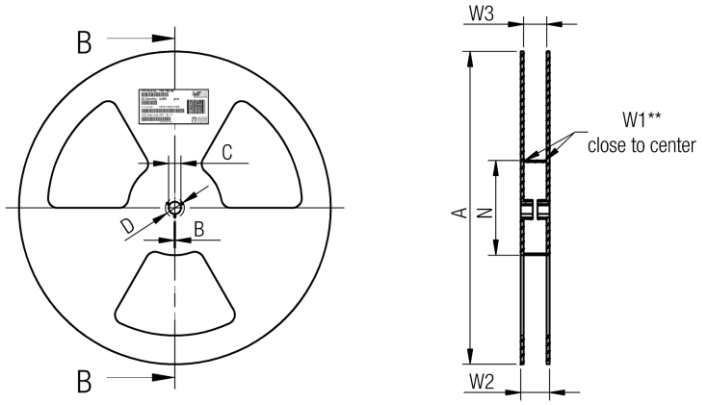
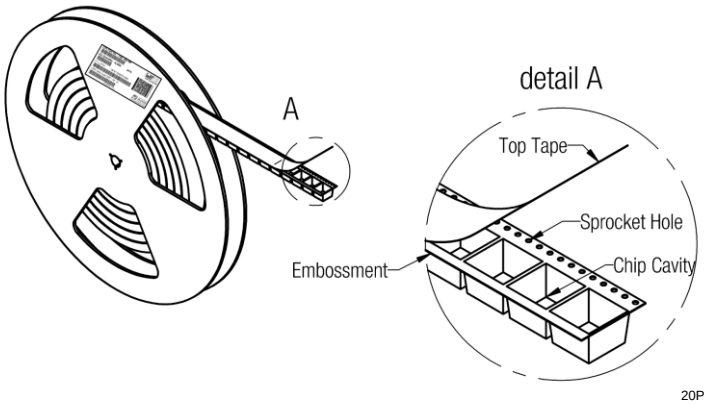
PACKAGING

Reel (mm)



		A	B	C	D	N	W1	W2	W3	W3
tolerance		± 2,0	min.	± 0,8	min.	± 2,0	+ 2	max.	min.	max.
Tape width	**24mm**	330,00	1,50	13,00	20,20	60,00	24,40	30,40	23,90	27,40



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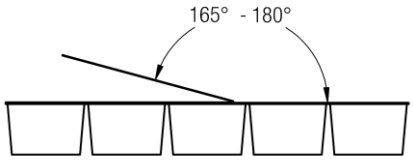
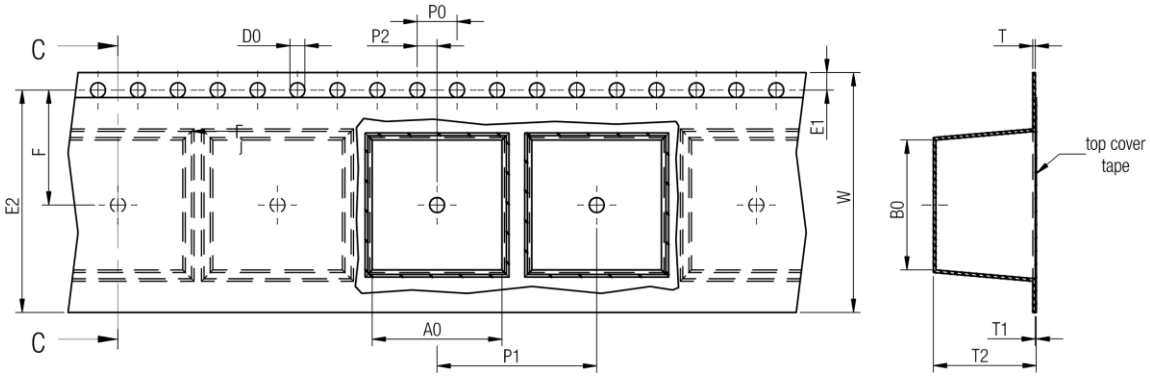
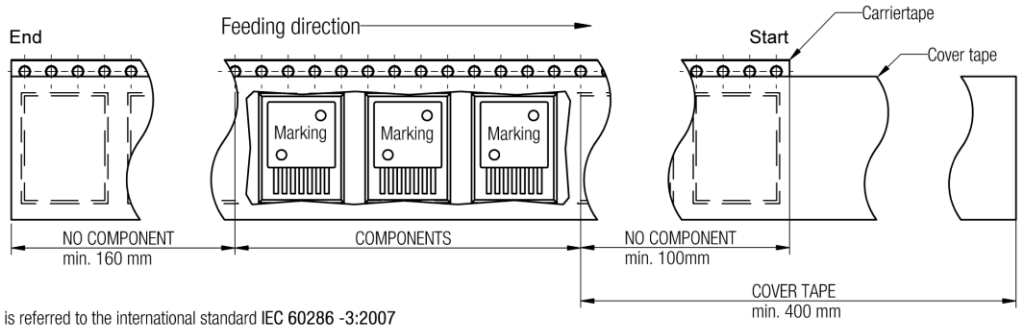
Tape (mm)



		Pull-of force
Tape width	**24 mm**	0,1 N - 1,3 N



		A0	B0	W	P1	T	T1	T2	D0	E1	E2	F	P0	P2	Tape	VPE / packaging unit
tolerance		typ.	typ.	+0,3 -0,1	± 0,1	± 0,1	max.	typ.	+0,3 -0,1	± 0,1	min.	± 0,05	± 0,1	± 0,05		
size	TO263-7EP	10,60	14,22	24,00	16,00	0,50	0,10	5,00	1,50	1,75	22,25	11,50	4,00	2,00	Polystyrene	250



Packaging is referred to the international standard IEC 60286 -3:2007

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DOCUMENT HISTORY

Revision	Date	Description	Page
1.0	10.03.2015	Release of final version	

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MagI³C Power Module
VDRM - Variable Step Down Regulator Module

CAUTIONS AND WARNINGS

The following conditions apply to all goods within the product series of MagI³C of Würth Elektronik eiSos GmbH & Co. KG:

General:
All recommendations according to the general technical specifications of the data-sheet have to be complied with.

The usage and operation of the product within ambient conditions which probably alloy or harm the component surface has to be avoided.

The responsibility for the applicability of customer specific products and use in a particular customer design is always within the authority of the customer. All technical specifications for standard products do also apply for customer specific products.

Residual washing varnish agent that is used during the production to clean the application might change the characteristics of the body, pins or termination. The washing varnish agent could have a negative effect on the long term function of the product.
Direct mechanical impact to the product shall be prevented as the material of the body, pins or termination could flake or in the worst case it could break. As these devices are sensitive to electrostatic discharge customer shall follow proper IC Handling Procedures.

Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Würth Elektronik eiSos GmbH & Co. KG components in its applications, notwithstanding any applications-related information or support that may be provided by Würth Elektronik eiSos GmbH & Co. KG. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Customer will fully indemnify Würth Elektronik eiSos and its representatives against any damages arising out of the use of any Würth Elektronik eiSos GmbH & Co. KG components in safety-critical applications.

Product specific:
Follow all instructions mentioned in the datasheet, especially:

- The solder profile has to comply with the technical reflow or wave soldering specification, otherwise this will void the warranty.
- All products are supposed to be used before the end of the period of 12 months based on the product date-code.
- Violation of the technical product specifications such as exceeding the absolute maximum ratings will void the warranty.
- It is also recommended to return the body to the original moisture proof bag and reseal the moisture proof bag again.
- ESD prevention methods need to be followed for manual handling and processing by machinery.

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VDRM - Variable Step Down Regulator Module

IMPORTANT NOTES

The following conditions apply to all goods within the product range of Würth Elektronik eiSos GmbH & Co. KG:

1. General Customer Responsibility
Some goods within the product range of Würth Elektronik eiSos GmbH & Co. KG contain statements regarding general suitability for certain application areas. These statements about suitability are based on our knowledge and experience of typical requirements concerning the areas, serve as general guidance and cannot be estimated as binding statements about the suitability for a customer application. The responsibility for the applicability and use in a particular customer design is always solely within the authority of the customer. Due to this fact it is up to the customer to evaluate, where appropriate to investigate and decide whether the device with the specific product characteristics described in the product specification is valid and suitable for the respective customer application or not. Accordingly, the customer is cautioned to verify that the datasheet is current before placing orders.

2. Customer Responsibility related to Specific, in particular Safety-Relevant Applications
It has to be clearly pointed out that the possibility of a malfunction of electronic components or failure before the end of the usual lifetime cannot be completely eliminated in the current state of the art, even if the products are operated within the range of the specifications. In certain customer applications requiring a very high level of safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health it must be ensured by most advanced technological aid of suitable design of the customer application that no injury or damage is caused to third parties in the event of malfunction or failure of an electronic component.

3. Best Care and Attention
Any product-specific notes, warnings and cautions must be strictly observed.

4. Customer Support for Product Specifications
Some products within the product range may contain substances which are subject to restrictions in certain jurisdictions in order to serve specific technical requirements. Necessary information is available on request. In this case the field sales engineer or the internal sales person in charge should be contacted who will be happy to support in this matter.

5. Product R&D
Due to constant product improvement product specifications may change from time to time. As a standard reporting procedure of the Product Change Notification (PCN) according to the JEDEC-Standard we inform about minor and major changes. In case of further queries regarding the PCN, the field sales engineer or the internal sales person in charge should be contacted. The basic responsibility of the customer as per Section 1 and 2 remains unaffected.

6. Product Life Cycle
Due to technical progress and economical evaluation we also reserve the right to discontinue production and delivery of products. As a standard reporting procedure of the Product Termination Notification (PTN) according to the JEDEC-Standard we will inform at an early stage about inevitable product discontinuance. According to this we cannot guarantee that all products within our product range will always be available. Therefore it needs to be verified with the field sales engineer or the internal sales person in charge about the current product availability expectancy before or when the product for application design-in disposal is considered. The approach named above does not apply in the case of individual agreements deviating from the foregoing for customer-specific products.

7. Property Rights
All the rights for contractual products produced by Würth Elektronik eiSos GmbH & Co. KG on the basis of ideas, development contracts as well as models or templates that are subject to copyright, patent or commercial protection supplied to the customer will remain with Würth Elektronik eiSos GmbH & Co. KG. Würth Elektronik eiSos GmbH & Co. KG does not warrant or represent that any license, either expressed or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, application, or process in which Würth Elektronik eiSos GmbH & Co. KG components or services are used.

8. General Terms and Conditions
Unless otherwise agreed in individual contracts, all orders are subject to the current version of the “General Terms and Conditions of Würth Elektronik eiSos Group”, last version available at www.we-online.com.