

Product Description

The PE43501 is a HaRP™-enhanced, high linearity, 5-bit RF Digital Step Attenuator (DSA). This highly versatile DSA covers a 7.75 dB attenuation range in 0.25 dB steps. The Peregrine 50Ω RF DSA provides a serial-addressable CMOS control interface. It maintains high attenuation accuracy over frequency and temperature and exhibits very low insertion loss and low power consumption. Performance does not change with V_{dd} due to on-board regulator. This next generation Peregrine DSA is available in a 5x5 mm 32-lead QFN footprint.

The PE43501 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Package Type

32-lead 5x5x0.85 mm QFN Package

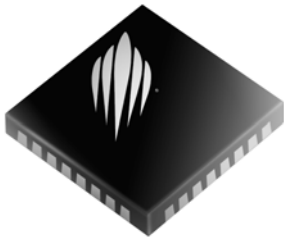
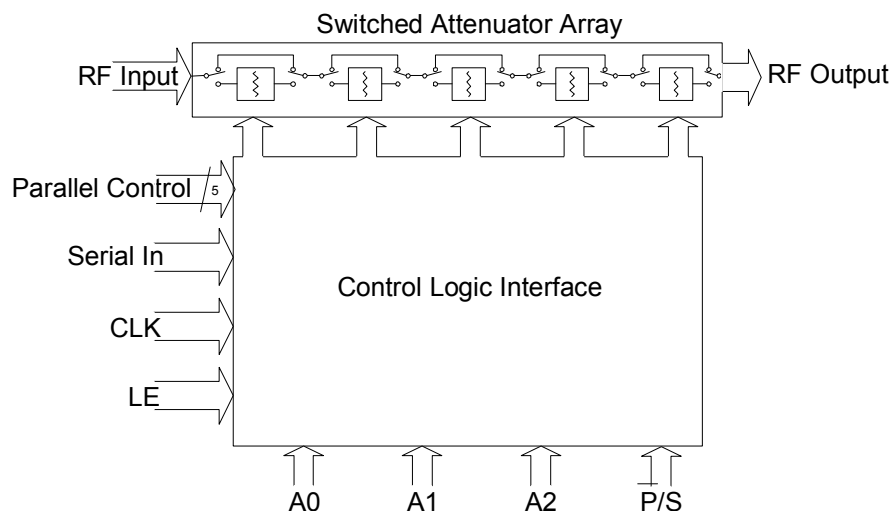


Figure 2. Functional Schematic Diagram



50 Ω RF Digital Attenuator
5-bit, 7.75 dB, DC-6.0 GHz

Features

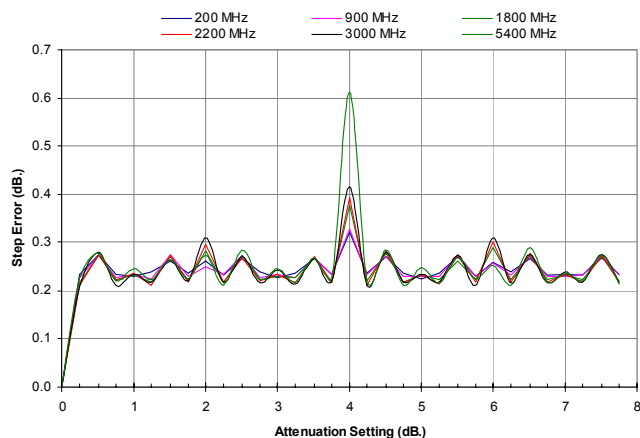
- HaRP™-enhanced UltraCMOS™ device
- Attenuation: 0.25 dB steps to 7.75 dB
- High Linearity: Typical +58 dBm IP3
 - Excellent low-frequency performance
- 3.3 V or 5.0 V Power Supply Voltage
- Fast switch settling time
- Programming Modes:
 - Direct Parallel
 - Latched Parallel
 - Serial-Addressable: Program up to eight addresses 000 - 111
- High-attenuation state @ power-up (PUP)
- CMOS Compatible
- No DC blocking capacitors required
- Packaged in a 32-lead 5x5x0.85 mm QFN

Table 1. Electrical Specifications @ +25°C, V_{DD} = 3.3 V or 5.0 V

Parameter	Test Conditions	Frequency	Min	Typical	Max	Units
Frequency Range				DC – 6		GHz
Attenuation Range	0.25 dB Step			0 – 7.75		dB
Insertion Loss		DC ≤ 6 GHz		2.3	2.8	dB
Attenuation Error	0 dB - 7.75 dB Attenuation settings	DC < 4 GHz			±(0.15+4%)	dB
	0dB to 3.5 dB Attenuation Settings	4 GHz ≤ 6 GHz			+0.2+4%	dB
	3.75 dB to 7.75 dB Attenuation Settings	4 GHz ≤ 6 GHz			+0.3+4%	dB
	0dB to 7.75dB Attenuation Settings	4 GHz ≤ 6 GHz			-0.2 - 4%	dB
Return Loss		DC - 6 GHz		18		dB
Relative Phase	All States	DC - 6 GHz		9		deg
P1dB	Input	20 MHz - 6 GHz	30	32		dBm
IIP3	Two tones at +18 dBm, 20 MHz spacing	20 MHz - 6 GHz		58		dBm
Typical Spurious Value		1 MHz		-110		dBm
Video Feed Through				10		mVpp
Switching Time	50% CTRL to 10% / 90% RF			650		ns
RF Trise/Tfall	10% / 90% RF			400		ns
Settling Time	RF settled to within 0.05 dB of final value RBW = 5 MHz, Averaging ON.			4		μs

Performance Plots

Figure 3. 0.25 dB Step Error vs. Frequency*



*Monotonicity is held so long as step-error does not cross zero.

Figure 5. 0.25 dB Major State Bit Error

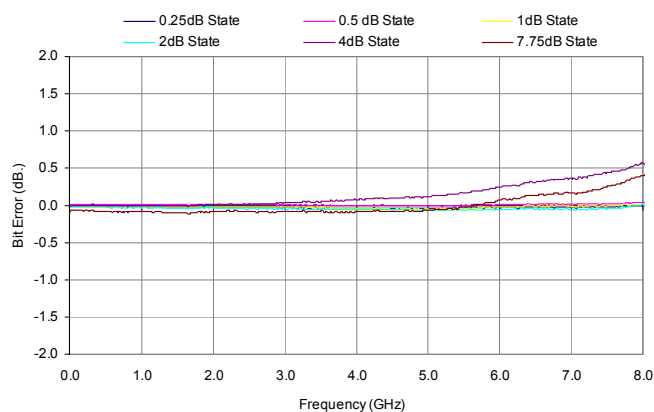


Figure 4. 0.25dB Attenuation vs. Attenuation State

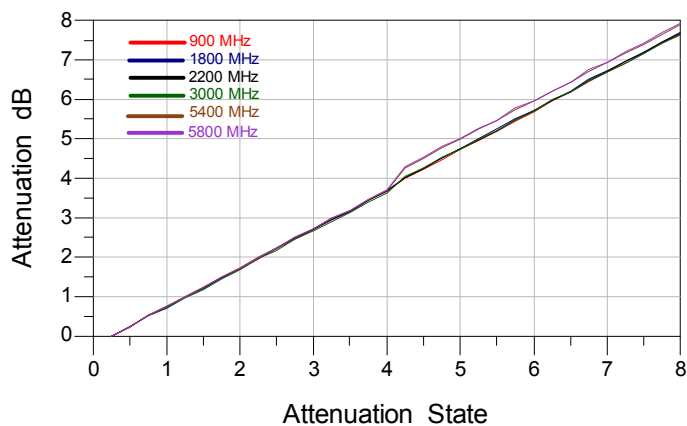


Figure 6. 0.25 dB Attenuation Error vs. Frequency

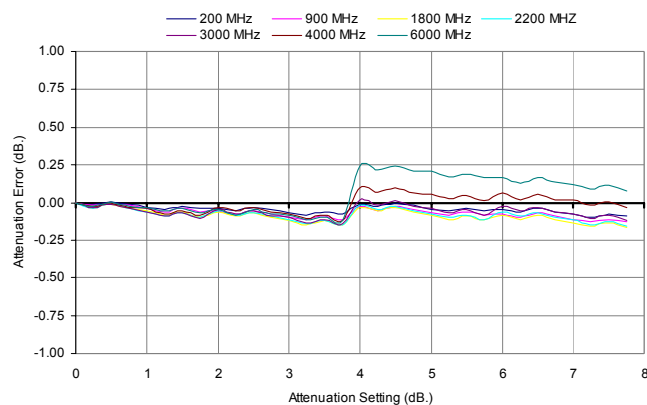


Figure 7. Insertion Loss vs. Temperature

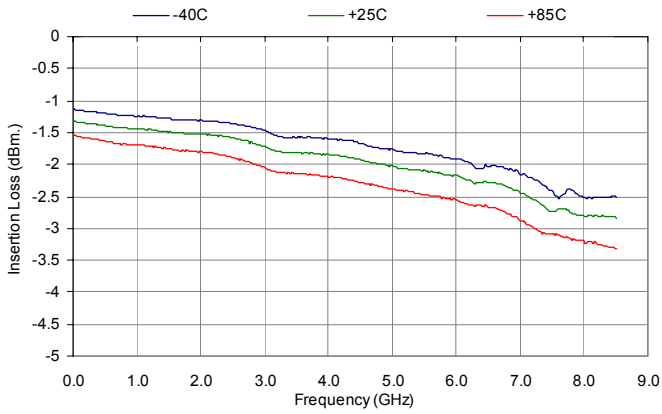


**Figure 8. Input Return Loss vs. Attenuation:
T = +25C**

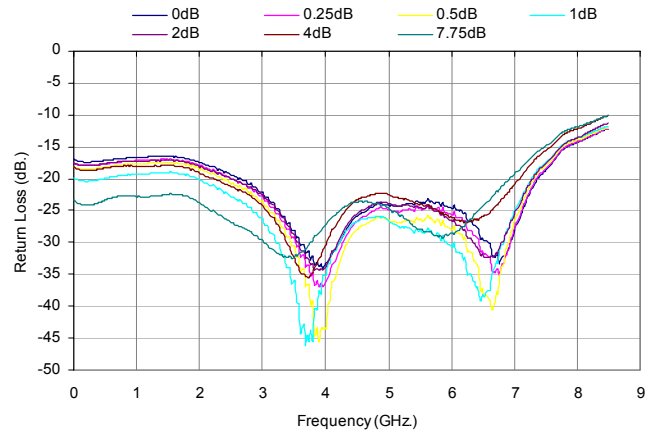


**Figure 9. Output Return Loss vs. Attenuation:
T = +25C**

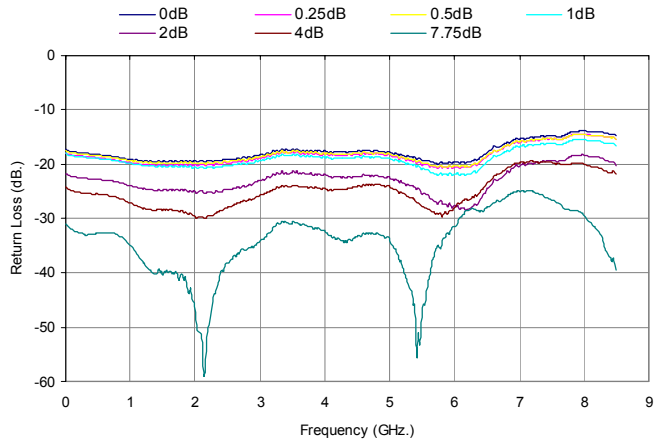


**Figure 10. Input Return Loss vs. Temperature:
7.75 dB State**

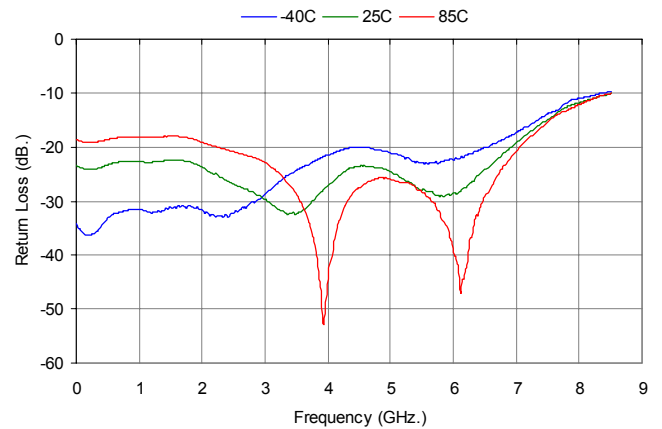


**Figure 11. Output Return Loss vs. Temperature:
7.75 dB State**

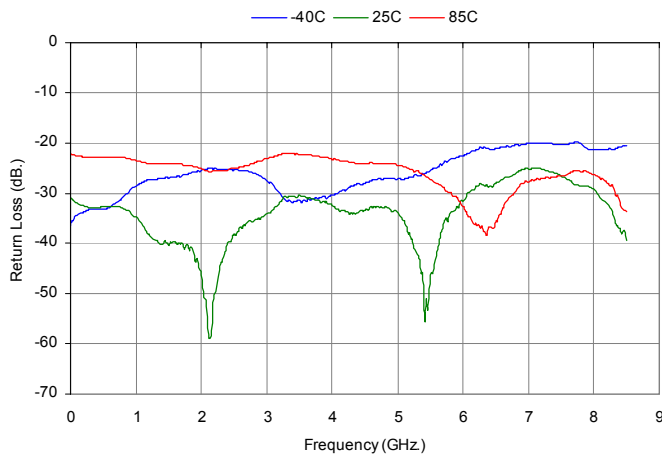


Figure 12. Relative Phase vs. Frequency

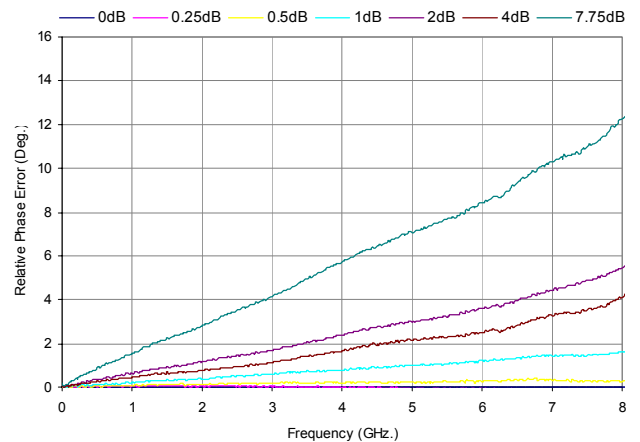


**Figure 13. Relative Phase vs. Temperature:
7.75 dB State**

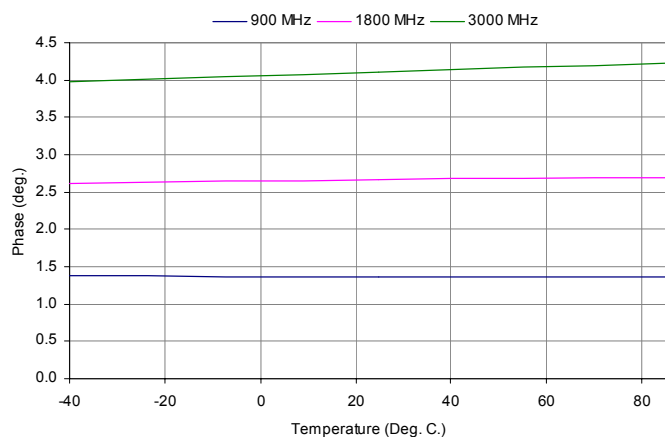


**Figure 14. Attenuation Error vs. Attenuation
Setting: 900 MHz**

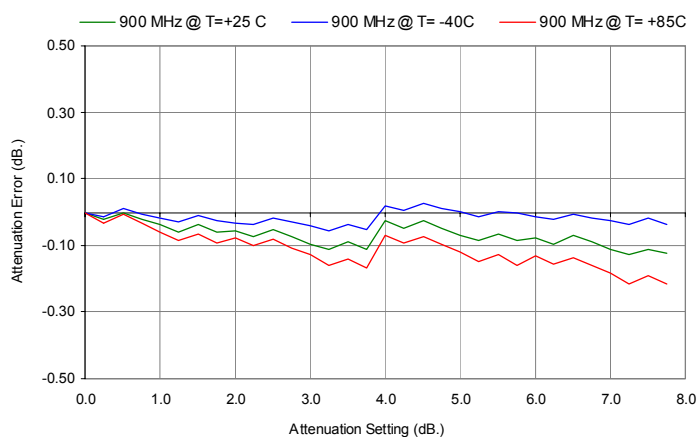


**Figure 15. Attenuation Error vs. Attenuation
Setting: 1800 MHz**

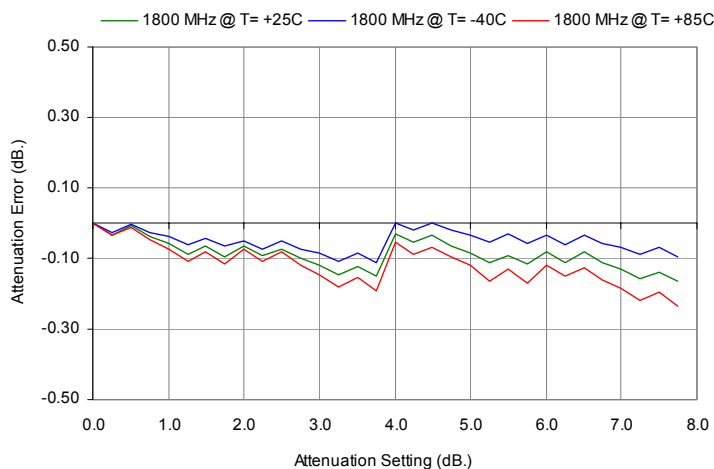


**Figure 16. Attenuation Error vs. Attenuation
Setting: 3000 MHz**

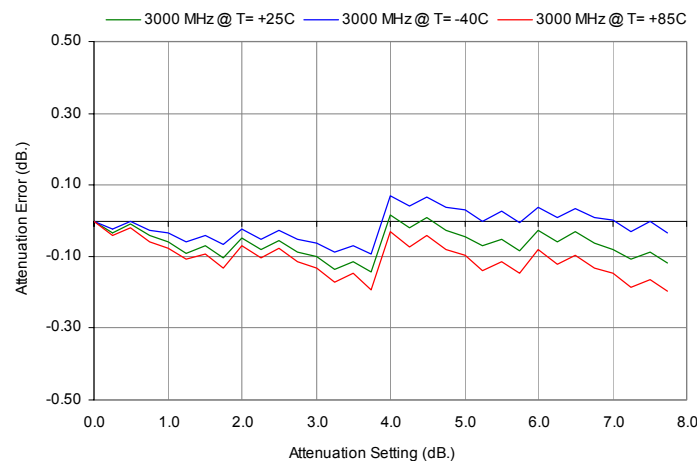


Figure 17. Input IP3 vs. Frequency

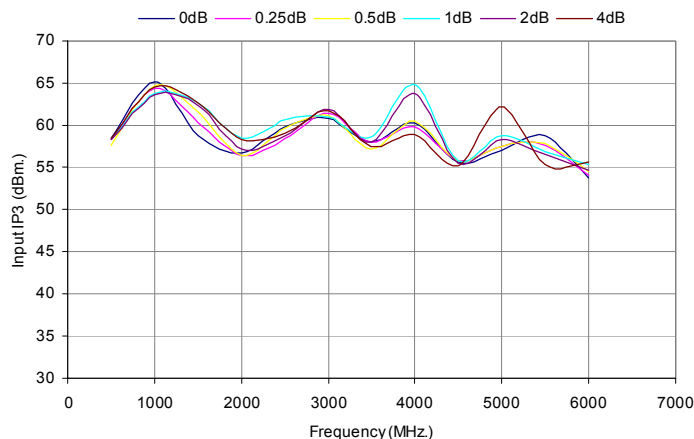


Figure 18. Pin Configuration (Top View)

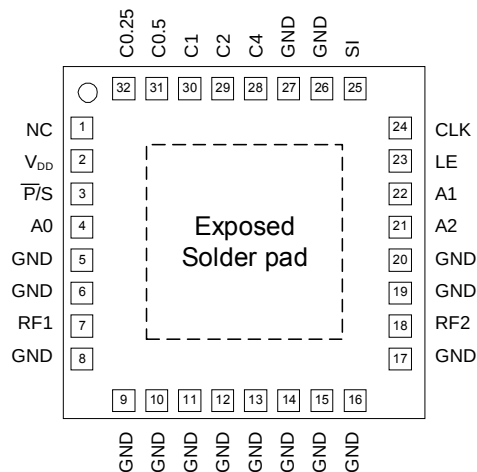


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	N/C	No Connect
2	V _{DD}	Power supply pin
3	P/S	Serial/Parallel mode select
4	A0	A0 connection
5, 6, 8-17, 19, 20, 26, 27	GND	Ground
7	RF1	RF1 port
18	RF2	RF2 port
21	A2	A2 connection
22	A1	A1 connection
23	LE	Latch Enable input
24	CLK	Serial interface clock input
25	SI	Serial Interface input
28	C4	Attenuation control bit, 4 dB
29	C2	Attenuation control bit, 2 dB
30	C1	Attenuation control bit, 1 dB
31	C0.5	Attenuation control bit, 0.5 dB
32	C0.25	Attenuation control bit, 0.25 dB
Paddle	GND	Ground for proper operation

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE43501 in the 32-lead 5x5 QFN package is MSL1.

Switching Frequency

The PE43501 has a maximum 25 kHz switching rate. Switching rate is defined to be the speed at which the DSA can be toggled across attenuation states.

Exposed Solder Pad Connection

The exposed solder pad on the bottom of the package must be grounded for proper device operation.

Table 3. Operating Ranges

Parameter	Min	Typ	Max	Units
V _{DD} Power Supply Voltage	3.0	3.3		V
V _{DD} Power Supply Voltage		5.0	5.5	V
I _{DD} Power Supply Current		70	350	μA
Digital Input High	2.6		5.5	V
P _{IN} Input power (50Ω): 1 Hz ≤ 20 MHz 20 MHz ≤ 4 GHz			See fig. 19 +23	dBm dBm
T _{OP} Operating temperature range	-40	25	85	°C
Digital Input Low	0		1	V
Digital Input Leakage ¹			15	μA

Note 1. Input leakage current per Control pin

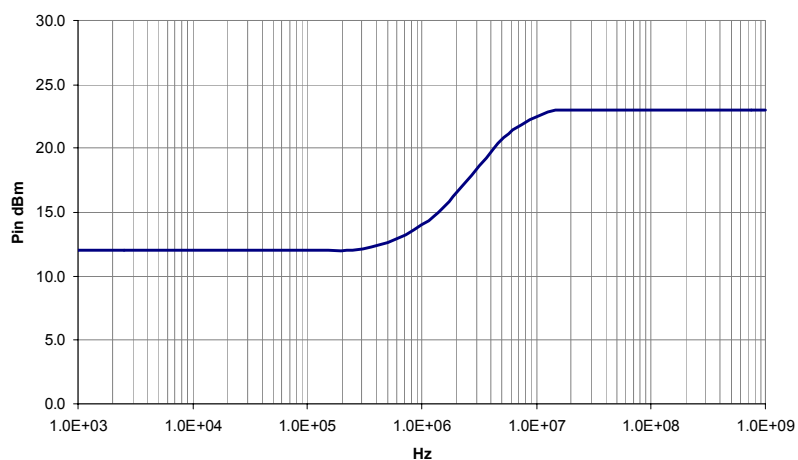
Table 4. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V _{DD}	Power supply voltage	-0.3	6.0	V
V _I	Voltage on any Digital input	-0.3	5.8	V
P _{IN}	Input power (50Ω) 1 Hz ≤ 20 MHz 20 MHz ≤ 4 GHz		See fig. 19 +23	dBm dBm
T _{ST}	Storage temperature range	-65	150	°C
V _{ESD}	ESD voltage (HBM) ¹ ESD voltage (Machine Model)		500 100	V V

Note: 1. Human Body Model (HBM, MIL_STD 883 Method 3015.7)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Figure 19. Maximum Power Handling Capability: Z₀ = 50 Ω



State	Bias Condition
Low	0 to +1.0 Vdc at 2 μ A (typ)
High	+2.6 to +5 Vdc at 10 μ A (typ)

Latch Enable	Shift Clock	Function
X	↑	Shift Register Clocked
↑	X	Contents of shift register transferred to attenuator core

Parallel Control Setting					Attenuation Setting RF1-RF2
D4	D3	D2	D1	D0	
L	L	L	L	L	Reference I.L.
L	L	L	L	H	0.25 dB
L	L	L	H	L	0.5 dB
L	L	H	L	L	1 dB
L	H	L	L	L	2 dB
H	L	L	L	L	4 dB
H	H	H	H	H	7.75 dB

Address Word								Address Setting
A7 (MSB)	A6	A5	A4	A3	A2	A1	A0	
X	X	X	X	X	L	L	L	000
X	X	X	X	X	L	L	H	001
X	X	X	X	X	L	H	L	010
X	X	X	X	X	L	H	H	011
X	X	X	X	X	H	L	L	100
X	X	X	X	X	H	L	H	101
X	X	X	X	X	H	H	L	110
X	X	X	X	X	H	H	H	111

Attenuation Word								Attenuation Setting RF1-RF2
D7	D6	D5	D4	D3	D2	D1	D0 (LSB)	
X	L	L	L	L	L	L	L	Reference I.L.
X	L	L	L	L	L	L	H	0.25 dB
X	L	L	L	L	L	H	L	0.5 dB
X	L	L	L	L	H	L	L	1 dB
X	L	L	L	H	L	L	L	2 dB
X	L	L	H	L	L	L	L	4 dB
X	L	L	H	H	H	H	H	7.75 dB

MSB (last in) Bits can either be set to logic high or logic low

Q15	Q14	Q13	Q12	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Address Word

Attenuation Word

LSB (first in)

Serial Input: XXXXX011X0001111

Programming Options

Parallel/Serial Selection

Either a parallel or serial interface can be used to control the PE43501. The $\bar{P}/S$ bit provides this selection, with $\bar{P}/S$ =LOW selecting the parallel interface and $\bar{P}/S$ =HIGH selecting the serial interface.

Parallel Mode Interface

The parallel interface consists of five CMOS-compatible control lines that select the desired attenuation state, as shown in *Table 7*.

The parallel interface timing requirements are defined by *Fig. 21* (Parallel Interface Timing Diagram), *Table 12* (Parallel Interface AC Characteristics), and switching speed (*Table 1*).

For *latched*-parallel programming the Latch Enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (*per Fig. 21*) to latch new attenuation state into device.

For *direct* parallel programming, the Latch Enable (LE) line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct Mode is ideal for manual control of the device (using hardware, switches, or jumpers).

Serial-Addressable Interface

The serial interface is a 16-bit serial-in, parallel-out shift register buffered by a transparent latch. The 16-bits make up two words comprised of 8-bits each. The first word is the Attenuation Word, which controls the state of the DSA. The second word is the Address Word, which is compared to the static (or programmed) logical states of the A0, A1 and A2 digital inputs. If there is an address match, the DSA changes state; otherwise its current state will remain unchanged. *Fig. 20* illustrates a example timing diagram for programming a state. It is recommended that all parallel control inputs be grounded when the DSA is used in serial mode.

The serial-addressable interface is controlled using three CMOS-compatible signals: Serial-In (SI), Clock (CLK), and Latch Enable (LE). The SI and CLK inputs allow data to be serially entered into the shift register. Serial data is clocked in LSB first, beginning with the attenuation word.

The shift register must be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data into the DSA. Address word and attenuation word truth tables are listed in *Table 8 & Table 9*, respectively. A programming example of the Serial-Addressable register is illustrated in *Table 10*. The serial-addressable timing diagram is illustrated in *Fig. 20*.

Power-up Control Settings

The PE43501 will always initialize to the maximum attenuation setting (7.75 dB) on power-up for both the serial-addressable and latched-parallel modes of operation and will remain in this setting until the user latches in the next programming word. In direct-parallel mode, the DSA can be preset to any state within the 7.75 dB range by pre-setting the parallel control pins prior to power-up. In this mode, there is a 400- μ s delay between the time the DSA is powered-up to the time the desired state is set. During this power-up delay, the device attenuates to the maximum attenuation setting (7.75 dB) before defaulting to the user defined state. If the control pins are left floating in this mode during power-up, the device will default to the minimum attenuation setting (insertion loss state).

Figure 20. Serial-Addressable Timing Diagram

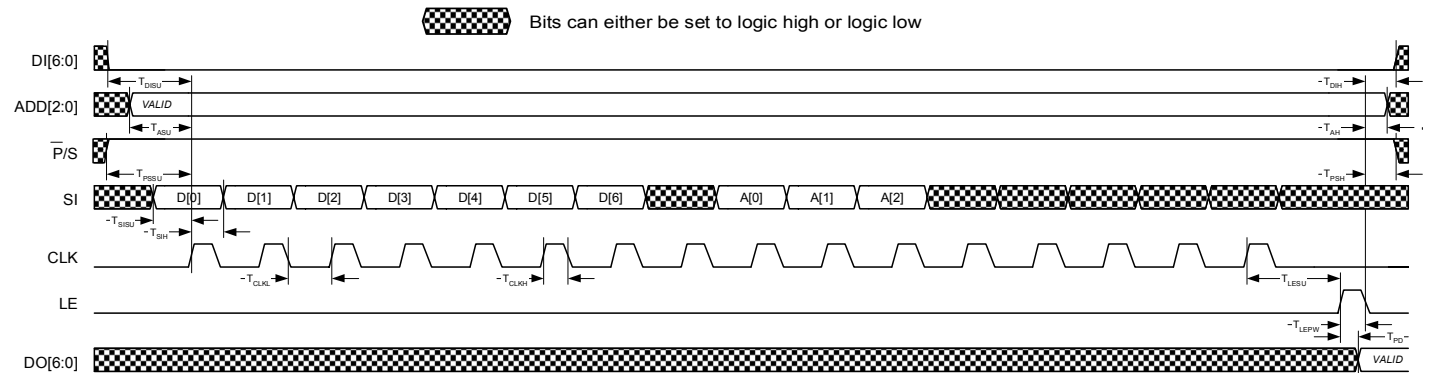


Figure 21. Latched-Parallel/Direct-Parallel Timing Diagram

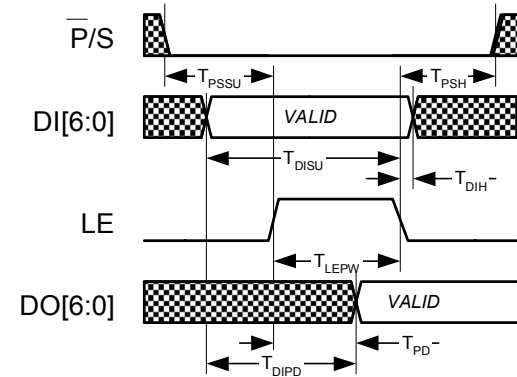


Table 11. Serial Interface AC Characteristics

$V_{DD} = 3.3$ or 5.0 V, $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$, unless otherwise specified

Symbol	Parameter	Min	Max	Unit
F_{CLK}	Serial clock frequency	-	10	MHz
T_{CLKH}	Serial clock HIGH time	30	-	ns
T_{CLKL}	Serial clock LOW time	30	-	ns
T_{LESU}	Last serial clock rising edge setup time to Latch Enable rising edge	10	-	ns
T_{LEPW}	Latch Enable min. pulse width	30	-	ns
T_{SISU}	Serial data setup time	10	-	ns
T_{SIH}	Serial data hold time	10	-	ns
T_{DISU}	Parallel data setup time	100	-	ns
T_{DIH}	Parallel data hold time	100	-	ns
T_{ASU}	Address setup time	100	-	ns
T_{AH}	Address hold time	100	-	ns
T_{PSSU}	Parallel/Serial setup time	100	-	ns
T_{PSH}	Parallel/Serial hold time	100	-	ns
T_{PD}	Digital register delay (internal)	-	10	ns

Note: f_{CLK} is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify f_{CLK} specification.

Table 12. Parallel and Direct Interface AC Characteristics

$V_{DD} = 3.3$ or 5.0 V, $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$, unless otherwise specified

Symbol	Parameter	Min	Max	Unit
T_{LEPW}	Latch Enable minimum pulse width	30	-	ns
T_{DISU}	Parallel data setup time	100	-	ns
T_{DIH}	Parallel data hold time	100	-	ns
T_{PSSU}	Parallel/Serial setup time	100	-	ns
T_{PSIH}	Parallel/Serial hold time	100	-	ns
T_{PD}	Digital register delay (internal)	-	10	ns
T_{DIPD}	Digital register delay (internal, direct mode only)	-	5	ns

Evaluation Kit

The Digital Attenuator Evaluation Kit board was designed to ease customer evaluation of the PE43501 Digital Step Attenuator.

Direct-Parallel Programming Procedure

For automated direct-parallel programming, connect the test harness provided with the EVK from the parallel port of the PC to the J1 & Serial header pin and set the D0-D4 SP3T switches to the 'MIDDLE' toggle position. Position the Parallel/Serial (P/S) select switch to the Parallel (or left) position. The evaluation software is written to operate the DSA in either Parallel or Serial-Addressable Mode. Ensure that the software is set to program in *Direct-Parallel* mode. Using the software, enable or disable each setting to the desired attenuation state. The software automatically programs the DSA each time an attenuation state is enabled or disabled.

For manual direct-parallel programming, disconnect the test harness provided with the EVK from the J1 and Serial header pins. Position the Parallel/Serial (P/S) select switch to the Parallel (or left) position. The LE pin on the Serial header must be tied to logic high. Switches D0-D4 are SP3T switches which enable the user to manually program the parallel bits. When any input D0-D4 is toggled 'UP', logic high is presented to the parallel input. When toggled 'DOWN', logic low is presented to the parallel input. Setting D0-D4 to the 'MIDDLE' toggle position presents an OPEN, which forces an on-chip logic low. Table 7 depicts the parallel programming truth table and Fig. 21 illustrates the parallel programming timing diagram.

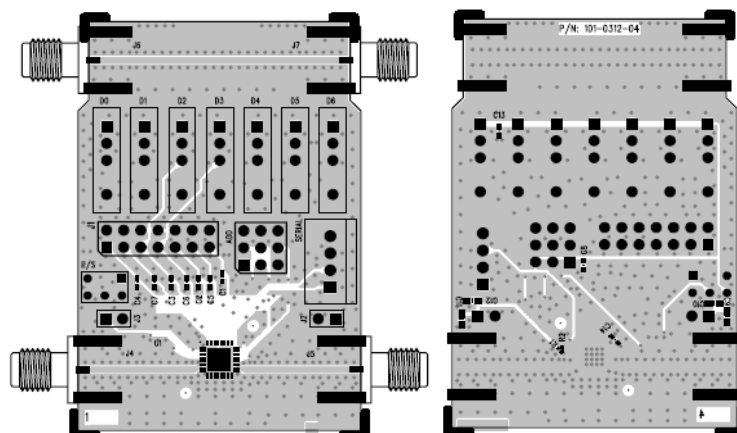
Latched-Parallel Programming Procedure

For automated latched-parallel programming, the procedure is identical to the direct-parallel method. The user only must ensure that *Latched-Parallel* is selected in the software.

For manual latched-parallel programming, the procedure is identical to direct-parallel except now

Figure 22. Evaluation Board Layout

Peregrine Specification 101-0312



Note: Reference Fig. 23 for Evaluation Board Schematic

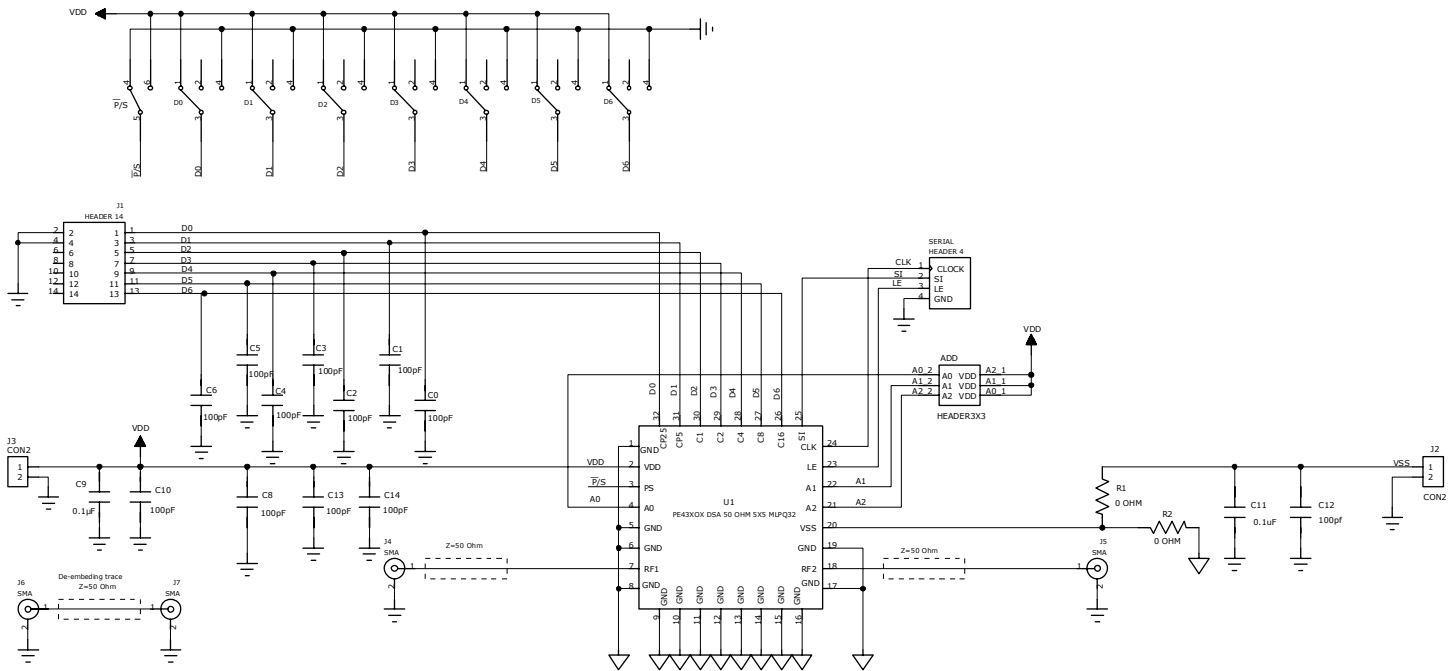
the LE pin on the Serial header must be logic low as the parallel bits are applied. The user must then pulse LE from 0V to V_{DD} and back to 0V to latch the programming word into the DSA. LE must be logic low prior to programming the next word.

Serial-Addressable Programming Procedure

Position the Parallel/Serial (P/S) select switch to the Serial (or right) position. Prior to programming, the user must define an address setting using the ADD header pin. Jump the middle pins on the ADD header A0-A2 (or lower) row of pins to set logic high, or jump the middle pins to the upper row of pins to set logic low. If the ADD pins are left open, then 000 become the default address. The evaluation software is written to operate the DSA in either Parallel or Serial-Addressable Mode. Ensure that the software is set to program in *Serial-Addressable* mode. Using the software, enable or disable each setting to the desired attenuation state. The software automatically programs the DSA each time an attenuation state is enabled or disabled.

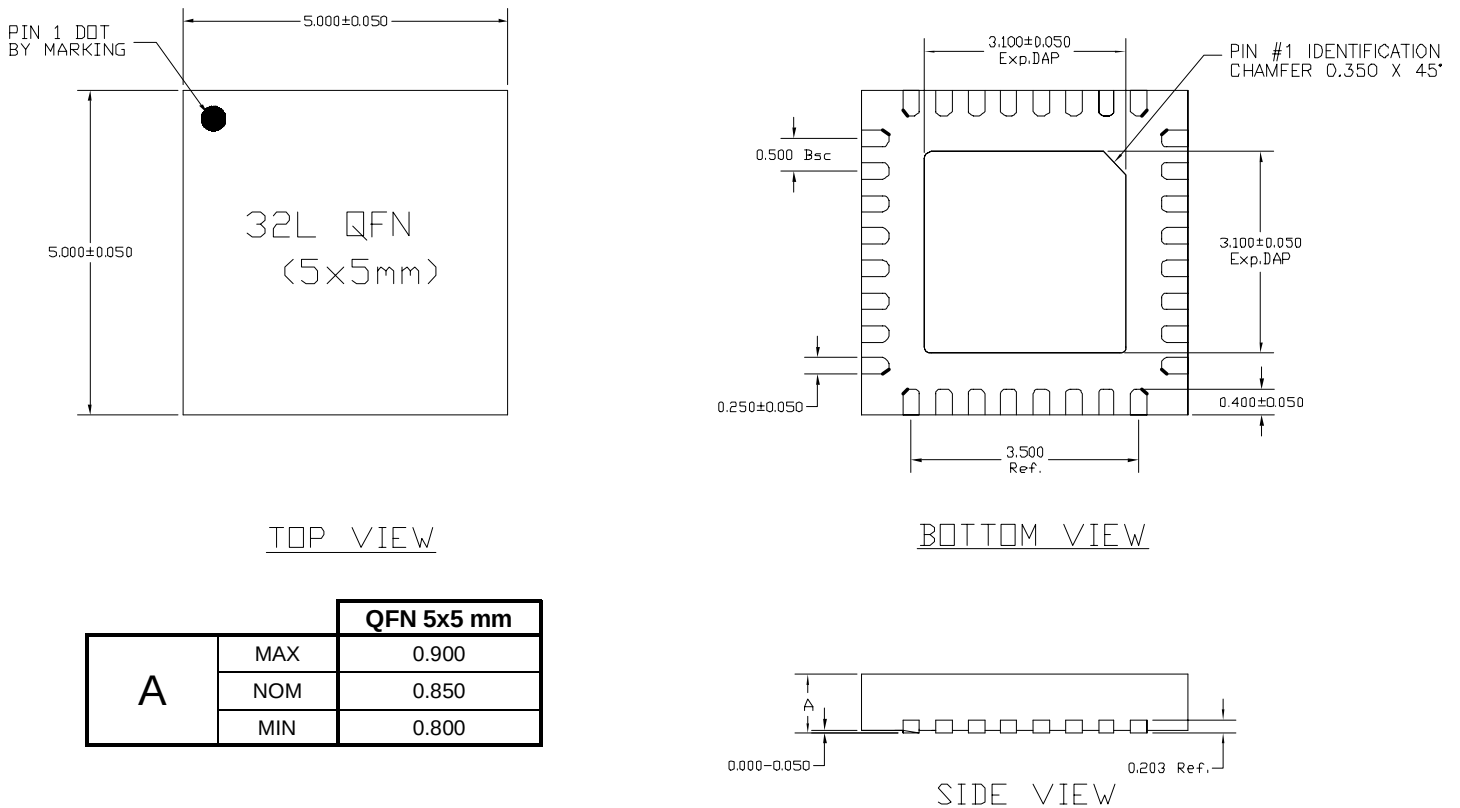
Figure 23. Evaluation Board Schematic

Peregrine Specification 102-0381



Note: Capacitors C1-C8, C13, & C14 may be omitted. Pin 26 & 27 are ground.

Figure 24. Package Drawing



[illegible]

1. 10 sprocket hole pitch cumulative tolerance ± 0.02 .
2. Camber not to exceed 1mm in 100mm.
3. Material: PS + C.
4. Ao and Bo measured as indicated.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

A diagram of a device's top surface. It features a central square area with a smaller square inside it. A callout line points from the top-left corner of the inner square to a black dot labeled "Pin 1". To the right of the main diagram is a grey rectangular box containing the text "Top of Device".

Device Orientation in Tape

43501
YYWW
ZZZZZ

YYWW = Date Code
ZZZZZ = Last five digits of Lot Number

Order Code	Part Marking	Description	Package	Shipping Method
PE43501MLI	43501	PE43501 G - 32QFN 5x5mm-75A	Green 32-lead 5x5mm QFN	Bulk or tape cut from reel
PE43501MLI-Z	43501	PE43501 G – 32QFN 5x5mm-3000C	Green 32-lead 5x5mm QFN	3000 units / T&R
EK43501-01	43501	PE43501 – 32QFN 5x5mm-EK	Evaluation Kit	1 / Box

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Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a DCN (Document Change Notice).

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