ELPIDA

DATA SHEET

1G bits DDR3 SDRAM

EDJ1104BASE (256M words × 4 bits)
EDJ1108BASE (128M words × 8 bits)
EDJ1116BASE (64M words × 16 bits)

Specifications

- Density: 1G bits
- Organization
  - 32M words × 4 bits × 8 banks (EDJ1104BASE)
  - 16M words × 8 bits × 8 banks (EDJ1108BASE)
  - 8M words × 16 bits × 8 banks (EDJ1116BASE)
- Package
  - 78-ball FBGA (EDJ1104/1108BASE)
  - 96-ball FBGA (EDJ1116BASE)
  - Lead-free (RoHS compliant)
- Power supply: VDD, VDDQ = 1.5V ± 0.075V
- Data rate
  - 1600Mbps/1333Mbps/1066Mbps/800Mbps (max.)
- 1KB page size (EDJ1104/1108BASE)
  - Row address: A0 to A13
  - Column address: A0 to A9, A11 (EDJ1104BASE)
    A0 to A9 (EDJ1108BASE)
- 2KB page size (EDJ1116BASE)
  - Row address: A0 to A12
  - Column address: A0 to A9
- Eight internal banks for concurrent operation
- Interface: SSTL_15
- Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- Burst type (BT):
  - Sequential (8, 4 with BC)
  - Interleave (8, 4 with BC)
- /CAS Latency (CL): 5, 6, 7, 8, 9, 10, 11
- /CAS Write Latency (CWL): 5, 6, 7, 8
- Precharge: auto precharge option for each burst access
- Driver strength: RZQ/7, RZQ/6 (RZQ = 240Ω)
- Refresh: auto-refresh, self-refresh
- Refresh cycles
  - Average refresh period
    7.8μs at 0°C ≤ TC ≤ +85°C
    3.9μs at +85°C < TC ≤ +95°C
- Operating case temperature range
  - TC = 0°C to +95°C

Features

- Double-data-rate architecture; two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted /CAS by programmable additive latency for better command and data bus efficiency
- On-Die Termination (ODT) for better signal quality
  - Synchronous ODT
  - Dynamic ODT
  - Asynchronous ODT
- Multi Purpose Register (MPR) for temperature read out
- ZQ calibration for DQ drive and ODT
- Programmable Partial Array Self-Refresh (PASR)
- /RESET pin for Power-up sequence and reset function
- SRT range:
  - Normal/extended
  - Auto/manual self-refresh
- Programmable Output driver impedance control

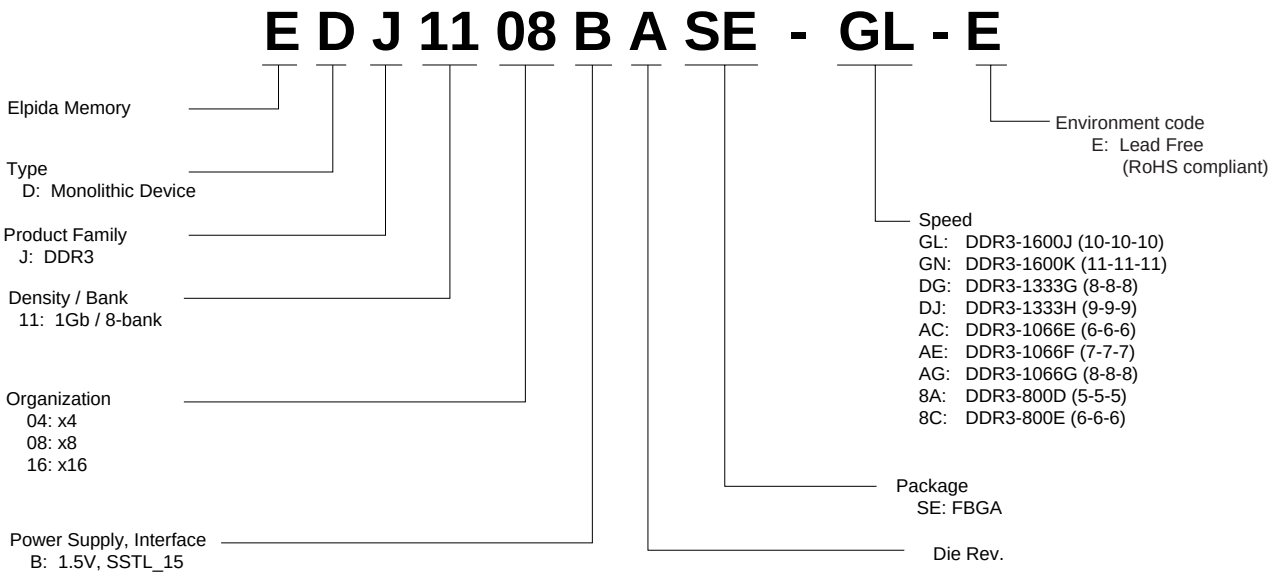
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Ordering Information

Part number	Die revision	Organization (words × bits)	Internal banks	JEDEC speed bin (CL-tRCD-tRP)	Package
EDJ1104BASE-DG-E	A	256M × 4	8	DDR3-1333G (8-8-8)	78-ball FBGA
EDJ1104BASE-DJ-E				DDR3-1333H (9-9-9)	
EDJ1104BASE-AC-E				DDR3-1066E (6-6-6)	
EDJ1104BASE-AE-E				DDR3-1066F (7-7-7)	
EDJ1104BASE-AG-E				DDR3-1066G (8-8-8)	
EDJ1104BASE-8A-E				DDR3-800D (5-5-5)	
EDJ1104BASE-8C-E				DDR3-800E (6-6-6)	
EDJ1108BASE-GL-E		128M × 8		DDR3-1600J (10-10-10)	
EDJ1108BASE-GN-E				DDR3-1600K (11-11-11)	
EDJ1108BASE-DG-E				DDR3-1333G (8-8-8)	
EDJ1108BASE-DJ-E				DDR3-1333H (9-9-9)	
EDJ1108BASE-AC-E				DDR3-1066E (6-6-6)	
EDJ1108BASE-AE-E				DDR3-1066F (7-7-7)	
EDJ1108BASE-AG-E				DDR3-1066G (8-8-8)	
EDJ1108BASE-8A-E				DDR3-800D (5-5-5)	
EDJ1108BASE-8C-E				DDR3-800E (6-6-6)	
EDJ1116BASE-DG-E		64M × 16		DDR3-1333G (8-8-8)	96-ball FBGA
EDJ1116BASE-DJ-E				DDR3-1333H (9-9-9)	
EDJ1116BASE-AC-E				DDR3-1066E (6-6-6)	
EDJ1116BASE-AE-E				DDR3-1066F (7-7-7)	
EDJ1116BASE-AG-E				DDR3-1066G (8-8-8)	
EDJ1116BASE-8A-E				DDR3-800D (5-5-5)	
EDJ1116BASE-8C-E				DDR3-800E (6-6-6)	

Part Number



Pin Configurations (×4, ×8 configuration)

/xxx indicates active low signal.

78-ball FBGA (×4 configuration)

	1	2	3	7	8	9
A	VSS	VDD	NC	NC	VSS	VDD
B	VSS	VSSQ	DQ0	DM	VSSQ	VDDQ
C	VDDQ	DQ2	DQS	DQ1	DQ3	VSSQ
D	VSSQ	NC	/DQS	VDD	VSS	VSSQ
E	VREFDQ	VDDQ	NC	NC	NC	VDDQ
F	NC	VSS	/RAS	CK	VSS	NC
G	ODT	VDD	/CAS	/CK	VDD	CKE
H	NC	/CS	/WE	A10(AP)	ZQ	NC
J	VSS	BA0	BA2	NC	VREFCA	VSS
K	VDD	A3	A0	A12(/BC)	BA1	VDD
L	VSS	A5	A2	A1	A4	VSS
M	VDD	A7	A9	A11	A6	VDD
N	VSS	/RESET	A13	NC	A8	VSS

(Top view)

78-ball FBGA (×8 configuration)

	1	2	3	7	8	9
A	VSS	VDD	NC	NU/(/TDQS)	VSS	VDD
B	VSS	VSSQ	DQ0	DM/TDQS	VSSQ	VDDQ
C	VDDQ	DQ2	DQS	DQ1	DQ3	VSSQ
D	VSSQ	DQ6	/DQS	VDD	VSS	VSSQ
E	VREFDQ	VDDQ	DQ4	DQ7	DQ5	VDDQ
F	NC	VSS	/RAS	CK	VSS	NC
G	ODT	VDD	/CAS	/CK	VDD	CKE
H	NC	/CS	/WE	A10(AP)	ZQ	NC
J	VSS	BA0	BA2	NC	VREFCA	VSS
K	VDD	A3	A0	A12(/BC)	BA1	VDD
L	VSS	A5	A2	A1	A4	VSS
M	VDD	A7	A9	A11	A6	VDD
N	VSS	/RESET	A13	NC	A8	VSS

(Top view)

Pin name	Function	Pin name	Function
A0 to A13*3	Address inputs A10 (AP): Auto precharge A12(/BC): Burst chop	/RESET*3	Active low asynchronous reset
BA0 to BA2*3	Bank select	VDD	Supply voltage for internal circuit
DQ0 to DQ7	Data input/output	VSS	Ground for internal circuit
DQS, /DQS	Differential data strobe	VDDQ	Supply voltage for DQ circuit
TDQS, /TDQS	Termination data strobe	VSSQ	Ground for DQ circuit
/CS*3	Chip select	VREFDQ	Reference voltage for DQ
/RAS, /CAS, /WE*3	Command input	VREFCA	Reference voltage
CKE*3	Clock enable	ZQ	Reference pin for ZQ calibration
CK, /CK	Differential clock input	NC*1	No connection
DM	Write data mask	NU*2	Not usable
ODT*3	ODT control		

Notes: 1. Not internally connected with die.
2. Don't connect. Internally connected.
3. Input only pins (address, command, CKE, ODT and /RESET) do not supply termination.

Pin Configurations (×16 configuration)

/xxx indicates active low signal.

96-ball FBGA

	1	2	3	7	8	9
A	VDDQ	DQU5	DQU7	DQU4	VDDQ	VSS
B	VSSQ	VDD	VSS	/DQSU	DQU6	VSSQ
C	VDDQ	DQU3	DQU1	DQSU	DQU2	VDDQ
D	VSSQ	VDDQ	DMU	DQU0	VSSQ	VDD
E	VSS	VSSQ	DQL0	DML	VSSQ	VDDQ
F	VDDQ	DQL2	DQSL	DQL1	DQL3	VSSQ
G	VSSQ	DQL6	/DQSL	VDD	VSS	VSSQ
H	VREFDQ	VDDQ	DQL4	DQL7	DQL5	VDDQ
J	NC	VSS	/RAS	CK	VSS	NC
K	ODT	VDD	/CAS	/CK	VDD	CKE
L	NC	/CS	/WE	A10(AP)	ZQ	NC
M	VSS	BA0	BA2	NC	VREFCA	VSS
N	VDD	A3	A0	A12(/BC)	BA1	VDD
P	VSS	A5	A2	A1	A4	VSS
R	VDD	A7	A9	A11	A6	VDD
T	VSS	/RESET	NC	NC	A8	VSS

(Top view)

Pin name	Function	Pin name	Function
A0 to A12*2	Address inputs A10(AP): Auto precharge A12(/BC): Burst chop	/RESET*2	Active low asynchronous reset
BA0 to BA2	Bank select	VDD	Supply voltage for internal circuit
DQU0 to DQU7 DQL0 to DQL7	Data input/output	VSS	Ground for internal circuit
DQSU, /DQSU DQSL, /DQSL	Differential data strobe	VDDQ	Supply voltage for DQ circuit
/CS*2	Chip select	VSSQ	Ground for DQ circuit
/RAS, /CAS, /WE*2	Command input	VREFDQ	Reference voltage for DQ
CKE*2	Clock enable	VREFCA	Reference voltage
CK, /CK	Differential clock input	ZQ	Reference pin for ZQ calibration
DMU, DML	Write data mask	NC*	No connection
ODT*2	ODT control		

Note: 1. Not internally connected with die.
2. Input only pins (address, command, CKE, ODT and /RESET) do not supply termination.

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Electrical Conditions

- All voltages are referenced to VSS (GND)
- Execute power-up and Initialization sequence before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Power supply voltage	VDD	−0.4 to +1.975	V	1, 3
Power supply voltage for output	VDDQ	−0.4 to +1.975	V	1, 3
Input voltage	VIN	−0.4 to +1.975	V	1
Output voltage	VOUT	−0.4 to +1.975	V	1
Reference voltage	VREFCA	−0.4 to 0.6 × VDD	V	3
Reference voltage for DQ	VREFDQ	−0.4 to 0.6 × VDDQ	V	3
Storage temperature	Tstg	−55 to +100	°C	1, 2
Power dissipation	PD	1.0	W	1
Short circuit output current	IOUT	50	mA	1

Notes: 1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Storage temperature is the case surface temperature on the center/top side of the DRAM.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must be no greater than 0.6 × VDDQ, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

Caution

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Notes
Operating case temperature	TC	0 to +95	°C	1, 2, 3

Notes: 1. Operating temperature is the case surface temperature on the center/top side of the DRAM.

2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C to +85°C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between +85°C and +95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9µs. (This double refresh requirement may not apply for some devices.)
   b) If Self-refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 bit [A6, A7] = [0, 1]) or enable the optional Auto Self-Refresh mode (MR2 bit [A6, A7] = [1, 0]).

Recommended DC Operating Conditions (TC = 0°C to +85°C, VDD, VDDQ = 1.5V ± 0.075V)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply voltage	VDD	1.425	1.5	1.575	V	1, 2
Supply voltage for DQ	VDDQ	1.425	1.5	1.575	V	1, 2
Input reference voltage	VREFCA (DC)	0.49 × VDD	0.50 × VDD	0.51 × VDD	V	3, 4
Input reference voltage for DQ	VREFDQ (DC)	0.49 × VDDQ	0.50 × VDDQ	0.51 × VDDQ	V	3, 4

Notes: 1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. The AC peak noise on VREF may not allow VREF to deviate from VREF(DC) by more than ±1% VDD (for reference: approx ±15 mV).
4. For reference: approx. VDD/2 ± 15 mV.

AC and DC Input Measurement Levels (TC = 0°C to +85°C, VDD, VDDQ = 1.5V ± 0.075V)

Single-Ended AC and DC Input Levels for Command and Address

Parameter	Symbol	min.	typ.	max.	Unit	Notes
DC input logic high	VIHCA (DC)	VREF + 0.100	—	VDD	V	1
DC input logic low	VILCA (DC)	VSS	—	VREF − 0.100	V	1
AC input logic high	VIHCA (AC)	VREF + 0.175	—	—*2	V	1
AC input logic low	VILCA (AC)	—*2	—	VREF − 0.175	V	1
AC input logic high	VIHCA (AC150)	VREF + 0.150	—	—*2	V	1
AC input logic low	VILCA (AC150)	—*2	—	VREF − 0.150	V	1

Notes: 1. For input only pins except /RESET; VREF = VREFCA.
2. See Overshoot and Undershoot Specifications section.

Single-Ended AC and DC Input Levels for DQ and DM

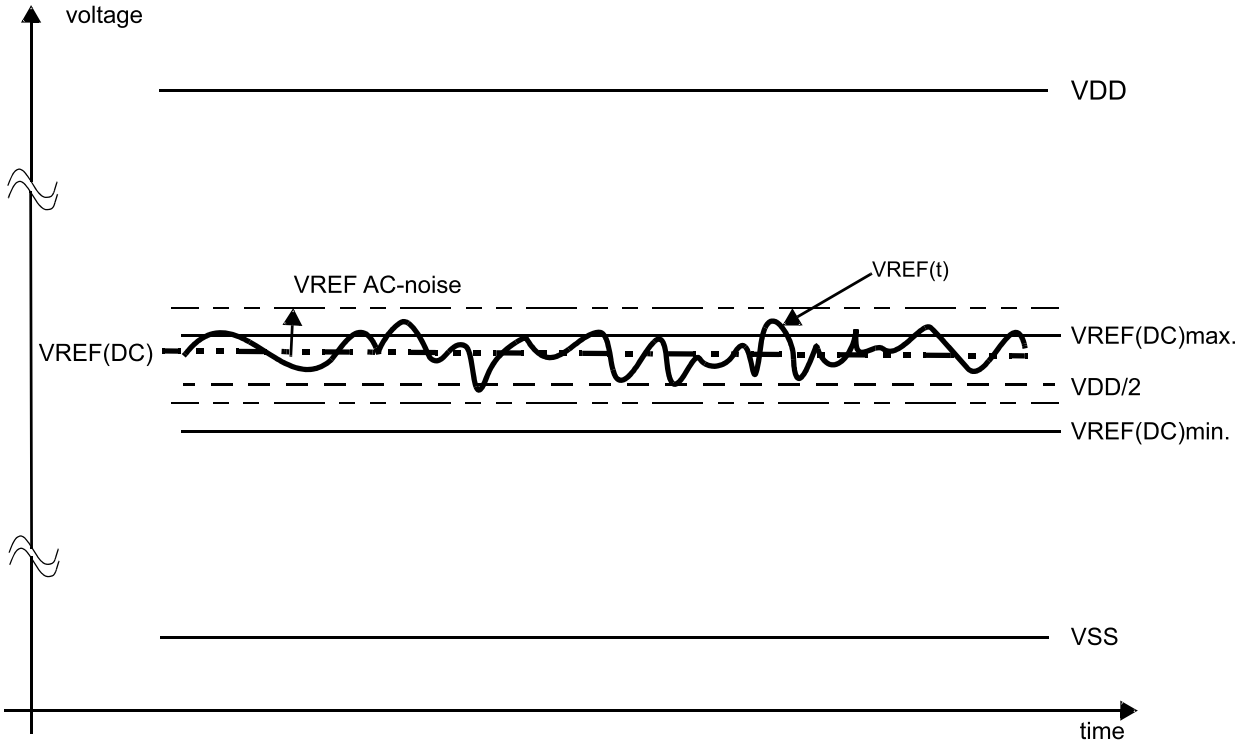
Parameter	Symbol	min.	typ.	max.	Unit	Notes
DC input logic high	VIHDQ (DC)	VREF + 0.100	—	VDD	V	1
DC input logic low	VILDQ (DC)	VSS	—	VREF − 0.100	V	1
AC input logic high DDR3-800, 1066	VIHDQ (AC)	VREF + 0.175	—	—*2	V	1, 3
DDR3-1333, 1600	VIHDQ (AC)	VREF + 0.150	—	—*2	V	1, 3
AC input logic low DDR3-800, 1066	VILDQ (AC)	—*2	—	VREF − 0.175	V	1, 3
DDR3-1333, 1600	VILDQ (AC)	—*2	—	VREF − 0.150	V	1, 3

Notes: 1. For DQ and DM: VREF = VREFDQ.
2. See Overshoot and Undershoot Specifications section.
3. Single-ended swing requirement for DQS, /DQS is 350 mV (peak to peak). Differential swing requirement for DQS, /DQS is 700 mV (peak to peak).

VREF Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages VREFCA and VREFDQ are shown in Figure VREF(DC) Tolerance and VREF AC-Noise Limits. It shows a valid reference voltage VREF(t) as a function of time. (VREF stands for VREFCA and VREFDQ likewise).

VREF(DC) is the linear average of VREF(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in the table of(Single-Ended AC and DC Input Levels for Command and Address). Furthermore VREF(t) may temporarily deviate from VREF(DC) by no more than +/- 1% VDD.



VREF(DC) Tolerance and VREF AC-Noise Limits

The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VREF.

VREF shall be understood as VREF(DC), as defined in figure above, VREF(DC) Tolerance and VREF AC-Noise Limits.

This clarifies that DC-variations of VREF affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for VREF(DC) deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with VREF AC-noise. Timing and voltage effects due to ac-noise on VREF up to the specified limit (±1% of VDD) are included in DRAM timings and their associated deratings.

Input Slew Rate Derating

For all input signals the total tIS, tDS (setup time) and tIH, tDH (hold time) required is calculated by adding the data sheet tIS (base), tDS (base) and tIH (base), tDH (base) value to the ΔtIS, ΔtDS and ΔtIH, ΔtDH derating value respectively.

Example: tDS (total setup time) = tDS (base) + ΔtDS.

Setup (tIS, tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF (DC) and the first crossing of VIH (AC) min. Setup (tIS, tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF (DC) and the first crossing of VIL (AC) max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF (DC) to AC region', use nominal slew rate for derating value (See the figure of Slew Rate Definition Nominal).

If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF (DC) to AC region', the slew rate of a tangent line to the actual signal from the AC level to DC level is used for derating value (see the figure of Slew Rate Definition Tangent).

Hold (tIH, tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL (DC) max. and the first crossing of VREF (DC). Hold (tIH, tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH (DC) min. and the first crossing of VREF (DC). If the actual signal is always later than the nominal slew rate line between shaded 'DC level to VREF (DC) region', use nominal slew rate for derating value (See the figure of Slew Rate Definition Nominal).

If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'DC to VREF (DC) region', the slew rate of a tangent line to the actual signal from the DC level to VREF (DC) level is used for derating value (see the figure of Slew Rate Definition Tangent).

For a valid transition the input signal has to remain above/below VIH/VIL(AC) for some time tVAC (see the table of Required time tVAC above VIH(AC) {below VIL(AC)} for valid transition).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL (AC) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL (AC).

For slew rates in between the values listed in the tables below, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

[Address/Command Setup and Hold Base-Values for 1V/ns]

	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Unit	Reference
tIS(base)	200	125	65	45	ps	VIH/VIL(AC)
tIH(base)	275	200	140	120	ps	VIH/VIL(DC)
tIS(base) AC150	200 + 150	125 + 150	65 + 125	45 + 125	ps	VIH/VIL(AC)

Notes: 1 AC/DC referenced for 1V/ns Address/Command slew rate and 2V/ns differential CK, /CK slew rate.

2. The tHS (base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100ps of derating to accommodate for the lower alternate threshold of 150mV and another 25ps to account for the earlier reference point [(175mv – 150mv)/1V/ns]

[Derating Values of tIS/tIH AC/DC Based (DDR3-800, 1066, 1333, 1600)]

ΔtIS, ΔtIH derating in [ps] AC/DC based

AC175 Threshold -> VIH(AC)=VREF(DC)+175mV, VIL(AC)=VREF(DC)-175mV

		CK, /CK differential slew rate																
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	Unit
CMD, ADD slew rate (V/ns)	2.0	+88	+50	+88	+50	+88	+50	+96	+58	+104	+66	+112	+74	+120	+84	+128	+100	ps
	1.5	+59	+34	+59	+34	+59	+34	+67	+42	+75	+50	+83	+58	+91	+68	+99	+84	ps
	1.0	0	0	0	0	0	0	+8	+8	+16	+16	+24	+24	+32	+34	+40	+50	ps
	0.9	–2	–4	–2	–4	–2	–4	+6	+4	+14	+12	+22	+20	+30	+30	+38	+46	ps
	0.8	–6	–10	–6	–10	–6	–10	+2	–2	+10	+6	+18	+14	+26	+24	+34	+40	ps
	0.7	–11	–16	–11	–16	–11	–16	–3	–8	+5	0	+13	+8	+21	+18	+29	+34	ps
	0.6	–17	–26	–17	–26	–17	–26	–9	–18	–1	–10	+7	–2	+15	+8	+23	+24	ps
	0.5	–35	–40	–35	–40	–35	–40	–27	–32	–19	–24	–11	–16	–2	–6	+5	+10	ps
	0.4	–62	–60	–62	–60	–62	–60	–54	–52	–46	–44	–38	–36	–30	–26	–22	–10	ps

[Derating Values of tIS/tIH AC/DC based-Alternate AC150 Threshold (DDR3-800, 1066, 1333, 1600)]

ΔtIS, ΔtIH derating in [ps] AC/DC based

Alternate AC150 Threshold -> VIH(AC)=VREF(DC)+150mV, VIL(AC)=VREF(DC)-150mV

		CK, /CK differential slew rate																
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	Unit
CMD, ADD slew rate (V/ns)	2.0	+75	+50	+75	+50	+75	+50	+83	+58	+91	+66	+99	+74	+107	+84	+115	+100	ps
	1.5	+50	+34	+50	+34	+50	+34	+58	+42	+66	+50	+74	+58	+82	+68	+90	+84	ps
	1.0	0	0	0	0	0	0	+8	+8	+16	+16	+24	+24	+32	+34	+40	+50	ps
	0.9	0	–4	0	–4	0	–4	+8	+4	+16	+12	+24	+20	+32	+30	+40	+46	ps
	0.8	0	–10	0	–10	0	–10	+8	–2	+16	+6	+24	+14	+32	+24	+40	+40	ps
	0.7	0	–16	0	–16	0	–16	+8	–8	+16	0	+24	+8	+32	+18	+40	+34	ps
	0.6	–1	–26	–1	–26	–1	–26	+7	–18	+15	–10	+23	–2	+31	+8	+39	+24	ps
	0.5	–10	–40	–10	–40	–10	–40	–2	–32	+6	–24	+14	–16	+22	–6	+30	+10	ps
	0.4	–25	–60	–25	–60	–25	–60	–17	–52	–9	–44	–1	–36	7	–26	15	–10	ps

[Required time tVAC above VIH(AC) {below VIL(AC)} for Valid Transition]

	tVAC @ 175 mV[ps]		tVAC @ 150 mV[ps]	
Slew rate (V/ns)	min.	max.	min.	max.
>2.0	75	—	175	—
2.0	57	—	170	—
1.5	50	—	167	—
1.0	38	—	163	—
0.9	34	—	162	—
0.8	29	—	161	—
0.7	22	—	159	—
0.6	13	—	155	—
0.5	0	—	150	—
<0.5	0	—	150	—

[Data Setup and Hold Base-Values]

	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Unit	Reference
tDS(base)	75	25	30	10	ps	VIH/VIL(AC)
tDH(base)	150	100	65	45	ps	VIH/VIL(DC)

Notes: 1 AC/DC referenced for 1V/ns DQ slew rate and 2V/ns DQS slew rate.

[Derating Values of tDS/tDH AC/DC based (DDR3-800, 1066)]

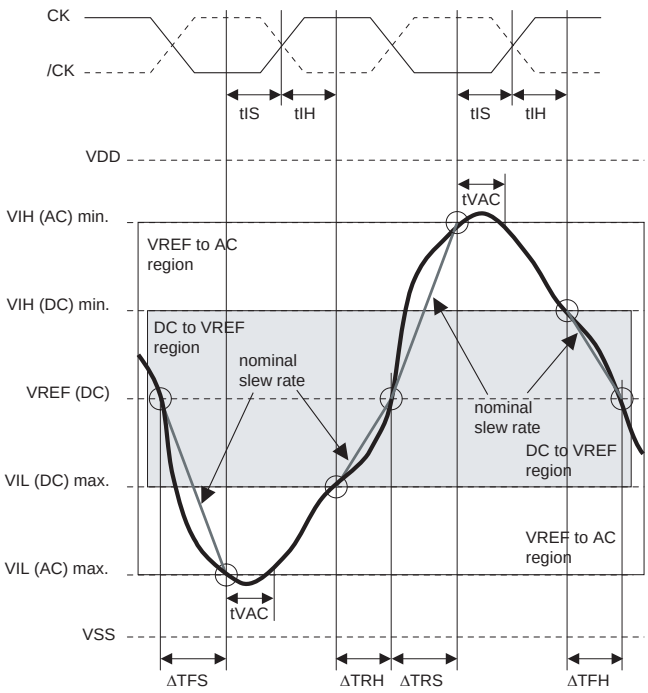
		ΔtDS, ΔtDH derating in [ps] AC/DC based																
		DQS, /DQS differential slew rate																
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	Unit
DQ slew rate (V/ns)	2.0	+88	+50	+88	+50	+88	+50	—	—	—	—	—	—	—	—	—	—	ps
	1.5	+59	+34	+59	+34	+59	+34	+67	+42	—	—	—	—	—	—	—	—	ps
	1.0	0	0	0	0	0	0	+8	+8	+16	+16	—	—	—	—	—	—	ps
	0.9	—	—	–2	–4	–2	–4	+6	+4	+14	+12	+22	+20	—	—	—	—	ps
	0.8	—	—	—	—	–6	–10	+2	–2	+10	+6	+18	+14	+26	+24	—	—	ps
	0.7	—	—	—	—	—	—	–3	–8	+5	0	+13	+8	+21	+18	+29	+34	ps
	0.6	—	—	—	—	—	—	—	—	–1	–10	+7	–2	+15	+8	+23	+24	ps
	0.5	—	—	—	—	—	—	—	—	—	—	–11	–16	–2	–6	+5	+10	ps
	0.4	—	—	—	—	—	—	—	—	—	—	—	—	–30	–26	–22	–10	ps

[Derating Values of tDS/tDH AC/DC based (DDR3-1333, 1600)]

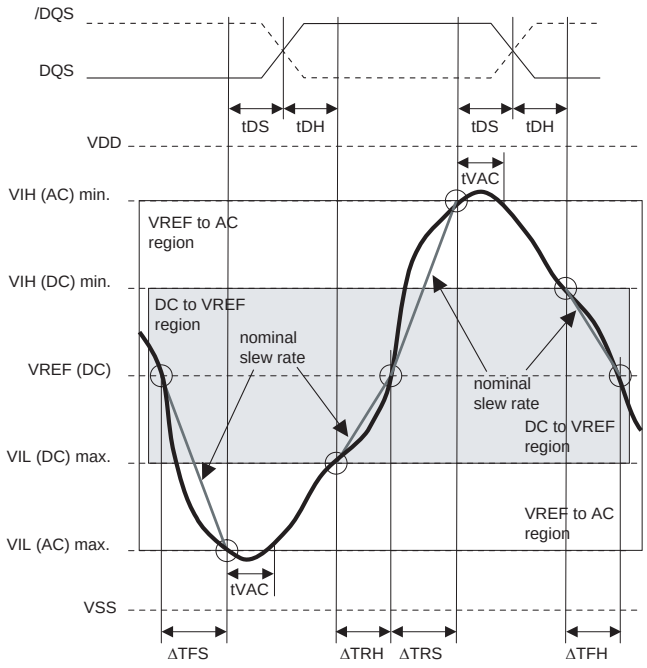
		ΔtDS, ΔtDH derating in [ps] AC/DC based																
		DQS, /DQS differential slew rate																
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	Unit
DQ slew rate (V/ns)	2.0	+75	+50	+75	+50	+75	+50	—	—	—	—	—	—	—	—	—	—	ps
	1.5	+59	+34	+59	+34	+59	+34	+58	+42	—	—	—	—	—	—	—	—	ps
	1.0	0	0	0	0	0	0	+8	+8	+16	+16	—	—	—	—	—	—	ps
	0.9	—	—	0	–4	0	–4	+8	+4	+16	+12	+24	+20	—	—	—	—	ps
	0.8	—	—	—	—		–10	+8	–2	+16	+6	+24	+14	+32	+24	—	—	ps
	0.7	—	—	—	—	—	—	+8	–8	+16	0	+24	+8	+32	+18	+40	+34	ps
	0.6	—	—	—	—	—	—	—	—	+15	–10	+23	–2	+31	+8	+39	+24	ps
	0.5	—	—	—	—	—	—	—	—	—	—	+14	–16	+22	–6	+30	+10	ps
	0.4	—	—	—	—	—	—	—	—	—	—	—	—	+7	–26	+15	–10	ps

[Required time tVAC above VIH(AC) {below VIL(AC)} for valid transition]

	DDR3-800, 1066		DDR3-1333, 1600	
	tVAC [ps]		tVAC [ps]	
Slew rate (V/ns)	min.	max.	min.	max.
>2.0	75	—	175	—
2.0	57	—	170	—
1.5	50	—	167	—
1.0	38	—	163	—
0.9	34	—	162	—
0.8	29	—	161	—
0.7	22	—	159	—
0.6	13	—	155	—
0.5	0	—	150	—
<0.5	0	—	150	—



Slew Rate Definition Nominal (CK, /CK)



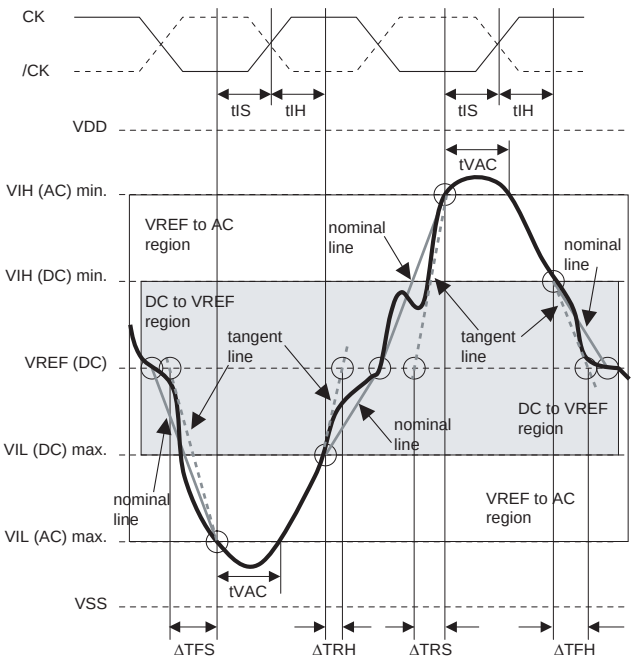
Slew Rate Definition Nominal (DQS, /DQS)

$$\text{Setup slew rate}_{\text{Falling signal}} = \frac{\text{VREF (DC)} - \text{VIL (AC) max.}}{\Delta\text{TFS}}$$

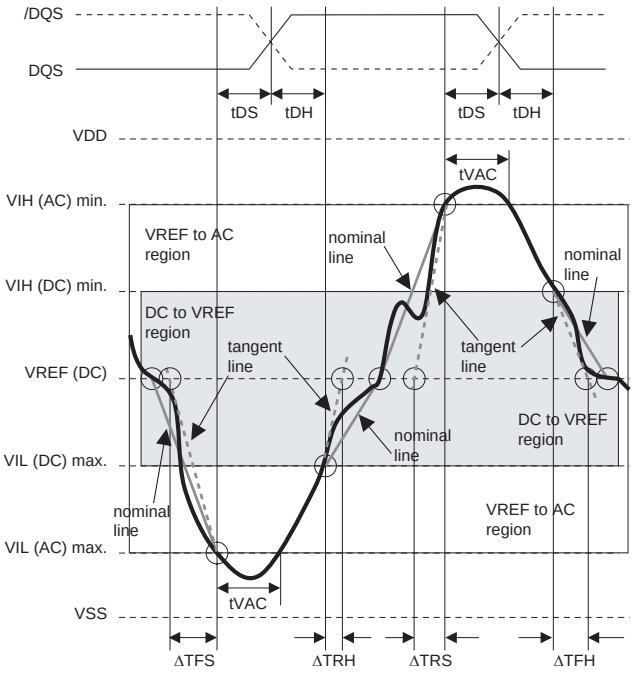
$$\text{Setup slew rate}_{\text{Rising signal}} = \frac{\text{VIH (AC) min.} - \text{VREF (DC)}}{\Delta\text{TRS}}$$

$$\text{Hold slew rate}_{\text{Rising signal}} = \frac{\text{VREF (DC)} - \text{VIL (DC) max.}}{\Delta\text{TRH}}$$

$$\text{Hold slew rate}_{\text{Falling signal}} = \frac{\text{VIH (DC) min.} - \text{VREF (DC)}}{\Delta\text{TFH}}$$



Slew Rate Definition Tangent (CK, /CK)



Slew Rate Definition Tangent (DQS, /DQS)

$$\text{Setup slew rate Falling signal} = \frac{\text{tangent line [VREF (DC) – VIL (AC) max.]}}{\Delta TFS}$$

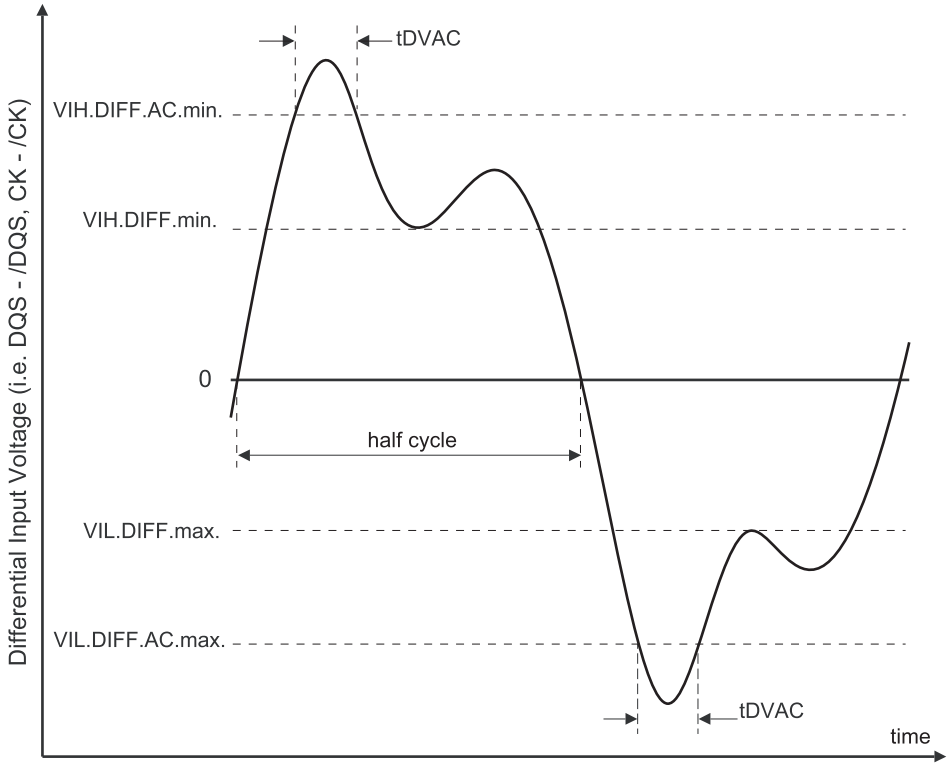
$$\text{Setup slew rate Rising signal} = \frac{\text{tangent line [VIH (AC) min. – VREF (DC)]}}{\Delta TRS}$$

$$\text{Hold slew rate Rising signal} = \frac{\text{tangent line [VREF (DC) – VIL (DC) max.]}}{\Delta TRH}$$

$$\text{Hold slew rate Falling signal} = \frac{\text{tangent line [VIH (DC) min. – VREF (DC)]}}{\Delta TFH}$$

AC and DC Logic Input Levels for Differential Signals

Differential signal definition



Definition of Differential AC-swing and "time above AC-level" tDVAC

[Differential AC and DC Input Levels]

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Differential input logic high	VIHdiff	+0.200	—	—*3	V	1
Differential input logic low	VILdiff	—*3	—	–0.200	V	1
Differential input logic AC	VIHdiff (AC)	2 × (VIH (AC) – VREF)	—	—*3	V	2
Differential input logic AC	VILdiff (AC)	—*3	—	2 × (VREF – VIL(AC))	V	2

Notes: 1 Used to define a differential signal slew-rate.

2. For CK, /CK use VIH/VIL(AC) of address/command and VREFCA; for strobes (DQS, /DQS, DQSL, /DQSL, DQSU, /DQSU) use VIH/VIL(AC) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

3 These values are not defined, however the single ended components of differential signal CK, /CK, DQS, /DQS, DQSL, /DQSL, DQSU, /DQSU need to be within the respective limits (VIH(DC) max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to Overshoot and Undershoot specifications.

[Required time tVAC above VIH(AC) {below VIL(AC)} for valid transition]

	@[VIH/Ldiff (AC)] = 350 mV		@[VIH/Ldiff (AC)] = 300 mV	
	tDVAC [ps]		tDVAC [ps]	
Slew rate (V/ns)	min.	max.	min.	max.
>4.0	75	—	175	—
4.0	57	—	170	—
3.0	50	—	167	—
2.0	38	—	163	—
1.8	34	—	162	—
1.6	29	—	161	—
1.4	22	—	159	—
1.2	13	—	155	—
1.0	0	—	150	—
<1.0	0	—	150	—

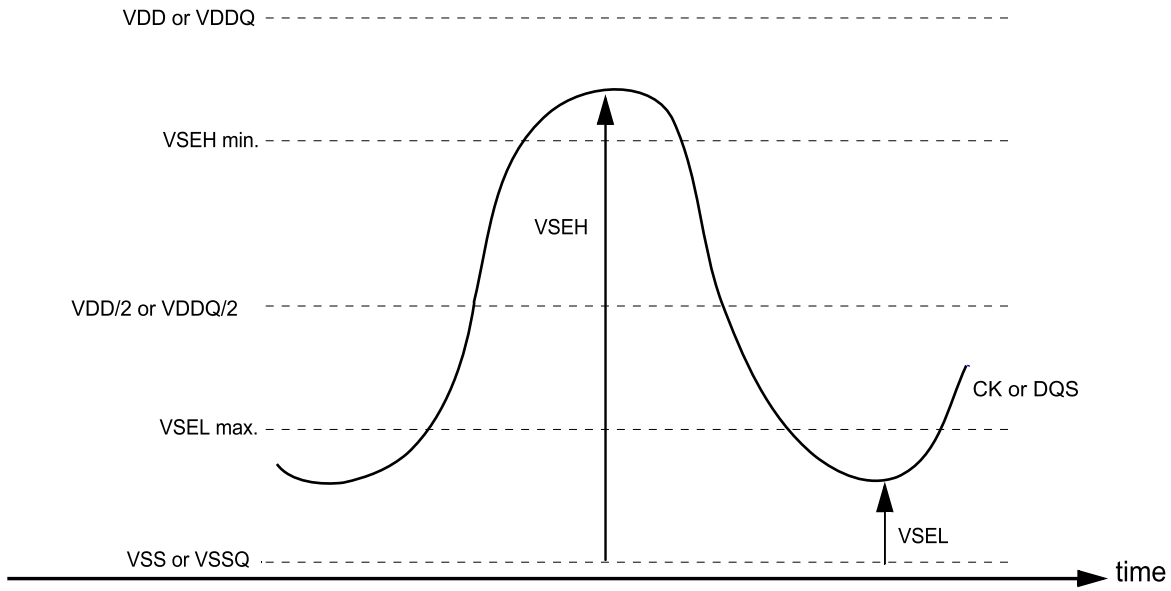
Single-Ended Requirements for Differential Signals

Each individual component of a differential signal (CK, DQS, DQSL, DQSU, /CK, /DQS, /DQSL or /DQSU) has also to comply with certain requirements for single-ended signals.

CK and /CK have to approximately reach VSEH min. / VSEL max. (approximately equal to the AC-levels (VIH(AC) / VIL(AC)) for Address/command signals) in every half-cycle.

DQS, DQSL, DQSU, /DQS, /DQSL have to reach VSEH min./VSEL max. (approximately the AC-levels (VIH(AC) / VIL(AC)) for DQ signals) in every half-cycle preceding and following a valid transition.

Note that the applicable ac-levels for Address/command and DQ's might be different per speed-bin etc. E.g. if VIH 150 (AC)/VIL 150 (AC) is used for Address/command signals, then these ac-levels apply also for the single ended components of differential CK and /CK.



Single-Ended Requirement for Differential Signals.

Note that while Address/command and DQ signal requirements are with respect to VREF, the single-ended components of differential signals have a requirement with respect to VDD / 2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSEL max, VSEH min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

[Single-ended levels for CK, DQS, DQSL, DQSU, /CK, /DQS, /DQSL or /DQSU]

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Single-ended high level for strobes	VSEH	(VDD/2) + 0.175	—	—*3	V	1, 2
Single-ended high level for CK, /CK		(VDD/2) + 0.175	—	—*3	V	1, 2
Single-ended low level for strobes	VSEL	—*3	—	(VDD/2) – 0.175	V	1, 2
Single-ended low level for CK, /CK		—*3	—	(VDD/2) – 0.175	V	1, 2

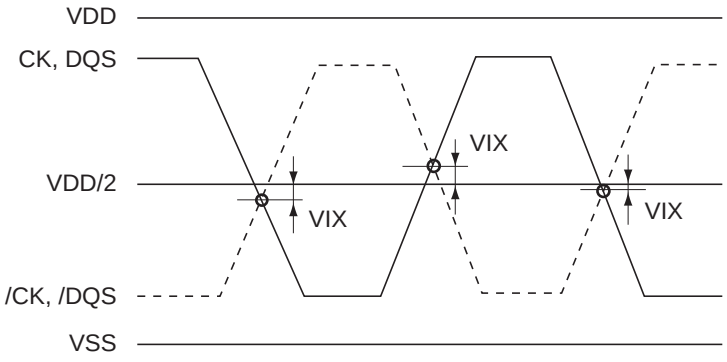
Notes: 1. For CK, /CK use VIH/VIL(AC) of ADD/CMD; for strobes (DQS, /DQS, DQSL, /DQSL, DQSU, /DQSU) use VIH/VIL(AC) of DQs.

2. VIH(AC)/VIL(AC) for DQs is based on VREFDQ; VIH(AC)/VIL(AC) for address/command is based on VREFCA; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

3 These values are not defined, however the single ended components of differential signals CK, /CK, DQS, /DQS, DQSL, /DQSL, DQSU, /DQSU need to be within the respective limits (VIH(DC) max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to Overshoot and Undershoot specifications.

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, /CK and DQS, /DQS) must meet the requirements in table above.

The differential input cross point voltage VIX is measured from the actual cross point of true and complement signal to the midlevel between of VDD and VSS.



VIX Definition

[Cross point voltage for differential input signals (CK, DQS)]

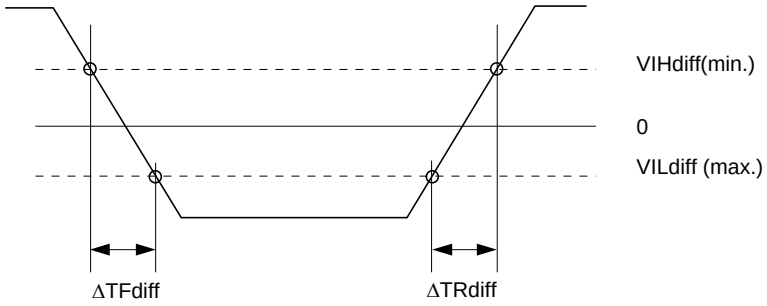
Parameter	Symbol	pins	min.	max.	Unit	Note
Differential input cross point voltage relative to VDD/2	VIX	CK, /CK	–150	150	mV	
			–175	175	mV	1
	VIX	DQS, /DQS	–150	150	mV	

Note: 1. Extended range for VIX is only allowed for clock and if CK and /CK are monotonic, have a single-ended swing VSEL/VSEH of at least VDD/2 +/-250 mV, and the differential slew rate of CK - /CK is larger than 3 V/ ns. Refer to the table of Cross point voltage for differential input signals (CK, DQS) for VSEL and VSEH standard values.

[Differential Input Slew Rate Definition]

Description	Measured From	Measured To	Defined by	Applicable for	Note
Differential input slew rate for rising edge (CK - /CK and DQS - /DQS)	VILdiff (max.)	VIHdiff (min.)	$\frac{\text{VIHdiff (min.) – VILdiff (max.)}}{\Delta\text{TRdiff}}$		
Differential input slew rate for falling edge (CK - /CK and DQS - /DQS)	VIHdiff (min.)	VILdiff (max.)	$\frac{\text{VIHdiff (min.). – VILdiff max.}}{\Delta\text{TFdiff}}$		

Note: The differential signal (i.e. CK, /CK and DQS, /DQS) must be linear between these thresholds.



$$\text{Falling slew} = \frac{\text{VIHdiff (min.)} - \text{VILdiff (max.)}}{\Delta\text{TFdiff}} \qquad \text{Rising slew} = \frac{\text{VIHdiff (min.)} - \text{VILdiff (max.)}}{\Delta\text{TRdiff}}$$

Differential Input Slew Rate Definition for DQS, /DQS and CK, /CK

AC and DC Output Measurement Levels (TC = 0°C to +85°C, VDD, VDDQ = 1.5V ± 0.075V)

Parameter	Symbol	Specification	Unit	Notes
DC output high measurement level (for IV curve linearity)	VOH (DC)	0.8 × VDDQ	V	
DC output middle measurement level (for IV curve linearity)	VOM (DC)	0.5 × VDDQ	V	
DC output low measurement level (for IV curve linearity)	VOL (DC)	0.2 × VDDQ	V	
AC output high measurement level (for output slew rate)	VOH (AC)	VTT + 0.1 × VDDQ	V	1
AC output low measurement level (for output slew rate)	VOL (AC)	VTT – 0.1 × VDDQ	V	1
AC differential output high measurement level (for output slew rate)	VOHdiff	0.2 × VDDQ	V	2
AC differential output low measurement level (for output slew rate)	VOLdiff	–0.2 × VDDQ	V	2
AC differential cross point voltage	VOX (AC)	TBD	V	

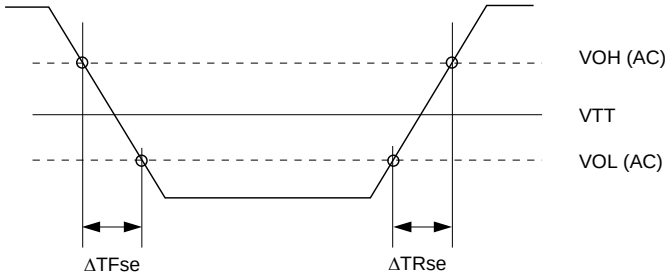
Notes: 1. The swing of ±0.1 × VDDQ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 34Ω and an effective test load of 25Ω to VTT = VDDQ/2 at each of the differential outputs.

2. The swing of ±0.2 × VDDQ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 34Ω and an effective test load of 25Ω to VTT = VDDQ/2 at each of the differential outputs.

Output Slew Rate Definitions

[Single-Ended Output Slew Rate Definition]

	Measured		
Description	From	To	Defined by
Output slew rate for rising edge	VOL (AC)	VOH (AC)	$\frac{VOH(AC) - VOL(AC)}{\Delta TRse}$
Output slew rate for falling edge	VOH (AC)	VOL (AC)	$\frac{VOH(AC) - VOL(AC)}{\Delta TFse}$

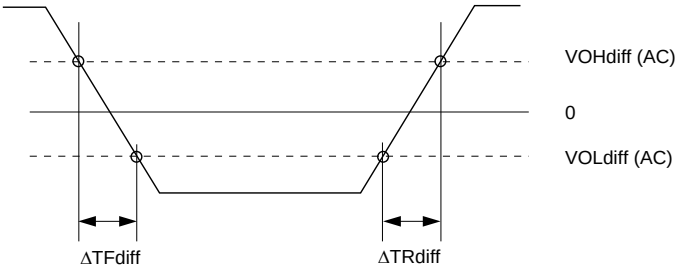


$$\text{Falling slew} = \frac{VOH(AC) - VOL(AC)}{\Delta TFse} \qquad \text{Rising slew} = \frac{VOH(AC) - VOL(AC)}{\Delta TRse}$$

Input Slew Rate Definition for Single-Ended Signals

[Differential Output Slew Rate Definition]

Description	Measured From	Measured To	Defined by
Differential output slew rate for rising edge	VOLdiff (AC)	VOHdiff (AC)	$\frac{\text{VOHdiff(AC)} - \text{VOLdiff (AC)}}{\Delta\text{TRdiff}}$
Differential output slew rate for falling edge	VOHdiff (AC)	VOLdiff (AC)	$\frac{\text{VOHdiff (AC)} - \text{VOLdiff (AC)}}{\Delta\text{TFdiff}}$



$$\text{Falling slew} = \frac{\text{VOHdiff (AC)} - \text{VOLdiff (AC)}}{\Delta\text{TFdiff}} \qquad \text{Rising slew} = \frac{\text{VOHdiff (AC)} - \text{VOLdiff (AC)}}{\Delta\text{TRdiff}}$$

Differential Input Slew Rate Definition for DQS, /DQS and CK, /CK

Output Slew Rate (RON = RZQ/7 setting)

Parameter	Symbol	Speed	min.	max.	Unit	Notes
Output slew rate (Single-ended)	SRQse	DDR3-800 DDR3-1066 DDR3-1333 DDR3-1600	2.5	5	V/ns	1
Output slew rate (Differential)	SRQdiff	DDR3-800 DDR3-1066 DDR3-1333 DDR3-1600	5	12	V/ns	1

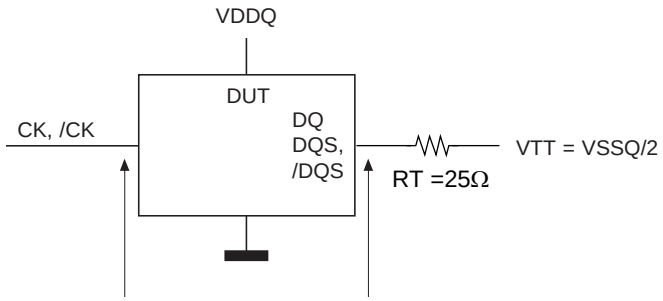
Remark: SR = slew rate. se = single-ended signals. diff = differential signals. Q = Query output

Note: 1.In two cases, a maximum slew rate of 6V/ns applies for a single DQ signal within a byte lane.

(a) is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).

(b) is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 5V/ns applies.

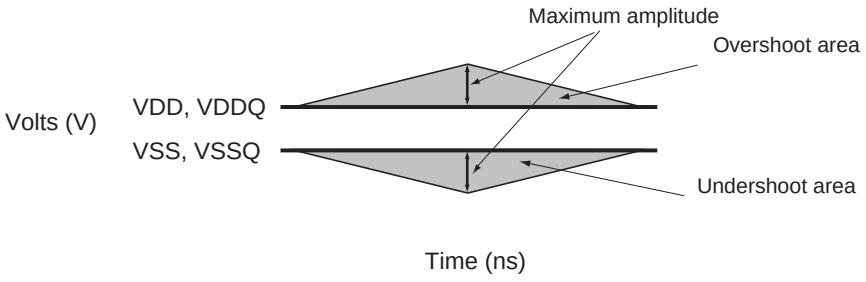
Reference Load for AC Timing and Output Slew Rate



Reference Output Load

AC Overshoot/Undershoot Specification

Parameter	Pins	Specification
Maximum peak amplitude allowed for overshoot	Command, Address, CKE, ODT	0.4V
Maximum peak amplitude allowed for undershoot		0.4V
Maximum overshoot area above VDD DDR3-1600		0.33V-ns
DDR3-1333		0.4V-ns
DDR3-1066		0.5V-ns
DDR3-800		0.67V-ns
Maximum undershoot area below VSS DDR3-1600		0.33V-ns
DDR3-1333		0.4V-ns
DDR3-1066		0.5V-ns
DDR3-800		0.67V-ns
Maximum peak amplitude allowed for overshoot	CK, /CK	0.4V
Maximum peak amplitude allowed for undershoot		0.4V
Maximum overshoot area above VDD DDR3-1600		0.13V-ns
DDR3-1333		0.15V-ns
DDR3-1066		0.19V-ns
DDR3-800		0.25V-ns
Maximum undershoot area below VSS DDR3-1600		0.13V-ns
DDR3-1333		0.15V-ns
DDR3-1066		0.19V-ns
DDR3-800		0.25V-ns
Maximum peak amplitude allowed for overshoot	DQ, DQS, /DQS, DM	0.4V
Maximum peak amplitude allowed for undershoot		0.4V
Maximum overshoot area above VDDQ DDR3-1600		0.13V-ns
DDR3-1333		0.15V-ns
DDR3-1066		0.19V-ns
DDR3-800		0.25V-ns
Maximum undershoot area below VSSQ DDR3-1600		0.13V-ns
DDR3-1333		0.15V-ns
DDR3-1066		0.19V-ns
DDR3-800		0.25V-ns



Overshoot/Undershoot Definition

Output Driver Impedance

RON will be achieved by the DDR3 SDRAM after proper I/O calibration. Tolerance and linearity requirements are referred to the Output Driver DC Electrical Characteristics table.

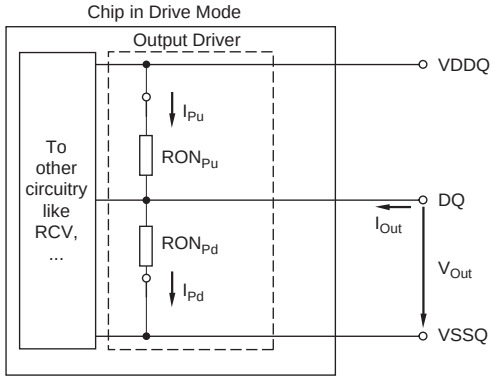
A functional representation of the output buffer is shown in the figure Output Driver: Definition of Voltages and Currents.

RON is defined by the value of the external reference resistor RZQ as follows:

- RON40 = RZQ/6
- RON34 = RZQ/7

The individual pull-up and pull-down resistors (RONPu and RONPd) are defined as follows:

Parameter	Symbol	Definition	Conditions
Output driver pull-up impedance	RONPu	$\frac{VDDQ - VOUT}{\lvert IOUT \rvert}$	RONPd is turned off
Output driver pull-down impedance	RONPd	$\frac{VOUT}{\lvert IOUT \rvert}$	RONPu is turned off



Output Driver: Definition of Voltages and Currents

Output Driver DC Electrical Characteristics

(RZQ = 240Ω, entire operating temperature range; after proper ZQ calibration)

RONnom	Resistor	VOUT	min.	nom.	max.	Unit	Notes
40Ω	RON40Pd	VOL (DC) = 0.2 × VDDQ	0.6	1.0	1.1	RZQ/6	1, 2, 3
		VOM (DC) = 0.5 × VDDQ	0.9	1.0	1.1		
		VOH (DC) = 0.8 × VDDQ	0.9	1.0	1.4		
	RON40Pu	VOL (DC) = 0.2 × VDDQ	0.9	1.0	1.4	RZQ/6	1, 2, 3
		VOM (DC) = 0.5 × VDDQ	0.9	1.0	1.1		
		VOH (DC) = 0.8 × VDDQ	0.6	1.0	1.1		
34Ω	RON34Pd	VOL (DC) = 0.2 × VDDQ	0.6	1.0	1.1	RZQ/7	1, 2, 3
		VOM (DC) = 0.5 × VDDQ	0.9	1.0	1.1		
		VOH (DC) = 0.8 × VDDQ	0.9	1.0	1.4		
	RON34Pu	VOL (DC) = 0.2 × VDDQ	0.9	1.0	1.4	RZQ/7	1, 2, 3
		VOM (DC) = 0.5 × VDDQ	0.9	1.0	1.1		
		VOH (DC) = 0.8 × VDDQ	0.6	1.0	1.1		
Mismatch between pull-up and pull down, MMPuPd		VOM (DC) = 0.5 × VDDQ	−10		10	%	1, 2, 4

Notes: 1. The tolerance limits are specified after calibration with stable voltage and temperature.
For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

2. The tolerance limits are specified under the condition that VDDQ = VDD and that VSSQ = VSS.
3. Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 × VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 × VDDQ and 0.8 × VDDQ.
4. Measurement definition for mismatch between pull-up and pull-down, MMPuPd:
Measure RONPu and RONPd, both at 0.5 × VDDQ:

$$MMPuPd = \frac{RONPu - RONPd}{RONnom} \times 100$$

Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the table Output Driver Sensitivity Definition and Output Driver Voltage and Temperature Sensitivity.

ΔT = T − T (@calibration); ΔV= VDDQ − VDDQ (@calibration); VDD = VDDQ

Note: dRONdT and dRONdV are not subject to production test but are verified by design and characterization.

[Output Driver Sensitivity Definition]

	min	max	unit
RONPu@VOH (DC)	0.6 − dRONdTH × |ΔT| − dRONdVH × |ΔV|	1.1 + dRONdTH × |ΔT| + dRONdVH × |ΔV|	RZQ/7
RON@ VOM (DC)	0.9 − dRONdTM × |ΔT| − dRONdVM × |ΔV|	1.1 + dRONdTM × |ΔT| + dRONdVM × |ΔV|	RZQ/7
RONPd@VOL (DC)	0.6 − dRONdTL × |ΔT| − dRONdVL × |ΔV|	1.1 + dRONdTL × |ΔT| + dRONdVL × |ΔV|	RZQ/7

[Output Driver Voltage and Temperature Sensitivity]

	min.	max.	Unit
dRONdTM	0	1.5	%/°C
dRONdVM	0	0.15	%/mV
dRONdTL	0	1.5	%/°C
dRONdVL	0	TBD	%/mV
dRONdTH	0	1.5	%/°C
dRONdVH	0	TBD	%/mV

On-Die Termination (ODT) Levels and I-V Characteristics

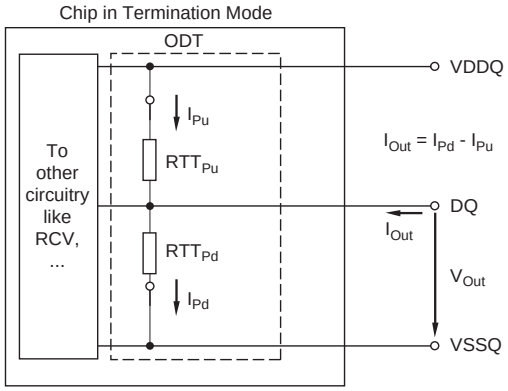
On-Die Termination effective resistance RTT is defined by bits A9, A6 and A2 of the MR1 Register.

ODT is applied to the DQ, DM, DQS, /DQS and TDQS, /TDQS (×8 devices only) pins.

A functional representation of the on-die termination is shown in the figure On-Die Termination: Definition of Voltages and Currents.

The individual pull-up and pull-down resistors (RTTPu and RTTPd) are defined as follows:

Parameter	Symbol	Definition	Conditions
ODT pull-up resistance	RTTPu	$\frlac{VDDQ - VOUT}{\lvert IOUT \rvert}$	RTTPd is turned off
ODT pull-down resistance	RTTPd	$\frac{VOUT}{\lvert IOUT \rvert}$	RTTPu is turned off



On-Die Termination: Definition of Voltages and Currents

The value of the termination resistor can be set via MRS command to RTT60 = RZQ/4 (nom) or RTT120 = RZQ/2 (nom).

RTT60 or RTT120 will be achieved by the DDR3 SDRAM after proper IO calibration has been performed. Tolerances requirements are referred to the ODT DC Electrical Characteristics table.

Measurement Definition for RTT

Apply VIH (AC) to pin under test and measure current I(VIH(AC)), then apply VIL(AC) to pin under test and measure current I(VIL(AC)) respectively.

$$RTT = \frac{VIH(AC) - VIL(AC)}{I(VIH(AC)) - I(VIL(AC))}$$

Measurement Definition for ΔVM

Measure voltage (VM) at test pin (midpoint) with no load.

$$\Delta VM = \left(\frac{2 \times VM}{VDDQ} - 1 \right) \times 100$$

ODT DC Electrical Characteristics

(RZQ = 240Ω, entire operating temperature range; after proper ZQ calibration)

MR1 [A9, A6, A2]	RTT	Resistor	VOUT	min.	nom.	max.	Unit	Notes
[0, 1, 0]	120Ω	RTT120Pd240	VOL (DC)	0.6	1.0	1.1	RZQ	1, 2, 3, 4
			VOM (DC)	0.9	1.0	1.1		
			VOH (DC)	0.9	1.0	1.4		
		RTT120Pu240	VOL (DC)	0.9	1.0	1.4	RZQ	1, 2, 3, 4
			VOM (DC)	0.9	1.0	1.1		
			VOH (DC)	0.6	1.0	1.1		
		RTT120	VIL (AC) to VIH (AC)	0.9	1.0	1.6	RZQ/2	1, 2, 5
[0, 0, 1]	60Ω	RTT60Pd120	VOL (DC)	0.6	1.0	1.1	RZQ/2	1, 2, 3, 4
			VOM (DC)	0.9	1.0	1.1		
			VOH (DC)	0.9	1.0	1.4		
		RTT60Pu120	VOL (DC)	0.9	1.0	1.4	RZQ/2	1, 2, 3, 4
			VOM (DC)	0.9	1.0	1.1		
			VOH (DC)	0.6	1.0	1.1		
		RTT60	VIL (AC) to VIH (AC)	0.9	1.0	1.6	RZQ/4	1, 2, 5
[0, 1.1]	40Ω	RTT40Pd80	VOL (DC)	0.6	1.0	1.1	RZQ/3	1, 2, 3, 4
			VOM (DC)	0.9	1.0	1.1		
			VOH (DC)	0.9	1.0	1.4		
		RTT40Pu80	VOL (DC)	0.9	1.0	1.4	RZQ/3	1, 2, 3, 4
			VOM (DC)	0.9	1.0	1.1		
			VOH (DC)	0.6	1.0	1.1		
		RTT40	VIL (AC) to VIH (AC)	0.9	1.0	1.6	RZQ/6	1, 2, 5
[1, 0, 1]	30Ω	RTT30Pd60	VOL (DC)	0.6	1.0	1.1	RZQ/4	1, 2, 3, 4
			VOM (DC)	0.9	1.0	1.1		
			VOH (DC)	0.9	1.0	1.4		
		RTT30Pu60	VOL (DC)	0.9	1.0	1.4	RZQ/4	1, 2, 3, 4
			VOM (DC)	0.9	1.0	1.1		
			VOH (DC)	0.6	1.0	1.1		
		RTT30	VIL (AC) to VIH (AC)	0.9	1.0	1.6	RZQ/8	1, 2, 5
[1, 0, 0]	20Ω	RTT20Pd40	VOL (DC)	0.6	1.0	1.1	RZQ/6	1, 2, 3, 4
			VOM (DC)	0.9	1.0	1.1		
			VOH (DC)	0.9	1.0	1.4		
		RTT20Pu40	VOL (DC)	0.9	1.0	1.4	RZQ/6	1, 2, 3, 4
			VOM (DC)	0.9	1.0	1.1		
			VOH (DC)	0.6	1.0	1.1		
		RTT20	VIL (AC) to VIH (AC)	0.9	1.0	1.6	RZQ/12	1, 2, 5
Deviation of VM w.r.t. VDDQ/2, ΔVM				–5		5	%	1, 2, 5, 6

Notes: 1. The tolerance limits are specified after calibration with stable voltage and temperature.
For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

2. The tolerance limits are specified under the condition that VDDQ = VDD and that VSSQ = VSS.

3. Pull-down and pull-up output resistors are recommended to be calibrated at 0.5 × VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 × VDDQ and 0.8 × VDDQ.

4. Not a specification requirement, but a design guide line.

5. Measurement Definition for RTT:
Apply VIH (AC) to pin under test and measure current I(VIH(AC)), then apply VIL(AC) to pin under test and measure current I(VIL(AC)) respectively.

$$RTT = \frac{VIH(AC) - VIL(AC)}{I(VIH(AC)) - I(VIL(AC))}$$

6. Measurement Definition for VM and ΔVM:
   Measure voltage (VM) at test pin (midpoint) with no load:

$$\Delta VM = \left(\frac{2 \times VM}{VDDQ} - 1 \right) \times 100$$

ODT Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the table ODT Sensitivity Definition and ODT Voltage and Temperature Sensitivity.

ΔT = T – T (@calibration); ΔV= VDDQ – VDDQ (@calibration); VDD = VDDQ

Note: dRTTdT and dRTTdV are not subject to production test but are verified by design and characterization.

[ODT Sensitivity Definition]

	min.	max.	Unit
RTT	0.9 – dRTTdT × |ΔT| - dRTTdV × |ΔV|	1.6 + dRTTdT×|ΔT| + dRTTdV × |ΔV|	RZQ/2, 4, 6, 8, 12

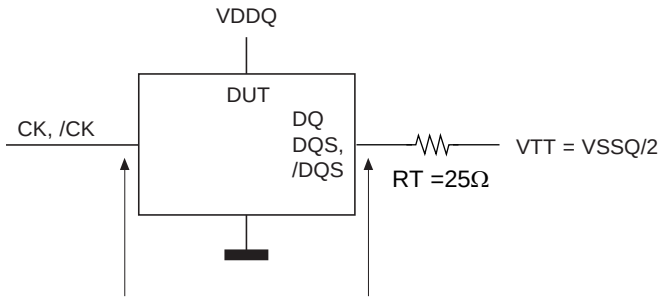
[ODT Voltage and Temperature Sensitivity]

	min.	max.	Unit
dRTTdT	0	1.5	%/°C
dRTTdV	0	0.15	%/mV

ODT Timing Definitions

Test Load for ODT Timings

Different than for timing measurements, the reference load for ODT timings are defined in ODT Timing Reference Load.



ODT Timing Reference Load

ODT Measurement Definitions

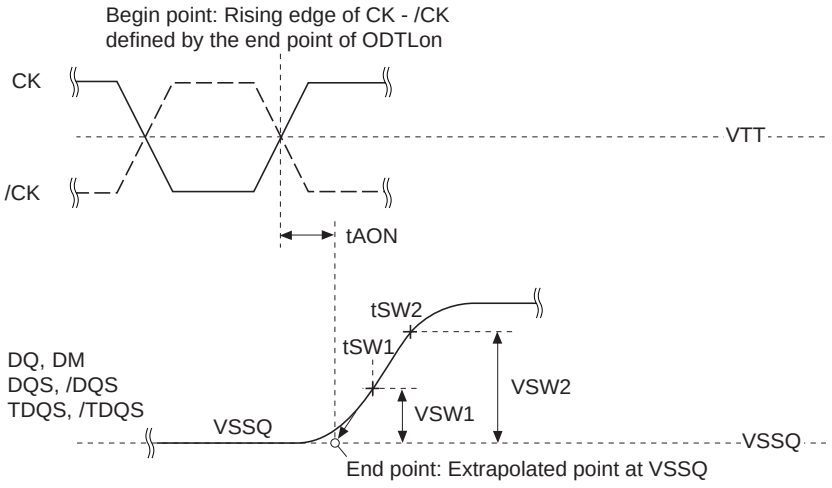
Definitions for tAON, tAONPD, tAOF, tAOFPD and tADC are provided in the following table and subsequent figures.

Symbol	Begin Point Definition	End Point Definition	Figure
tAON	Rising edge of CK - /CK defined by the end point of ODTLon	Extrapolated point at VSSQ	Figure a)
tAONPD	Rising edge of CK - /CK with ODT being first registered high	Extrapolated point at VSSQ	Figure b)
tAOF	Rising edge of CK - /CK defined by the end point of ODTLoff	End point: Extrapolated point at VRTT_Nom	Figure c)
tAOFPD	Rising edge of CK - /CK with ODT being first registered low	End point: Extrapolated point at VRTT_Nom	Figure d)
tADC	Rising edge of CK - /CK defined by the end point of ODTLcnw, ODTLcwn4 or ODTLcwn8	End point: Extrapolated point at VRTT_WR and VRTT_Nom respectively	Figure e)

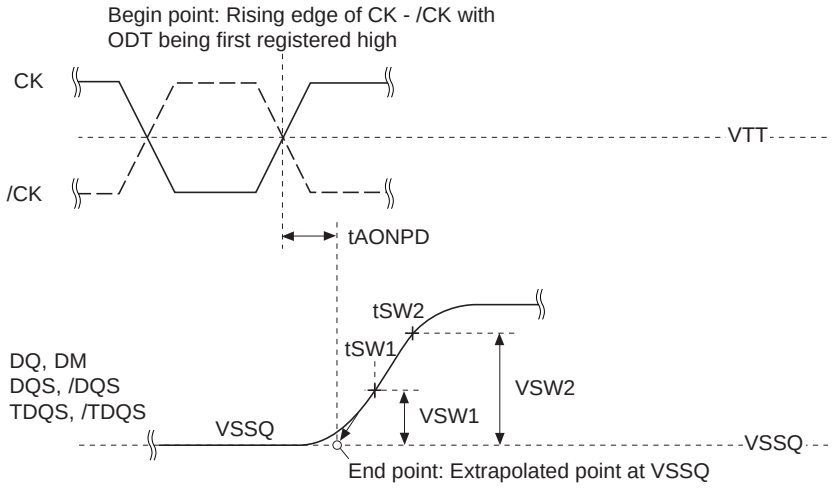
Reference Settings for ODT Timing Measurements

Measurement reference settings are provided in the following Table.

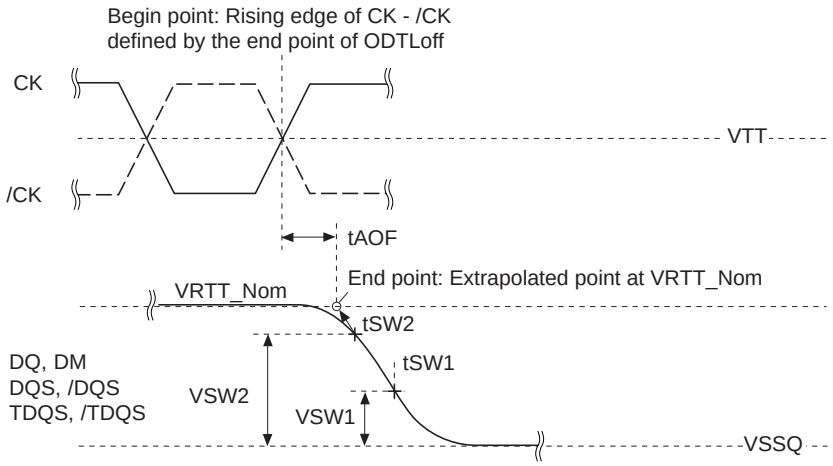
Measured Parameter	RTT_Nom Setting	RTT_WR Setting	VSW1 [V]	VSW2 [V]	Note
tAON	RZQ/4	N/A	0.05	0.10	
	RZQ/12	N/A	0.10	0.20	
tAONPD	RZQ/4	N/A	0.05	0.10	
	RZQ/12	N/A	0.10	0.20	
tAOF	RZQ/4	N/A	0.05	0.10	
	RZQ/12	N/A	0.10	0.20	
tAOFPD	RZQ/4	N/A	0.05	0.10	
	RZQ/12	N/A	0.10	0.20	
tADC	RZQ/12	RZQ/2	0.20	0.30	



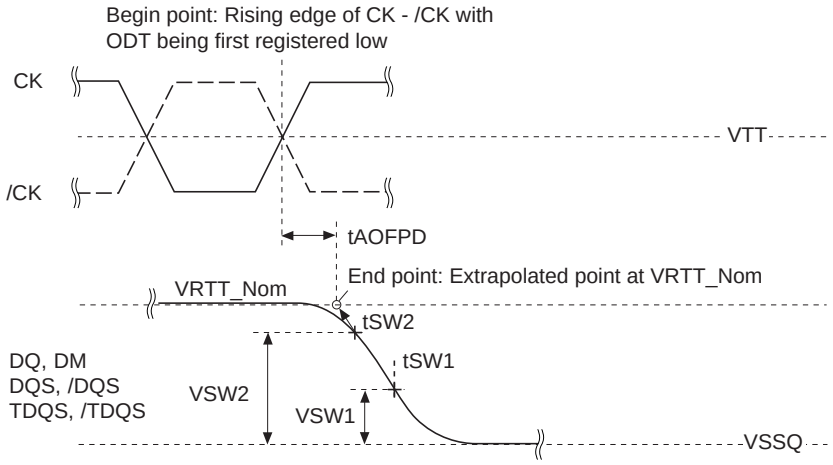
a) Definition of tAON



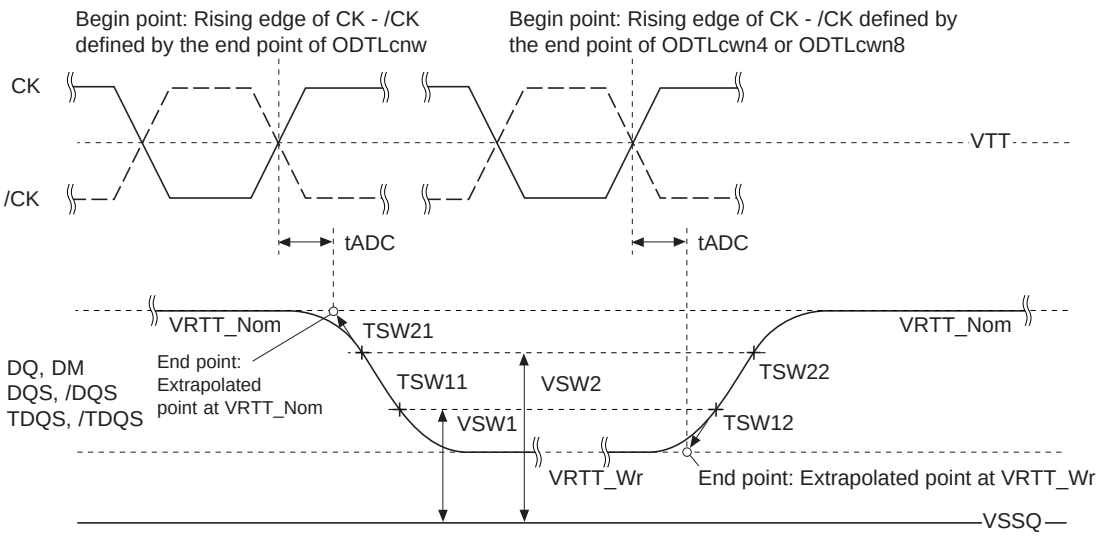
b) Definition of tAONPD



c) Definition of tAOF



d) Definition of tAOFPD



e) Definition of tADC

IDD Measurement Conditions (TC = 0°C to +85°C, VDD, VDDQ = 1.5V ± 0.075V)

Within the tables about IDD measurement conditions, the following definitions are used:

- L: VIN ≤ VIL (AC)(max.)
- H: VIN ≥ VIH (AC)(min.);
- STABLE: inputs are stable at H or L level
- FLOATING: inputs are VREF = VDDQ / 2
- SWITCHING: Described in the following Definition of SWITCHING table.
- N/A: not available

[Definition of SWITCHING]

Signals	Definitions
Address (row, column)	If not otherwise mentioned the inputs are stable at H or L during 4 clocks and change then to the opposite value (e.g. Ax Ax Ax Ax /Ax /Ax /Ax /Ax Ax Ax Ax Ax ..... Please see each IDDx definition for details
Bank address	If not otherwise mentioned the bank addresses should be switched like the row/column addresses - please see each IDDx definition for details
Command (/CS, /RAS, /CAS, /WE)	Define D = {/CS, /RAS, /CAS, /WE } := {H, L, L, L} Define /D = {/CS, /RAS, /CAS, /WE } := {H, H, H, H} Define Command Background Pattern = D D /D /D D D /D /D D D /D /D ... If other commands are necessary (e.g. ACT for IDD0 or Read for IDD4R) the Background Pattern Command is substituted by the respective /CS, /RAS, /CAS, /WE levels of the necessary command. See each IDDx definition for details and figures of Example of IDD1, IDD2N/IDD3N, IDD4R.
Data (DQ)	Data DQ is changing between H and L every other data transfer (once per clock) for DQ signals, which means that data DQ is stable during one clock; see each IDDx definition for exceptions from this rule and for further details. See figures of Example of IDD1, IDD2N/IDD3N, IDD4R.
Data Masking (DM)	NO Switching; DM must be driven L all the time

AC Timing for IDD Test Conditions

For purposes of IDD testing, the following parameters are to be utilized.

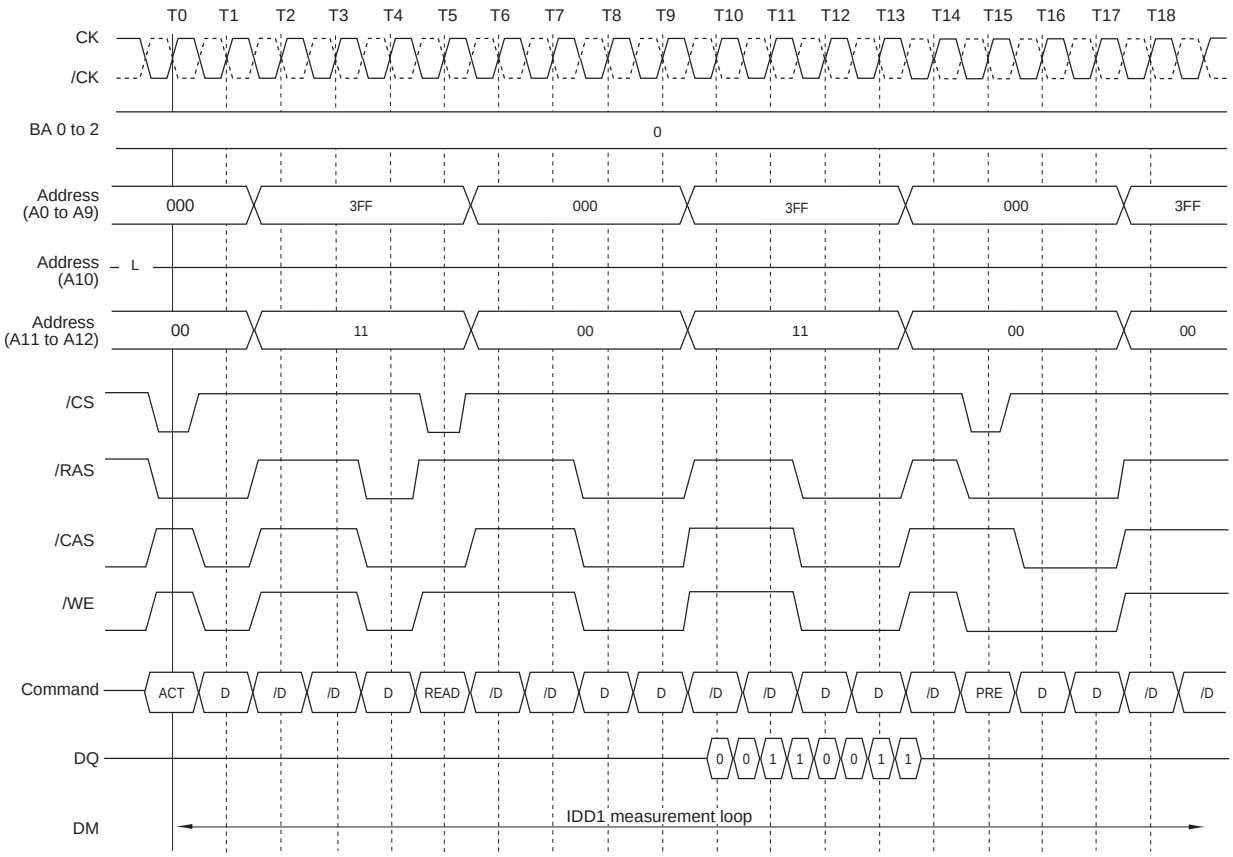
	DDR3-1600		DDR3-1333		DDR3-1066			DDR3-800		
Parameter	10-10-10	11-11-11	8-8-8	9-9-9	6-6-6	7-7-7	8-8-8	5-5-5	6-6-6	Unit
CL (IDD)	10	11	8	9	6	7	8	5	6	tCK
tCK min.(IDD)	1.25	1.25	1.5	1.5	1.875	1.875	1.875	2.5	2.5	ns
tRCD min. (IDD)	12.5	13.75	12	13.5	11.25	13.13	15	12.5	15	ns
tRC min. (IDD)	47.5	48.75	48	49.5	48.75	50.63	52.50	50	52.5	ns
tRAS min.(IDD)	35	35	36	36	37.5	37.5	37.5	37.5	37.5	ns
tRP min. (IDD)	12.5	13.75	12	13.5	11.25	13.13	15	12.5	15	ns
tFAW (IDD)-×4/×8	30	30	30	30	37.5	37.5	37.5	40	40	ns
tFAW (IDD)-×16	—	—	45	45	50	50	50	50	50	ns
tRRD (IDD)-×4/×8	6.0	6.0	6.0	6.0	7.5	7.5	7.5	10	10	ns
tRRD (IDD)-×16	—	—	7.5	7.5	10	10	10	10	10	ns
tRFC (IDD)	110	110	110	110	110	110	110	110	110	ns

The following conditions apply:

- IDD specifications are tested after the device is properly initialized.
- Input slew rate is specified by AC Parametric test conditions.
- IDD parameters are specified with ODT and output buffer disabled (MR1 bit A12 = 1).

IDD Measurement Conditions for IDD0 and IDD1

Symbol	IDD0	IDD1
Name	Operating Current 0 -> One Bank Activate -> Precharge	Operating Current 1 -> One Bank Activate -> Read -> Precharge
Measurement Condition		
Timing Diagram Example	—	Figure IDD1 Example
CKE	H	H
External Clock	on	on
tCK	tCK min (IDD)	tCK min (IDD)
tRC	tRC min (IDD)	tRC min (IDD)
tRAS	tRAS min (IDD)	tRAS min (IDD)
tRCD	N/A	tRCD min (IDD)
tRRD	N/A	N/A
CL	N/A	CL(IDD)
AL	N/A	0
/CS	H between. Activate and Precharge Commands	H between Activate, Read and Precharge
Command inputs (/CS, /RAS, /CAS, /WE)	SWITCHING (see Definition of SWITCHING table); only exceptions are Activate and Precharge commands; example of IDD0 pattern: A0 D /D /D D D /D /D D D /D/D D D /D P0 (DDR3-800: tRAS = 37.5ns between (A)ctivate and (P)recharge to bank 0; Definition of D and /D: see Definition of SWITCHING table	SWITCHING (see Definition of SWITCHING table); only exceptions are Activate, Read and Precharge commands; example of IDD1 pattern: A0 D /D /D D R0 /D /D D D /D/D D D /D P0 (DDR3-800 -555: tRCD = 12.5ns between (A)ctivate and (R)ead to bank 0; Definition of D and /D: see Definition of SWITCHING table
Row, column addresses	Row addresses SWITCHING (see Definition of SWITCHING table); A10 must be L all the time!	Row addresses SWITCHING (see Definition of SWITCHING table);A10 must be L all the time!
Bank addresses	Bank address is fixed (bank 0)	Bank address is fixed (bank 0)
Data I/O	SWITCHING (see Definition of SWITCHING table)	Read Data: output data switches every clock, which means that Read data is stable during one clock cycle. To achieve IOUT = 0mA the output buffer should be switched off by MR1 bit A12 set to “1”. When there is no read data burst from DRAM the DQ I/O should be FLOATING.
Output Buffer DQ, DQS / MR1 bit A12	off / 1	off / 1
ODT / MR1 bits [A9, A6, A2] / MR2 bits [A1, A0]	disabled / [0,0,0] / [0,0]	disabled / [0,0,0] / [0,0]
Burst length	N/A	8 fixed / MR0 bits [A1, A0] = {0,0}
Active banks	one ACT-PRE loop	one ACT-READ-PRE loop
Idle banks	all other	all other
Precharge Power-down Mode / MR0 bit A12	N/A	N/A



IDD1 Example* (DDR3-800-555, 512Mb ×8)

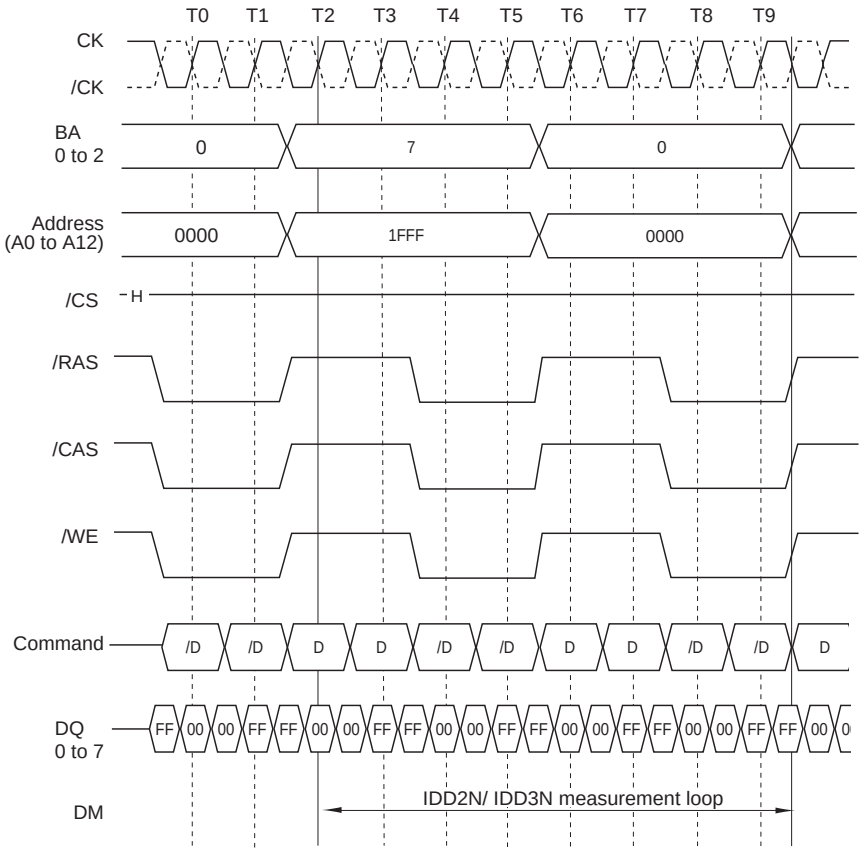
Note: Data DQ is shown but the output buffer should be switched off (per MR1 bit A12 = 1) to achieve IOUT = 0mA. Address inputs are split into 3 parts.

IDD Measurement Conditions for IDD2N, IDD2P (1), IDD2P (0) and IDD2Q

Symbol	IDD2N	IDD2P (1)*1	IDD2P (0)*1	IDD2Q
Name	Precharge standby current	Precharge power-down current (fast exit MR0 bit A12= 1)	Precharge power-down current (slow exit MR0 bit A12= 0)	Precharge quiet standby current
Measurement Condition				
Timing Diagram Example	Figure IDD2N/IDD3N Example	—	—	—
CKE	H	L	L	H
External Clock	on	on	on	on
tCK	tCK min (IDD)	tCK min (IDD)	tCK min (IDD)	tCK min (IDD)
tRC	N/A	N/A	N/A	N/A
tRAS	N/A	N/A	N/A	N/A
tRCD	N/A	N/A	N/A	N/A
tRRD	N/A	N/A	N/A	N/A
CL	N/A	N/A	N/A	N/A
AL	N/A	N/A	N/A	N/A
/CS	H	STABLE	STABLE	H
Bank address, row address and command inputs	SWITCHING (see Definition of SWITCHING table)	STABLE	STABLE	STABLE
Data inputs	SWITCHING	FLOATING	FLOATING	FLOATING
Output buffer DQ, DQS / MR1 bit A12	off / 1	off / 1	off / 1	off / 1
ODT / MR1 bits [A9, A6, A2] / MR2 bits [A1, A0]	disabled / [0,0,0] / [0,0]	disabled / [0,0,0] / [0,0]	disabled / [0,0,0] / [0,0]	disabled / [0,0,0] / [0,0]
Burst length	N/A	N/A	N/A	N/A
Active banks	none	none	none	none
Idle banks	all	all	all	all
Precharge Power-down Mode / MR0 bit A12	N/A	Fast exit / 1 (any valid command after tXP*2)	Slow exit / 0 Slow exit (READ and ODT commands must satisfy tXPDLL-AL)	N/A

Notes: 1. In DDR3 the MR0 bit A12 defines DLL-on/off behaviors only for precharge power-down. There are two different precharge power-down states possible: one with DLL-on (fast exit, bit A12 = 1) and one with DLL-off (slow exit, bit A12 = 0).

2. Because it is an exit after precharge power-down the valid commands are: bank activate (ACT), auto-refresh (REF), mode register set (MRS), self-refresh (SELF).



IDD2N/IDD3N Example (DDR3-800-555, 512Mb ×8)

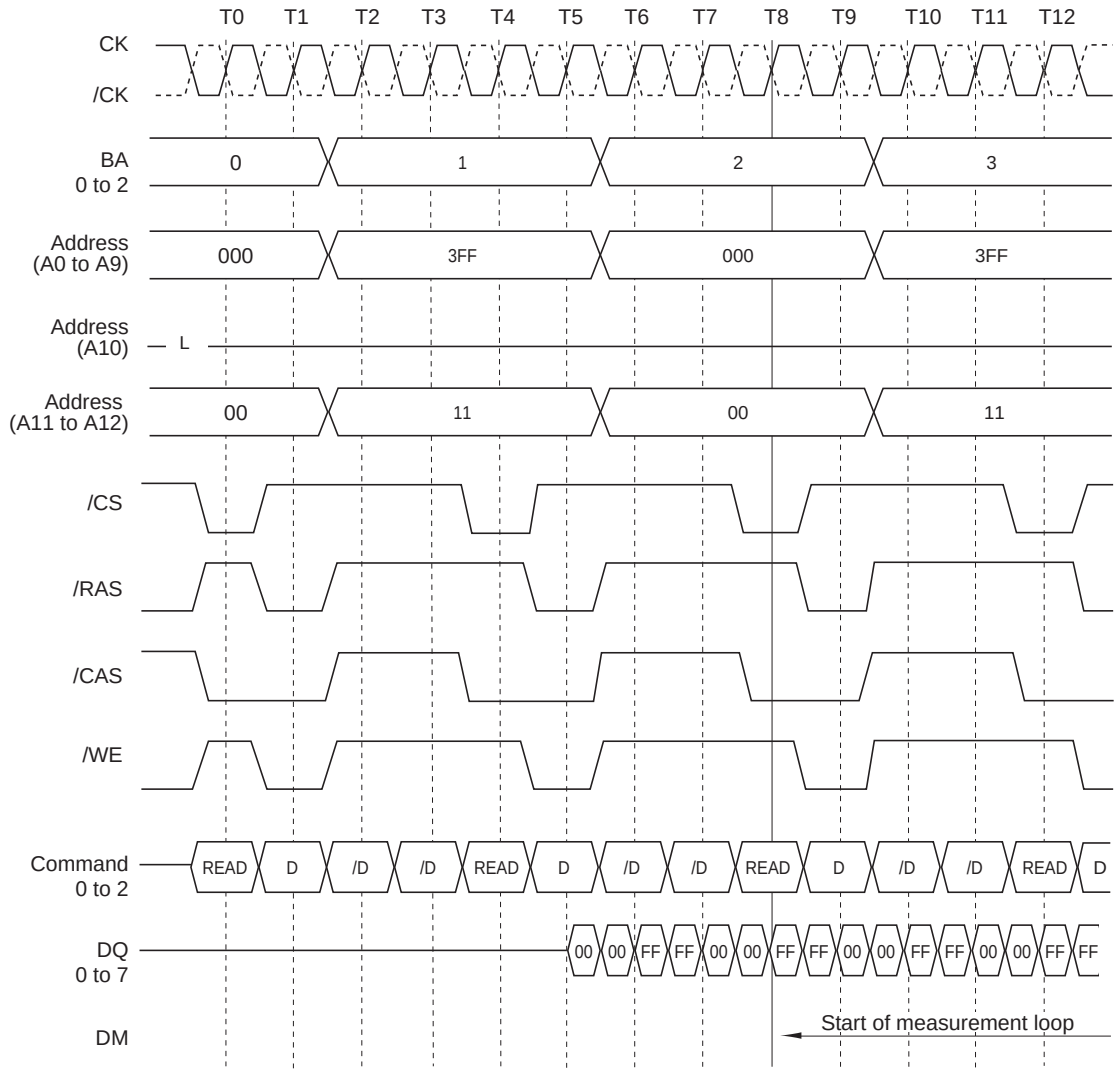
IDD Measurement Conditions for IDD3N, IDD3P (fast exit)

Symbol	IDD3N	IDD3P (1)
Name	Active standby current	Active power-down current* (always fast exit)
Measurement Condition		
Timing Diagram Example	Figure IDD2N/IDD3N Example	—
CKE	H	L
External Clock	on	on
tCK	tCK min (IDD)	tCK min (IDD)
tRC	N/A	N/A
tRAS	N/A	N/A
tRCD	N/A	N/A
tRRD	N/A	N/A
CL	N/A	N/A
AL	N/A	N/A
/CS	H	STABLE
Address and command inputs	SWITCHIN (see Definition of SWITCHING table)	STABLE
Data inputs	SWITCHING (see Definition of SWITCHING table)	FLOATING
Output buffer DQ, DQS / MR1 bit A12	off / 1	off / 1
ODT / MR1 bits [A9, A6, A2] / MR2 bits [A1, A0]	disabled / [0,0,0] / [0,0]	disabled / [0,0,0] / [0,0]
Burst length	N/A	N/A
Active banks	all	all
Idle banks	none	none
Precharge Power-down Mode / MR0 bit A12	N/A	N/A (Active Power-down Mode is always “Fast Exit” with DLL-on)

Note: DDR3 will offer only one active power-down mode with DLL-on (-> fast exit). MR0 bit A12 will not be used for active power-down. Instead bit A12 will be used to switch between two different precharge power-down modes.

IDD Measurement Conditions for IDD4R, IDD4W and IDD7

Symbol	IDD4R	IDD4W	IDD7
Name	Operating current (Burst read operating)	Operating current (Burst write operating)	All bank interleave read current
Measurement Condition			
Timing Diagram Example	IDD4R Example	—	—
CKE	H	H	H
External Clock	on	on	on
tCK	tCK min (IDD)	tCK min (IDD)	tCK min (IDD)
tRC	N/A	N/A	tRC min. (IDD)
tRAS	N/A	N/A	tRAS min. (IDD)
tRCD	N/A	N/A	tRCD min. (IDD)
tRRD	N/A	N/A	tRRD min. (IDD)
CL	CL (IDD)	CL (IDD)	CL (IDD)
AL	0	0	tRCD min. – 1tCK
/CS	H between valid commands	H between valid commands	H between valid commands
Command inputs (/CS, /RAS, /CAS, /WE)	SWITCHING (see Definition of SWITCHING table); only exceptions are read commands -> IDD4R pattern: R0 D /D /D R1 D /D /D R2 D /D /D R3 D /D /D R4 ..... Rx = Read from bank x; Definition of D and /D: see Definition of SWITCHING table	SWITCHING (see Definition of SWITCHING table); only exceptions are write commands -> IDD4W pattern: W0 D /D /D W1 D /D /D W2 D /D /D W3 D /D /D W4... Wx = Write to bank x; Definition of D and /D: see Definition of SWITCHING table	For patterns see pattern in IDD7 Timing Patterns section
Row, column addresses	Column addresses SWITCHING (see Definition of SWITCHING table); A10 must be L all the time!	Column addresses SWITCHING (see Definition of SWITCHING table); A10 must be L all the time!	STABLE during DESELECTs
Bank addresses	bank address cycling (0 -> 1 -> 2 -> 3 ...)	bank address cycling (0 -> 1 -> 2 -> 3 ...)	bank address cycling (0 -> 1 -> 2 -> 3 ...), see pattern in IDD7 Timing Patterns section
Data I/O	Seamless read data burst (BL8): output data switches every clock, which means that Read data is stable during one clock cycle. To achieve IOUT = 0mA the output buffer should be switched off by MR1 bit A12 set to “1”.	Seamless write data burst (BL8): input data switches every clock, which means that write data is stable during one clock cycle. DM is low all the time	Read data (BL8): output data switches every clock, which means that Read data is stable during one clock cycle. To achieve IOUT = 0mA the output buffer should be switched off by MR1 bit A12 set to “1”.
Output Buffer DQ, DQS / MR1 bit A12	off / 1	off / 1	off / 1
ODT / MR1 bits [A9, A6, A2] / MR2 bits [A1, A0]	disabled / [0,0,0] / [0,0]	disabled / [0,0,0] / [0,0]	disabled / [0,0,0] / [0,0]
Burst length	8 fixed / MR0 [A1, A0] = {0,0}	8 fixed / MR0 bits [A1, A0] = {0,0}	8 fixed / MR0 bits [A1, A0] = {0,0}
Active banks	all	all	all, rotational
Idle banks	none	none	none
Precharge Power-down Mode / MR0 bit A12	N/A	N/A	N/A



IDD4R Example* (DDR3-800-555, 512Mb ×8)

Note: Data DQ is shown but the output buffer should be switched off (per MR1 bit A12 = 1) to achieve IOUT = 0mA. Address inputs are split into 3 parts.

IDD7 Timing Patterns

The detailed timings are shown in the IDD7 Timing Patterns for 8 Banks tables.

Speed bins	Bin	Organization	tFAW (ns)	tFAW (tCK)	tRRD (ns)	tRRD (tCK)	Timing Patterns
DDR3-800	all	×4/×8	40	16	10	4	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D
	all	×16	50	20	10	4	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D D D
DDR3-1066	all	×4/×8	37.5	20	7.5	4	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D D D
	all	×16	50	27	10	6	A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D D D D A3 RA3 D D D D D D D A4 RA4 D D D D A5 RA5 D D D D A6 RA6 D D D D A7 RA7 D D D D D D D
DDR3-1333	all	×4/×8	30	20	6	4	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D D D
	all	×16	45	30	7.5	5	A0 RA0 D D D A1 RA1 D D D A2 RA2 D D D A3 RA3 D D D D D D D D D D D A4 RA4 D D D A5 RA5 D D D A6 RA6 D D D A7 RA7 D D D D D D D D D D D D
DDR3-1600	all	×8	30	24	6	5	A0 RA0 D D D A1 RA1 D D D A2 RA2 D D D A3 RA3 D D D D D D A4 RA4 D D D A5 RA5 D D D A6 RA6 D D D A7 RA7 D D D D D D D

Remark: Ax = Active command for bank x.
RAx = Read with auto precharge command from bank x.
ex. RA0 = READA command from bank 0

Notes: 1. All banks are being interleaved at minimum tRC (IDD) without violating tRRD (IDD) and tFAW (IDD) using a burst length = 8.
2. Control and address bus inputs are STABLE during DESELECTs.
3. IOUT = 0mA.

IDD Measurement Conditions for IDD5B

Symbol	IDD5B
Name	Burst refresh current
Measurement Condition	
Timing Diagram Example	
CKE	H
External Clock	on
tCK	tCK min. (IDD)
tRC	N/A
tRAS	N/A
tRCD	N/A
tRRD	N/A
tRFC	tRFC min. (IDD)
CL	N/A
AL	N/A
/CS	H between valid commands
Address and command inputs	SWITCHING
Data inputs	SWITCHING
Output buffer DQ, DQS / MR1 bit A12	off / 1
ODT / MR1 bits [A9, A6, A2] / MR2 bits [A1, A0]	disabled / [0,0,0] / [0,0]
Burst length	N/A
Active banks	Refresh command every tRFC = tRFC (min.)
Idle banks	none
Precharge Power-down Mode / MR0 bit A12	N/A

IDD Measurement Conditions for IDD6 and IDD6ET

Symbol	IDD6	IDD6ET
Name	Self-refresh current normal temperature range TC = 0 to +85°C	Self-refresh current extended temperature range TC = 0 to +95°C
Measurement Condition		
Temperature	TC = +85°C	TC = +95°C
Auto Self-refresh (ASR) / MR2 bit A6	Disabled / 0	Disabled / 0
Self-Refresh Temperature Range (SRT) / MR2 bit A7	Disabled / 0	Enabled / 1
CKE	L	L
External Clock	OFF; CK and /CK at L	OFF; CK and /CK at L
tCK	N/A	N/A
tRC	N/A	N/A
tRAS	N/A	N/A
tRCD	N/A	N/A
tRRD	N/A	N/A
CL	N/A	N/A
AL	N/A	N/A
/CS	FLOATING	FLOATING
Command inputs /RAS, /CAS, /WE)	FLOATING	FLOATING
Row, column addresses	FLOATING	FLOATING
Bank addresses	FLOATING	FLOATING
Data I/O	FLOATING	FLOATING
Output Buffer DQ, DQS / MR1 bit A12	off / 1	off / 1
ODT / MR1 bits [A9, A6, A2] / MR2 bits [A1, A0]	disabled / [0,0,0] / [0,0]	disabled / [0,0,0] / [0,0]
Burst length	8 fixed / MR0 bits [A1, A0] = {0,0}	8 fixed / MR0 bits [A1, A0] = {0,0}
Active banks	all during self-refresh actions	all during self-refresh actions
Idle banks	all between self-refresh actions	all between self-refresh actions
Precharge Power-down Mode / MR0 bit A12	N/A	N/A

IDD6 Current Definition

Parameter	Symbol	Parameter/Condition
Normal temperature range self-refresh current	IDD6	CKE ≤ 0.2V; external clock off, CK and /CK at 0V; Other control and address inputs are FLOATING; Data Bus inputs are FLOATING, PASR disabled. Applicable for MR2 settings A6 = 0 and A7 = 0.
Extended temperature range self-refresh current	IDD6ET	CKE ≤ 0.2V; external clock off, CK and /CK at 0V; Other control and address inputs are FLOATING; Data Bus inputs are FLOATING, PASR disabled. Applicable for MR2 settings A6 = 0 and A7 = 1
Auto self-refresh current	IDD6TC	CKE ≤ 0.2V; external clock off, CK and /CK at 0V; Other control and address inputs are FLOATING; Data Bus inputs are FLOATING, PASR disabled. Applicable when ASR is enabled by MR2 settings A6 = 1 and A7 = 0.

Electrical Specifications

DC Characteristics 1 (TC = 0°C to +85°C, VDD, VDDQ = 1.5V ± 0.075V)

Parameter	Symbol	Data rate (Mbps)	× 4 max.	× 8 max.	× 16 max.	Unit	Notes
Operating current (ACT-PRE)	IDD0	1600	—	TBD	—	mA	
		1333	120	120	140		
		1066	110	110	130		
		800	100	100	115		
Operating current (ACT-READ-PRE)	IDD1	1600	—	TBD	—	mA	
		1333	140	140	170		
		1066	125	125	155		
		800	115	115	140		
Precharge power-down standby current	IDD2PF	1600	—	TBD	—	mA	Fast PD Exit
		1333	40	40	40		
		1066	35	35	35		
		800	30	30	30		
	IDD2PS	1600	—	TBD	—	mA	Slow PD Exit
		1333	14	14	14		
		1066	13	13	13		
		800	12	12	12		
Precharge quiet standby current	IDD2Q	1600	—	TBD	—	mA	
		1333	70	70	70		
		1066	60	60	60		
		800	50	50	50		
Precharge standby current	IDD2N	1600	—	TBD	—	mA	
		1333	75	75	75		
		1066	65	65	65		
		800	55	55	55		
Active power-down current (Always fast exit)	IDD3P	1600	—	TBD	—	mA	
		1333	45	45	45		
		1066	40	40	40		
		800	35	35	35		
Active standby current	IDD3N	1600	—	TBD	—	mA	
		1333	85	85	95		
		1066	75	75	85		
		800	65	65	75		
Operating current (Burst read operating)	IDD4R	1600	—	TBD	—	mA	
		1333	200	220	290		
		1066	165	180	230		
		800	130	140	180		
Operating current (Burst write operating)	IDD4W	1600	—	TBD	—	mA	
		1333	210	240	330		
		1066	175	200	270		
		800	140	160	220		
Burst refresh current	IDD5B	1600	—	TBD	—	mA	
		1333	335	335	335		
		1066	315	315	315		
		800	295	295	295		
All bank interleave read current	IDD7R	1600	—	TBD	—	mA	
		1333	330	345	380		
		1066	270	285	330		
		800	250	260	315		

Self-Refresh Current (TC = 0°C to +85°C, VDD, VDDQ = 1.5V ± 0.075V)

Parameter	Symbol	Grade	× 4 max.	× 8 max.	× 16 max.	Unit	Notes
Self-refresh current normal temperature range	IDD6S		10	10	10	mA	
Self-refresh current extended temperature range	IDD6ET		18	18	18	mA	
Auto self-refresh current	IDD6TC		18	18	18	mA	

DC Characteristics 2 (TC = 0°C to +85°C, VDD, VDDQ = 1.5V ± 0.075V)

Parameter	Symbol	Value	Unit	Notes
Input leakage current	$\|I_{LI}\|$	2	μA	VDD ≥ VIN ≥ VSS
Output leakage current	$\|I_{LO}\|$	5	μA	VDDQ ≥ VOUT ≥ VSS

Pin Capacitance (TC = 25°C, VDD, VDDQ = 1.5V ± 0.075V)

Parameter	Symbol	Pins	min.	max.	Unit	Notes
Input pin capacitance, CK and /CK						
DDR3-1600, 1333	CCK	CK, /CK	0.8	1.4	pF	1, 3
DDR3-1066, 800			0.8	1.6	pF	1, 3
Delta input pin capacitance, CK and /CK						
DDR3-1600, 1333	CDCK		0	0.15	pF	1, 2
DDR3-1066, 800			0	0.15	pF	1, 2
Input pin capacitance, control pins						
DDR3-1600, 1333	CIN_CTRL	/CS, CKE, ODT	0.75	1.3	pF	1
DDR3-1066, 800			0.75	1.5	pF	1
Input pin capacitance, address and command pins						
DDR3-1600, 1333	CIN_ADD_CMD	/RAS, /CAS, /WE, Address	0.75	1.3	pF	1
DDR3-1066, 800			0.75	1.5	pF	1
Delta input pin capacitance, control pins						
DDR3-1600, 1333	CDIN_CTRL	/CS, CKE, ODT	−0.4	0.2	pF	1, 4
DDR3-1066, 800			−0.5	0.3	pF	1, 4
Delta input pin capacitance, address and command pins						
DDR3-1600, 1333	CDIN_ADD_CMD	/RAS, /CAS, /WE, Address	−0.4	0.4	pF	1, 5
DDR3-1066, 800			−0.5	0.5	pF	1, 5
Input/output pin capacitance						
DDR3-1600	CIO	DQ, DQS, /DQS, TDQS, /TDQS DM	1.5	2.3	pF	1, 6
DDR3-1333			1.5	2.5	pF	1, 6
DDR3-1066, 800			1.5	3.0	pF	1, 6
Delta input/output pin capacitance						
DDR3-1600, 1333	CDIO		−0.5	0.3	pF	1, 7, 8
DDR3-1066, 800			−0.5	0.3	pF	1, 7, 8
Delta input/output pin capacitance						
DDR3-1600, 1333	CDDQS	DQS, /DQS	0	0.15	pF	1, 10
DDR3-1066, 800			0	0.2	pF	1, 10
Input/output pin capacitance of ZQ	CZQ	ZQ	—	3	pF	1, 9

Notes: 1. VDD, VDDQ, VSS, VSSQ applied and all other pins (except the pin under test) floating.
VDD = VDDQ =1.5V, VBIAS=VDD/2

2. Absolute value of CCK(CK-pin) − CCK(/CK-pin)
3. CCK (min.) will be equal to CIN (min.)
4. CDIN_CTRL = CIN_CTRL − 0.5 × (CCK(CK-pin) + CCK(/CK-pin))
5. CDIN_ADD_CMD = CIN_ADD_CMD − 0.5 × (CCK(CK-pin) + CCK(/CK-pin))
6. Although the DM, TDQS and /TDQS pins have different functions, the loading matches DQ and DQS.
7. DQ should be in high impedance state.
8. CDIO = CIO (DQ, DM) −0.5 × (CIO(DQS-pin) + CIO(/DQS-pin)).
9. Maximum external load capacitance on ZQ pin: 5pF.
10 Absolute value of CIO(DQS) − CIO(/DQS)

Standard Speed Bins

[DDR3-1600 Speed Bins]

Speed Bin		DDR3-1600		DDR3-1600			
CL-tRCD-tRP		10-10-10		11-11-11			
Symbol	/CAS write latency	min.	max.	min.	max.	Unit	Notes
tAA		12.5	20	13.75	20	ns	
tRCD		12.5	—	13.75	—	ns	
tRP		12.5	—	13.75	—	ns	
tRC		47.5	—	48.75	—	ns	
tRAS		35	9 × tREFI	35	9 × tREFI	ns	9
tCK (avg)@CL=5	CWL = 5	2.5	3.3	Reserved	Reserved	ns	1, 2, 3, 4, 8
	CWL = 6, 7, 8	Reserved	Reserved	Reserved	Reserved	ns	4
tCK (avg)@CL=6	CWL = 5	2.5	3.3	2.5	3.3	ns	1, 2, 3, 8
	CWL = 6	Reserved	Reserved	Reserved	Reserved	ns	1, 2, 3, 4, 8
	CWL = 7, 8	Reserved	Reserved	Reserved	Reserved	ns	4
tCK (avg)@CL=7	CWL = 5	Reserved	Reserved	Reserved	Reserved	ns	4
	CWL = 6	1.875	< 2.5	Reserved	Reserved	ns	1, 2, 3, 4, 8
	CWL = 7	Reserved	Reserved	Reserved	Reserved	ns	1, 2, 3, 4
	CWL = 8	Reserved	Reserved	Reserved	Reserved	ns	1, 2, 3, 4
tCK (avg)@CL=8	CWL = 5	Reserved	Reserved	Reserved	Reserved	ns	4
	CWL = 6	1.875	< 2.5	1.875	< 2.5	ns	1, 2, 3, 8
	CWL = 7	Reserved	Reserved	Reserved	Reserved	ns	1, 2, 3, 4
	CWL = 8	Reserved	Reserved	Reserved	Reserved	ns	1, 2, 3, 4
tCK (avg)@CL=9	CWL = 5, 6	Reserved	Reserved	Reserved	Reserved	ns	4
	CWL= 7	1.5	< 1.875	Reserved	Reserved	ns	1, 2, 3, 4
	CWL= 8	Reserved	Reserved	Reserved	Reserved	ns	1, 2, 3, 4
tCK (avg)@CL=10	CWL = 5, 6	Reserved	Reserved	Reserved	Reserved	ns	4
	CWL= 7	1.5	< 1.875	1.5	< 1.875	ns	1, 2, 3
	CWL= 8	1.25	< 1.5	Reserved	Reserved	ns	5
tCK (avg)@CL=11	CWL = 5, 6, 7	Reserved	Reserved	Reserved	Reserved	ns	4
	CWL= 8	1.25	< 1.5	1.25	< 1.5	ns	1, 2, 3
	CWL= 8	Optional	Optional	1.25	< 1.5		5
Supported CL settings		5, 6, 7, 8, 9, 10		6, 8, 10, 11		nCK	
Supported CWL settings		5, 6, 7, 8		5, 6, 7, 8		nCK	

[DDR3-1333 Speed Bins]

Speed Bin		DDR3-1333G		DDR3-1333H			
CL-tRCD-tRP		8-8-8		9-9-9			
Symbol	/CAS write latency	min.	max.	min.	max.	Unit	Notes
tAA		12	20	13.5	20	ns	
tRCD		12	—	13.5	—	ns	
tRP		12	—	13.5	—	ns	
tRC		48.0	—	49.5	—	ns	
tRAS		36	9 × tREFI	36	9 × tREFI	ns	9
tCK (avg)@CL=5	CWL = 5	2.5	3.3	Reserved	Reserved	ns	1, 2, 3, 4, 7
	CWL = 6, 7	Reserved	Reserved	Reserved	Reserved	ns	4
tCK (avg)@CL=6	CWL = 5	2.5	3.3	2.5	3.3	ns	1, 2, 3, 7
	CWL = 6	Reserved	Reserved	Reserved	Reserved	ns	1, 2, 3, 4, 7
	CWL = 7	Reserved	Reserved	Reserved	Reserved	ns	4
tCK (avg)@CL=7	CWL = 5	Reserved	Reserved	Reserved	Reserved	ns	4
	CWL = 6	1.875	< 2.5	Reserved	Reserved	ns	1, 2, 3, 4, 7
	CWL = 7	Reserved	Reserved	Reserved	Reserved	ns	1, 2, 3, 4
tCK (avg)@CL=8	CWL = 5	Reserved	Reserved	Reserved	Reserved	ns	4
	CWL = 6	1.875	< 2.5	1.875	< 2.5	ns	1, 2, 3, 7
	CWL = 7	1.5	< 1.875	Reserved	Reserved	ns	1, 2, 3, 4
tCK (avg)@CL=9	CWL = 5, 6	Reserved	Reserved	Reserved	Reserved	ns	4
	CWL= 7	1.5	< 1.875	< 1.5	< 1.875	ns	1, 2, 3, 4
tCK (avg)@CL=10	CWL = 5, 6	Reserved	Reserved	Reserved	Reserved	ns	4
	CWL= 7	1.5	< 1.875	1.5	< 1.875	ns	1, 2, 3
	CWL= 7	Optional	Optional	Optional	Optional	ns	5
Supported CL settings		5, 6, 7, 8, 9, 10		6, 8, 9, 10		nCK	
Supported CWL settings		5, 6, 7		5, 6, 7		nCK	

[DDR3-1066 Speed Bins]

Speed Bin		DDR3-1066E		DDR3-1066F		DDR3-1066G			
CL-tRCD-tRP		6-6-6		7-7-7		8-8-8			
Symbol	/CAS write latency	min.	max.	min.	max.	min.	max.	Unit	Notes
tAA		11.25	20	13.125	20	15	20	ns	
tRCD		11.25	—	13.125	—	15	—	ns	
tRP		11.25	—	13.125	—	15	—	ns	
tRC		48.75	—	50.625	—	52.50	—	ns	
tRAS		37.5	9 × tREFI	37.5	9 × tREFI	37.5	9 × tREFI	ns	9
tCK (avg)@CL=5	CWL = 5	2.5	3.3	Reserved	Reserved	Reserved	Reserved	ns	1, 2, 3, 4, 6
	CWL = 6	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ns	4
tCK (avg)@CL=6	CWL = 5	2.5	3.3	2.5	3.3	2.5	3.3	ns	1, 2, 3, 6
	CWL = 6	1.875	< 2.5	Reserved	Reserved	Reserved	Reserved	ns	1, 2, 3, 4
tCK (avg)@CL=7	CWL = 5	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ns	4
	CWL = 6	1.875	< 2.5	1.875	< 2.5	Reserved	Reserved	ns	1, 2, 3, 4
tCK (avg)@CL=8	CWL = 5	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ns	4
	CWL = 6	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	ns	1, 2, 3
Supported CL settings		5, 6, 7, 8		6, 7, 8		6, 8		nCK	
Supported CWL settings		5, 6		5, 6		5, 6		nCK	

[DDR3-800 Speed Bins]

Speed Bin		DDR3-800F		DDR3-800E			
CL-tRCD-tRP		5-5-5		6-6-6			
Symbol	/CAS write latency	min.	max.	min.	max.	Unit	Notes
tAA		12.5	20	15	20	ns	
tRCD		12.5	—	15	—	ns	
tRP		12.5	—	15	—	ns	
tRC		50	—	52.5	—	ns	
tRAS		37.5	9 × tREFI	37.5	9 × tREFI	ns	9
tCK (avg)@CL=5	CWL = 5	2.5	3.3	Reserved	Reserved	ns	1, 2, 3, 4
tCK (avg)@CL=6	CWL = 5	2.5	3.3	2.5	3.3	ns	1, 2, 3
Supported CL settings		5, 6		6		nCK	
Supported CWL settings		5		5		nCK	

Notes: 1 The CL setting and CWL setting result in tCK (avg) (min.) and tCK (avg) (max.) requirements. When making a selection of tCK (avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.

2. tCK (avg) (min.) limits: Since /CAS latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK (avg) value (2.5, 1.875, 1.5, or 1.25ns) when calculating CL (nCK) = tAA (ns) / tCK (avg)(ns), rounding up to the next 'Supported CL'.
3. tCK (avg) (max.) limits: Calculate tCK (avg) + tAA (max.)/CL selected and round the resulting tCK (avg) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875ns or 1.25ns). This result is tCK (avg) (max.) corresponding to CL selected.

4. ‘Reserved’ settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature.
6. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table DDR3-1066 Speed Bins which are not subject to production tests but verified by design/characterization.
7. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table DDR3-1333 Speed Bins which is not subject to production tests but verified by design/characterization.
8 Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table DDR3-1600 Speed Bins which is not subject to production tests but verified by design/characterization.
9. tREFI depends on operating case temperature (TC).

AC Characteristics (TC = 0°C to +85°C, VDD, VDDQ = 1.5V ± 0.075V, VSS, VSSQ = 0V)

- New units tCK(avg) and nCK, are introduced in DDR3.
  tCK(avg): actual tCK(avg) of the input clock under operation.
  nCK: one clock cycle of the input clock, counting the actual clock edges.

AC Characteristics [DDR3-1600, 1333]

		-GL, -GN		-DG, -DJ			
Data rate (Mbps)		1600		1333			
Parameter	Symbol	min.	max.	min.	max.	Unit	Notes
Average clock cycle time	tCK (avg)	1250	3333	1500	3333	ps	
Minimum clock cycle time (DLL-off mode)	tCK (DLL-off)	8	—	8	—	ns	6
Average CK high-level width	tCH (avg)	0.47	0.53	0.47	0.53	tCK (avg)	
Average CK low-level width	tCL (avg)	0.47	0.53	0.47	0.53	tCK (avg)	
Active to read or write command delay	tRCD	12.5 (GL) 13.75 (GN)	—	12 (DG) 13.5 (DJ)	—	ns	26
Precharge command period	tRP	12.5 (GL) 13.75 (GN)	—	12 (DG) 13.5 (DJ)	—	ns	26
Active to active/auto-refresh command time	tRC	47.5 (GL) 48.75 (GN)	—	48 (DG) 49.5 (DJ)	—	ns	26
Active to precharge command	tRAS	35	9 × tREFI	36	9 × tREFI	ns	26
Active bank A to active bank B command period	tRRD	—	—	6	—	ns	26, 27
(x4)	tRRD	—	—	4	—	nCK	26, 27
Active bank A to active bank B command period	tRRD	6	—	6	—	ns	26, 27
(x8)	tRRD	4	—	4	—	nCK	26, 27
Active bank A to active bank B command period	tRRD	—	—	7.5	—	ns	26, 27
(x16)	tRRD	—	—	4	—	nCK	26, 27
Four active window (x4)	tFAW	—	—	30	—	ns	26
(x8)	tFAW	30	—	30	—	ns	26
(x16)	tFAW	—	—	45	—	ns	26
Address and control input hold time (VIH/VIL (DC) levels)	tIH (base)	120	—	140	—	ps	16, 23
Address and control input setup time (VIH/VIL (AC) levels)	tIS (base)	45	—	65	—	ps	16, 23
Address and control input setup time (VIH/VIL (AC150) levels)	tIS (base) AC150	45 + 125	—	65 + 125	—	ps	16, 23, 31
DQ and DM input hold time (VIH/VIL (DC) levels)	tDH (base)	45	—	65	—	ps	17, 25
DQ and DM input setup time (VIH/VIL (AC) levels)	tDS (base)	10	—	30	—	ps	17, 25
Control and Address input pulse width for each input	tIPW	560	—	620	—	ps	32
DQ and DM input pulse width for each input	tDIPW	360	—	400	—	ps	32
DQ high-impedance time	tHZ (DQ)	—	225	—	250	ps	12, 13, 14, 37
DQ low-impedance time	tLZ (DQ)	–450	225	–500	250	ps	12, 13, 14, 37
DQS, /DQS high-impedance time (RL + BL/2 reference)	tHZ (DQS)	—	225	—	250	ps	12, 13, 14, 37
DQS, /DQS low-impedance time (RL – 1 reference)	tLZ (DQS)	–450	225	–500	250	ps	12, 13, 14, 37

		-GL, -GN		-DG, -DJ			
Data rate (Mbps)		1600		1333			
Parameter	Symbol	min.	max.	min.	max.	Unit	Notes
DQS, /DQS to DQ skew, per group, per access	tDQSQ	—	100	—	125	ps	12, 13
/CAS to /CAS command delay	tCCD	4	—	4	—	nCK	
DQ output hold time from DQS, /DQS	tQH	0.38	—	0.38	—	tCK (avg)	12, 13, 38
DQS, /DQS rising edge output access time from rising CK, /CK	tDQSCK	−225	225	−255	255	ps	12, 13, 37
DQS latching rising transitions to associated clock edges	tDQSS	−0.27	0.27	−0.25	0.25	tCK (avg)	24
DQS falling edge hold time from rising CK	tDSH	0.18	—	0.2	—	tCK (avg)	24, 36
DQS falling edge setup time to rising CK	tDSS	0.18	—	0.2	—	tCK (avg)	24, 36
DQS input high pulse width	tDQSH	0.45	0.55	0.45	0.55	tCK (avg)	34, 35
DQS input low pulse width	tDQSL	0.45	0.55	0.45	0.55	tCK (avg)	33, 35
DQS output high time	tQSH	0.40	—	0.40	—	tCK (avg)	12, 13, 38
DQS output low time	tQSL	0.40	—	0.40	—	tCK (avg)	12, 13, 38
Mode register set command cycle time	tMRD	4	—	4	—	nCK	
Mode register set command update delay	tMOD	15	—	15	—	ns	27
	tMOD	12	—	12	—	nCK	27
Read preamble	tRPRE	0.9	—	0.9	—	tCK (avg)	1, 19, 38
Read postamble	tRPST	0.3	—	0.3	—	tCK (avg)	11, 12, 13, 38
Write preamble	tWPRE	0.9	—	0.9	—	tCK (avg)	1
Write postamble	tWPST	0.3	—	0.3	—	tCK (avg)	1
Write recovery time	tWR	15	—	15	—	ns	26
Auto precharge write recovery + precharge time	tDAL	WR + RU (tRP/tCK (avg))	—	WR + RU (tRP/tCK (avg))	—	nCK	
Multi-Purpose register recovery time	tMPRR	1	—	1	—	nCK	29
Read to write command delay (BC4MRS, BC4OTF)	tRTW	RL + tCCD/2 + 2nCK − WL	—	RL + tCCD/2 + 2nCK − WL	—		
(BL8MRS, BL8OTF)	tRTW	RL + tCCD + 2nCK − WL	—	RL + tCCD + 2nCK − WL	—		
Internal write to read command delay	tWTR	7.5	—	7.5	—	ns	18, 26, 27
	tWTR	4	—	4	—	nCK	18, 26, 27
Internal read to precharge command delay	tRTP	7.5	—	7.5	—	ns	26, 27
	tRTP	4	—	4	—	nCK	26, 27
Active to READ with auto precharge command delay	tRAP	tRCD min	—	tRCD min	—		28
Minimum CKE low width for self-refresh entry to exit timing	tCKESR	tCKE (min.) +1nCK	—	tCKE (min.) +1nCK	—		
Valid clock requirement after self-refresh entry or power-down entry	tCKSRE	10	—	10	—	ns	27
	tCKSRE	5	—	5	—	nCK	27

		-GL, -GN		-DG, -DJ			
Data rate (Mbps)		1600		1333			
Parameter	Symbol	min.	max.	min.	max.	Unit	Notes
Valid clock requirement before self-refresh exit or power-down exit	tCKSRX	10	—	10	—	ns	27
	tCKSRX	5	—	5	—	nCK	27
Exit self-refresh to commands not requiring a locked DLL	tXS	tRFC (min.) + 10	—	tRFC (min.) + 10	—	ns	27
	tXS	5	—	5	—	nCK	27
Exit self-refresh to commands requiring a locked DLL	tXSDLL	tDLLK (min.)	—	tDLLK (min.)	—	nCK	
Auto-refresh to active/auto-refresh command time	tRFC	110	—	110	—	ns	
Average periodic refresh interval (0°C ≤ TC ≤ +85°C)	tREFI	—	7.8	—	7.8	µs	
(+85°C < TC ≤ +95°C)	tREFI	—	3.9	—	3.9	µs	
CKE minimum pulse width (high and low pulse width)	tCKE	5	—	5.625	—	ns	27
	tCKE	3	—	3	—	nCK	27
Exit reset from CKE high to a valid command	tXPR	tRFC (min.)+10	—	tRFC (min.)+10	—	ns	27
	tXPR	5	—	5	—	nCK	27
DLL locking time	tDLLK	512	—	512	—	nCK	
Power-down entry to exit time	tPD	tCKE (min.)	9 × tREFI	tCKE (min.)	9 × tREFI		15
Exit precharge power-down with DLL frozen to commands requiring a locked DLL	tXPDLL	24	—	24	—	ns	2
	tXPDLL	10	—	10	—	nCK	2
Exit power-down with DLL on to any valid command; Exit precharge power-down with DLL frozen to commands not requiring a locked DLL	tXP	6	—	6	—	ns	27
	tXP	3	—	3	—	nCK	27
Command pass disable/enable delay	tCPDED	1	—	1	—	nCK	
Timing of last ACT command to power-down entry	tACTPDEN	1	—	1	—	nCK	20
Timing of last PRE command to power-down entry	tPRPDEN	1	—	1	—	nCK	20
Timing of last READ/READA command to power-down entry	tRDPDEN	RL + 4 + 1	—	RL + 4 + 1	—	nCK	
Timing of last WRIT command to power-down entry (BL8MRS, BL8OTF, BC4OTF)	tWRPDEN	WL + 4 + tWR/tCK (avg)	—	WL + 4 + tWR/tCK (avg)	—	nCK	9
(BC4MRS)	tWRPDEN	WL + 2 + tWR/tCK (avg)	—	WL + 2 + tWR/tCK (avg)	—	nCK	9
Timing of last WRITA command to power-down entry (BL8MRS, BL8OTF, BC4OTF)	tWRAPDEN	WL + 4 + WR + 1	—	WL + 4 + WR + 1	—	nCK	10
(BC4MRS)	tWRAPDEN	WL + 2 + WR + 1	—	WL + 2 + WR + 1	—	nCK	10
Timing of last REF command to power-down entry	tREFPDEN	1	—	1	—	nCK	20, 21
Timing of last MRS command to power-down entry	tMRSPDEN	tMOD (min.)	—	tMOD (min.)	—		

ODT AC Electrical Characteristics [DDR3-1600, 1333]

		-GL, -GN		-DG, -DJ			
Data rate (Mbps)		1600		1333			
Parameter	Symbol	min.	max.	min.	max.	Unit	Notes
RTT turn-on	tAON	–225	225	–250	250	ps	7, 12, 37
Asynchronous RTT turn-on delay (power-down with DLL frozen)	tAONPD	2	8.5	2	8.5	ns	
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	tCK (avg)	8, 12, 37
Asynchronous RTT turn-off delay (power-down with DLL frozen)	tAOFPD	2	8.5	2	8.5	ns	
ODT to power-down entry/exit latency	tANPD	WL – 1.0	—	WL – 1.0	—	nCK	
ODT turn-on Latency	ODTLon	WL – 2	WL – 2	WL – 2.0	WL – 2.0	nCK	
ODT turn-off Latency	ODTLoff	WL – 2	WL – 2	WL – 2.0	WL – 2.0	nCK	
ODT Latency for changing from RTT_Nom to RTT_WR	ODTLcnw	WL – 2	WL – 2	WL – 2.0	WL – 2.0	nCK	
ODT Latency for change from RTT_WR to RTT_Nom (BC4)	ODTLcwn4	—	4 + ODTLoff	—	4 + ODTLoff	nCK	
ODT Latency for change from RTT_WR to RTT_Nom (BL8)	ODTLcwn8	—	6 + ODTLoff	—	6 + ODTLoff	nCK	
ODT high time without WRIT command or with WRIT command and BC4	ODTH4	4	—	4	—	nCK	
ODT high time with WRIT command and BL8	ODTH8	6	—	6	—	nCK	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	tCK (avg)	12, 37
Power-up and reset calibration time	tZQinit	512	—	512	—	nCK	
Normal operation full calibration time	tZQoper	256	—	256	—	nCK	
Normal operation short calibration time	tZQCS	64	—	64	—	nCK	30

Write Leveling Characteristics [DDR3-1600, 1333]

		-GL, -GN		-DG, -DJ			
		1600		1333			
Parameter	Symbol	min.	max.	min.	max.	Unit	Notes
First DQS pulse rising edge after write leveling mode is programmed	tWLMRD	40	—	40	—	nCK	3
DQS, /DQS delay after write leveling mode is programmed	tWLDQSEN	25	—	25	—	nCK	3
Write leveling setup time from rising CK, /CK crossing to rising DQS, /DQS crossing	tWLS	165	—	195	—	ps	
Write leveling hold time from rising DQS, /DQS crossing to rising CK, /CK crossing	tWLH	165	—	195	—	ps	
Write leveling output delay	tWLO	0	7.5	0	9	ns	
Write leveling output error	tWLOE	0	2	0	2	ns	

AC Characteristics [DDR3-1066, 800]

		-AC, -AE, -AG		-8A, -8C			
Data rate (Mbps)		1066		800			
Parameter	Symbol	min.	max.	min.	max.	Unit	Notes
Clock cycle time Average CL = X	tCK(avg)	1875	3333	2500	3333	ps	
Minimum clock cycle time (DLL-off mode)	tCK(DLL-off)	8	—	8	—	ns	6
Average duty cycle high-level	tCH (avg)	0.47	0.53	0.47	0.53	tCK (avg)	
Average duty cycle low-level	tCL (avg)	0.47	0.53	0.47	0.53	tCK (avg)	
Active to read or write command delay	tRCD	11.25 (AC) 13.1 (AE) 15 (AG)	—	12.5 (8A) 15 (8C)	—	ns	26
Precharge command period	tRP	11.25 (AC) 13.1 (AE) 15 (AG)	—	12.5 (8A) 15 (8C)	—	ns	26
Active to active/auto-refresh command time	tRC	48.75 (AC) 50.6 (AE) 52.5 (AG)	—	50 (8A) 52.5 (8C)	—	ns	26
Active to precharge command	tRAS	37.5	9 × tREFI	37.5	9 × tREFI	ns	26
Active bank A to active bank B command period	tRRD	7.5	—	10	—	ns	26, 27
(x4/x8)	tRRD	4	—	4	—	nCK	26, 27
Active bank A to active bank B command period	tRRD	10	—	10	—	ns	26, 27
(x16)	tRRD	4	—	4	—	nCK	26, 27
Four active window (x4/x8)	tFAW	37.5	—	40	—	ns	26
(x16)	tFAW	50	—	50	—	ns	26
Address and control input hold time (VIH/VIL (DC) levels)	tIH (base)	200	—	275	—	ps	16, 23
Address and control input setup time (VIH/VIL (AC) levels)	tIS (base)	125	—	200	—	ps	16, 23
Address and control input setup time (VIH/VIL (AC150) levels)	tIS (base) AC150	125 + 150	—	200 + 150	—	ps	16, 23, 31
DQ and DM input hold time (VIH/VIL (DC) levels)	tDH (base)	100	—	150	—	ps	17, 25
DQ and DM input setup time (VIH/VIL (AC) levels)	tDS (base)	25	—	75	—	ps	17, 25
Control and Address input pulse width for each input	tIPW	780	—	900	—	ps	32
DQ and DM input pulse width for each input	tDIPW	490	—	600	—	ps	32
DQ high-impedance time	tHZ (DQ)	—	300	—	400	ps	12, 13, 14, 37
DQ low-impedance time	tLZ (DQ)	–600	300	–800	400	ps	12, 13, 14, 37
DQS, /DQS high-impedance time (RL + BL/2 reference)	tHZ (DQS)	—	300	—	400	ps	12, 13, 14, 37
DQS, /DQS low-impedance time (RL – 1 reference)	tLZ (DQS)	–600	300	–800	400	ps	12, 13, 14, 37
DQS, /DQS -DQ skew, per group, per access	tDQSQ	—	150	—	200	ps	12, 13
/CAS to /CAS command delay	tCCD	4	—	4	—	nCK	
DQ output hold time from DQS, /DQS	tQH	0.38	—	0.38	—	tCK (avg)	12, 13, 38

		-AC, -AE, -AG		-8A, -8C			
Data rate (Mbps)		1066		800			
Parameter	Symbol	min.	max.	min.	max.	Unit	Notes
DQS, /DQS rising edge output access time from rising CK, /CK	tDQSCK	−300	+300	−400	+400	ps	12, 13, 37
DQS latching rising transitions to associated clock edges	tDQSS	−0.25	0.25	−0.25	0.25	tCK (avg)	24
DQS falling edge hold time from rising CK	tDSH	0.2	—	0.2	—	tCK (avg)	24, 36
DQS falling edge setup time to rising CK	tDSS	0.2	—	0.2	—	tCK (avg)	24, 36
DQS input high pulse width	tDQSH	0.45	0.55	0.45	0.55	tCK (avg)	34, 35
DQS input low pulse width	tDQSL	0.45	0.55	0.45	0.55	tCK (avg)	33, 35
DQS output high time	tQSH	0.38	—	0.38	—	tCK (avg)	12, 13, 38
DQS output low time	tQSL	0.38	—	0.38	—	tCK (avg)	12, 13, 38
Mode register set command cycle time	tMRD	4	—	4	—	nCK	
Mode register set command update delay	tMOD	15	—	15	—	ns	27
	tMOD	12	—	12	—	nCK	27
Read preamble	tRPRE	0.9	—	0.9	—	tCK (avg)	1, 19, 38
Read postamble	tRPST	0.3	—	0.3	—	tCK (avg)	11, 12, 13, 38
Write preamble	tWPRE	0.9	—	0.9	—	tCK (avg)	1
Write postamble	tWPST	0.3	—	0.3	—	tCK (avg)	1
Write recovery time	tWR	15	—	15	—	ns	26
Auto precharge write recovery + precharge time	tDAL	WR + RU (tRP/tCK (avg))	—	WR + RU (tRP/tCK (avg))	—	nCK	
Multi-Purpose register recovery time	tMPRR	1	—	1	—	nCK	29
Read to write command delay (BC4MRS, BC4OTF)	tRTW	RL + tCCD/2 + 2nCK − WL	—	RL + tCCD/2 + 2nCK − WL	—		
(BL8MRS, BL8OTF)	tRTW	RL + tCCD + 2nCK − WL	—	RL + tCCD + 2nCK − WL	—		
Internal write to read command delay	tWTR	7.5	—	7.5	—	ns	18, 26, 27
	tWTR	4	—	4	—	nCK	18, 26, 27
Internal read to precharge command delay	tRTP	7.5	—	7.5	—	ns	26, 27
	tRTP	4	—	4	—	nCK	26, 27
Active to READ with auto precharge command delay	tRAP	tRCD min	—	tRCD min	—		28
Minimum CKE low width for self-refresh entry to exit timing	tCKESR	tCKE (min.) +1nCK	—	tCKE (min.) +1nCK	—		
Valid clock requirement after self-refresh entry or power-down entry	tCKSRE	10	—	10	—	ns	27
	tCKSRE	5	—	5	—	nCK	27
Valid clock requirement before self-refresh exit or power-down exit	tCKSRX	10	—	10	—	ns	27
	tCKSRX	5	—	5	—	nCK	27
Exit self-refresh to commands not requiring a locked DLL	tXS	tRFC (min.) + 10	—	tRFC (min.) + 10	—	ns	27
	tXS	5	—	5	—	nCK	27

		-AC, -AE, -AG		-8A, -8C			
Data rate (Mbps)		1066		800			
Parameter	Symbol	min.	max.	min.	max.	Unit	Notes
Exit self-refresh to commands requiring a locked DLL	tXSDLL	tDLLK (min.)	—	tDLLK (min.)	—	nCK	
Auto-refresh to active/auto-refresh command time	tRFC	110	—	110	—	ns	
Average periodic refresh interval (0°C ≤ TC ≤ +85°C)	tREFI	—	7.8	—	7.8	µs	
(+85°C < TC ≤ +95°C)	tREFI	—	3.9	—	3.9	µs	
CKE minimum pulse width (high and low pulse width)	tCKE	5.625	—	7.5	—	ns	27
	tCKE	3	—	3	—	nCK	27
Exit reset from CKE high to a valid command	tXPR	tRFC(min.)+10	—	tRFC(min.)+10	—	ns	27
	tXPR	5	—	5	—	nCK	27
DLL locking time	tDLLK	512	—	512	—	nCK	
Power-down entry to exit time	tPD	tCKE (min.)	9 × tREFI	tCKE (min.)	9 × tREFI		15
Exit precharge power-down with DLL frozen to commands requiring a locked DLL	tXPDLL	24	—	24	—	ns	2
	tXPDLL	10	—	10	—	nCK	2
Fast exit/active precharge power-down to any command	tXP	7.5	—	7.5	—	ns	27
	tXP	3	—	3	—	nCK	27
Command pass disable/enable delay	tCPDED	1	—	1	—	nCK	
Timing of last ACT command to power-down entry	tACTPDEN	1	—	1	—	nCK	20
Timing of last PRE command to power-down entry	tPRPDEN	1	—	1	—	nCK	20
Timing of last READ/READA command to power-down entry	tRDPDEN	RL + 4 + 1	—	RL + 4 + 1	—	nCK	
Timing of last WRIT command to power-down entry (BL8MRS, BL8OTF, BC4OTF)	tWRPDEN	WL + 4 + tWR/tCK (avg)	—	WL + 4 + tWR/tCK (avg)	—	nCK	9
(BC4MRS)	tWRPDEN	WL + 2 + tWR/tCK (avg)	—	WL + 2 + tWR/tCK (avg)	—	nCK	9
Timing of last WRITA command to power-down entry (BL8MRS, BL8OTF, BC4OTF)	tWRAPDEN	WL + 4 + WR + 1	—	WL + 4 + WR + 1	—	nCK	10
(BC4MRS)	tWRAPDEN	WL + 2 + WR + 1	—	WL + 2 + WR + 1	—	nCK	10
Timing of last REF command to power-down entry	tREFPDEN	1	—	1	—	nCK	20, 21
Timing of last MRS command to power-down entry	tMRSPDEN	tMOD (min.)	—	tMOD (min.)	—		

ODT AC Electrical Characteristics [DDR3-1066, 800]

		-AC, -AE, -AG		-8A, -8C			
Data rate (Mbps)		1066		800			
Parameter	Symbol	min.	max.	min.	max.	Unit	Notes
RTT turn-on	tAON	–300	300	–400	400	ps	7, 12, 37
Asynchronous RTT turn-on delay (power-down with DLL frozen)	tAONPD	2	8.5	2	8.5	ns	
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	tCK (avg)	8, 12, 37
ODT turn-off (power-down mode)	tAOFPD	2	8.5	2	8.5	ns	
ODT to power-down entry/exit latency	tANPD	WL – 1.0	—	WL – 1.0	—	nCK	
ODT turn-on Latency	ODTLon	WL – 2.0	WL – 2.0	WL – 2.0	WL – 2.0	nCK	
ODT turn-off Latency	ODTLoff	WL – 2.0	WL – 2.0	WL – 2.0	WL – 2.0	nCK	
ODT Latency for changing from RTT_Nom to RTT_WR	ODTLcnw	WL – 2.0	WL – 2.0	WL – 2.0	WL – 2.0	nCK	
ODT Latency for change from RTT_WR to RTT_Nom (BC4)	ODTLcwn4	—	4 + ODTLoff	—	4 + ODTLoff	nCK	
ODT Latency for change from RTT_WR to RTT_Nom (BL8)	ODTLcwn8	—	6 + ODTLoff	—	6 + ODTLoff	nCK	
ODT high time without WRIT command or with WRIT command and BC4	ODTH4	4	—	4	—	nCK	
ODT high time with WRIT command and BL8	ODTH8	6	—	6	—	nCK	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	tCK (avg)	12, 37
Power-up and reset calibration time	tZQinit	512	—	512	—	nCK	
Normal operation full calibration time	tZQoper	256	—	256	—	nCK	
Normal operation short calibration time	tZQCS	64	—	64	—	nCK	30

Write Leveling Characteristics [DDR3-1066, 800]

		-AC, -AE, -AG		-8A, -8C			
		1066		800			
Parameter	Symbol	min.	max.	min.	max.	Unit	Notes
First DQS pulse rising edge after write leveling mode is programmed	tWLMRD	40	—	40	—	nCK	3
DQS, /DQS delay after write leveling mode is programmed	tWLDQSEN	25	—	25	—	nCK	3
Write leveling setup time from rising CK, /CK crossing to rising DQS, /DQS crossing	tWLS	245	—	325	—	ps	
Write leveling hold time from rising DQS, /DQS crossing to rising CK, /CK crossing	tWLH	245	—	325	—	ps	
Write leveling output delay	tWLO	0	9	0	9	ns	
Write leveling output error	tWLOE	0	2	0	2	ns	

Notes for AC Electrical Characteristics

Notes: 1. Actual value dependent upon measurement level definitions that are TBD.

2. Commands requiring locked DLL are: READ (and READA) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register.
5. Value must be rounded-up to next integer value.
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
7. ODT turn on time (min.) is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time (max.) is when the ODT resistance is fully on. Both are measured from ODTLon.
8. ODT turn-off time (min.) is when the device starts to turn-off ODT resistance. ODT turn-off time (max.) is when the bus is in high impedance. Both are measured from ODTLoff.
9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.
10. WR in clock cycles as programmed in MR0.
11. The maximum read postamble is bound by tDQSCK(min.) plus tQSH(min.) on the left side and tHZ(DQS)(max.) on the right side.
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD.
13. Value is only valid for RON34.
14. Single ended signal parameter. Refer to the section of tLZ (DQS), tLZ (DQ), tHZ (DQS), tHZ (DQ) Notes for definition and measurement method.
15. tREFI depends on operating case temperature (TC).
16. tIS(base) and tIH(base) values are for 1V/ns command/address single-ended slew rate and 2V/ns CK, /CK differential slew rate. Note for DQ and DM signals, VREF(DC) = VREFDQ(DC). For input only pins except /RESET, VREF(DC) = VREFCA(DC). See Address / Command Setup, Hold and Derating section
17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, /DQS differential slew rate. Note for DQ and DM signals, VREF(DC) = VREFDQ(DC). For input only pins except /RESET, VREF(DC) = VREFCA(DC). See Data Setup, Hold and Slew Rate Derating section.
18. Start of internal write transaction is definited as follows:

    For BL8 (fixed by MRS and on- the-fly): Rising clock edge 4 clock cycles after WL.

    For BC4 (on-the-fly): Rising clock edge 4 clock cycles after WL.

    For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
19. The maximum read preamble is bound by tLZ(DQS)(min.) on the left side and tDQSCK(max.) on the right side.
20. CKE is allowed to be registered low while operations such as row activation, precharge, auto precharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
21. Although CKE is allowed to be registered low after a refresh command once tREFPDEN(min.) is satisfied, there are cases where additional time such as tXPDLL(min.) is also required. See Figure Power-Down Entry/Exit Clarifications - Case 2.
22. tJIT(duty) = $\pm$ { 0.07 $\times$ tCK(avg) – [(0.5 - (min (tCH(avg), tCL(avg))) $\times$ tCK(avg)] }.

    For example, if tCH/tCL was 0.48/0.52, tJIT(duty) would calculate out to $\pm$125ps for DDR3-800.

    The tCH(avg) and tCL(avg) values listed must not be exceeded.
23. These parameters are measured from a command/address signal (CKE, /CS, /RAS, /CAS, /WE, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK, /CK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

24 These parameters are measured from a data strobe signal ((L/U/T)DQS, /DQS) crossing to its respective clock signal (CK, /CK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

25. These parameters are measured from a data signal ((L/U)DM, (L/U)DQ0, (L/U)DQ1, etc.) transition edge to its respective data strobe signal ((L/U/T)DQS/DQS) crossing.

26. For these parameters, the DDR3 SDRAM device is characterized and verified to support tnPARAM [nCK] = RU{tPARAM [ns] / tCK(avg)}, which is in clock cycles, assuming all input clock jitter specifications are satisfied.

    For example, the device will support tnRP = RU{tRP / tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which tRP = 15ns, the device will support tnRP =RU{tRP / tCK(avg)} = 6, i.e. as long as the input clock jitter specifications are met, precharge command at Tm and active command at Tm+6 is valid even if (Tm+6 – Tm) is less than 15ns due to input clock jitter.

27. These parameters should be the larger of the two values, analog (ns) and number of clocks (nCK).

28 The tRAS lockout circuit internally delays the Precharge operation until the array restore operation has been completed so that the auto precharge command may be issued with any read or write command.

29 Defined between end of MPR read burst and MRS which reloads MPR or disables.

30 One ZQCS command can effectively correct a minimum of 0.5% (ZQCorrection) of RON and RTT impedance error within 64nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.

    One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(\text{Tsens} \times \text{Tdriftrate}) + (\text{Vsens} \times \text{Vdriftrate})}$$

    where TSens = max.(dRTTdT, dRONdTM) and VSens = max.(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities. For example, if TSens = 1.5%/°C, VSens = 0.15%/mV, Tdriftrate = 1°C/sec and Vdriftrate = 15mV/sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 = 128\text{ms}$$

31 The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100ps of derating to accommodate for the lower alternate threshold of 150mV and another 25ps to account for the earlier reference point [(175mV – 150mV)/1V/ns].

32 Pulse width of a input signal is defined as the width between the first crossing of VREF(DC) and the consecutive crossing of VREF(DC).

33 tDQSL describes the instantaneous differential input low pulse width on DQS – /DQS, as measured from one falling edge to the next consecutive rising edge.

34 tDQSH describes the instantaneous differential input high pulse width on DQS –/DQS, as measured from one rising edge to the next consecutive falling edge.

35 tDQSH,act + tDQSL,act = 1tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.

36 tDSH,act + tDSS,act = 1tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.

37 When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(mper),act of the input clock, where 2 ≤ m ≤ 12. (output deratings are relative to the SDRAM input clock.)

    For example, if the measured jitter into a DDR3-800 SDRAM has tERR(mper),act,min = –172ps and tERR(mper),act,max = +193ps, then tDQSCK,min(derated) = tDQSCK,min – tERR(mper),act,max = –400ps – 193ps = –593ps and tDQSCK,max(derated) =tDQSCK,max – tERR(mper),act,min = 400ps + 172ps = +572ps. Similarly, tLZ(DQ) forDDR3-800 derates to tLZ(DQ),min(derated) = –800ps – 193ps = –993ps and tLZ(DQ),max(derated) = 400ps + 172ps = +572ps. Note that tERR(mper),act,min is the minimum measured value of tERR(nper) where 2 ≤ n ≤ 12, and tERR(mper),act,max is the maximum measured value of tERR(nper) where 2 ≤ n ≤ 12.

38 When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per),act of the input clock. (output deratings are relative to the SDRAM input clock.)

    For example, if the measured jitter into a DDR3-800 SDRAM has tCK(avg),act = 2500ps, tJIT(per),act,min = – 72ps and tJIT(per),act,max = +93ps, then tRPRE,min(derated) = tRPRE,min + tJIT(per),act,min = 0.9 × tCK(avg),act + tJIT(per),act,min = 0.9 × 2500ps – 72ps = +2178ps. Similarly, tQH,min(derated) = tQH,min + tJIT(per),act,min = 0.38 × tCK(avg),act + tJIT(per),act,min = 0.38 × 2500ps – 72ps = + 878ps.

Clock Jitter [DDR3-1600, 1333]

		-GL, -GN		-DG, -DJ			
Data rate (Mbps)		1600		1333			
Parameter	Symbol	min.	max.	min.	max.	Unit	Notes
Average clock period	tCK (avg)	1250	3333	1500	3333	ps	1
Absolute clock period	tCK (abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max+ tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max+ tJIT(per)max	ps	2
Clock period jitter	tJIT (per)	–70	70	–80	80	ps	6
Clock period jitter during DLL locking period	tJIT (per, lck)	–60	60	–70	70	ps	6
Cycle to cycle period Jitter	tJIT (cc)	—	140	—	160	ps	7
Cycle to cycle clock period jitter during DLL locking period	tJIT (cc, lck)	—	120	—	140	ps	7
Cumulative error across 2 cycles	tERR (2per)	–103	103	–118	118	ps	8
Cumulative error across 3 cycles	tERR (3per)	–122	122	–140	140	ps	8
Cumulative error across 4 cycles	tERR (4per)	–136	136	–155	155	ps	8
Cumulative error across 5 cycles	tERR (5per)	–147	147	–168	168	ps	8
Cumulative error across 6 cycles	tERR (6per)	–155	155	–177	177	ps	8
Cumulative error across 7 cycles	tERR (7per)	–163	163	–186	186	ps	8
Cumulative error across 8 cycles	tERR (8per)	–169	169	–193	193	ps	8
Cumulative error across 9 cycles	tERR (9per)	–175	175	–200	200	ps	8
Cumulative error across 10 cycles	tERR (10per)	–180	180	–205	205	ps	8
Cumulative error across 11 cycles	tERR (11per)	–184	184	–210	210	ps	8
Cumulative error across 12 cycles	tERR (12per)	–188	188	–215	215	ps	8
Cumulative error across n = 13, 14…49, 50 cycles	tERR (nper)	tERR (nper) min. = (1+0.68in(n)) x tJIT(per) min tERR (nper) max. = (1+0.68in(n)) x tJIT(per) max				ps	9
Average high pulse width	tCH (avg)	0.47	0.53	0.47	0.53	tCK (avg)	3
Average low pulse width	tCL (avg)	0.47	0.53	0.47	0.53	tCK (avg)	4
Absolute clock high pulse width	tCH (abs)	0.43	—	0.43	—	tCK (avg)	10, 11
Absolute clock low pulse width	tCL (abs)	0.43	—	0.43	—	tCK (avg)	10, 12
Duty cycle jitter	tJIT (duty)	—	—	—	—	ps	5

Clock Jitter [DDR3-1066, 800]

		-AC, -AE, -AG		-8A, -8C			
Data rate (Mbps)		1066		800			
Parameter	Symbol	min.	max.	min.	max.	Unit	Notes
Average clock period	tCK (avg)	1875	3333	2500	3333	ps	1
Absolute clock period	tCK (abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max+ tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max+ tJIT(per)max	ps	2
Clock period jitter	tJIT (per)	–90	90	–100	100	ps	6
Clock period jitter during DLL locking period	tJIT (per, lck)	–80	80	–90	90	ps	6
Cycle to cycle period jitter	tJIT (cc)	—	180	—	200	ps	7
Cycle to cycle clock period jitter during DLL locking period	tJIT (cc, lck)	—	160	—	180	ps	7
Cumulative error across 2 cycles	tERR (2per)	–132	132	–147	147	ps	8
Cumulative error across 3 cycles	tERR (3per)	–157	157	–175	175	ps	8
Cumulative error across 4 cycles	tERR (4per)	–175	175	–194	194	ps	8
Cumulative error across 5 cycles	tERR (5per)	–188	188	–209	209	ps	8
Cumulative error across 6 cycles	tERR (6per)	–200	200	–222	222	ps	8
Cumulative error across 7 cycles	tERR (7per)	–209	209	–232	232	ps	8
Cumulative error across 8 cycles	tERR (8per)	–217	217	–241	241	ps	8
Cumulative error across 9 cycles	tERR (9per)	–224	224	–249	249	ps	8
Cumulative error across 10 cycles	tERR (10per)	–231	231	–257	257	ps	8
Cumulative error across 11 cycles	tERR (11per)	–237	237	–263	263	ps	8
Cumulative error across 12 cycles	tERR (12per)	–242	242	–269	269	ps	8
Cumulative error across n=13, 14…49,50 cycles	tERR (nper)	tERR (nper) min. = (1+0.68in(n)) x tJIT(per) min tERR (nper) max. = (1+0.68in(n)) x tJIT(per) max				ps	9
Average high pulse width	tCH (avg)	0.47	0.53	0.47	0.53	tCK (avg)	3
Average low pulse width	tCL (avg)	0.47	0.53	0.47	0.53	tCK (avg)	4
Absolute clock high pulse width	tCH (abs)	0.43	—	0.43	—	tCK (avg)	10, 11
Absolute clock low pulse width	tCL (abs)	0.43	—	0.43	—	tCK (avg)	10, 12
Duty cycle jitter	tJIT (duty)	—	—	—	—	ps	5

Notes: 1. tCK (avg) is calculated as the average clock period across any consecutive 200cycle window, where each clock period is calculated from rising edge to rising edge.

$$\left(\sum_{j=1}^{N} tCKj \right) \Big/ N \qquad N = 200$$

2. tCK (abs) is the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK (abs) is not subject to production test.
3. tCH (avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$\left(\sum_{j=1}^{N} tCHj \right) \Big/ (N \times tCK(avg)) \qquad N = 200$$

4. tCL (avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$\left(\sum_{j=1}^{N=200} tCL_j \right) \Big/ (N \times t_{CK(avg)})$$

5. tJIT (duty) is defined as the cumulative set of tCH jitter and tCL jitter. tCH jitter is the largest deviation of any single tCH from tCH (avg). tCL jitter is the largest deviation of any single tCL from tCL (avg). tJIT (duty) is not subject to production test.

   tJIT (duty) = Min./Max. of {tJIT (CH), tJIT (CL)}, where:

   tJIT (CH) = {tCH_j- tCH (avg) where j = 1 to 200}

   tJIT (CL) = {tCL_j- tCL (avg) where j = 1 to 200}

6. tJIT (per) is defined as the largest deviation of any single tCK from tCK (avg).

   tJIT (per) = Min./Max. of { tCK_j – tCK (avg) where j = 1 to 200}

   tJIT (per) defines the single period jitter when the DLL is already locked. tJIT (per, lck) uses the same definition for single period jitter, during the DLL locking period only. tJIT (per) and tJIT (per, lck) are not subject to production test.

7. tJIT (cc) is defined as the absolute difference in clock period between two consecutive clock cycles:

   tJIT (cc) = Max. of {tCK_{j+1} - tCK_j}

   tJIT (cc) is defines the cycle when the DLL is already locked. tJIT (cc, lck) uses the same definition for cycle-to-cycle jitter, during the DLL locking period only. tJIT (cc) and tJIT (cc, lck) are not subject to production test.

8. tERR (nper) is defined as the cumulative error across n multiple consecutive cycles from tCK (avg).

   tERR (nper) is not subject to production test.

9 n = from 13 cycles to 50 cycles. This row defines 38 parameters.

10. These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing hold at all times.

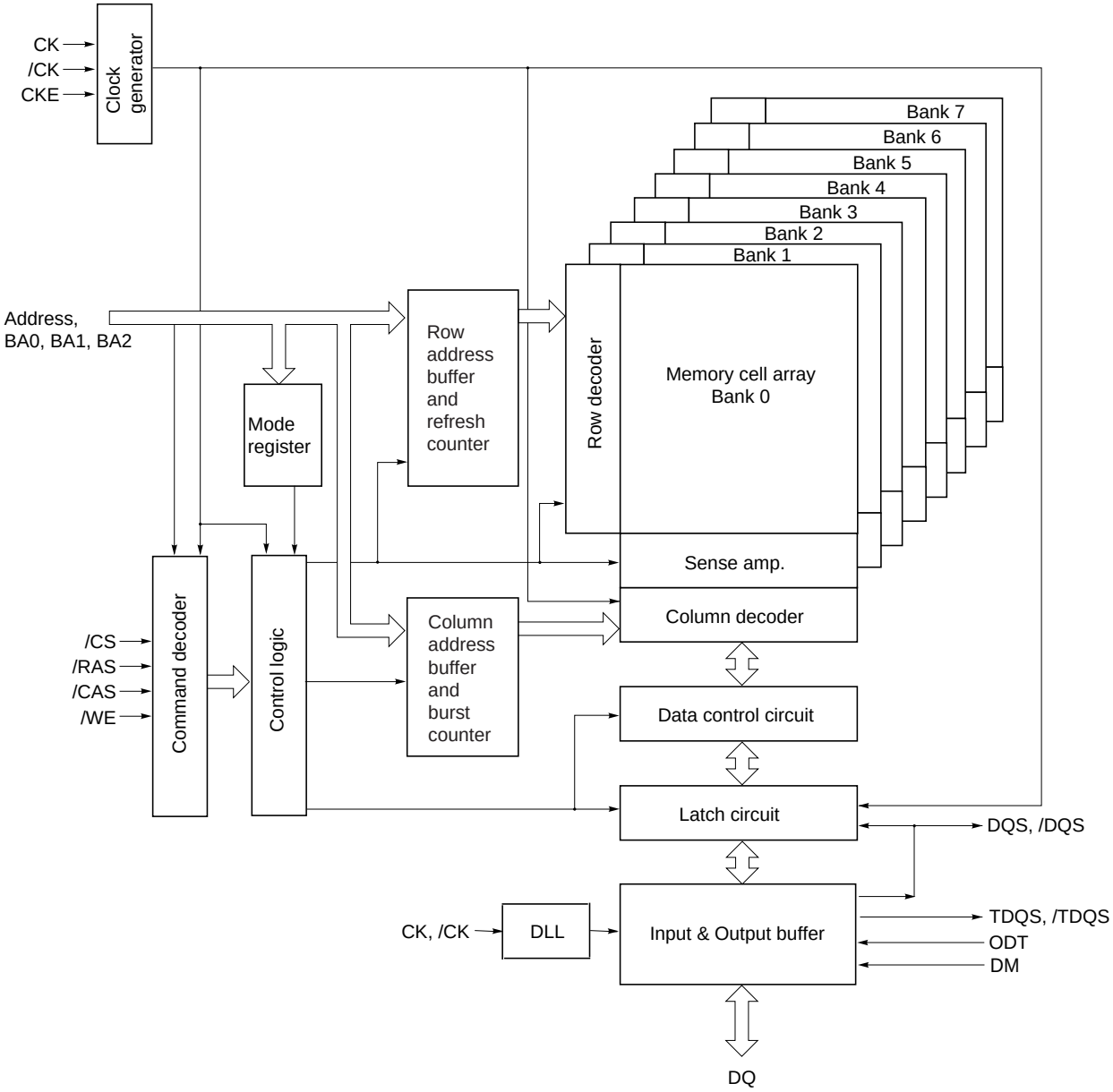
    (minimum and maximum of spec values are to be used for calculations in the table below.)

Parameter	Symbol	min.	max.	Unit
Absolute clock period	tCK (abs)	tCK (avg), min. + tJIT (per),min.	tCK (avg), max. + tJIT (per),max.	ps
Absolute clock high pulse width	tCH (abs)	tCH (avg), min. × tCK (avg),min. + tJIT (duty),min.	tCH (avg), max. × tCK (avg),max. + tJIT (duty),max.	ps
Absolute clock low pulse width	tCL (abs)	tCL (avg), min. × tCK (avg),min. + tJIT (duty),min.	tCL (avg), max. × tCK (avg),max. + tJIT (duty),max.	ps

11 tCH (abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.

12 tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

Block Diagram



Pin Function

CK, /CK (input pins)

CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).

/CS (input pin)

All commands are masked when /CS is registered high. /CS provides for external rank selection on systems with multiple ranks. /CS is considered part of the command code.

/RAS, /CAS, /WE (input pins)

/RAS, /CAS and /WE (along with /CS) define the command being entered.

A0 to A13 (input pins)

Provided the row address for active commands and the column address for read/write commands to select one location out of the memory array in the respective bank. (A10(AP) and A12(/BC) have additional functions, see below) The address inputs also provide the op-code during mode register set commands.

[Address Pins Table]

		Address (A0 to A13)		
Part number	Page size	Row address (RA)	Column address (CA)	Note
EDJ1104BASE	1KB	AX0 to AX13	AY0 to AY9, AY11	
EDJ1108BASE		AX0 to AX13	AY0 to AY9	
EDJ1116BASE	2KB	AX0 to AX12	AY0 to AY9	1

Note: A13 pin is NC for x16 organization.

A10(AP) (input pin)

A10 is sampled during read/write commands to determine whether auto precharge should be performed to the accessed bank after the read/write operation. (high: auto precharge; low: no auto precharge)

A10 is sampled during a precharge command to determine whether the precharge applies to one bank (A10 = low) or all banks (A10 = high). If only one bank is to be precharged, the bank is selected by bank addresses (BA).

A12(/BC) (input pin)

A12 is sampled during read and write commands to determine if burst chop (on-the-fly) will be performed.

(A12 = high: no burst chop, A12 = low: burst chopped.) See command truth table for details.

BA0 to BA2 (input pins)

BA0, BA1 and BA2 define to which bank an active, read, write or precharge command is being applied. BA0 and BA1 also determine which mode register (MR0 to MR3) is to be accessed during a MRS cycle.

[Bank Select Signal Table]

	BA0	BA1	BA2
Bank 0	L	L	L
Bank 1	H	L	L
Bank 2	L	H	L
Bank 3	H	H	L
Bank 4	L	L	H
Bank 5	H	L	H
Bank 6	L	H	H
Bank 7	H	H	H

Remark: H: VIH. L: VIL.

CKE (input pin)

CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides precharge power-down and self-refresh operation (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self-refresh exit. After VREF has become stable during the power-on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must be maintained to this input. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, /CK, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self-refresh.

DM, DMU, DML (input pins)

DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a write access. DM is sampled on both edges of DQS. For ×8 configuration, the function of DM or TDQS, /TDQS is enabled by mode register A11 setting in MR1.

DQ, DQU, DQL (input/output pins)

Bi-directional data bus.

DQS, /DQS, DQSU, /DQSU, DQSL, /DQSL (input/output pins)

Output with read data, input with write data. Edge-aligned with read data, center-aligned with write data.
The data strobe DQS is paired with differential signal /DQS to provide differential pair signaling to the system during READs and WRITEs.

TDQS, /TDQS (output pins)

TDQS and /TDQS is applicable for ×8 configuration only. When enabled via mode register A11 = 1 in MR1, DRAM will enable the same termination resistance function on TDQS, /TDQS as is applied to DQS, /DQS. When disabled via mode register A11 = 0 in MR1, DM/TDQS will provide the data mask function and /TDQS is not used.
In ×4/×16 configuration, the TDQS function must be disabled via mode register A11 = 0 in MR1.

/RESET (input pin)

/RESET is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD (1.20V for DC high and 0.30V for DC low).

It is negative active signal (active low) and is referred to GND. There is no termination required on this signal. It will be heavily loaded across multiple chips. /RESET is destructive to data contents.

ODT (input pins)

ODT (registered high) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, /DQS, DM/TDQS, NU(/TDQS) (when TDQS is enabled via mode register A11 = 1 in MR1) signal for ×4/×8 configuration. For ×16 configuration ODT is applied to each DQ, DQSU, /DQSU, DQSL, /DQSL, DMU, and DML signal. The ODT pin will be ignored if the mode register (MR1) is programmed to disable ODT.

ZQ (supply)

Reference pin for ZQ calibration.

VDD, VSS, VDDQ, VSSQ (power supply)

VDD and VSS are power supply pins for internal circuits. VDDQ and VSSQ are power supply pins for the output buffers.

VREFCA, VREFDQ (power supply)

Reference voltage

Command Operation

Command Truth Table

The DDR3 SDRAM recognizes the following commands specified by the /CS, /RAS, /CAS, /WE and address pins.

Function	Symbol	CKE		/CS	/RAS	/CAS	/WE	BA0 to BA2	A12 (/BC)	A10 (AP)	Address	Notes
		Previous cycle	Current cycle									
Mode register set	MRS	H	H	L	L	L	L	BA	op-code			
Auto-refresh	REF	H	H	L	L	L	H	V	V	V	V	
Self-refresh entry	SELF	H	L	L	L	L	H	V	V	V	V	6, 8, 11
Self-refresh exit	SREX	L	H	H	×	×	×	×	×	×	×	6, 7, 8, 11
		L	H	L	H	H	H	V	V	V	V	
Single bank precharge	PRE	H	H	L	L	H	L	BA	V	L	V	
Precharge all banks	PALL	H	H	L	L	H	L	V	V	H	V	
Bank activate	ACT	H	H	L	L	H	H	BA	RA			12
Write (Fixed BL)	WRIT	H	H	L	H	L	L	BA	V	L	CA	
Write (BC4, on the fly)	WRS4	H	H	L	H	L	L	BA	L	L	CA	
Write (BL8, on the fly)	WRS8	H	H	L	H	L	L	BA	H	L	CA	
Write with auto precharge (Fixed BL)	WRITA	H	H	L	H	L	L	BA	V	H	CA	
Write with auto precharge (BC4, on the fly)	WRAS4	H	H	L	H	L	L	BA	L	H	CA	
Write with auto precharge (BL8, on the fly)	WRAS8	H	H	L	H	L	L	BA	H	H	CA	
Read (Fixed BL)	READ	H	H	L	H	L	H	BA	V	L	CA	
Read (BC4, on the fly)	RDS4	H	H	L	H	L	H	BA	L	L	CA	
Read (BL8, on the fly)	RDS8	H	H	L	H	L	H	BA	H	L	CA	
Read with auto precharge (Fixed BL)	READA	H	H	L	H	L	H	BA	V	H	CA	
Read with auto precharge (BC4, on the fly)	RDAS4	H	H	L	H	L	H	BA	L	H	CA	
Read with auto precharge (BL8, on the fly)	RDAS8	H	H	L	H	L	H	BA	H	H	CA	
No operation	NOP	H	H	L	H	H	H	V	V	V	V	9
Device deselect	DESL	H	H	H	×	×	×	×	×	×	×	10
Power-down mode entry	PDEN	H	L	H	×	×	×	×	×	×	×	5, 11
		H	L	L	H	H	H	V	V	V	V	
Power-down mode exit	PDEX	L	H	H	×	×	×	×	×	×	×	5, 11
		L	H	L	H	H	H	V	V	V	V	
ZQ calibration long	ZQCL	H	H	L	H	H	L	×	×	H	×	
ZQ calibration short	ZQCS	H	H	L	H	H	L	×	×	L	×	

Remark: H = VIH. L = VIL. × = Don't care (defined or undefined (including floating around VREF)) logic level. V = VIH or VIL (defined logic level).

BA = Bank addresses. RA = Row Address. CA = Column Address. /BC = Burst Chop.

Notes: 1. All DDR3 commands are defined by states of /CS, /RAS, /CAS, /WE and CKE at the rising edge of the clock. The most significant bit (MSB) of BA, RA, and CA are device density and configuration dependent.
2. /RESET is an active low asynchronous signal that must be driven high during normal operation
3. Bank Addresses (BA) determine which bank is to be operated upon. For MRS, BA selects an mode register.
4. Burst READs or WRITEs cannot be terminated or interrupted and fixed/on the fly BL will be defined by MRS.
5. The power-down mode does not perform any refresh operations.
6. The state of ODT does not affect the states described in this table. The ODT function is not available during self-refresh.
7. Self-refresh exit is asynchronous.
8. VREF (Both VREFDQ and VREFCA) must be maintained during self-refresh operation.
9. The No Operation command (NOP) should be used in cases when the DDR3 SDRAM is in an idle or a wait state. The purpose of the NOP command is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A NOP command will not terminate a previous operation that is still executing, such as a burst read or write cycle.
10. The DESL command performs the same function as a NOP command.
11. Refer to the CKE Truth Table for more detail with CKE transition.
12. No more than 4 banks may be activated in a rolling tFAW window. Converting to clocks is done by dividing tFAW (ns) by tCK (ns) and rounding up to next integer value. As an example of the rolling window, if (tFAW/tCK) rounds up to 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued in clock N+1 through N+9.

No Operation Command [NOP]

The No Operation command (NOP) should be used in cases when the DDR3 SDRAM is in an idle or a wait state. The purpose of the NOP command is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A NOP command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

The no operation (NOP) command is used to instruct the selected DDR3 SDRAM to perform a NOP (/CS low, /RAS, /CAS, /WE high). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

Device Deselect Command [DESL]

The deselect function (/CS high) prevents new commands from being executed by the DDR3 SDRAM. The DDR3 SDRAM is effectively deselected. Operations already in progress are not affected.

Mode Register Set Command [MR0 to MR3]

The mode registers are loaded via row address inputs. See mode register descriptions in the Programming the Mode Register section. The mode register set command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until tMRD is met.

Bank Activate Command [ACT]

This command is used to open (or activate) a row in a particular bank for a subsequent access. The values on the BA inputs select the bank, and the address provided on row address inputs selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank. A precharge command must be issued before opening a different row in the same bank.

Note: No more than 4 banks may be activated in a rolling tFAW window. Converting to clocks is done by dividing tFAW (ns) by tCK (ns) and rounding up to next integer value. As an example of the rolling window, if (tFAW/tCK) rounds up to 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued in clock N+1 through N+9.

Read Command [READ, RDS4, RDS8, READA, RDAS4, RDAS8]

The read command is used to initiate a burst read access to an active row. The values on the BA inputs select the bank, and the address provided on column address inputs selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

Write Command [WRIT, WRS4, WRS8, WRITA, WRAS4, WRAS8]

The write command is used to initiate a burst write access to an active row. The values on the BA inputs select the bank, and the address provided on column address inputs selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered low, the corresponding data will be written to memory; if the DM signal is registered high, the corresponding data inputs will be ignored, and a write will not be executed to that byte/column location.

Precharge Command [PRE, PALL]

The precharge command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA select the bank. Otherwise BA are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any read or write commands being issued to that bank. A precharge command will be treated as a NOP if there is no open row in that bank (idle state), or if the previously open row is already in the process of precharging.

Auto precharge Command [READA, WRITA]

Before a new row in an active bank can be opened, the active bank must be precharged using either the precharge command or the auto precharge function. When a read or a write command is given to the DDR3 SDRAM, the /CAS timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the read or write command is issued, then normal read or write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is high when the read or write command is issued, then the auto precharge function is engaged. During auto precharge, a read command will execute as normal with the exception that the active bank will begin to precharge on the rising edge which is /CAS latency (CL) clock cycles before the end of the read burst. (This timing is equal to the rising edge which is (AL* + BL/2) cycles later from the read with auto precharge command.)

Auto precharge can also be implemented during write commands. The precharge operation engaged by the Auto precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array.

This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon /CAS latency) thus improving system performance for random data access. The tRAS lockout circuit internally delays the Precharge operation until the array restore operation has been completed so that the auto precharge command may be issued with any read or write command.

Note: AL (Additive Latency), refer to Posted /CAS description in the Register Definition section.

Auto-Refresh Command [REF]

Auto-refresh is used during normal operation of the DDR3 SDRAM and is analogous to /CAS-before-/RAS (CBR) refresh in FPM/EDO DRAM. This command is nonpersistent, so it must be issued each time a refresh is required.

The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an auto-refresh command.

A maximum of eight auto-refresh commands can be posted to any given DDR3, meaning that the maximum absolute interval between any auto-refresh command and the next auto-refresh command is $9 \times$ tREFI. This maximum absolute interval is to allow DDR3 output drivers and internal terminators to automatically recalibrate compensating for voltage and temperature changes.

Self-Refresh Command [SELF]

The self-refresh command can be used to retain data in the DDR3, even if the rest of the system is powered down. When in the self-refresh mode, the DDR3 retains data without external clocking. The self-refresh command is initiated like an auto-refresh command except CKE is disabled (low). The DLL is automatically disabled upon entering self-refresh and is automatically enabled and reset upon exiting self-refresh. The active termination is also disabled upon entering self-refresh and enabled upon exiting self-refresh. (512 clock cycles must then occur before a read command can be issued). Input signals except CKE are "Don't Care" during self-refresh. The procedure for exiting self-refresh requires a sequence of commands. First, CK and /CK must be stable prior to CKE going back high. Once CKE is high, the DDR3 must have NOP commands issued for tXSDLL because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh, DLL requirements and out-put calibration is to apply NOPs for 512 clock cycles before applying any other command to allow the DLL to lock and the output drivers to recalibrate.

ZQ calibration Command [ZQCL, ZQCS]

ZQ calibration command (short or long) is used to calibrate DRAM RON and ODT values over PVT.

ZQ Calibration Long (ZQCL) command is used to perform the initial calibration during power-up initialization sequence.

ZQ Calibration Short (ZQCS) command is used to perform periodic calibrations to account for VT variations.

All banks must be precharged and tRP met before ZQCL or ZQCS commands are issued by the controller.

ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self-refresh.

CKE Truth Table

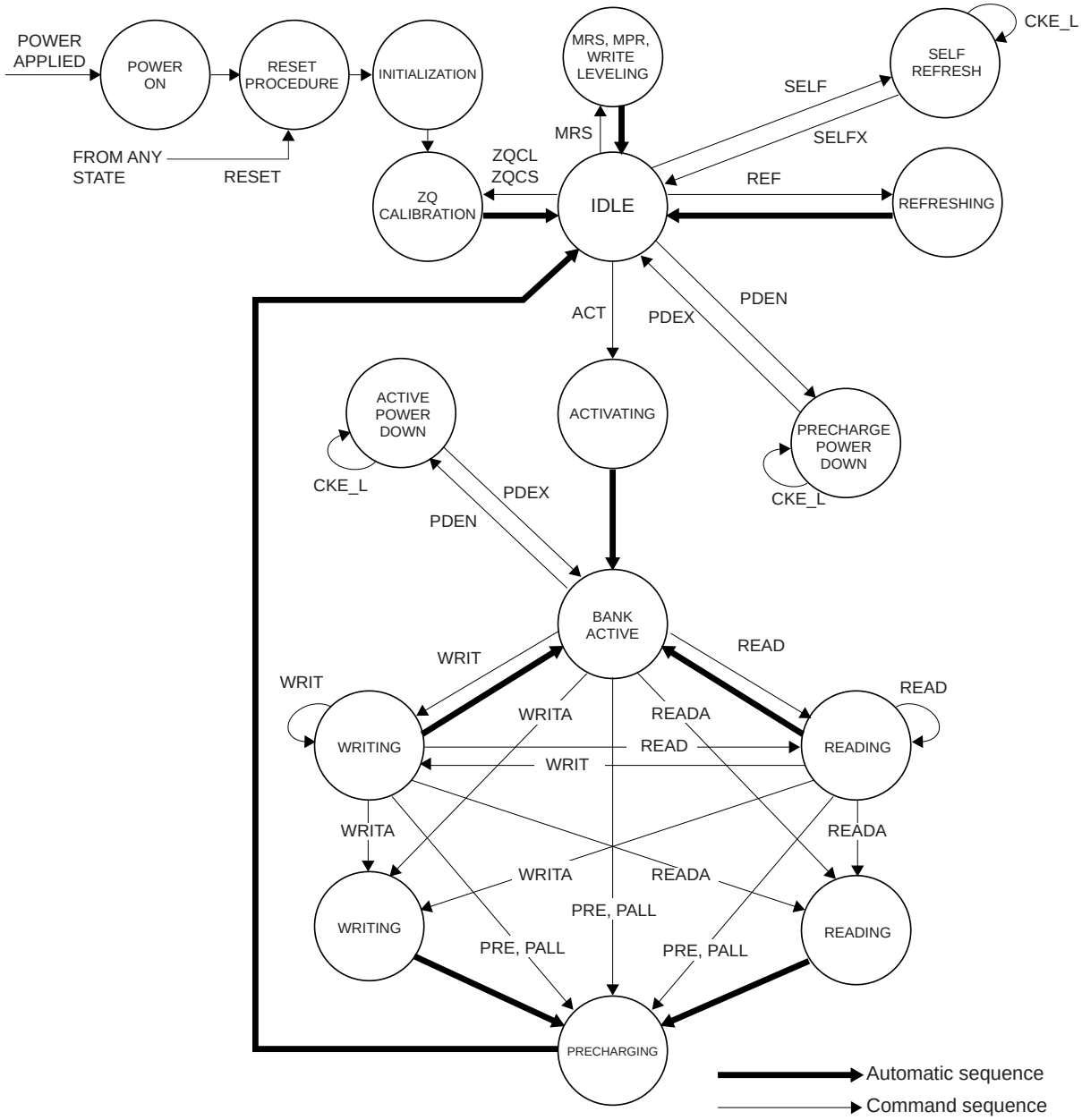
Current state*2	CKE Previous cycle (n-1)*1	CKE Current cycle (n)*1	Command (n)*3 /CS, /RAS, /CAS, /WE	Operation (n)*3	Notes
Power-down	L	L	×	Maintain power-down	14, 15
	L	H	DESL or NOP	Power-down exit	11, 14
Self-refresh	L	L	×	Maintain self-refresh	15, 16
	L	H	DESL or NOP	Self-refresh exit	8, 12, 16
Bank Active	H	L	DESL or NOP	Active power-down entry	11, 13, 14
Reading	H	L	DESL or NOP	Power-down entry	11, 13, 14, 17
Writing	H	L	DESL or NOP	Power-down entry	11, 13, 14, 17
Precharging	H	L	DESL or NOP	Power-down entry	11, 13, 14, 17
Refreshing	H	L	DESL or NOP	Precharge power-down entry	11
All banks idle	H	L	DESL or NOP	Precharge power-down entry	11, 13, 14, 18
	H	L	REFRESH	Self-refresh entry	9, 13, 18
Any state other than listed above	H	H	Refer to the Command Truth Table		10

Remark: H = VIH. L = VIL. × = Don't care

Notes: 1. CKE (n) is the logic state of CKE at clock edge n; CKE (n−1) is the state of CKE at the previous clock edge.

2. Current state is the state of the DDR3 SDRAM immediately prior to clock edge n.
3. Command (n) is the command registered at clock edge n, and operation (n) is a result of Command (n). ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during self-refresh.
6. CKE must be registered with the same value on tCKE (min.) consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the tCKE (min.) clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + tCKE (min.) + tIH.
7. DESL and NOP are defined in the Command Truth Table.
8. On self-refresh exit, DESL or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT command may be issued only after tXSDLL is satisfied.
9. Self-refresh mode can only be entered from the all banks idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for power-down entry and exit are NOP and DESL only.
12. Valid commands for self-refresh exit are NOP and DESL only.
13. Self-refresh can not be entered while read or write operations, (extended) mode register set operations or precharge operations are in progress. See section Power-Down and self-refresh Command for a detailed list of restrictions.
14. The power-down does not perform any refresh operations.
15. "×" means "don't care" (including floating around VREF) in self-refresh and power-down. It also applies to address pins.
16. VREF (Both VREFDQ and VREFCA) must be maintained during self-refresh operation.
17. If all banks are closed at the conclusion of the read, write or precharge command, the precharge power-down is entered, otherwise active power-down is entered.
18. Idle state means that all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress. CKE is high and all timings from previous operation are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all self-refresh exit and power-down exit parameters are satisfied (tXS, tXP, tXPDLL, etc).

Simplified State Diagram



RESET and Initialization Procedure

Power-Up and Initialization Sequence

1. Apply power (/RESET is recommended to be maintained below 0.2 × VDD, (all other inputs may be undefined).) /RESET needs to be maintained for minimum 200μs with stable power. CKE is pulled low anytime before /RESET being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to VDD (min.) must be no greater than 200ms; and during the ramp, VDD > VDDQ and (VDD − VDDQ) < 0.3V.

- VDD and VDDQ are driven from a single power converter output

  AND

- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95V max once power ramp is finished,

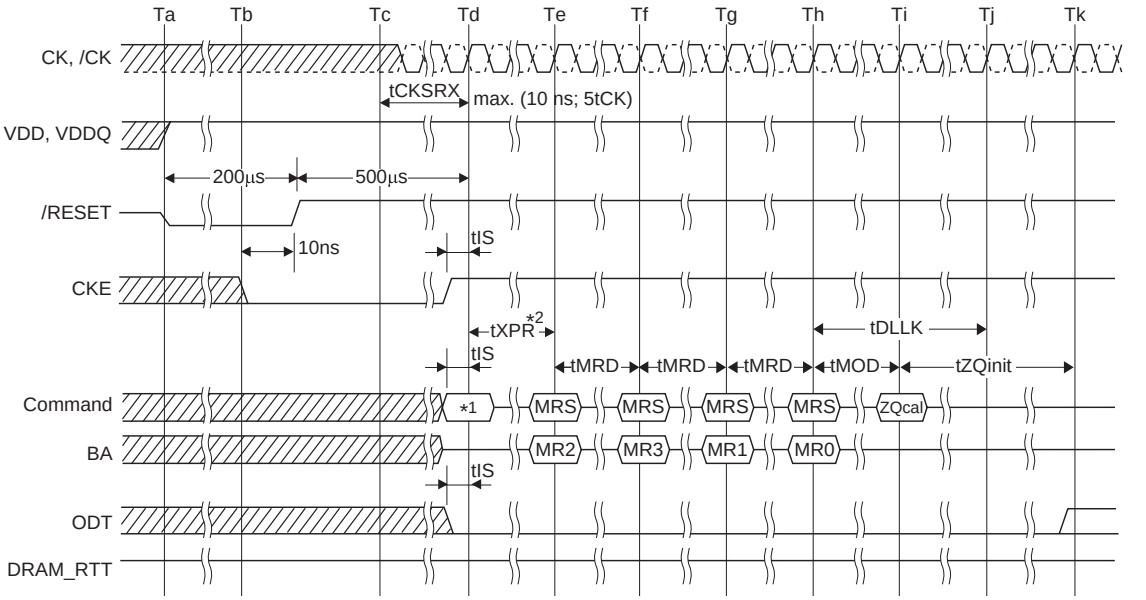
  AND

- VREF tracks VDDQ/2.

OR

- Apply VDD without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT and VREF.
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

2. After /RESET is de-asserted, wait for another 500μs until CKE become active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.
3. Clocks (CK, /CK) need to be started and stabilized for at least 10ns or 5tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must be met. Also a NOP or DESL command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE registered “high” after Reset, CKE needs to be continuously registered high until the initialization sequence is finished, including expiration of tDLLK and tZQinit.
4. The DDR3 SDRAM will keep its on-die termination in high-impedance state during /RESET being asserted at least until CKE being registered high. Therefore, the ODT signal may be in undefined state until tIS before CKE being registered high. After that, the ODT signal must be kept inactive (low) until the power-up and initialization sequence is finished, including expiration of tDLLK and tZQinit.
5. After CKE being registered high, wait minimum of tXPR, before issuing the first MRS command to load mode register. (tXPR = max. (tXS ; 5 × tCK)
6. Issue MRS command to load MR2 with all application settings. (To issue MRS command for MR2, provide low to BA0 and BA2, high to BA1.)
7. Issue MRS command to load MR3 with all application settings. (To issue MRS command for MR3, provide low to BA2, high to BA0 and BA1.)
8. Issue MRS command to load MR1 with all application settings and DLL enabled. (To issue DLL Enable command, provide low to A0, high to BA0 and low to BA1 and BA2).
9. Issue MRS command to load MR0 with all application settings and DLL reset. (To issue DLL reset command, provide high to A8 and low to BA0 to BA2).
10. Issue ZQCL command to start ZQ calibration.
11. Wait for both tDLLK and tZQinit completed.
12. The DDR3 SDRAM is now ready for normal operation.



Notes: 1. From time point "Td" until "Tk", NOP or DESL commands must be applied between MRS and ZQcal commands.
2. tXPR = max. (tXS; 5tCK)

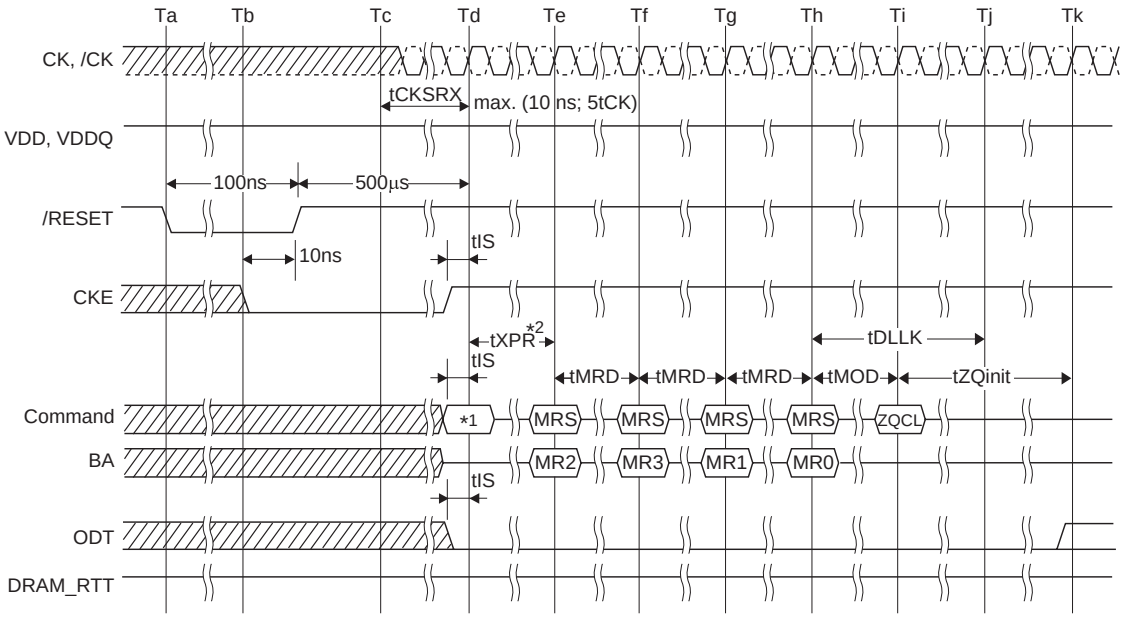
: VIH or VIL

Reset and Initialization Sequence at Power-On Ramping

Reset and Initialization with Stable Power

The following sequence is required for /RESET at no power interruption initialization.

1. Assert /RESET below 0.2 × VDD anytime when reset is needed (all other inputs may be undefined). /RESET needs to be maintained for minimum 100ns. CKE is pulled low before /RESET being de-asserted (minimum time 10ns).
2. Follow Power-Up Initialization Sequence steps 2 to 12.
3. The reset sequence is now completed; DDR3 SDRAM is ready for normal operation.



Notes: 1. From time point "Td" until"Tk", NOP or DESL commands must be applied between MRS and ZQCL commands.
2. tXPR = max. (tXS; 5tCK)

: VIH or VIL

Reset Procedure at Power Stable Condition

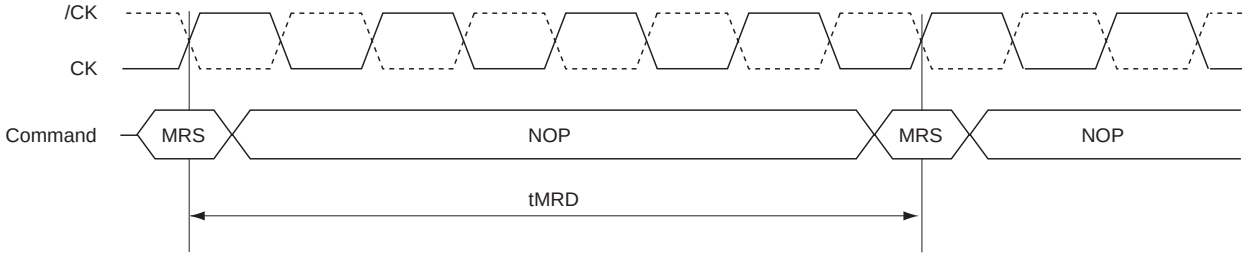
Programming the Mode Register

For application flexibility, various functions, features and modes are programmable in four mode registers, provided by the DDR3 SDRAM, as user defined variables, and they must be programmed via a Mode Register Set (MRS) command. As the default values of the Mode Registers (MR#) are not defined, content of mode registers must be fully initialized and/or re-initialized, i.e. written, after Power-up and/or reset for proper operation. Also the contents of the mode registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset does not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents.

The mode register set command cycle time, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands. The MRS command to non-MRS command delay, tMOD, is required for the DRAM to update the features except DLL reset and is the minimum time required from an MRS command to a non-MRS command excluding NOP and DESL. The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e. all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is already high prior to writing into the mode register. The mode registers are divided into various fields depending on the functionality and/or modes.

Mode Register Set Command Cycle Time (tMRD)

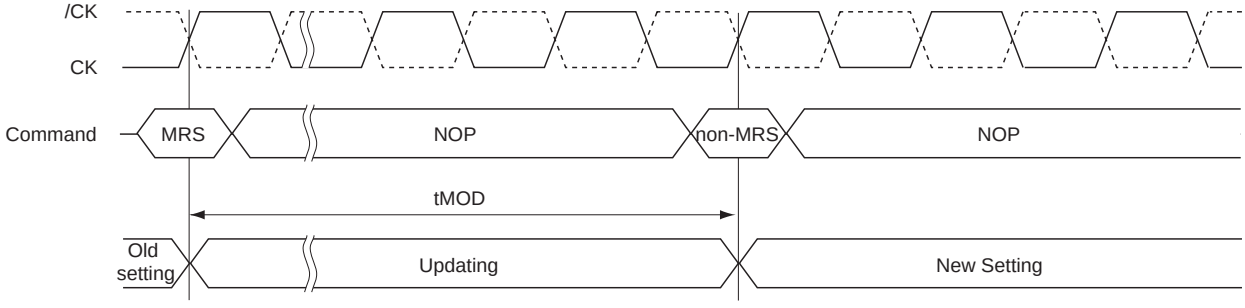
tMRD is the minimum time required from an MRS command to the next MRS command. As DLL enable and DLL reset are both MRS commands, tMRD is applicable between MRS to MR1 for DLL enable and MRS to MR0 for DLL reset, and not tMOD.



tMRD Timing

MRS Command to Non-MRS Command Delay (tMOD)

tMOD is the minimum time required from an MRS command to a non-MRS command excluding NOP and DESL. Note that additional restrictions may apply, for example, MRS to MR0 for DLL reset followed by read.

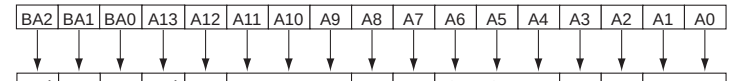


tMOD Timing

DDR3 SDRAM Mode Register 0 [MR0]

The mode register MR0 stores the data for controlling various operating modes of DDR3 SDRAM.

It controls burst length, read burst type, /CAS latency, test mode, DLL reset, WR and DLL control for precharge power-down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on /CS, /RAS, /CAS, /WE, BA0 and BA1, while controlling the states of address pins according to the table below.



A8	DLL reset
0	No
1	Yes

A7	Mode
0	Normal
1	Test

A3	Read burst type
0	Nibble sequential
1	Interleave

Burst length

A1	A0	BL
0	0	8 (Fixed)
0	1	4 or 8 (on the fly)
1	0	4 (Fixed)
1	1	Reserved

BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A12	DLL Control for Precharge PD
0	Slow exit (DLL off)
1	Fast exit (DLL on)

Write recovery for autoprecharge

A11	A10	A9	WR
0	0	0	Reserved
0	0	1	5*2
0	1	0	6*2
0	1	1	7*2
1	0	0	8*2
1	0	1	10*2
1	1	0	12*2
1	1	1	Reserved

/CAS latency

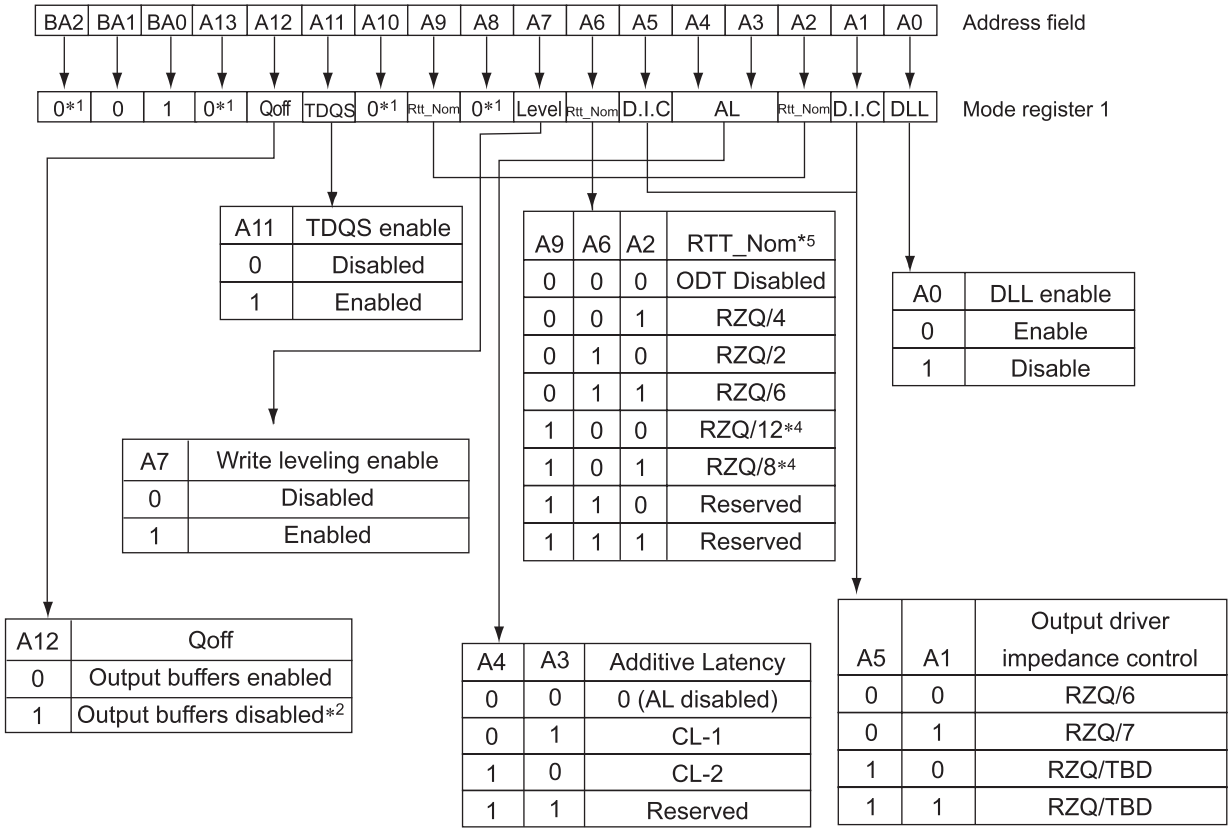
A6	A5	A4	A2	Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	Reserved

Notes: 1. BA2 and A13 are reserved for future use and must be programmed to 0 during MRS.
2. WR (min.) (Write Recovery for autoprecharge) is determined by tCK (max.) and WR (max.) is determined by tCK (min.). WR in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer (WR (min.) [cycles] = roundup tWR (ns) / tCK (ns)).
(The WR value in the mode register must be programmed to be equal or larger than WR (min.)
This is also used with tRP to determine tDAL.

MR0 Programming

DDR3 SDRAM Mode Register 1 [MR1]

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, RTT_Nom impedance, additive latency, write leveling enable, TDQS enable and Qoff. The Mode Register 1 is written by asserting low on /CS, /RAS, /CAS, /WE, high on BA0 and low on BA1, while controlling the states of address pins according to the table below



A11	TDQS enable
0	Disabled
1	Enabled

A9	A6	A2	RTT_Nom*5
0	0	0	ODT Disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/12*4
1	0	1	RZQ/8*4
1	1	0	Reserved
1	1	1	Reserved

A0	DLL enable
0	Enable
1	Disable

A7	Write leveling enable
0	Disabled
1	Enabled

A12	Qoff
0	Output buffers enabled
1	Output buffers disabled*2

A4	A3	Additive Latency
0	0	0 (AL disabled)
0	1	CL-1
1	0	CL-2
1	1	Reserved

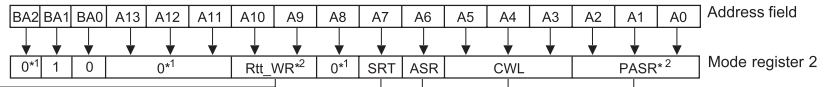
A5	A1	Output driver impedance control
0	0	RZQ/6
0	1	RZQ/7
1	0	RZQ/TBD
1	1	RZQ/TBD

Notes: 1. BA2, A8, A10 and A13 are reserved for future use (RFU) and must be programmed to 0 during MRS.
2. Outputs disabled - DQ, DQS, /DQS.
3. RZQ = 240Ω
4. If RTT_Nom is used during writes, only the values RZQ/2, RZQ/4 and RAQ/6 are allowed.
5. In Write leveling Mode (MR1[bit7] = 1) with MR1[bit12]=1, all RTT_Nom settings are allowed; in Write Leveling Mode (MR1[bit7] =1) with MR1[bit12]=0, only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed

MR1 Programming

DDR3 SDRAM Mode Register 2 [MR2]

The Mode Register MR2 stores the data for controlling refresh related features, RTT_WR impedance and /CAS write latency (CWL). The Mode Register 2 is written by asserting low on /CS, /RAS, /CAS, /WE, high on BA1 and low on BA0, while con-trolling the states of address pins according to the table below.



A7	Self-refresh range
0	Normal self-refresh
1	Extend temperture self-refresh (Optional)

A6	Auto self-refresh method
0	Manual SR reference (SRT)
1	ASR enable (Optional)

Partial array self-refresh

A2	A1	A0	Refresh array	
0	0	0	Full	—
0	0	1	Half : Bank 0 to Bank 3	(BA [2:0] = 000, 001, 010, 011)
0	1	0	Quarter: Bank 0 and Bank 1	(BA [2:0] = 000, 001)
0	1	1	1/8 : Bank 0	(BA [2:0] = 000)
1	0	0	3/4 : Bank 2 to Bank 7	(BA [2:0] = 010, 011, 100, 101,110 ,111)
1	0	1	Half : Bank 4 to Bank 7	(BA [2:0] = 100, 101, 110, 111)
1	1	0	Quarter: Bank 6 and Bank 7	(BA [2:0] = 110, 111)
1	1	1	1/8 : Bank 7	(BA [2:0] = 111)

A10	A9	Rtt_WR
0	0	Dynamic ODT off (write does not affect Rtt value)
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

A5	A4	A3	CAS write Latency (CWL)
0	0	0	5 (tCK ≥ 2.5ns)
0	0	1	6 (2.5ns > tCK ≥ 1.875ns)
0	1	0	7 (1.875ns > tCK ≥ 1.5ns)
0	1	1	8 (1.5ns > tCK ≥ 1.25ns)
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Notes: 1. BA2, A8, and A11 to A13 are RFU and must be programmed to 0 during MRS.

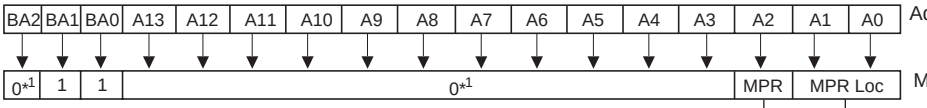
2. The Rtt_WR value can be applied during writes even when Rtt_Nom is desabled. Dring write leveling, Dynamic ODT is not avaiable.

3. Optiona in DDR3 SDRAM: If PASR (Partial Array Self-Refresh) is enabled, data located in areas of the array beyond the specified address range will be lost if self-refresh is entered. Data integrity will be maintained if tREF conditions are met and no self-refresh command is issued.

MR2 Programming

DDR3 SDRAM Mode Register 3 [MR3]

The Mode Register MR3 controls Multi Purpose Registers (MPR). The Mode Register 3 is written by asserting low on /CS, /RAS, /CAS, /WE, high on BA1 and BA0, while controlling the states of address pins according to the table below.



MPR Operation

A2	MPR
0	Normal operation*3
1	Data flow from MPR

MPR Address

A1	A0	MPR location
0	0	Predefined pattern*2
0	1	RFU
1	0	RFU
1	1	RFU

Notes : 1. BA2, A3 to A13 are reserved for future use (RFU) and must be programmed to 0 during MRS.
2. The predefined pattern will be used for read synchronization.
3 . When MPR control is set for normal operation, MR3 A[2]=0, MR3 A[1:0] will be ignored.

MR3 Programming

Burst Length (MR0)

Read and write accesses to the DDR3 are burst oriented, with the burst length being programmable, as shown in the figure MR0 Programming. The burst length determines the maximum number of column locations that can be accessed for a given read or write command. Burst length options include fixed BC4, fixed BL8, and on the fly which allows BC4 or BL8 to be selected coincident with the registration of a read on write command Via A12 (/BC).

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

Burst Chop

In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on the fly via A12(/BC), the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.

Burst Type (MR0)

[Burst Length and Sequence]

Burst length	Operation	Starting address (A2, A1, A0)	Sequential addressing (decimal)	Interleave addressing (decimal)
4 (burst chop)	READ	000	0, 1, 2, 3, T, T, T, T	0, 1, 2, 3, T, T, T, T
		001	1, 2, 3, 0, T, T, T, T	1, 0, 3, 2, T, T, T, T
		010	2, 3, 0, 1, T, T, T, T	2, 3, 0, 1, T, T, T, T
		011	3, 0, 1, 2, T, T, T, T	3, 2, 1, 0, T, T, T, T
		100	4, 5, 6, 7, T, T, T, T	4, 5, 6, 7, T, T, T, T
		101	5, 6, 7, 4, T, T, T, T	5, 4, 7, 6, T, T, T, T
		110	6, 7, 4, 5, T, T, T, T	6, 7, 4, 5, T, T, T, T
		111	7, 4, 5, 6, T, T, T, T	7, 6, 5, 4, T, T, T, T
	WRITE	0VV	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X
		1VV	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X
8	READ	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
		001	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
		010	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
		011	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
		100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
		101	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
		110	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
		111	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0
	WRITE	VVV	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7

Remark: T: Output driver for data and strobes are in high impedance.
V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.
X: Don't Care.

Notes: 1. Page length is a function of I/O organization and column addressing
2. 0...7 bit number is value of CA [2:0] that causes this bit to be the first read during a burst.

DLL Enable (MR1)

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering self-refresh operation and is automatically re-enabled upon exit of self-refresh operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON or tAOF parameters. During tDLLK, CKE must continuously be registered high.

DDR3 SDRAM does not require DLL for any write operation. DDR3 does not require DLL to be locked prior to any write operation. DDR3 requires DLL to be locked only for read operation and to achieve synchronous ODT timing.

DLL-off Mode

DDR3 DLL-off mode is entered by setting MR1 bit A0 to 1; this will disable the DLL for subsequent operations until A0 bit set back to 0. The MR1 A0 bit for DLL control can be switched either during initialization or later.

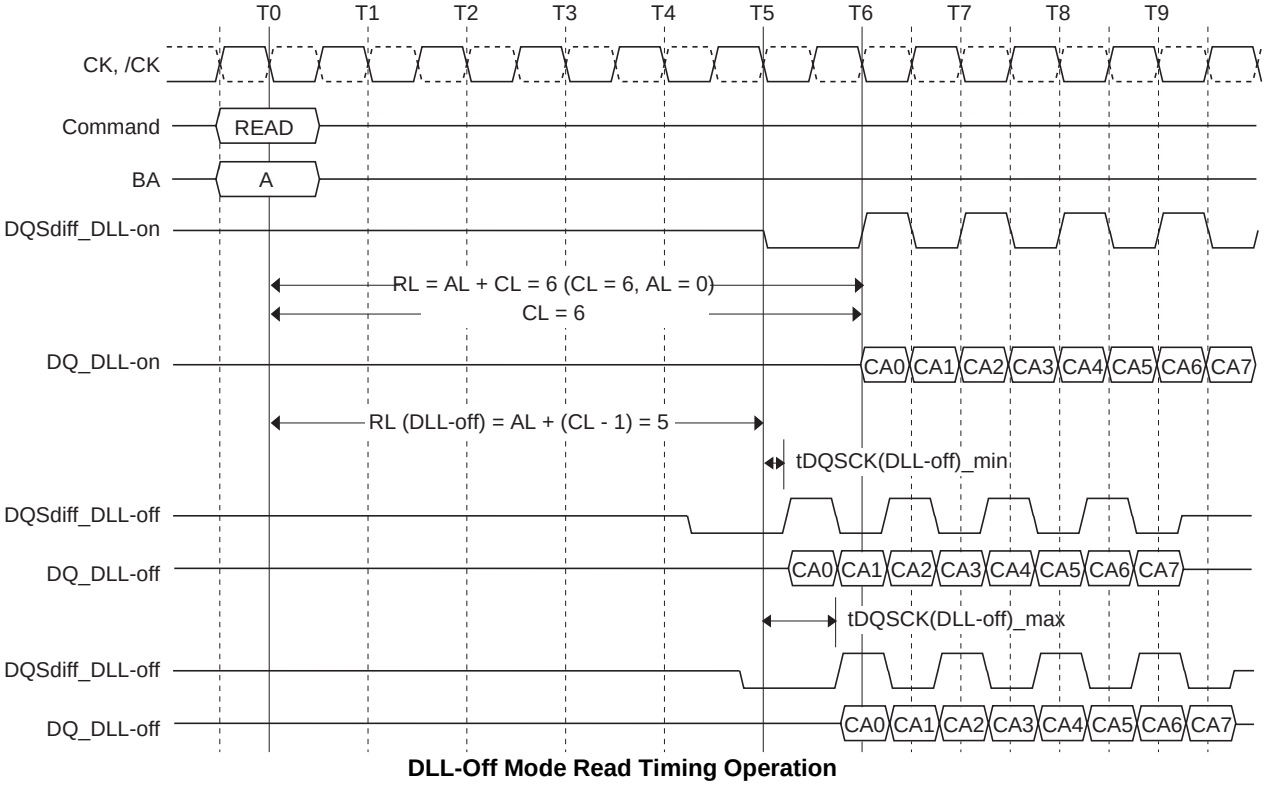
The DLL-off mode operations listed below are an optional feature for DDR3. The maximum clock frequency for DLL-off mode is specified by the parameter tCKDLL_OFF. There is no minimum frequency limit besides the need to satisfy the refresh interval, tREFI.

Due to latency counter and timing restrictions, only one value of /CAS Latency (CL) in MR0 and CAS Write Latency (CWL) in MR2 are supported. The DLL-off mode is only required to support setting of both CL = 6 and CWL = 6.

DLL-off mode will affect the Read data Clock to Data Strobe relationship (tDQSCK) but not the Data Strobe to Data relationship (tDQSQ, tQH, tQHS). Special attention is needed to line up Read data to controller time domain.

Comparing with DLL-on mode, where tDQSCK starts from the rising clock edge (AL + CL) cycles after the Read command, the DLL-off mode tDQSCK starts (AL + CL – 1) cycles after the read command. Another difference is that tDQSCK may not be small compared to tCK (it might even be larger than tCK) and the difference between tDQSCK (min.). and tDQSCK (max.) is significantly larger than in DLL-on mode.

The timing relations on DLL-off mode READ operation are shown at following Timing Diagram (CL = 6, BL8):



DLL-Off Mode Read Timing Operation

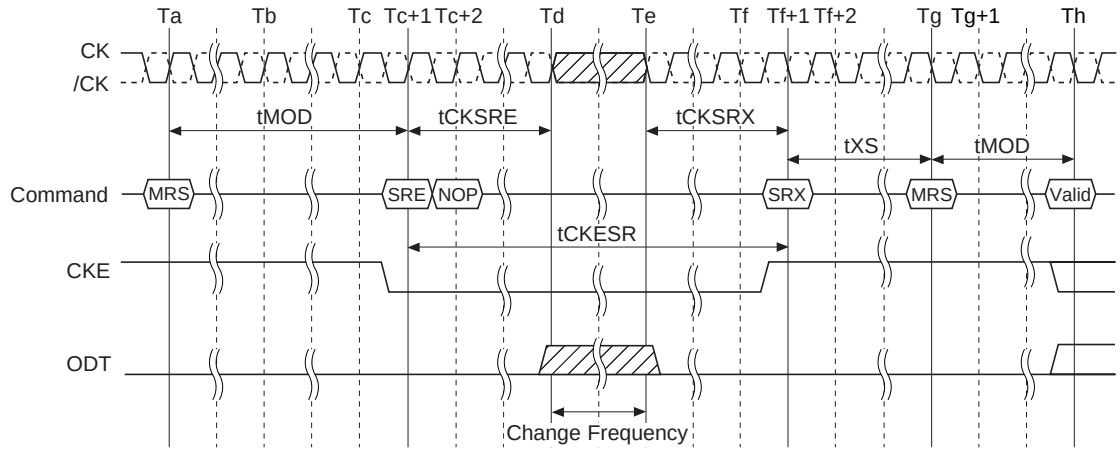
DLL on/off switching procedure

DDR3 DLL-off mode is entered by setting MR1 bit A0 to "1"; this will disable the DLL for subsequent operations until A0 bit set back to "0".

DLL "on" to DLL "off" Procedure

To switch from DLL "on" to DLL "off" requires the frequency to be changed during self-refresh outlined in the following procedure:

1. Starting from Idle state (all banks pre-charged, all timings fulfilled, and DRAMs On-die Termination resistors, RTT, must be in high impedance state before MRS to MR1 to disable the DLL.)
2. Set MR1 Bit A0 to "1" to disable the DLL.
3. Wait tMOD.
4. Enter self-refresh mode; wait until (tCKSRE) satisfied.
5. Change frequency, in guidance with Input Clock Frequency Change during Precharge Power-Down section.
6. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs. After stable clock, wait tCKSRX before issuing SRX command.
7. Starting with the self-refresh exit command, CKE must continuously be registered high until all tMOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when self-refresh mode was entered, the ODT signal must continuously be registered low until all tMOD timings from any MRS command are satisfied. If both ODT features were disabled in the mode registers when self-refresh mode was entered, ODT signal can be registered low or high.
8. Wait tXS, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. A ZQCL command may also be issued after tXS).
9. Wait for tMOD, then DRAM is ready for next command.

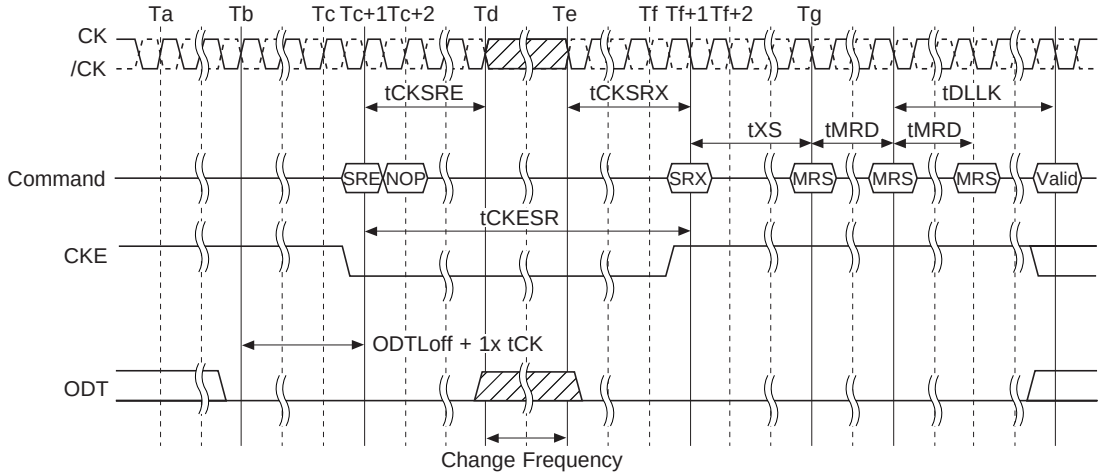


DLL Switch Sequence from DLL-on to DLL-off

DLL "off" to DLL "on" Procedure

To Switch from DLL "off" to DLL "on" (with required frequency change) during Self-Refresh:

1. Starting from Idle state (all banks pre-charged, all timings fulfilled and DRAMs On-die Termination resistors (RTT) must be in high impedance state before Self-Refresh mode is entered.)
2. Enter Self-refresh Mode, wait until tCKSRE satisfied.
3. Change frequency, in guidance with Input Clock Frequency Change during Precharge Power-Down section.
4. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
5. Starting with the self-refresh exit command, CKE must continuously be registered high until all tDLLK timing from subsequent DLL Reset command is satisfied. In addition, if any ODT features were enabled in the mode registers when Self-refresh mode was entered, the ODT signal must continuously be registered low until tDLLK timings from subsequent DLL Reset command is satisfied. If both ODT features are disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered low or high.
6. Wait tXS, then set MR1 bit A0 to "0" to enable the DLL.
7. Wait tMRD, then set MR0 bit A8 to "1" to start DLL Reset.
8. Wait tMRD, and then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. After tMOD is satisfied from any proceeding MRS command, a ZQCL command may also be issued during or after tDLLK.)
9. Wait for tMOD, and then DRAM is ready for next command (remember to wait tDLLK after DLL Reset before applying command requiring a locked DLL!). In addition, wait also for tZQoper in case a ZQCL command was issued.



DLL Switch Sequence from DLL-Off to DLL-On

Additive Latency (MR1)

A posted /CAS read or write command when issued is held for the time of the Additive Latency (AL) before it is issued inside the device. The read or write posted /CAS command may be issued with or without auto precharge.

The Read Latency (RL) is controlled by the sum of AL and the /CAS latency (CL).

The value of AL is also added to compute the overall Write Latency (WL).

MRS (1) bits A4 and A3 are used to enable Additive latency.

MRS1

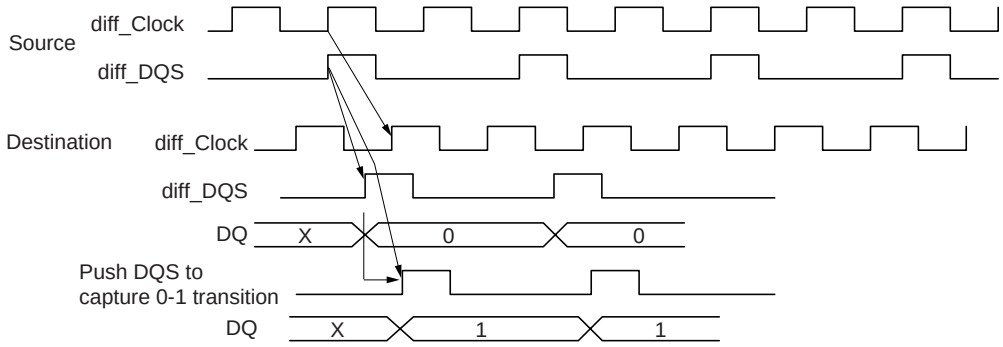
A4	A3	AL*
0	0	0 (posted CAS disabled)
0	1	CL – 1
1	0	CL – 2
1	1	Reserved

Note: AL has a value of CL – 1 or CL – 2 as per the CL value programmed in the /CAS latency MRS setting.

Write Leveling (MR1)

For better signal integrity, DDR3 memory module adopts fly by topology for the commands, addresses, control signals and clocks. The fly by topology has benefits for reducing number of stubs and their length but in other aspect, causes flight time skew between clock and strobe at every DRAM on DIMM. It makes Controller hard to maintain tDQSS, tDSS and tDSH specification. Therefore, the controller should support 'write leveling' in DDR3 SDRAM to compensate the skew.

Write leveling is a scheme to adjust DQS to CK relationship by the controller, with a simple feedback provided by the DRAM. The memory controller involved in the leveling must have adjustable delay setting on DQS to align the rising edge of DQS with that of the clock at the DRAM pin. DRAM asynchronously feeds back CK, sampled with the rising edge of DQS, through the DQ bus. The controller repeatedly delays DQS until a transition from 0 to 1 is detected. The DQS delay established through this exercise would ensure tDQSS, tDSS and tDSH specification. A conceptual timing of this scheme is shown as below.



Write leveling concept

DQS, /DQS driven by the controller during leveling mode must be terminated by the DRAM, based on the ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

One or more data bits should carry the leveling feedback to the controller across the DRAM configurations ×4, ×8 and ×16. On a ×16 device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS (diff_DQSU) to clock relationship whereas the lower data bits would indicate the lower diff_DQS (diff_DQSL) to clock relationship.

DRAM Setting for Write Leveling and DRAM Termination Function in That Mode

DRAM enters into Write leveling mode if A7 in MR1 set 1. And after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 set 0 (MR1 Setting Involved in the Leveling Procedure table).

Note that in write leveling mode, only DQS/DQS terminations are activated and deactivated via ODT pin, not like normal operation (refer to the DRAM Termination Function in The Leveling Mode table)

[MR1 Setting Involved in the Leveling Procedure]

Function	MR1 bit	Enable	Disable	Note
Write leveling enable	A7	1	0	
Output buffer mode (Qoff)	A12	0	1	1

Note: 1. Output buffer mode definition is consistent with DDR2

[DRAM Termination Function in The Leveling Mode]

ODT pin@DRAM	DQS, /DQS termination	DQs termination
De-asserted	Off	Off
Asserted	On	Off

Note: In Write Leveling Mode with its output buffer disabled (MR1 [bit7] = 1 with MR1 [bit12] = 1) all RTT_Nom settings are allowed; in Write Leveling Mode with its output buffer enabled (MR1 [bit7] = 1 with MR1 [bit12] = 0) only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.

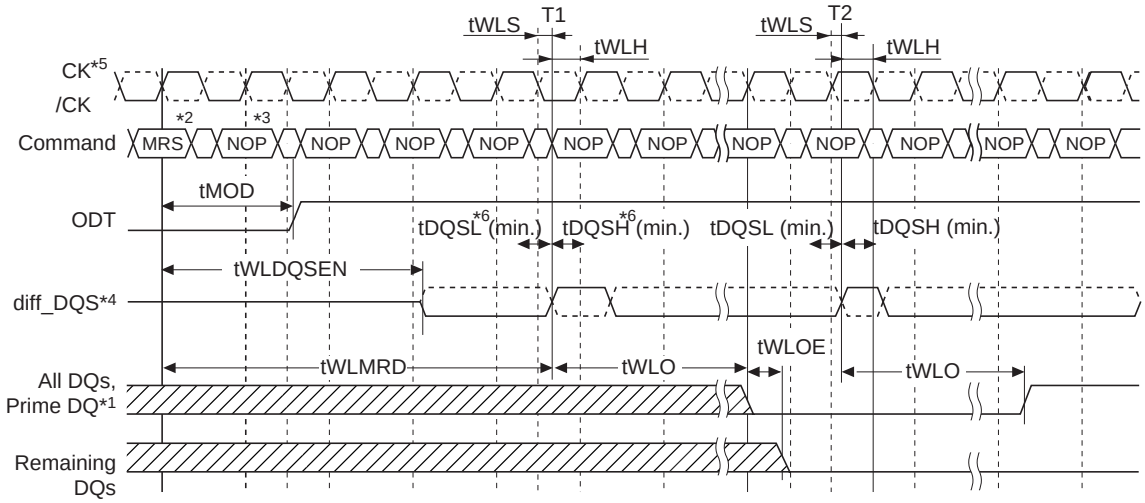
Write Leveling Procedure

Memory controller initiates Leveling mode of all DRAMs by setting bit 7 of MR1 to 1. Since the controller levelizes rank at a time, the output of other rank must be disabled by setting MR1 bit A12 to 1. Controller may assert ODT after tMOD, time at which DRAM is ready to accept the ODT signal.

Controller may drive DQS low and /DQS high after a delay of tWLDQSEN, at which time DRAM has applied on-die termination on these signals. After tWLMRD, controller provides a single DQS, /DQS edge which is used by the DRAM to sample CK driven from controller. tWLMRD timing is controller dependent.

DRAM samples CK status with rising edge of DQS and provides feedback on all the DQ bits asynchronously after tWLO timing. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits; there are no read strobes (DQS, /DQS) needed for these DQs. Controller samples incoming DQ and decides to increment or decrement DQS delay setting and launches the next DQS, /DQS pulse after some time, which is controller dependent.

Once a 0 to 1 transition is detected, the controller locks DQS delay setting and write leveling is achieved for the device. The below figure describes detailed timing diagram for overall procedure and the timing parameters are shown in below figure.



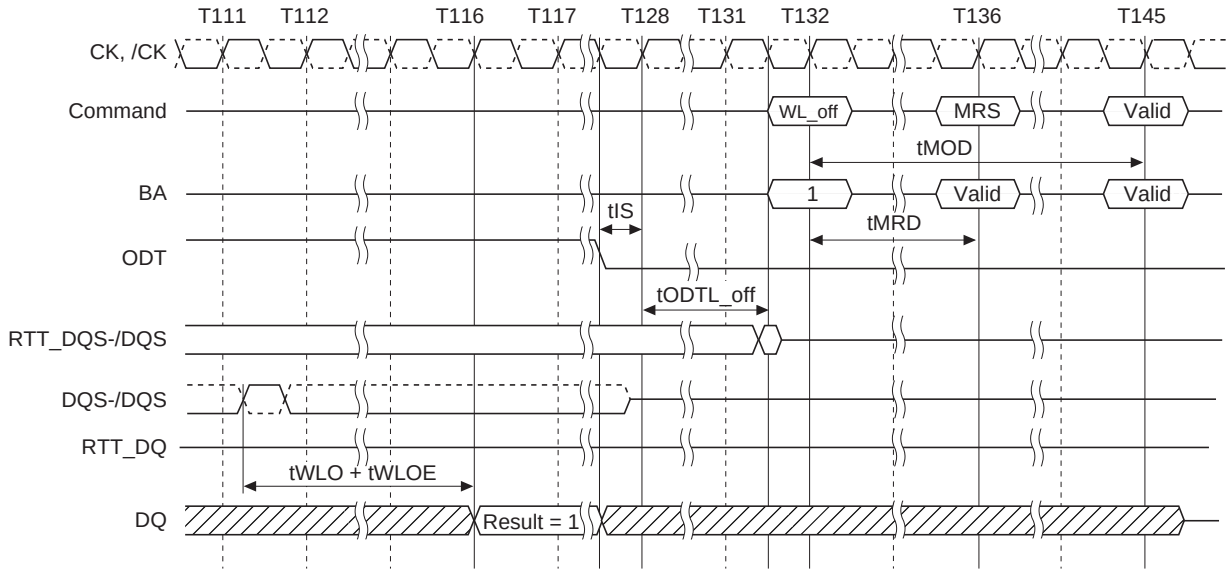
Notes:1. DRAM has the option to drive leveling feedback on a prime DQ or all DQs. If feedback is driven only on one DQ, the remaining DQs must be driven low as shown in above Figure, and maintained at this state through out the leveling procedure.
2. MRS : Load MR1 to enter write leveling mode.
3. NOP : NOP or deselec
4. diff_DQS is the differential data strobe (DQS, /DQS). Timing reference points are the zero crossing. DQS is shown with solid line, /DQS is shown with dotted line.
5. CK, /CK : CK is shown with solid dark line, where as /CK is drawn with dotted line.
6. DQS needs to fulfill minimum pulse width requirements tDQSH (min.) and tDQSL (min.) as defined for regular writes; the max pulse width is system dependent.

Timing Details Write leveling Sequence

Write Leveling Mode Exit

The following sequence describes how the Write Leveling Mode should be exited:

1. After the last rising strobe edge(see T111), stop driving the strobe signals (see ~T128). Note: From now on, DQ pins are in undefined driving mode, and will remain undefined, until tMOD after the respective MR command (T145).
2. Drive ODT pin low (tIS must be satisfied) and continue registering low (see T128).
3. After the RTT is switched off: disable Write Level Mode via MR command (see T132).
4. After tMOD is satisfied (T145), any valid commands may be registered. (MR commands may already be issued after tMRD (T136).



Timing Details Write leveling Exit

TDQS, /TDQS function (MR1)

TDQS (Termination Data Strobe) is a feature of ×8 DDR3 SDRAM that provides additional termination resistance outputs that may be useful in some system configurations.

TDQS is not supported in ×4 or ×16 configurations. When enabled via the mode register, the same termination resistance function is applied to the TDQS and /TDQS pins that are applied to the DQS and /DQS pins.

In contrast to the RDQS function of DDR2 SDRAM, TDQS provides the termination resistance function only. The data strobe function of RDQS is not provided by TDQS.

The TDQS and DM functions share the same pin. When the TDQS function is enabled via the mode register, the DM function is not supported. When the TDQS function is disabled, the DM function is provided and the /TDQS pin is not used. See Table TDQS, /TDQS function for details.

The TDQS function is available in ×8 DDR3 SDRAM only and must be disabled via the mode register A11 = 0 in MR1 for ×4 and ×16 configurations.

[TDQS, /TDQS function]

A11@MR1	TDQS enable
0	Disable
1	Enable

Notes: 1. If TDQS is enabled, the DM function is disabled.
2. When not used, TDQS function can be disabled to save termination power
3. TDQS function is only available for ×8 DRAM and must be disabled for ×4 and ×16

[Function matrix]

A11@MR1 (TDQS enable)	DM/TDQS	NU/ /TDQS
0	DM	High-Z
1	TDQS	/TDQS

Extended Temperature Usage (MR2)

[Mode Register Description]

Field	Bits	Description		Description
ASR	A6	0 1	Manual SR Reference (SRT) ASR enable (optional)	Auto self-refresh (ASR) (Optional) when enabled, DDR3 SDRAM automatically provides self-refresh power management functions for all supported operating temperature values. If not enabled, the SRT bit must be programmed to indicate TC during subsequent self-refresh operation
SRT	A7	0 1	Normal operating temperature range Extended (optional) operating temperature range	Self-Refresh Temperature (SRT) Range If ASR = 0, the SRT bit must be programmed to indicate TC during subsequent self-refresh operation If ASR = 1, SRT bit must be set to 0

Partial Array Self-Refresh (PASR)

Optional in DDR3 SDRAM: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material. If PASR (Partial Array Self-Refresh) is enabled, data located in areas of the array beyond the specified address range shown in figure of MR2 programming will be lost if Self-Refresh is entered. Data integrity will be maintained if tREFI conditions are met and no Self-Refresh command is issued.

/CAS Write Latency (CWL)

The /CAS Write Latency is defined by MR2 bits [A3, A5], as shown in figure of MR2 programming. /CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. DDR3 SDRAM does not support any half-clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + /CAS Write Latency (CWL); WL = AL + CWL. For more information on the sup-ported CWL and AL settings based on the operating clock frequency, refer to “Standard Speed Bins”. For detailed Write operation refer to “WRITE Operation”.

Auto Self-Refresh Mode - ASR Mode (optional)

DDR3 SDRAM provides an Auto Self-Refresh mode (ASR) for application ease. ASR mode is enabled by setting MR2 bit A6 = 1 and MR2 bit A7 = 0. The DRAM will manage self-refresh entry in either the Normal or Extended (optional) Temperature Ranges. In this mode, the DRAM will also manage self-refresh power consumption when the DRAM operating temperature changes, lower at low temperatures and higher at high temperatures.

If the ASR option is not supported by the DRAM, MR2 bit A6 must be set to 0.

If the ASR mode is not enabled (MR2 bit A6 = 0), the SRT bit (MR2 A7) must be manually programmed with the operating temperature range required during self-refresh operation.

Support of the ASR option does not automatically imply support of the Extended Temperature Range.

Self- Refresh Temperature Range - SRT (optional)

If ASR = 0, the Self-Refresh Temperature (SRT) Range bit must be programmed to guarantee proper self-refresh operation. If SRT = 0, then the DRAM will set an appropriate refresh rate for self-refresh operation in the Normal Temperature Range. If SRT = 1 then the DRAM will set an appropriate, potentially different, refresh rate to allow self-refresh operation in either the Normal or Extended Temperature Ranges. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details.

For parts that do not support the Extended Temperature Range, MR2 bit A7 must be set to 0 and the DRAM should not be operated outside the Normal Temperature Range.

[Self-Refresh Mode Summary]

MR2

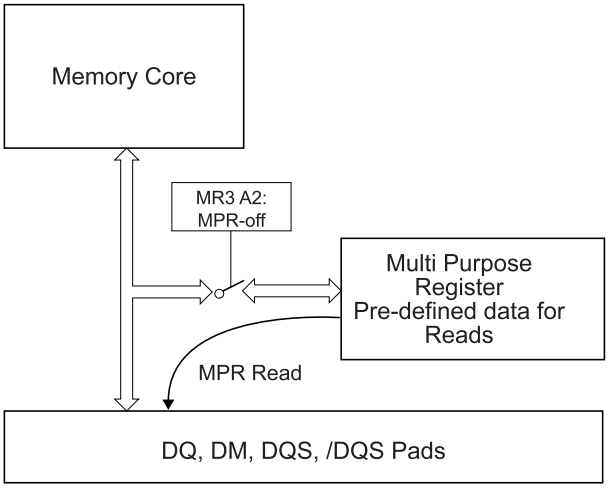
A6	A7	Self-refresh operation	Allowed operating temperature range for self-refresh mode
0	0	Self-refresh rate appropriate for the Normal Temperature Range	Normal (0°C to +85°C)
0	1	Self-refresh rate appropriate for either the Normal or Extended Temperature Ranges. The DRAM must support Extended Temperature Range. The value of the SRT bit can effect self-refresh power consumption, please refer to the Self- refresh Current for details.	Normal and Extended (0°C to +95°C)
1	0	ASR enabled (for devices supporting ASR and Normal Temperature Range). Self-refresh power consumption is temperature dependent	Normal (0°C to +85°C)
1	0	ASR enabled (for devices supporting ASR and Extended Temperature Range). Self-refresh power consumption is temperature dependent	Normal and Extended (0°C to +95°C)
1	1	Illegal	

Dynamic ODT (Rtt_WR)

DDR3 SDRAM introduces a new feature “Dynamic ODT”. In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. MR2 register locations A9 and A10 configure the Dynamic ODT settings. In Write leveling mode, only RTT_Nom is available. For details on Dynamic ODT operation, refer to “Dynamic ODT”.

Multi Purpose Register (MR3)

The Multi Purpose Register (MPR) function is used to read out predefined system timing calibration bit sequence.



- Pre-defined data pattern can be loaded into Multi Purpose Register (MPR) and read out by external read command.
- MR3 bit A2 defines dataflow from normal memory core or MPR. Once the dataflow defined, the MPR contents can be continuously read out by regular READ or READ with Auto Precharge command.

Conceptual Block Diagram of Multi Purpose Register

To enable the MPR, a mode register set (MRS) command must be issued to MR3 register with bit A2 = 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP/tRPA met). Once the MPR is enabled, any subsequent READ or READA commands will be redirected to the multi purpose register. The resulting operation when a READ or READA command is issued is defined by MR3 bits [A1: A0] when the MPR is enabled. When the MPR is enabled, only READ or READA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2=0). Power-down mode, self-refresh, and any other non-READ/READA command are not allowed during MPR enable mode. The /RESET function is supported during MPR enable mode.

[Functional Description of MR3 Bits for MPR]

MR3

A2	A [1:0]		
MPR	MPR-Loc	Function	Notes
0	Don't care (0 or 1)	Normal operation, no MPR transaction. All subsequent reads will come from DRAM array. All subsequent WRITEs will go to DRAM array.	
1	MR3 A [1:0]	Enable MPR mode, subsequent READ/READA commands defined by MR3 A [1:0] bits.	1

Note: 1. See Available Data Locations and Burst Order Bit Mapping for Multi Purpose Register table

• One bit wide logical interface via all DQ pins during READ operation

— Register Read on ×4:
DQ [0] drives information from MPR.
DQ [3:1] either drive the same information as DQ [0], or they drive 0.

— Register Read on ×8:
DQ [0] drives information from MPR.
DQ [7:1] either drive the same information as DQ [0], or they drive 0.

— Register Read on ×16:
DQL [0] and DQU [0] drive information from MPR.
DQL [7:1] and DQU [7:1] either drive the same information as DQL [0], or they drive 0.

Note: A standardization of which DQ is used by DDR3 SDRAM for MPR reads is strongly recommended to ensure functionality also for AMB2 on DDR3 FB-DIMM.

• Addressing during Multi Purpose Register reads for all MPR agents:

— BA [2:0]: don't care.

— A [1:0]: A [1:0] must be equal to '00'b. Data read burst order in nibble is fixed

— A [2]:
For BL8, A [2] must be equal to 0.
Burst order is fixed to [0,1,2,3,4,5,6,7] *1
For Burst Chop 4 cases, the burst order is switched on nibble base
A [2] = 0, Burst order: 0,1,2,3 *1
A [2] = 1, Burst order: 4,5,6,7 *1

— A [9:3]: don't care

— A10(AP): don't care

— A12(/BC): Selects burst chop mode on-the-fly, if enabled within MR0

— A11: don't care

• Regular interface functionality during register reads:

— Support two burst ordering which are switched with A2 and A [1:0] = 00.

— Support of read burst chop (MRS and on-the-fly via A12(/BC).

— All other address bits (remaining column address bits including A10, all bank address bits) will be ignored by the DDR3 SDRAM.

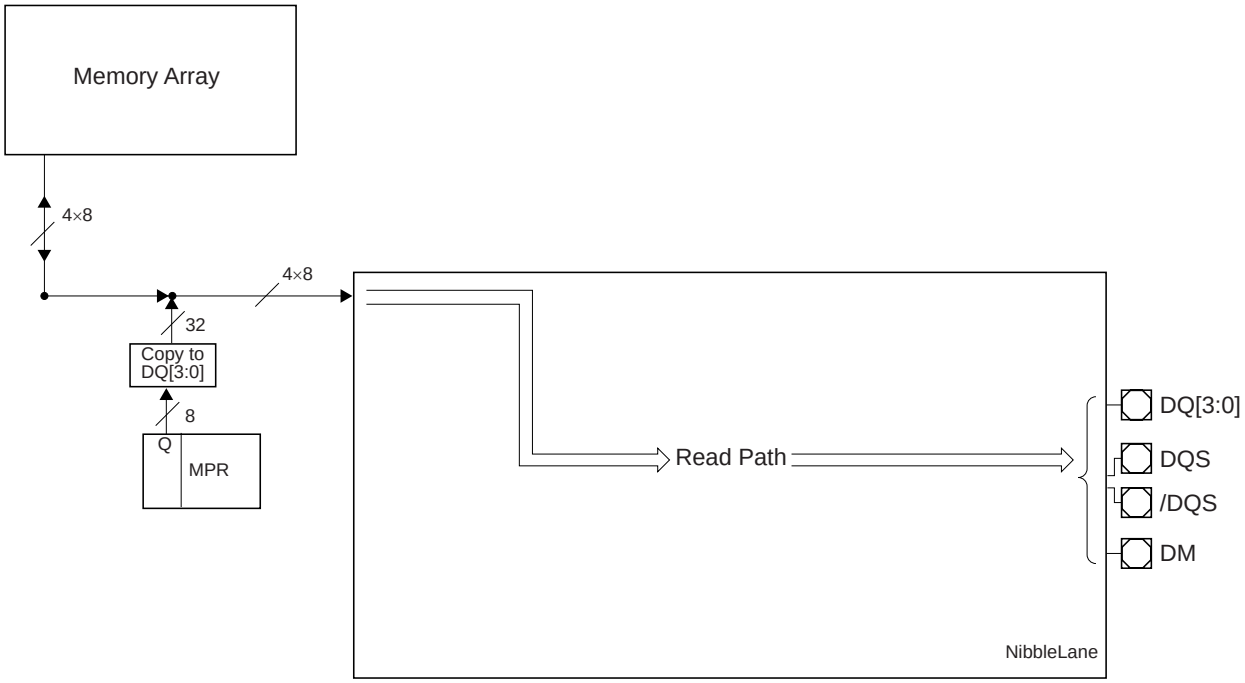
— Regular read latencies and AC timings apply.

— DLL must be locked prior to MPR Reads.

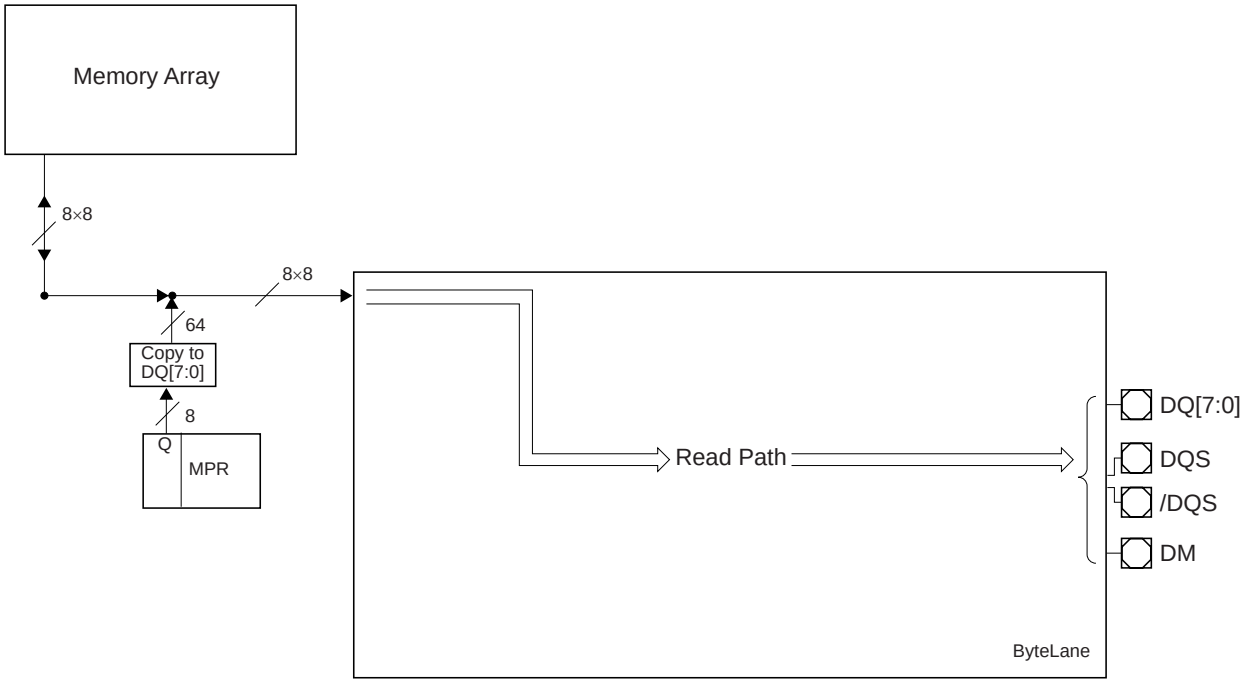
Note: Burst order bit 0 is assigned to LSB and burst order bit 7 is assigned to MSB of the selected MPR agent.

Functional Block Diagrams

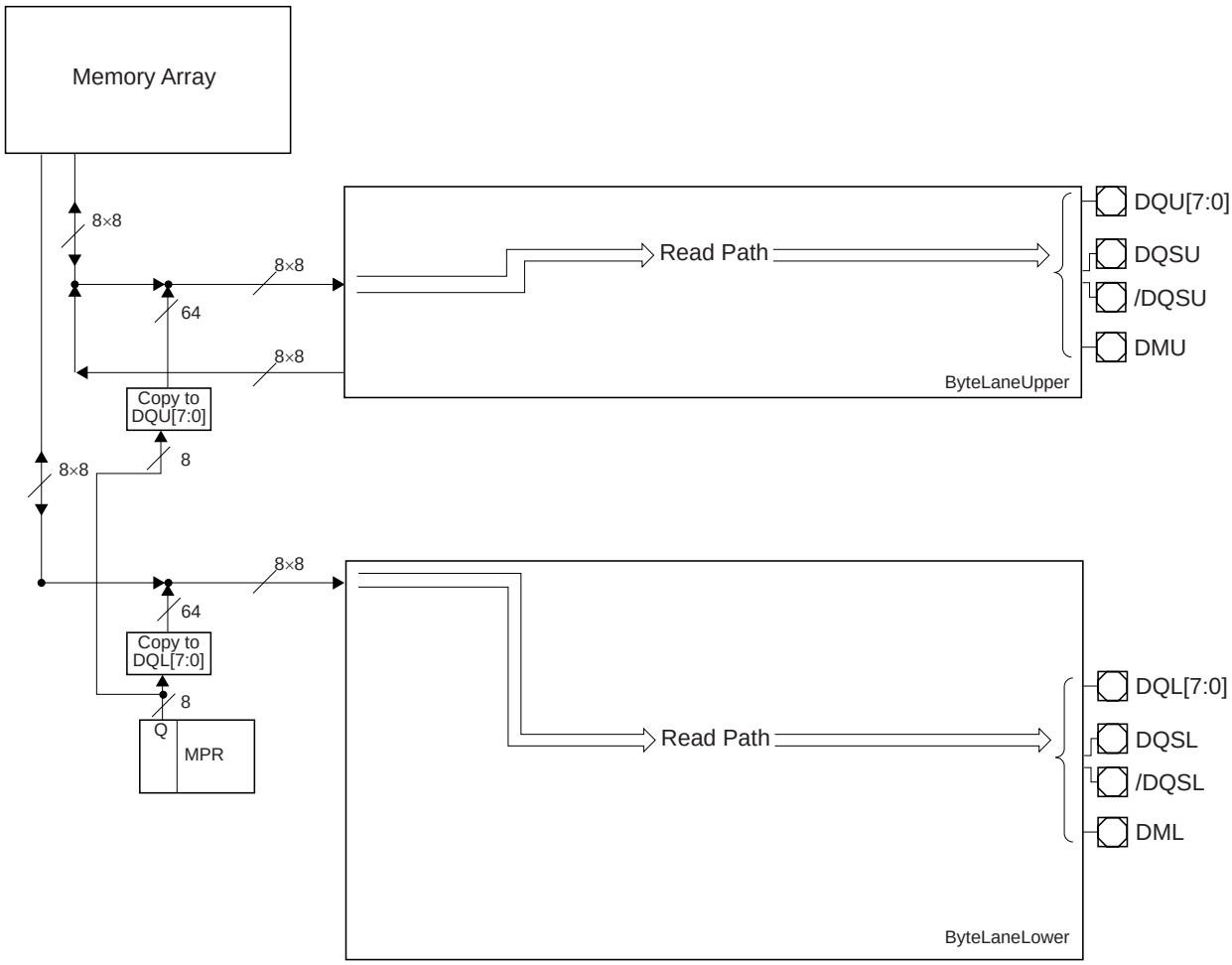
Figures below provide functional block diagrams for the multi purpose register in ×4, ×8 and ×16 DDR3 SDRAM.



Functional Block Diagram of Multi Purpose Register in ×4 DDR3 SDRAM



Functional Block Diagram of Multi Purpose Register in ×8 DDR3 SDRAM



Functional Block Diagram of Multi Purpose Register in ×16 DDR3 SDRAM

Register Address Table

The table below provides an overview of the available data locations, how they are addressed by MR3 A [1:0] during a MR0 to MR3, and how their individual bits are mapped into the burst order bits during a multi purpose register read.

[Available Data Locations and Burst Order Bit Mapping for Multi Purpose Register]

MR3 A [2]	MR3 A [1:0]	Function	Burst Length	Read Address A [2:0]	Burst Order and Data Pattern	Notes
1	00	Read predefined pattern for system calibration	BL8	000	Burst order 0,1,2,3,4,5,6,7 Pre-defined pattern [0,1,0,1,0,1,0,1]	1
			BC4	000	Burst order 0,1,2,3, Pre-defined pattern [0,1,0,1]	1
			BC4	100	Burst order 4,5,6,7 Pre-defined pattern [0,1,0,1]	1
1	01	RFU	BL8	000	Burst order 0,1,2,3,4,5,6,7	1
			BC4	000	Burst order 0,1,2,3	1
			BC4	100	Burst order 4,5,6,7	1
1	10	RFU	BL8	000	Burst order 0,1,2,3,4,5,6,7	1
			BC4	000	Burst order 0,1,2,3	1
			BC4	100	Burst order 4,5,6,7	1
1	11	RFU	BL8	000	Burst order 0,1,2,3,4,5,6,7	1
			BC4	000	Burst order 0,1,2,3,	1
			BC4	100	Burst order 4,5,6,7	1

Note: 1. Burst order bit 0 is assigned to LSB and burst order bit 7 is assigned to MSB of the selected MPR agent.

Relevant Timing Parameters

The following AC timing parameters are important for operating the Multi Purpose Register: tRP, tMRD, tMOD and tMPRR.

Besides these timings, all other timing parameters needed for proper operation of the DDR3 SDRAM need to be observed.

[MPR Recovery Time tMPRR]

Symbol	Description
tMPRR	Multi Purpose Register Recovery Time, defined between end of MPR read burst and MRS which reloads MPR or disables MPR function

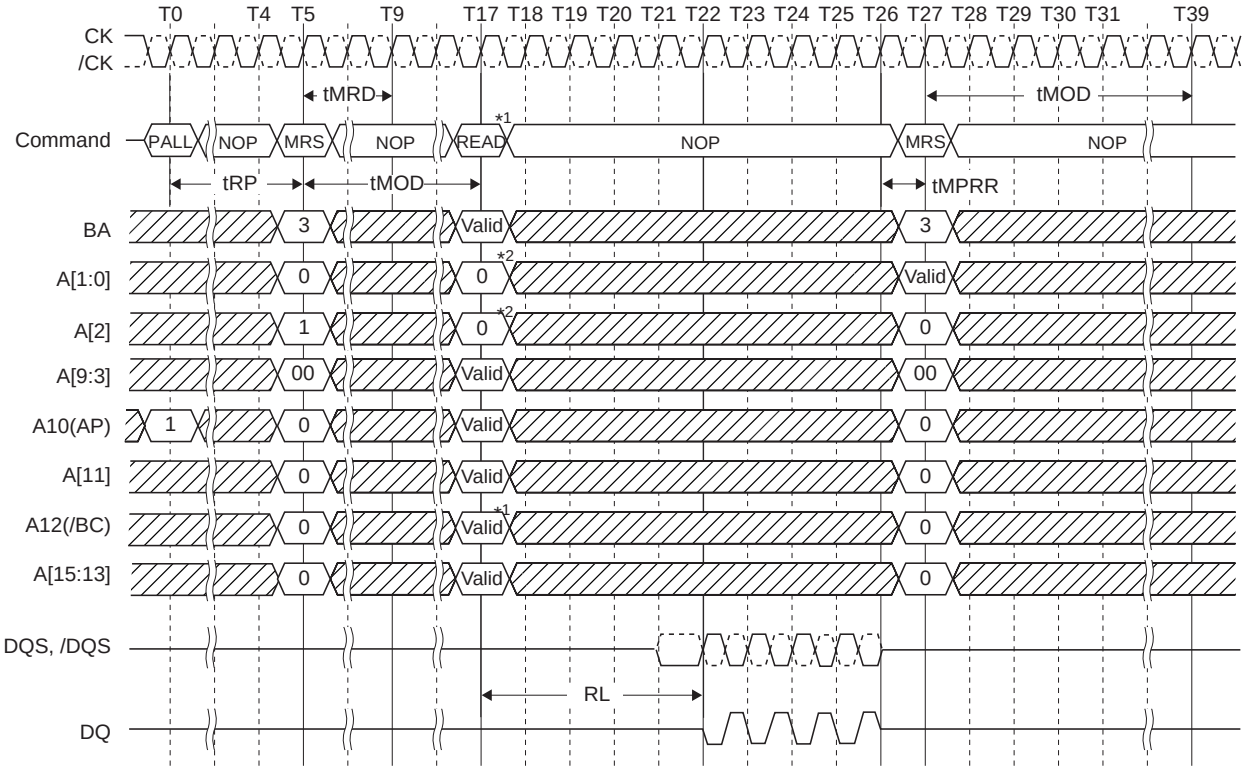
Protocol Examples

Protocol Example: Read Out Predetermined Read-Calibration Pattern

Multiple reads from Multi Purpose Register, in order to do system level read timing calibration based on predetermined and standardized pattern.

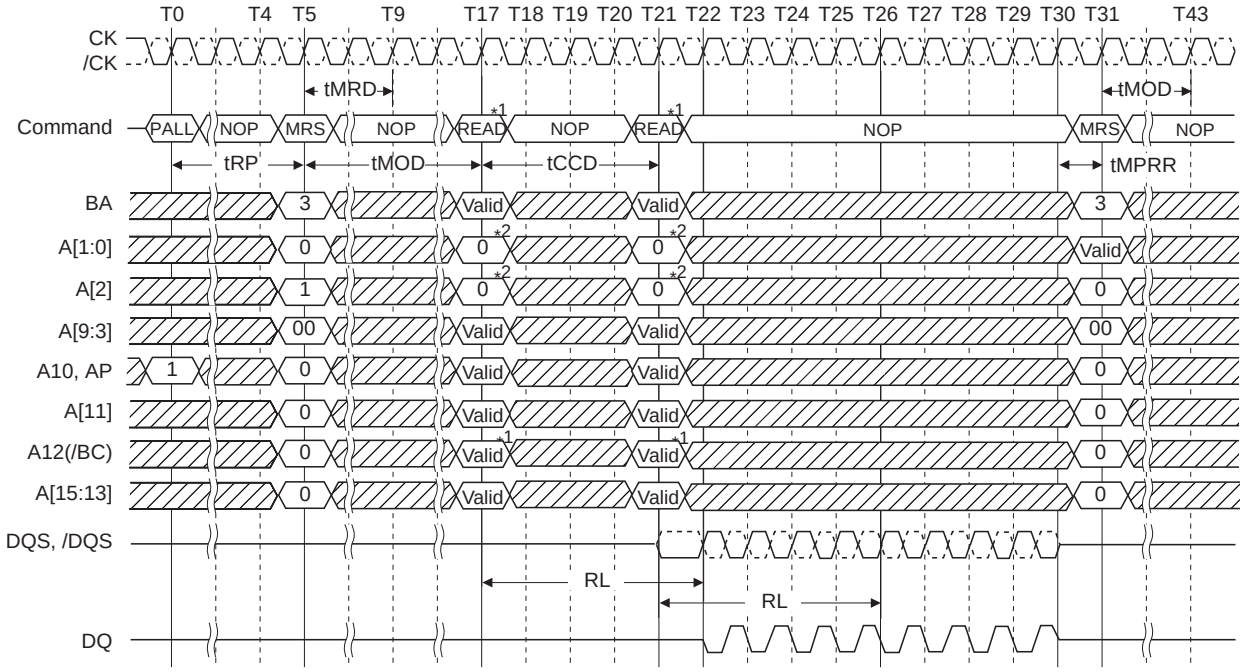
Protocol Steps:

- Precharge All
- Wait until tRP is satisfied
- MRS MR3, op-code “A2 = 1 “ and “A[1:0] = 00“
  - Redirect all subsequent reads into the Multi Purpose Register, and load Pre-defined pattern into MPR.
- Wait until tMRD and tMOD are satisfied (Multi Purpose Register is then ready to be read). During the period MR3 A2 =1, no data write operation is allowed.
- Read:
  - A [1:0] = ‘00’ (Data burst order is fixed starting at nibble, always 00 here)
  - A [2] = ‘0’ (For BL8, burst order is fixed as 0,1,2,3,4,5,6,7)
  - A12(/BC) = 1 (use regular burst length of 8)
  - All other address pins (including BA [2:0] and A10(AP)): don’t care.
- After RL = AL + CL, DRAM bursts out the predefined Read Calibration Pattern.
- Memory controller repeats these calibration reads until read data capture at memory controller is optimized.
- After end of last MPR read burst wait until tMPRR is satisfied.
- MRS MR3, op-code “A2 = 0“ and “A[1:0] = valid data but value are don’t care“
  - All subsequent read and write accesses will be regular READs and WRITEs from/to the DRAM array.
- Wait until tMRD and tMOD are satisfied
- Continue with “regular” DRAM commands, like activate a memory bank for regular read or write access,



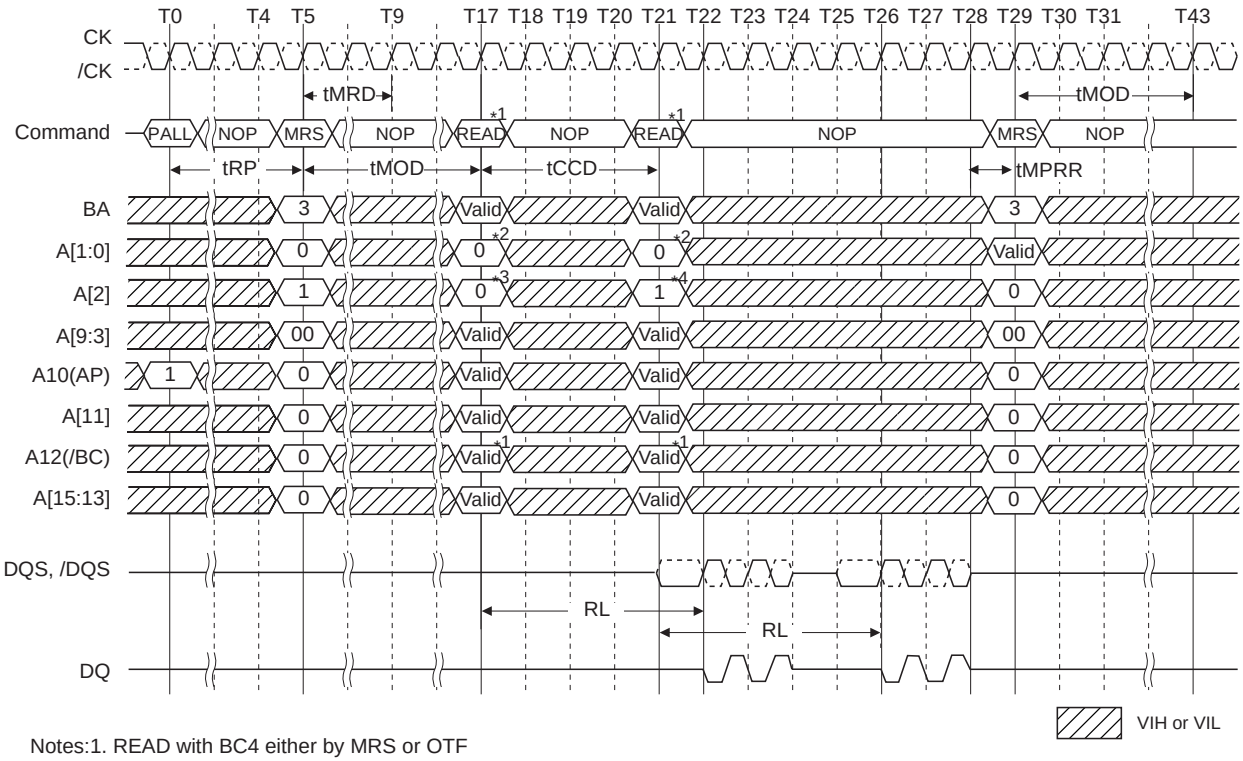
Notes: 1. READ with BL8 either by MRS or OTF
2. Memory Control must drive 0 on A[2:0]

MPR Readout of Predefined Pattern, BL8 fixed Burst Order, Single Readout



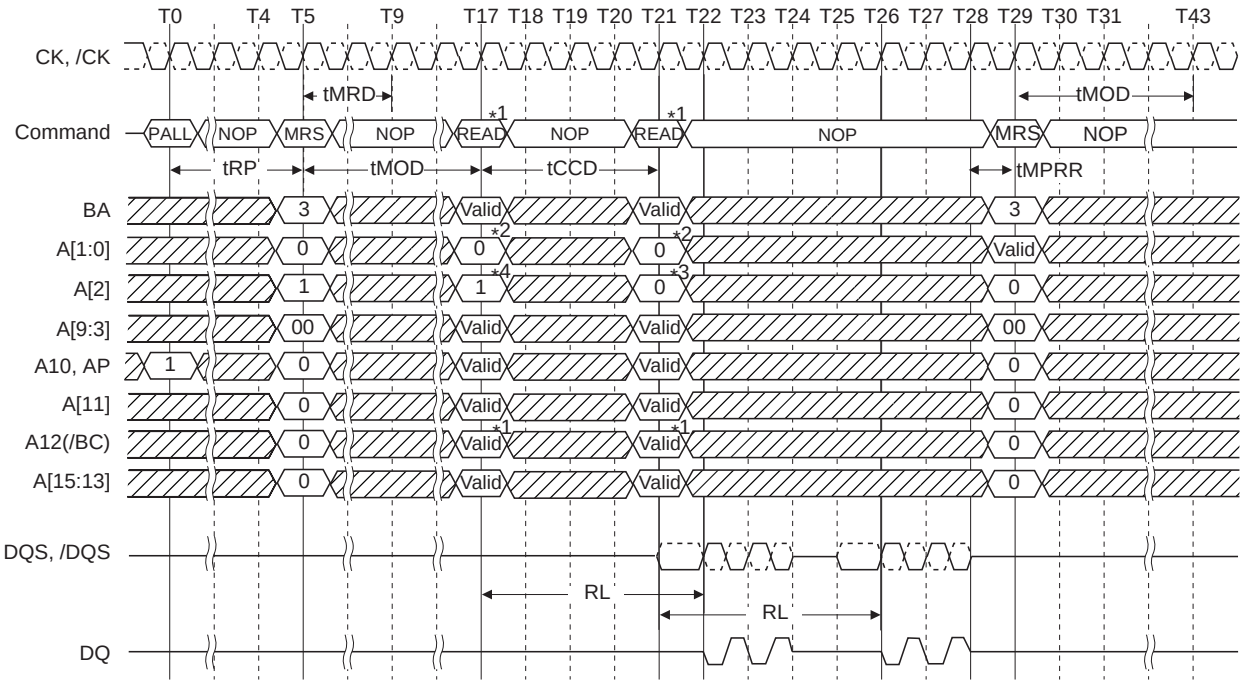
Notes: 1. READ with BL8 either by MRS or OTF
2. Memory Control must drive 0 on A[2:0]

MPR Readout of Predefined Pattern, BL8 Fixed Burst Order, Back-to-Back Readout



Notes:1. READ with BC4 either by MRS or OTF
2. Memory Control must drive 0 on A[1:0]
3. A[2] = 0 selects lower 4 nibble bits 0 ... 3
4. A[2] = 1 selects upper 4 nibble bits 4 ... 7

MPR Readout Predefined Pattern, BC4, Lower Nibble Then Upper Nibble



Notes:1. READ with BC4 either by MRS or OTF
2. Memory Control must drive 0 on A[1:0]
3. A[2] = 0 selects lower 4 nibble bits 0 ... 3
4. A[2] = 1 selects upper 4 nibble bits 4 ... 7

VIH or VIL

MPR Readout of Predefined Pattern, BC4, Upper Nibble Then Lower Nibble

Operation of the DDR3 SDRAM

Read Timing Definition

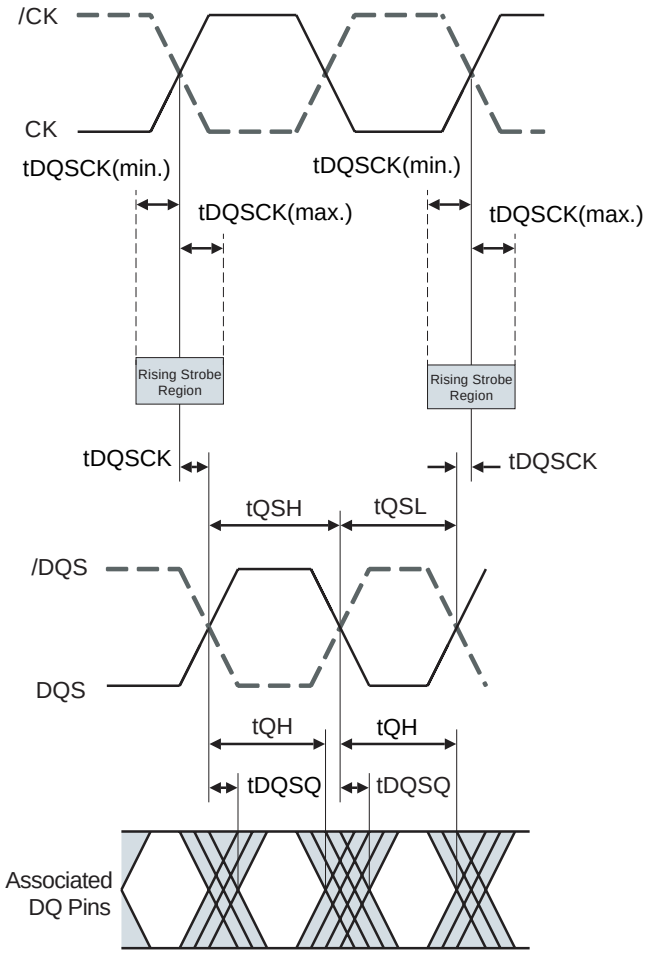
Read timing is shown in the following Figure and is applied when the DLL is enabled and locked.
Rising data strobe edge parameters:

- tDQSCK min/max describes the allowed range for a rising data strobe edge relative to CK, /CK.
- tDQSCK is the actual position of a rising strobe edge relative to CK, /CK.
- tQSH describes the DQS, /DQS differential output high time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

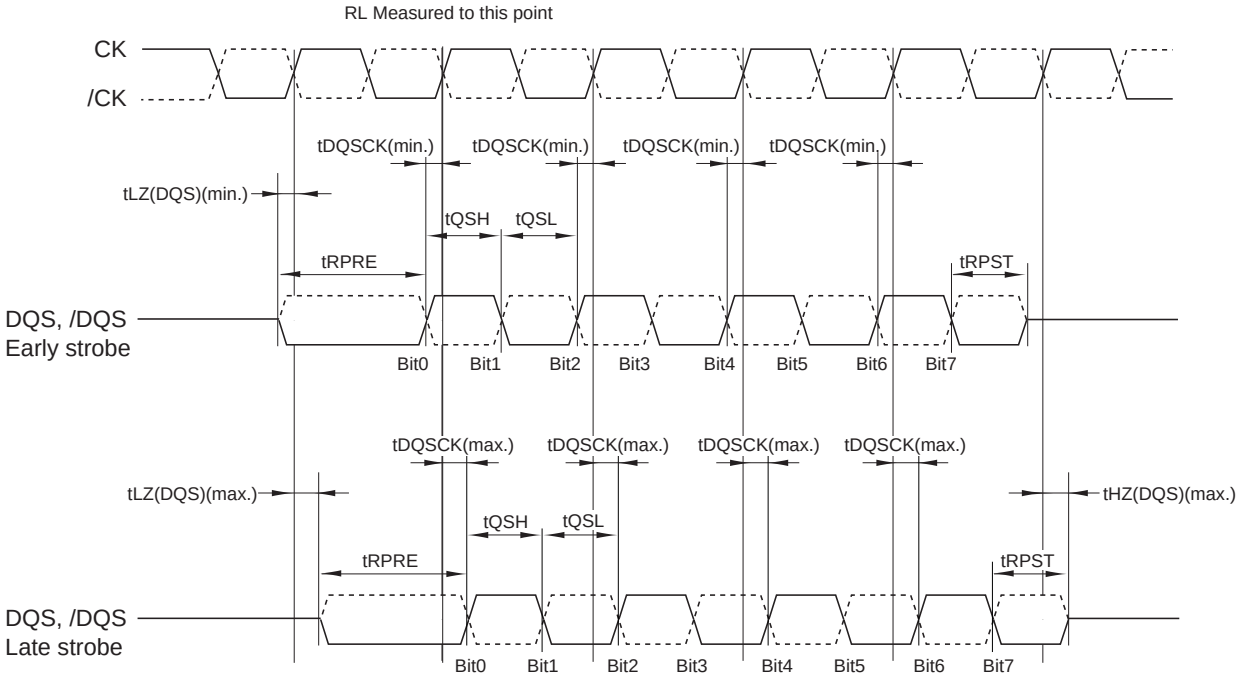
- tQSL describes the DQS, /DQS differential output low time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

tDQSQ; both rising/falling edges of DQS, no tAC defined.



READ Timing Definition

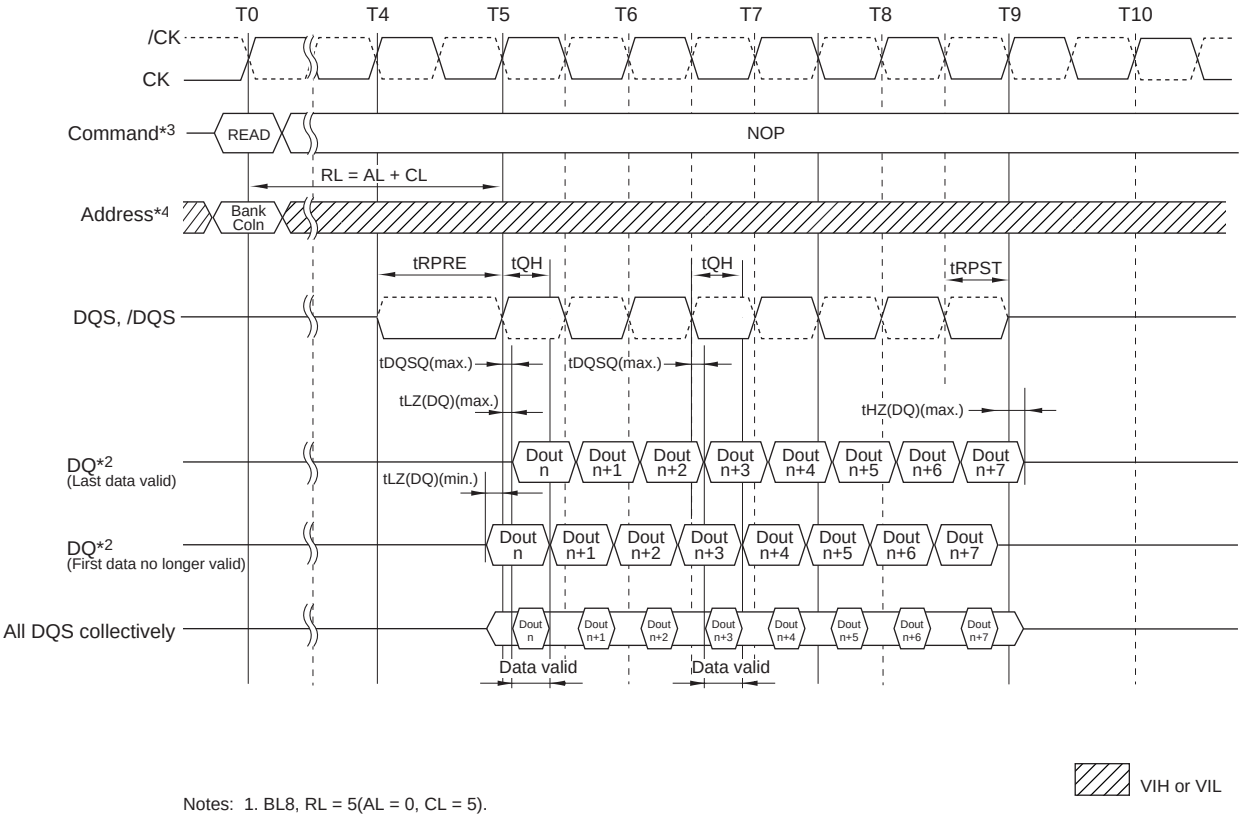
- CK, /CK crossing to DQS, /DQS crossing
- tDQSCK; rising edges only of CK and DQS
- tQSH; rising edges of DQS to falling edges of DQS
- tQSL; rising edges of / DQS to falling edges of /DQS
- tLZ (DQS), tHZ (DQS) for preamble/postamble (see tHZ (DQS), tLZ (DQS)



Notes: Within a burst, rising strobe edge is not necessarily fixed to be always at tDQSCK(min.) or tDQSCK(max.).
Instead, rising strobe edge can vary between tDQSCK(min.) or tDQSCK(max.) within a burst.
Likewise tLZ(DQS)(min.) and tHZ(DQS)(min.) are not tied to tDQSCK(min.) (early strobe case) and
tLZ(DQS)(max.) and tHZ(DQS)(max.) are not tied to tDQSCK(max.) (late strobe case).
The minimum pulse width of read preamble is defined by tRPRE(min.).
The minimum pulse width of read preamble is defined by tRPST(min.).

DDR3 Clock to Data Strobe Relationship

- DQS, /DQS crossing to Data Output
- tDQSQ; both rising/falling edges of DQS, no tAC defined



VIH or VIL

Notes: 1. BL8, RL = 5(AL = 0, CL = 5).
2. Dout n = data-out from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0 bit [A1, A0] = [0, 0] and A12 = 1 during READ command at T0.
5. Output timings are referenced to VDDQ/2, and DLL on for locking.
6. tDQSQ defines the skew between DQS, /DQS to data and does not define DQS, /DQS to clock.
7. Early data transitions may not always happen at the same DQ.
Data transitions of a DQ can vary(either early or late) within a busy.

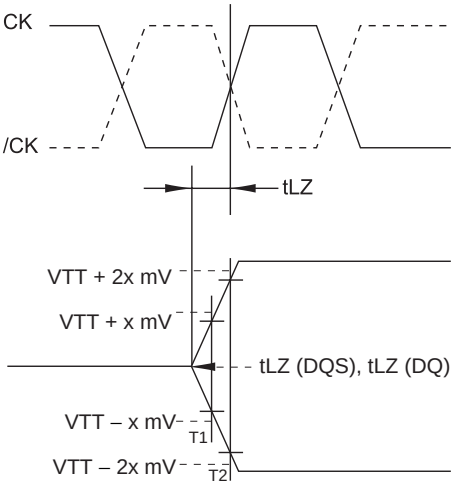
DDR3 Data Strobe to Data Relationship

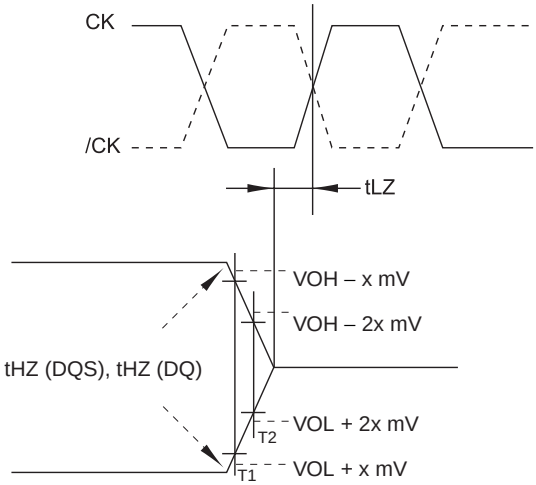
tLZ (DQS), tLZ (DQ), tHZ (DQS), tHZ (DQ) Notes

tHZ and tLZ transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ). The figure below shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as singled ended.

tLZ (DQS): CK-/CK rising crossing at RL-1
tLZ (DQ): CK-/CK rising crossing at RL

tHZ (DQS), tHZ (DQ) with BL8: CK-/CK rising crossing at RL + 4nCK
tHZ (DQS), tHZ (DQ) with BL4: CK-/CK rising crossing at RL + 2nCK





tLZ (DQS), tLZ (DQ) begin point = 2 × T1 - T2

tHZ (DQS), tHZ (DQ) end point = 2 × T1 - T2

Method for Calculating Transitions and Endpoints

Read Operation

During read or write command DDR3 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (auto precharge can be enabled or disabled).

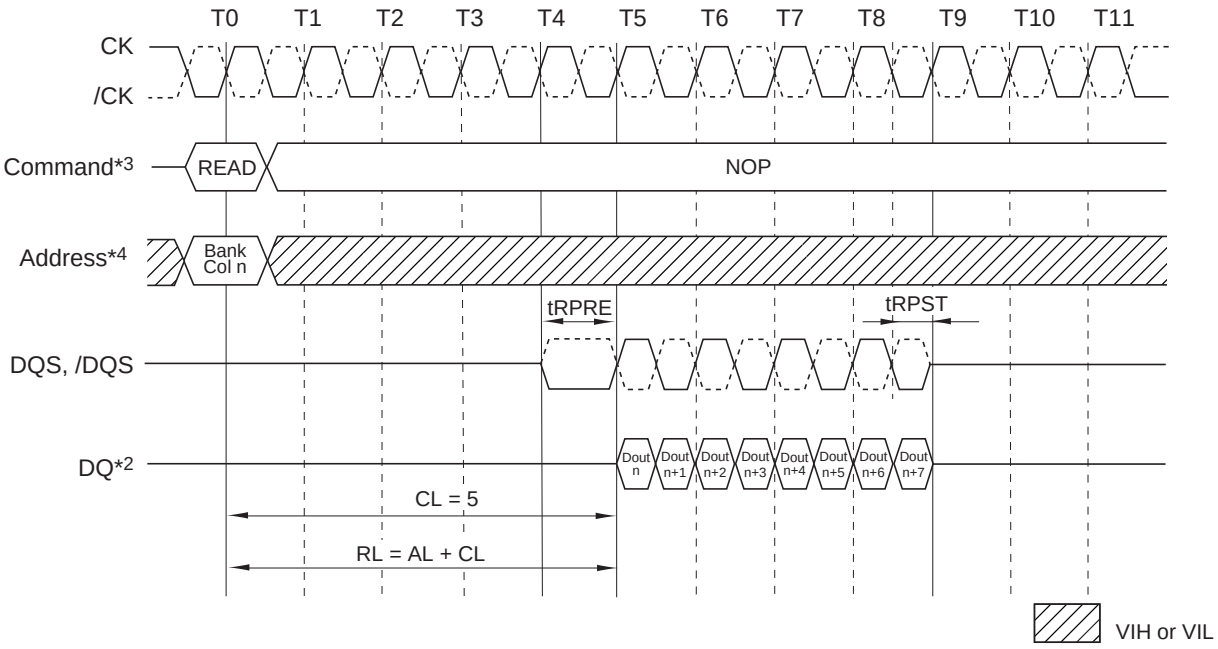
- A12 = 0, BC4 (BC4 = burst chop, tCCD = 4)
- A12 = 1, BL8

A12 will be used only for burst length control, not a column address.

The Burst Read command is initiated by having /CS and /CAS low while holding /RAS and /WE high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The delay from the start of the command to when the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The data strobe output (DQS) is driven low 1 clock cycle before valid data (DQ) is driven onto the data bus.

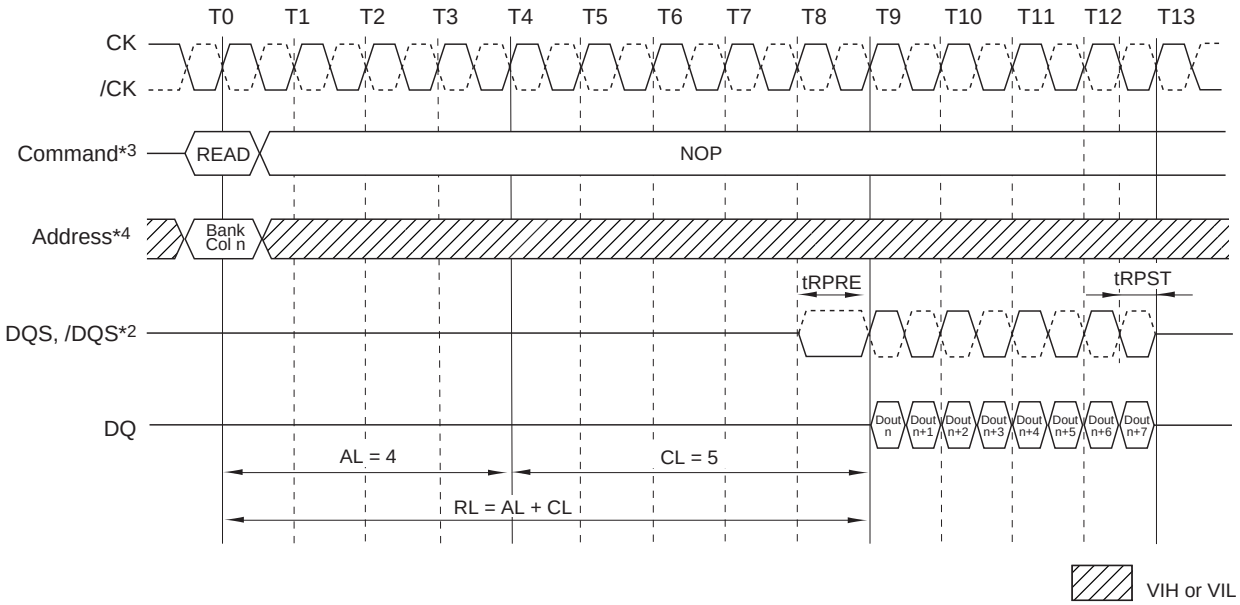
The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner.

The RL is equal to an additive latency (AL) plus /CAS latency (CL). The CL is defined by the mode register 0 (MR0), similar to the existing SDR and DDR-I SDRAMs. The AL is defined by the mode register 1



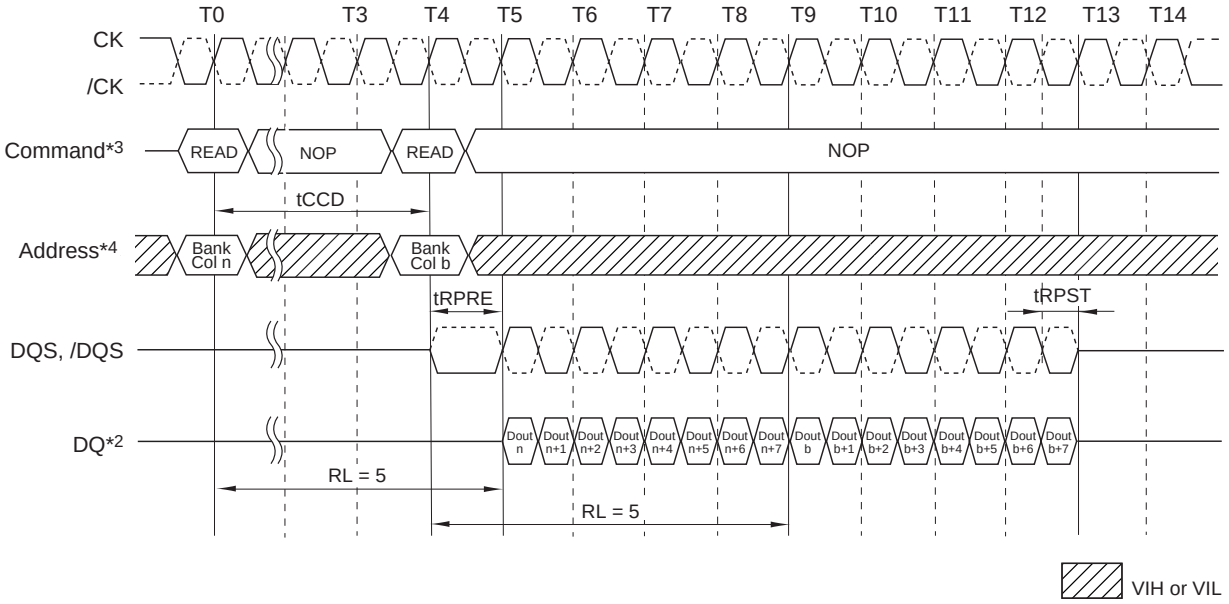
Notes: 1. BL8, AL = 0, RL = 5, CL = 5
2. Dout n = data-out from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0 bit [A1, A0] = [0, 0] or MR0 bit [A1, A0] = [0, 1] and A12 = 1 during READ command at T0.

Burst Read Operation, RL = 5



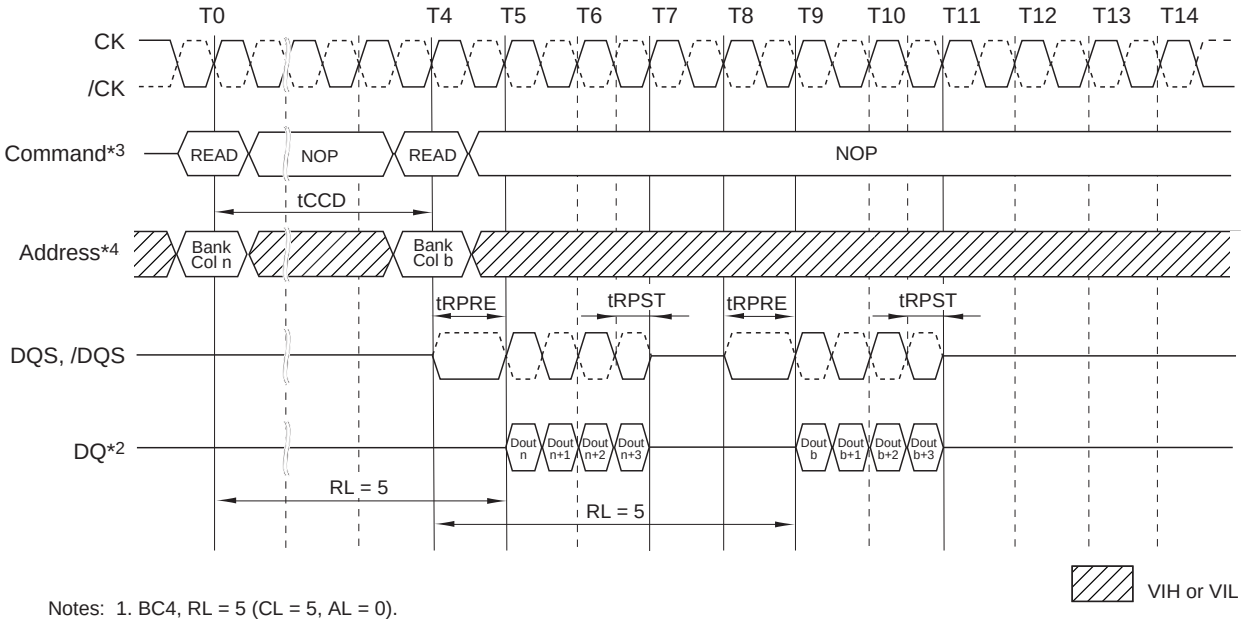
Notes: 1. BL8, RL = 9, AL = (CL – 1), CL = 5
2. Dout n = data-out from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0 bit [A1, A0] = [0, 0] or MR0 bit [A1, A0] = [0, 1] and A12 = 1 during READ command at T0.

Burst Read Operation, RL = 9



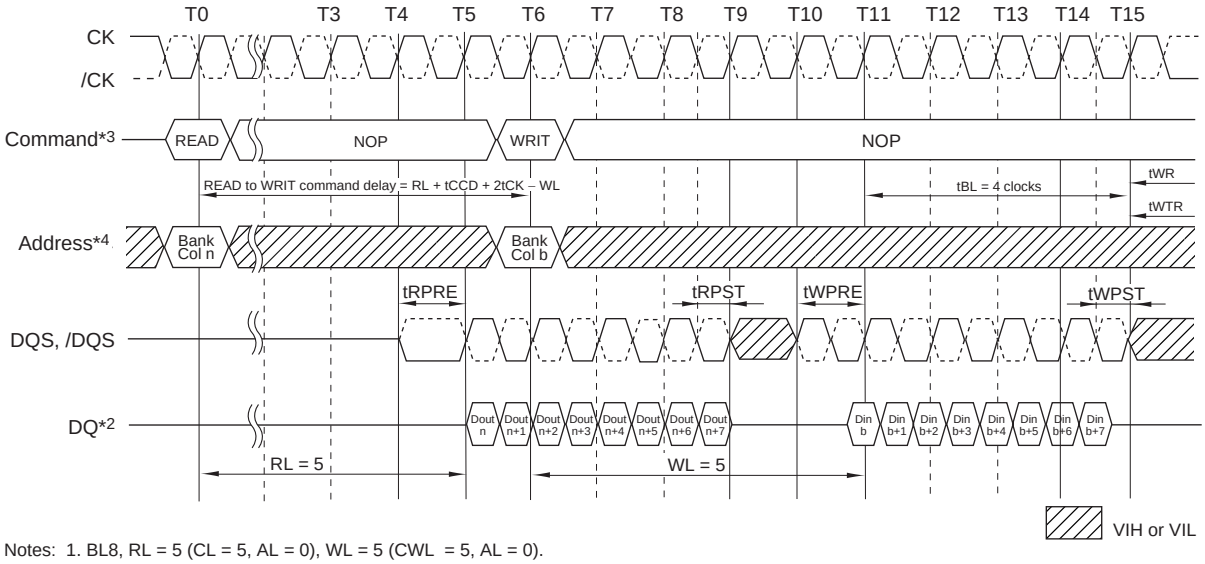
Notes: 1. BL8, RL = 5 (CL = 5, AL = 0).
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0 bit [A1, A0] = [0, 0] or MR0 bit [A1, A0] = [0, 1] and A12 = 1 during READ command at T0 and T4.

READ (BL8) to READ (BL8)



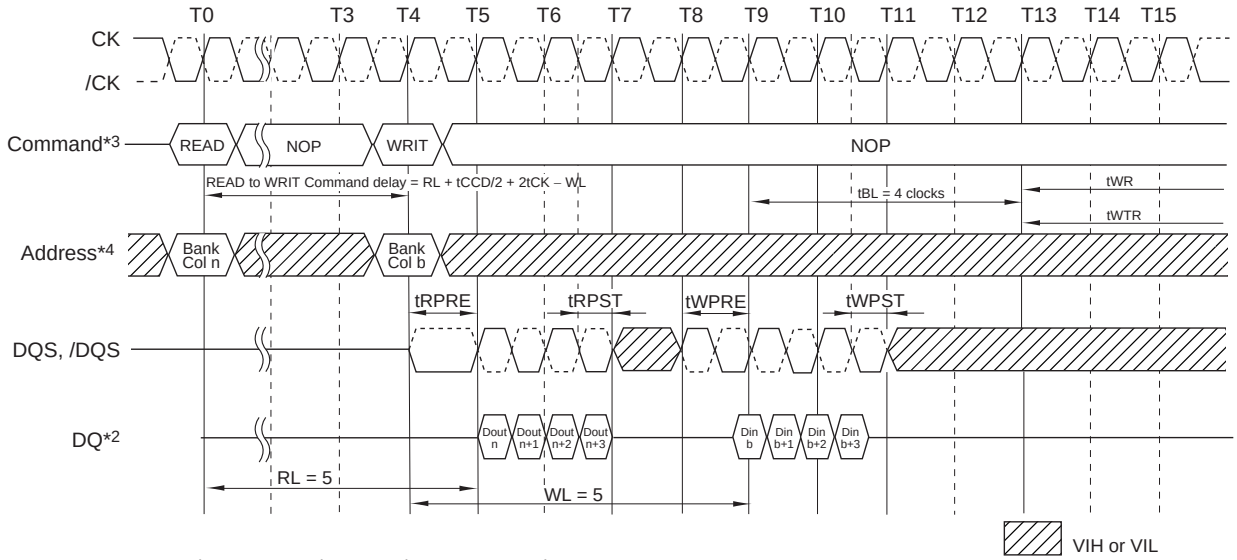
Notes: 1. BC4, RL = 5 (CL = 5, AL = 0).
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0 bit [A1, A0] = [1, 0] or MR0 bit [A1, A0] = [0, 1] and A12 = 0 during READ command at T0 and T4.

READ (BC4) to READ (BC4)



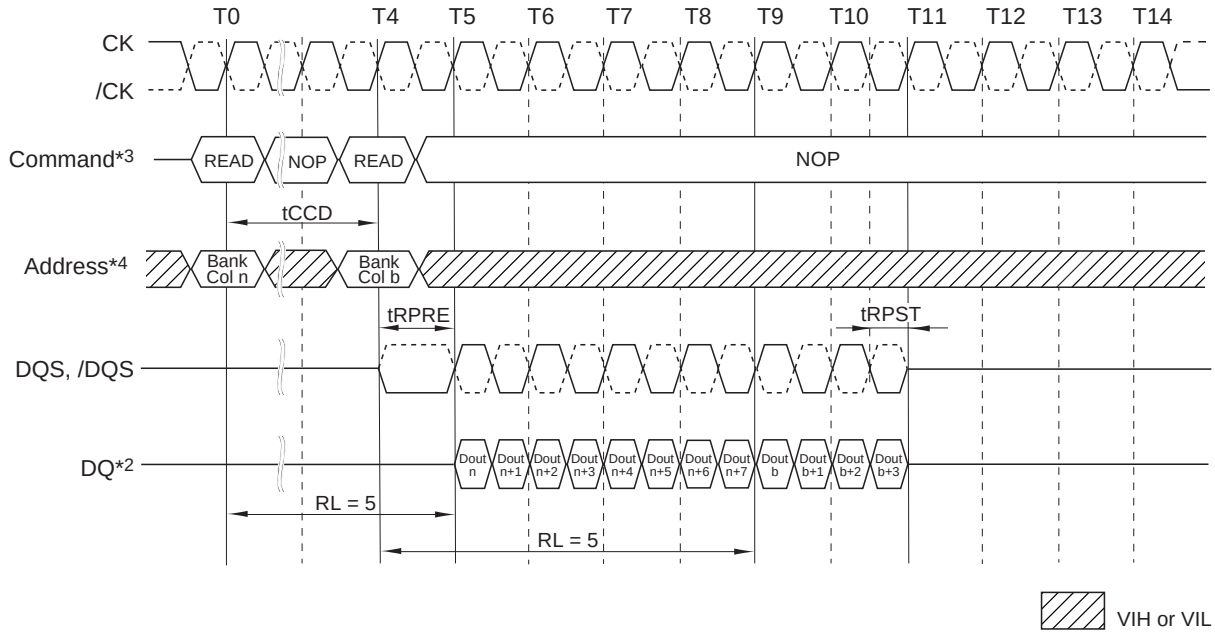
Notes: 1. BL8, RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0).
2. Dout n = data-out from column n, Din b= data-in from column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0 bit [A1, A0] = [0, 0] or MR0 bit [A1, A0] = [0, 1] and A12 = 1 during READ command at T0 and WRIT command T6.

READ (BL8) to WRITE (BL8)



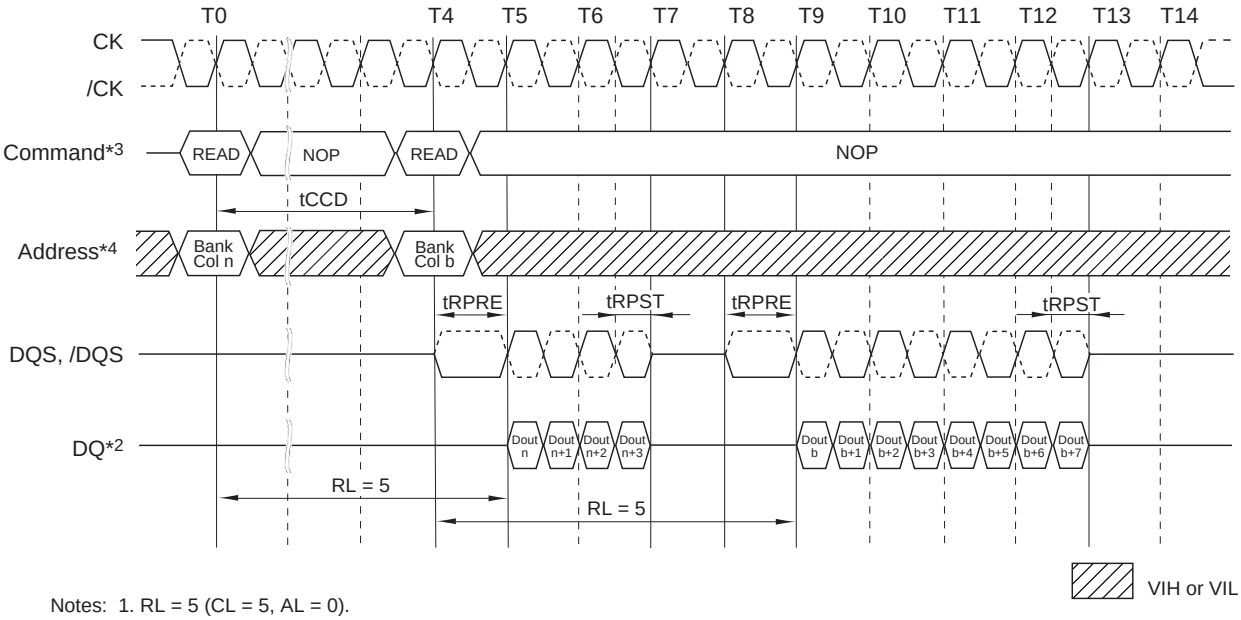
Notes: 1. BC4, RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0).
2. Dout n = data-out from column n, Din b= data-in from column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0 bit [A1, A0] = [0, 1] and A12 = 0 during READ command at T0 and WRIT command T4.

READ (BC4) to WRITE (BC4) OTF



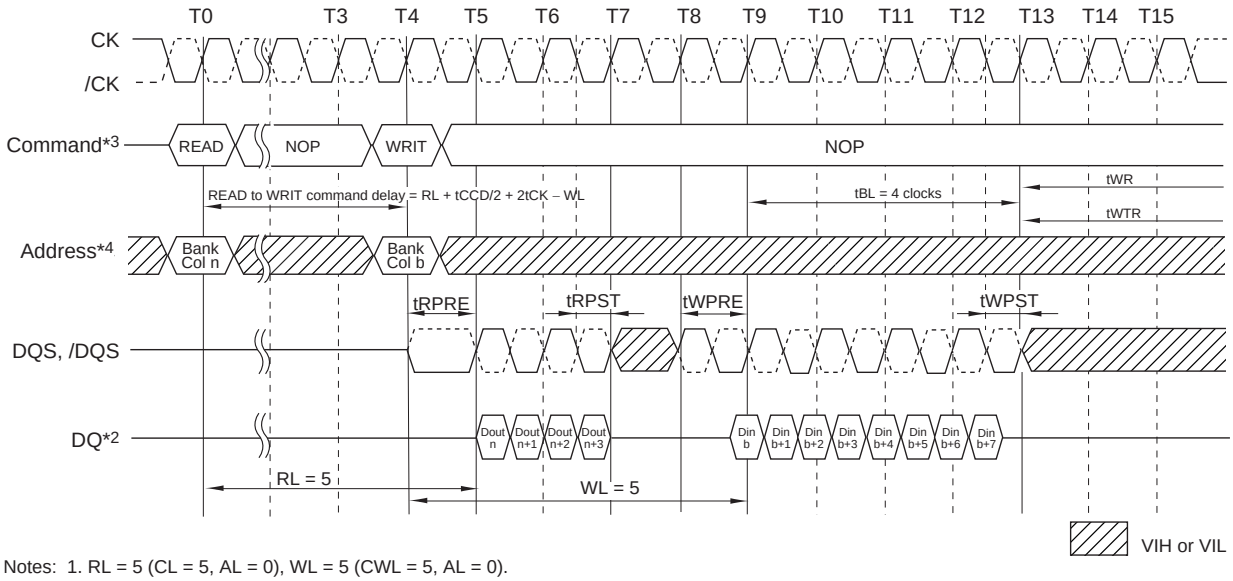
Notes: 1. RL = 5 (CL = 5, AL = 0).
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0 bit [A1, A0] = [0, 1] and A12 = 0 during READ command at T4.
BL8 setting activated by MR0 bit [A1, A0] = [0, 1] and A12 = 1 during READ command at T0.

READ (BL8) to READ (BC4) OTF



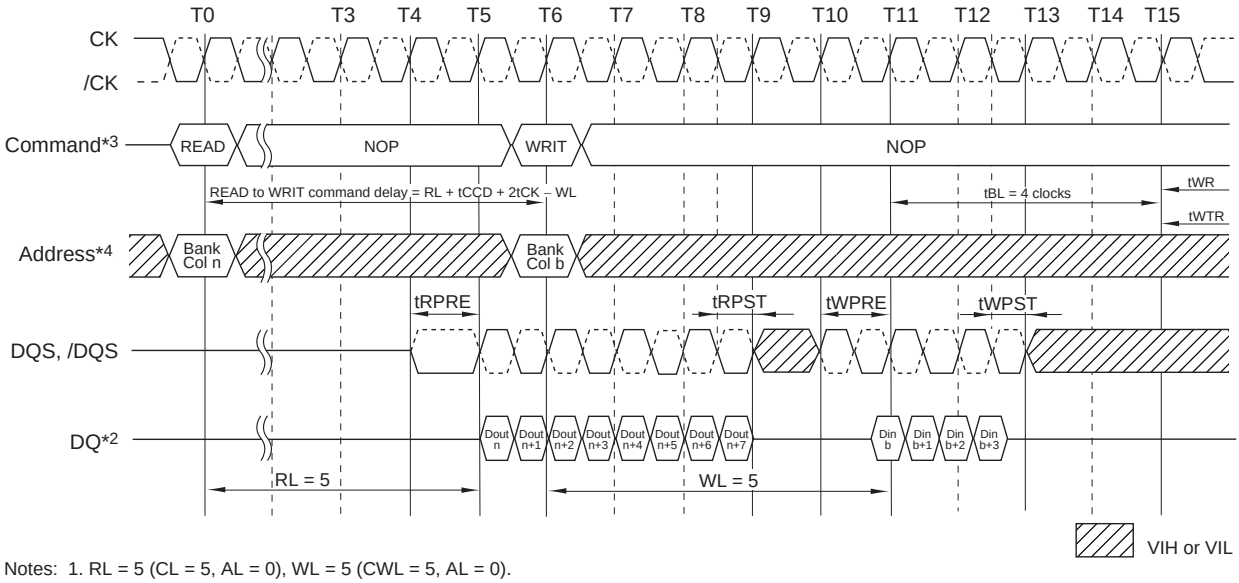
Notes: 1. RL = 5 (CL = 5, AL = 0).
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0 bit [A1, A0] = [0, 1] and A12 = 0 during READ command at T0.
BL8 setting activated by MR0 bit [A1, A0] = [0, 1] and A12 = 1 during READ command at T4.

READ (BC4) to READ (BL8) OTF



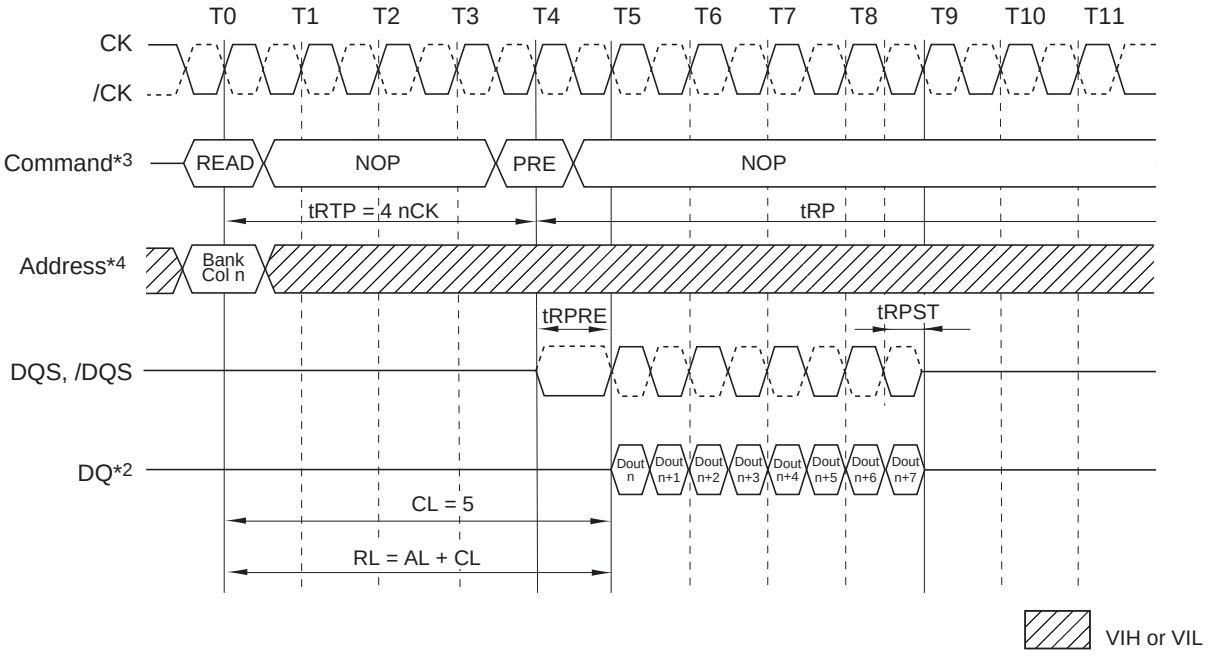
Notes: 1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0).
2. Dout n = data-out from column n , Din b= data-in from column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0 bit [A1, A0] = [0, 1] and A12 = 0 during READ command at T0.
BL8 setting activated by MR0 bit [A1, A0] = [0, 1] and A12 = 1 during WRIT command at T4.

READ (BC4) to WRITE (BL8) OTF



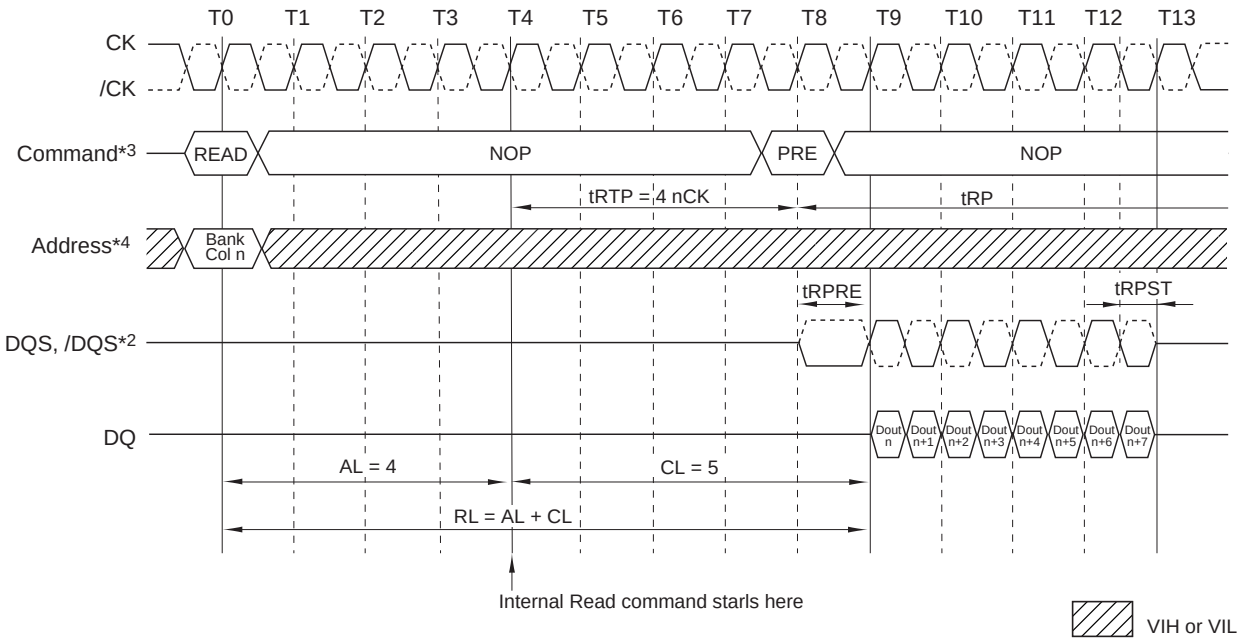
Notes: 1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0).
2. Dout n = data-out from column n, n Din b= data-in from column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0 bit [A1, A0] = [0, 1] and A12 = 1 during READ command at T0.
BC4 setting activated by MR0 bit [A1, A0] = [0, 1] and A12 = 0 during WRIT command at T6.

READ (BL8) to WRITE (BC4) OTF



Notes: 1. BL8, AL = 0, RL = 5, CL = 5
2. Dout n = data-out from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0 bit [A1, A0] = [0, 0] or MR0 bit [A1, A0] = [0, 1] and A12 = 1 during READ command at T0.

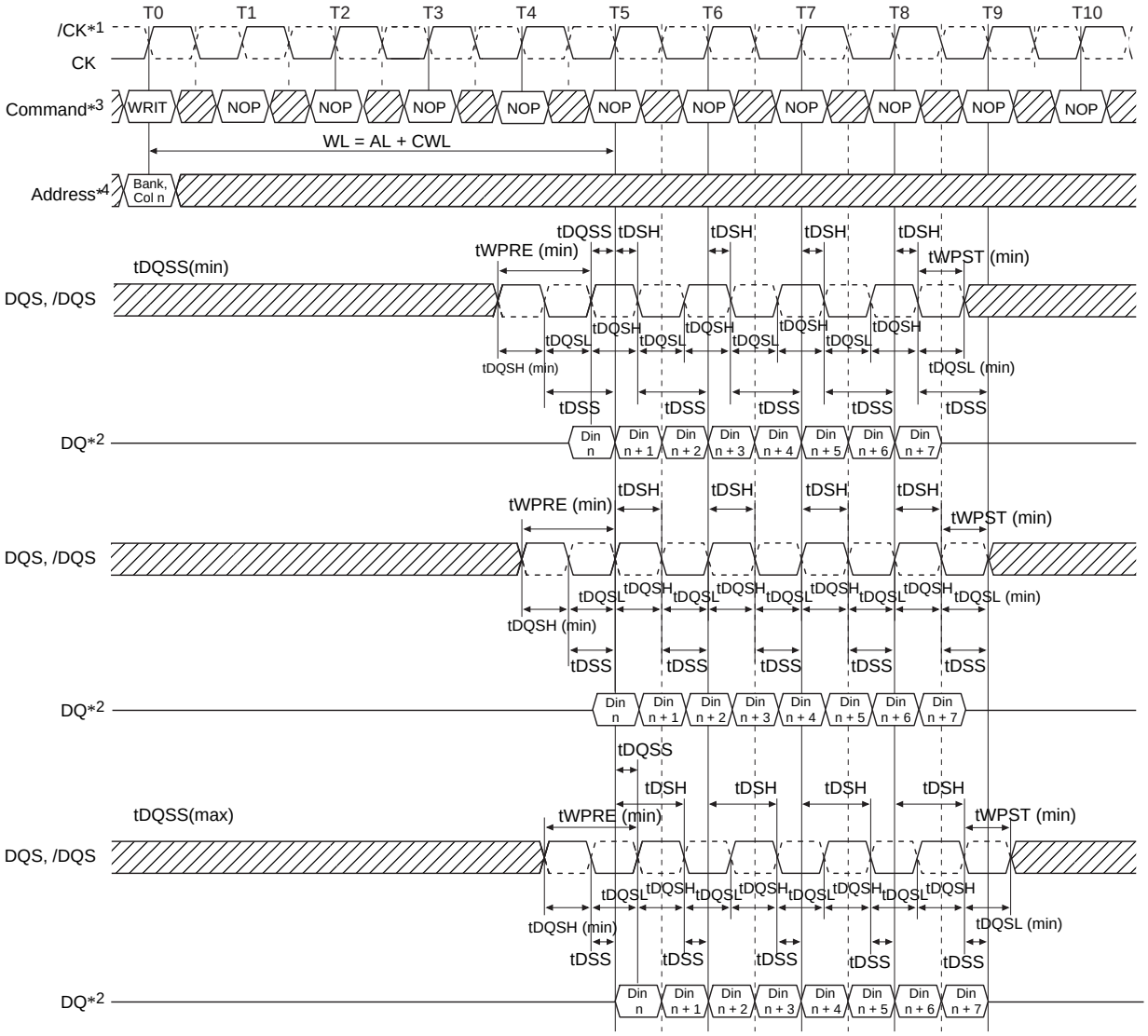
Burst Read Precharge Operation, RL = 5



Notes: 1. BL8, RL = 9, AL = (CL – 1), CL = 5
2. Dout n = data-out from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0 bit [A1, A0] = [0, 0] or MR0 bit [A1, A0] = [0, 1] and A12 = 1 during READ command at T0.

Burst Read Precharge Operation, RL = 9

Write Timing Definition



Notes: 1. BL8, WL = 5 (AL = 0, CWL = 5)

2. Din n = data-in from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0 bit [A1, A0] = [0, 0] or MR0 bit [A1, A0] = [0, 1] and A12 = 1 during WRIT command at T0.
5. tDQSS must be met at each rising clock edge.

Write Timing Definition

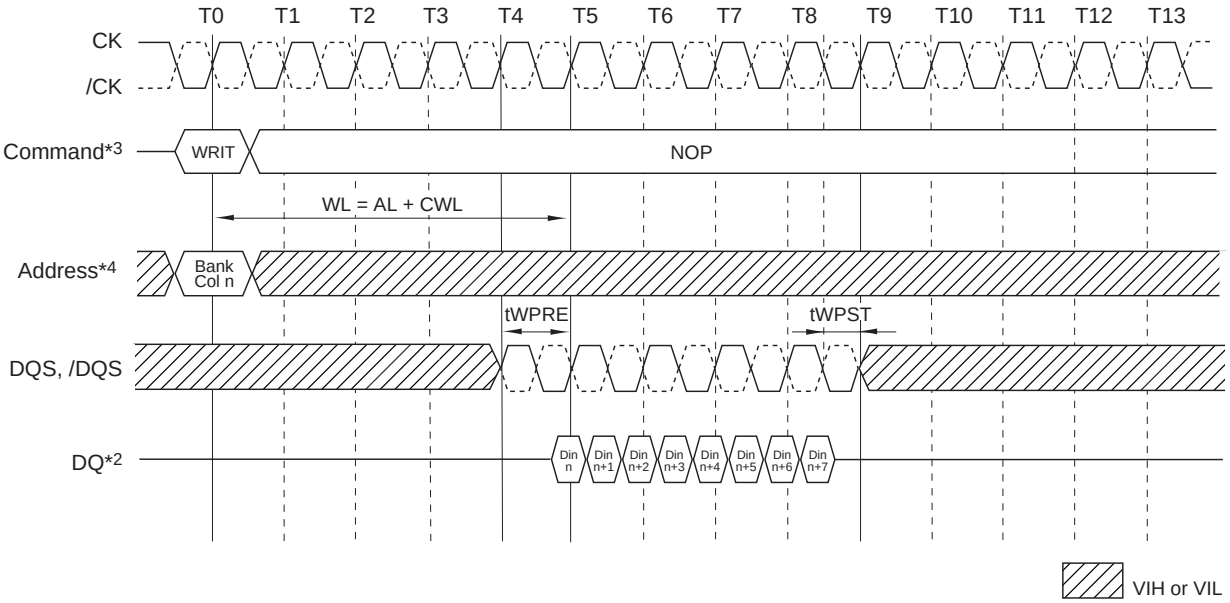
Write Operation

During read or write command DDR3 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (auto precharge can be enabled or disabled).

- A12 = 0, BC4 (BC4 = burst chop, tCCD = 4)
- A12 = 1, BL8

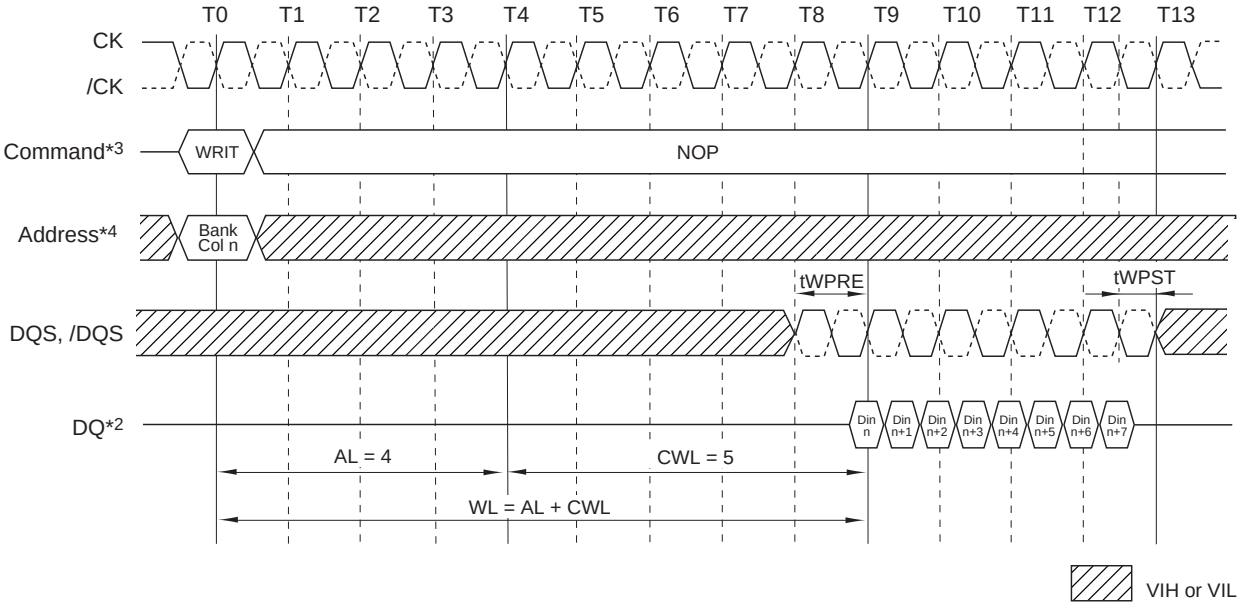
A12 will be used only for burst length control, not a column address.

The Burst Write command is initiated by having /CS, /CAS and /WE low while holding /RAS high at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is equal to (AL + CWL). A data strobe signal (DQS) should be driven low (preamble) one clock prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The tDQSS specification must be satisfied for write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length of 4 is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ Signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is the write recovery time (tWR).



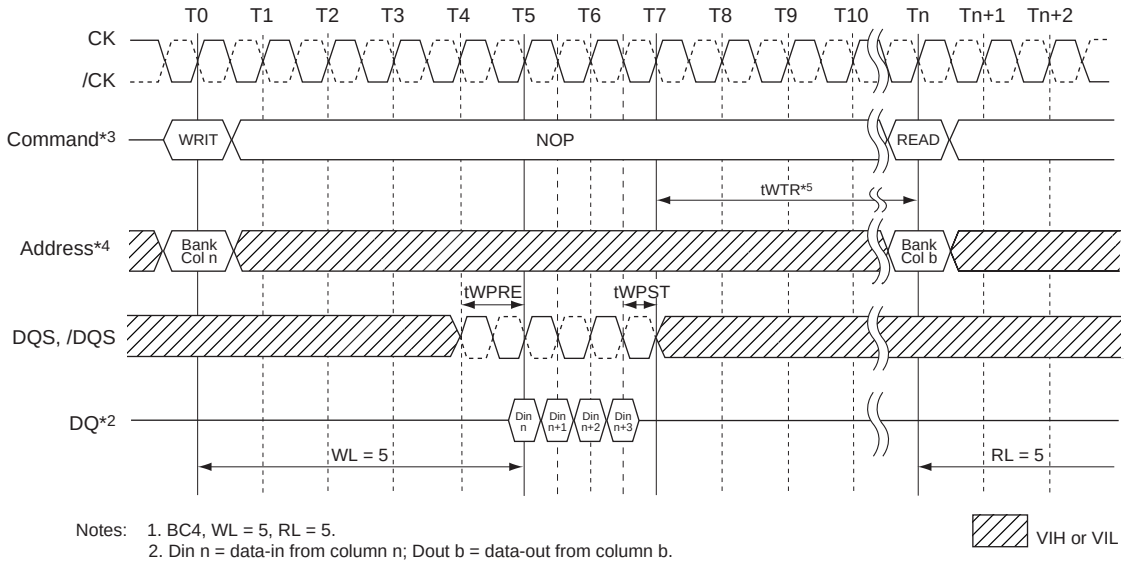
Notes: 1. BL8, WL = 5 (AL = 0, CWL = 5)
2. Din n = data-in from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0 bit [A1, A0] = [0, 0] or MR0 bit [A1, A0] = [0, 1] and A12 = 1 during WRIT command at T0.

Burst Write Operation, WL = 5



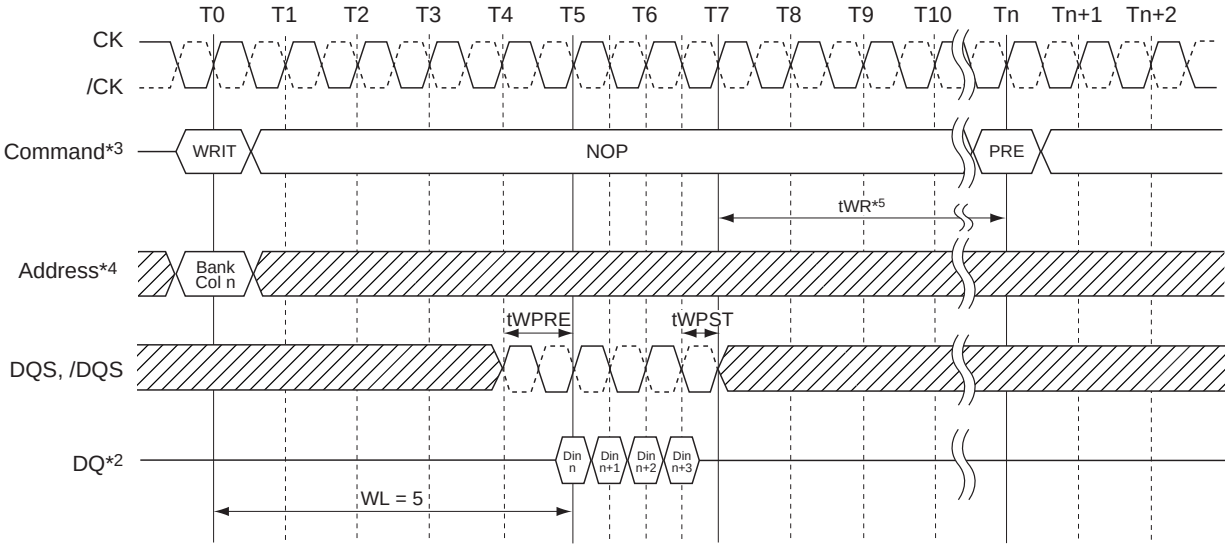
Notes: 1. BL8, WL = 9 (AL = (CL – 1), CL = 5, CWL = 5)
2. Din n = data-in from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0 bit [A1, A0] = [0, 0] or MR0 bit [A1, A0] = [0, 1] and A12 = 1 during WRITcommand at T0.

Burst Write Operation, WL = 9



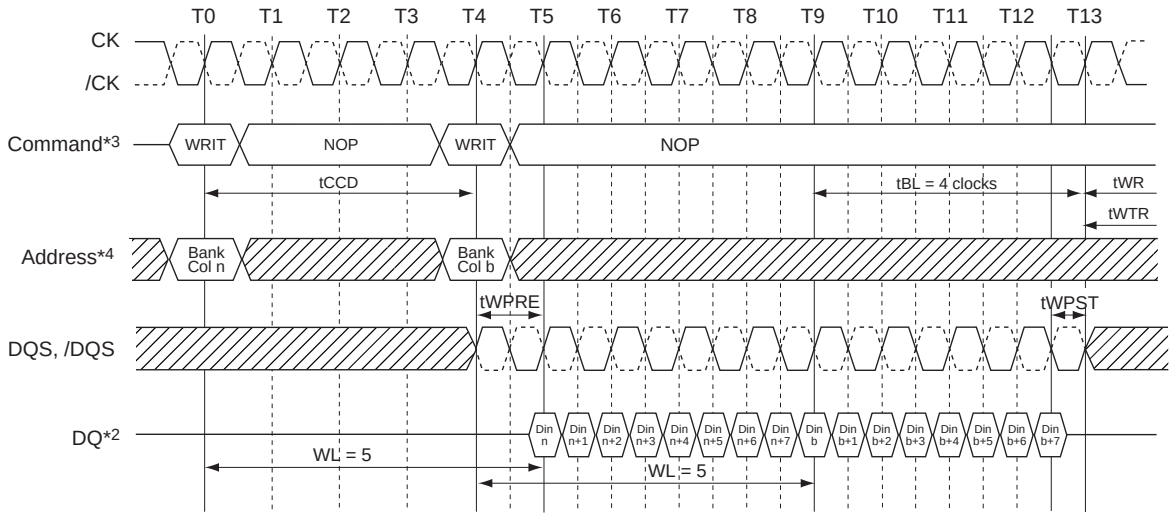
Notes: 1. BC4, WL = 5, RL = 5.
2. Din n = data-in from column n; Dout b = data-out from column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0 bit [A1, A0] = [1, 0] during WRIT command at T0 and READ command at Tn.
5. tWTR controls the write to read delay to the same device and starts with the first rising clock edge after the last write data shown at T7.

Write to Read Operation



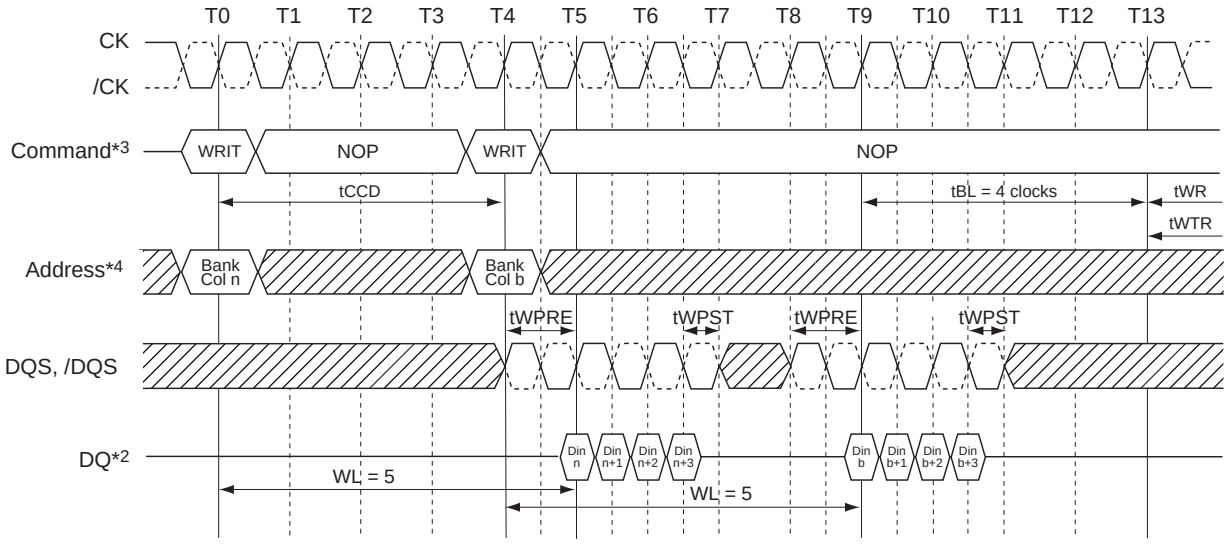
Notes: 1. BC4, WL = 5, RL = 5.
2. Din n = data-in from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0 bit [A1, A0] = [1, 0] during WRIT command at T0.
5. The write recovery time (tWR) referenced from the first rising clock edge after the last write data shown at T7.
tWR specifies the last burst write cycle until the precharge command can be issued to the same bank .

Write to Precharge Operation



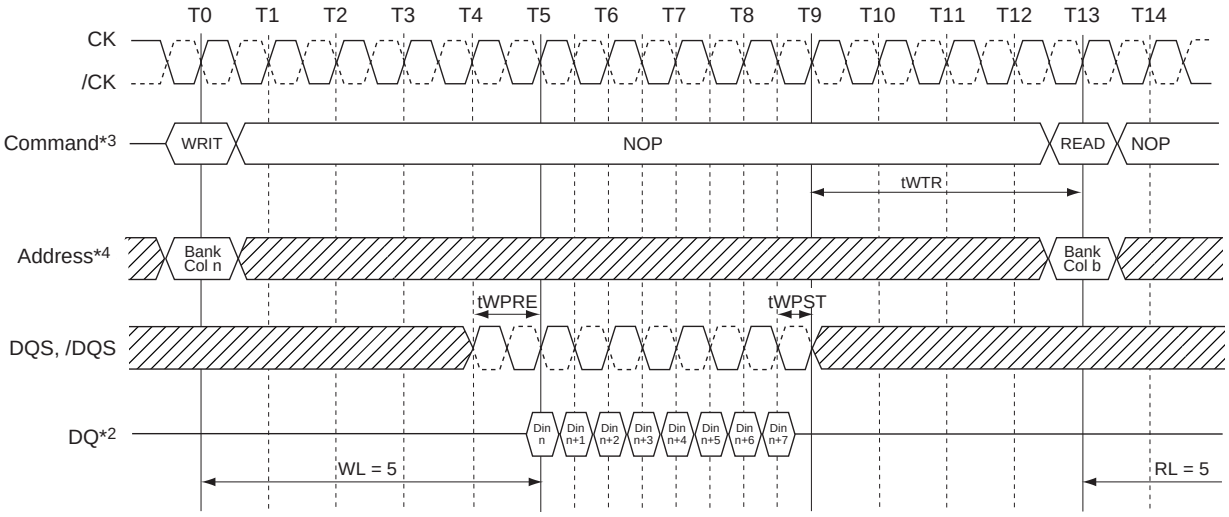
Notes: 1. BL8, WL = 5 (CWL = 5, AL = 0)
2. Din n (or b) = data-in from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0 bit [A1, A0] = [0, 0] or MR0 bit [A1, A0] = [0, 1] and A12 = 1 during WRIT command at T0 and T4.

WRITE (BL8) to WRITE (BL8)



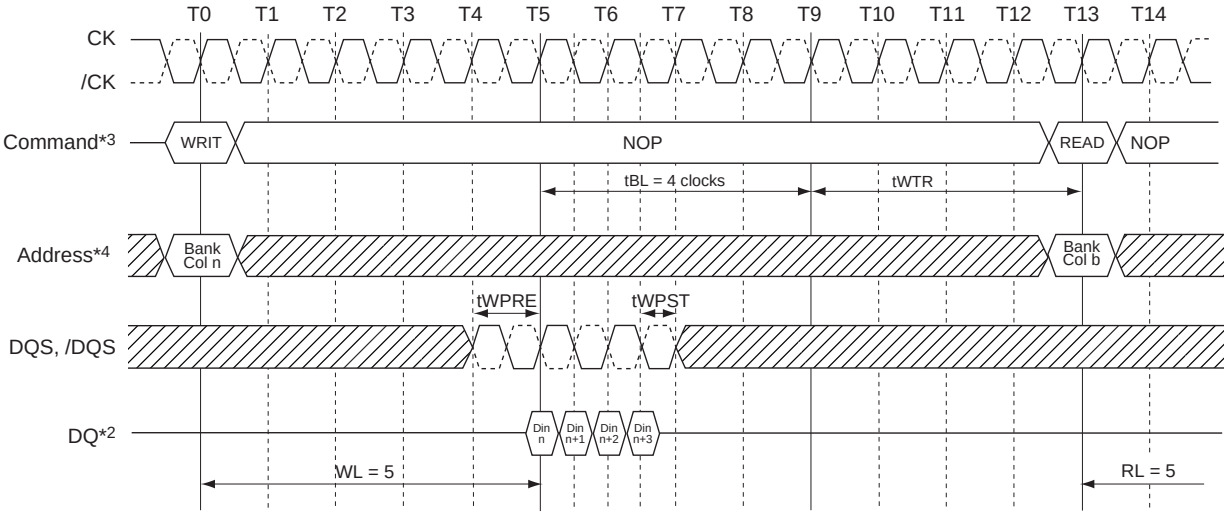
Notes: 1. BC4, WL = 5 (CWL = 5, AL = 0)
2. Din n (or b) = data-in from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0 bit [A1, A0] = [0, 1] and A12 = 0 during WRIT command at T0 and T4.

WRITE (BC4) to WRITE (BC4)



Notes: 1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. Din n = data-in from column n; DOUT b = data-out from column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0 bit [A1, A0] = [0, 0] or MR0 bit [A1, A0] = [0, 1] and A12 = 1 during WRIT command at T0.
READ command at T13 can be either BC4 or BL8 depending on MR0 bit [A1, A0] and A12 status at T13.

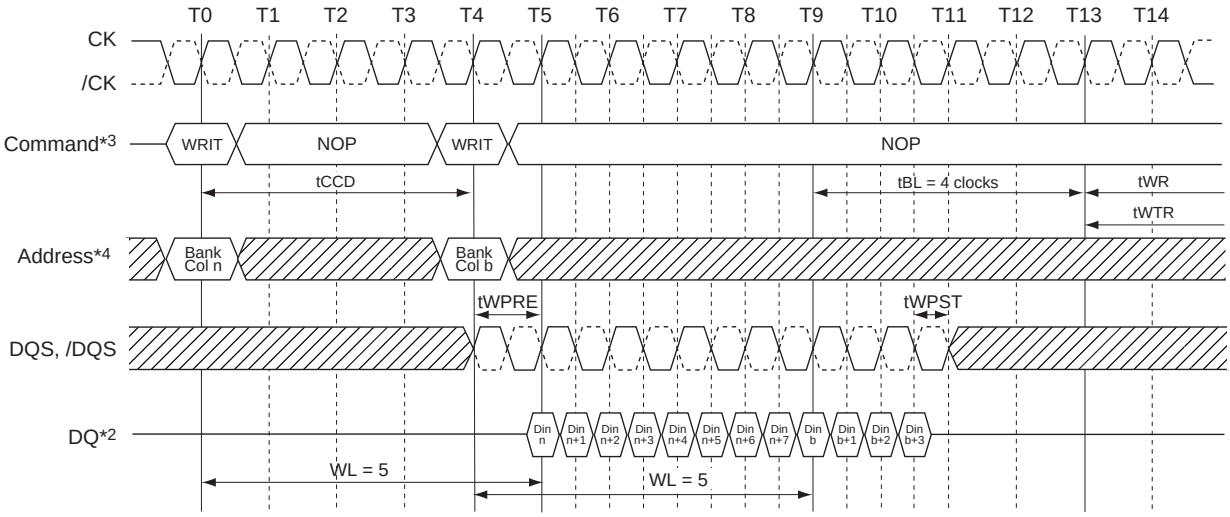
WRITE (BL8) to READ (BC4/BL8)



Notes: 1. BC4, RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. Din n = data-in from column n; Dout b = data-out from column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0 bit [A1, A0] = [0, 1] and A12 = 0 during WRIT command at T0.
READ command at T13 can be either BC4 or BL8 depending on MR0 bit [A1, A0] and A12 status at T13.

VIH or VIL

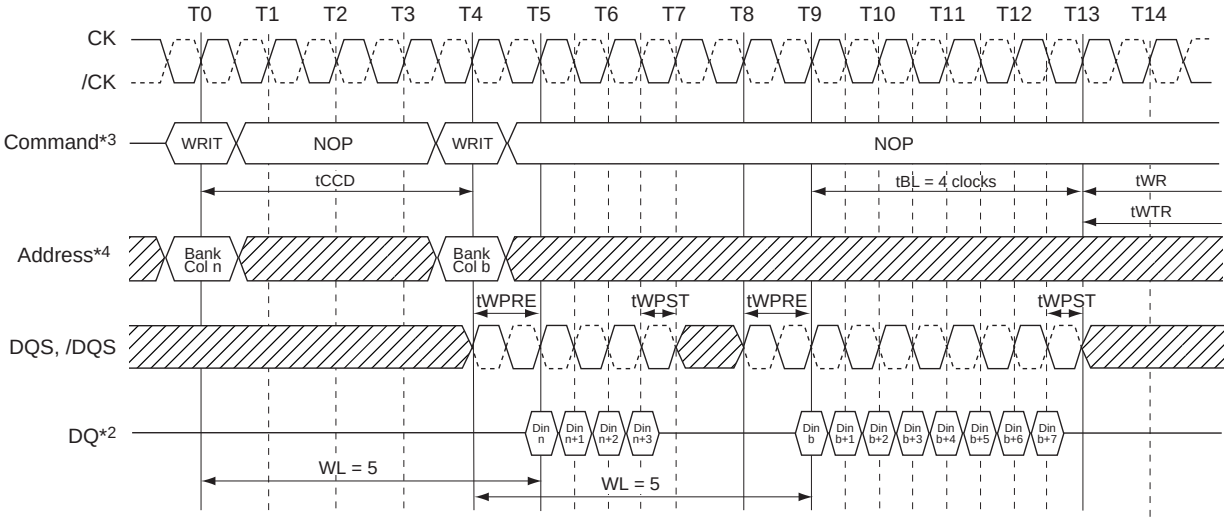
WRITE (BC4) to READ (BC4/BL8)



Notes: 1. WL = 5 (CWL = 5, AL = 0)
2. Din n (or b) = data-in from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0 bit [A1, A0] = [0, 1] and A12 = 1 during WRIT command at T0.
BC4 setting activated by MR0 bit [A1, A0] = [0, 1] and A12 = 0 during WRIT command at T4.

VIH or VIL

WRITE (BL8) to WRITE (BC4)



Notes: 1. WL = 5 (CWL = 5, AL = 0)
2. Din n (or b) = data-in from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0 bit [A1, A0] = [0, 1] and A12 = 0 during WRIT command at T0.
BL8 setting activated by MR0 bit [A1, A0] = [0, 1] and A12 = 1 during WRIT command at T4.

WRITE (BC4) to WRITE (BL8)

Write Timing Violations

Motivation

Generally, if timing parameters are violated, a complete reset/initialization procedure has to be initiated to make sure the DRAM works properly.

However it is desirable for certain minor violations, that the DRAM is guaranteed not to "hang up" and error to be limited to that particular operation.

For the following it will be assumed that there are no timing violations w.r.t to the write command itself (including ODT etc.) and that it does satisfy all timing requirements not mentioned below.

Data Setup and Hold Violations

Should the data to strobe timing requirements (tDS, tDH) be violated, for any of the strobe edges associated with a write burst, then wrong data might be written to the memory location addressed with this write command.

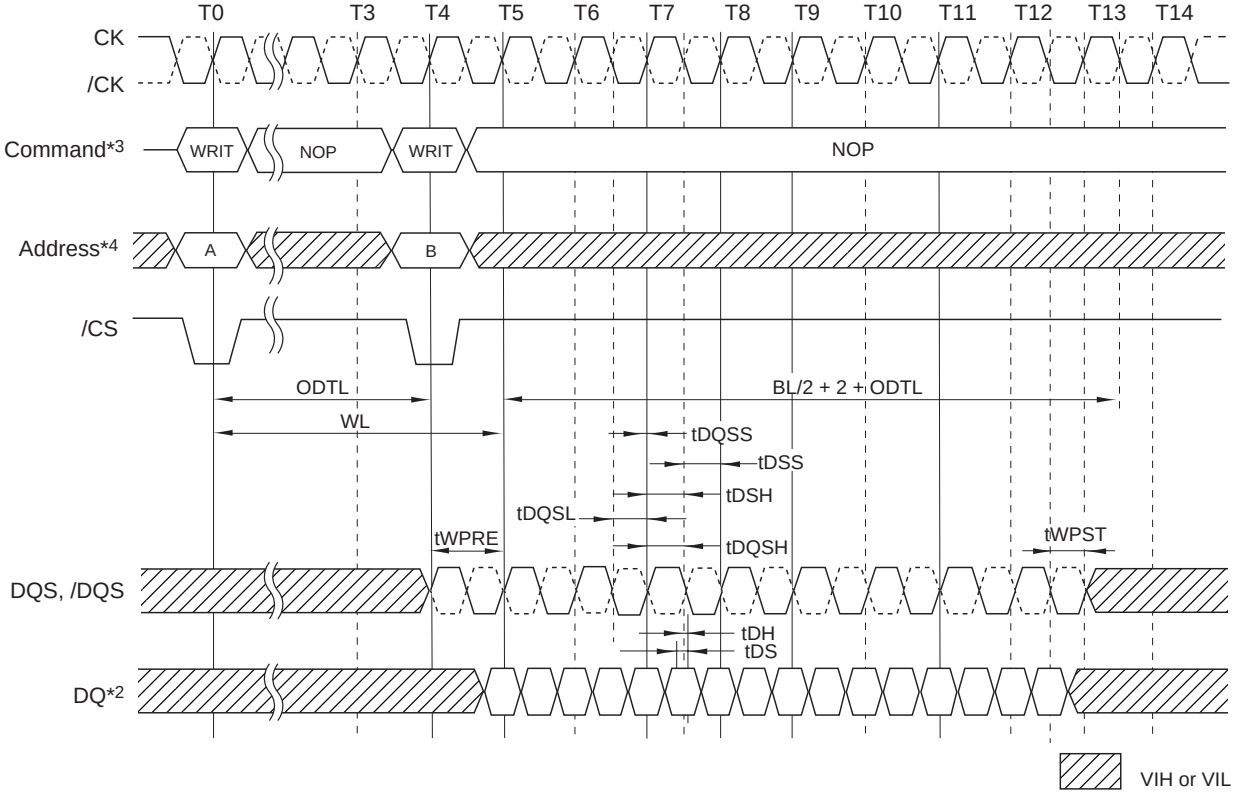
In the example (Figure Write Timing Parameters) the relevant strobe edges for write burst A are associated with the clock edges: T5, T5.5, T6, T6.5, T7, T7.5, T8, T8.5.

Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise.

Strobe to Strobe and Strobe to Clock Violations

Should the strobe timing requirements (tDQSH, tDQSL, tWPRE, tWPST) or the strobe to clock timing requirements (tDSS, tDSH tDQSS) be violated for any of the strobe edges associated with a write burst, then wrong data might be written to the memory location addressed with the offending write command. Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise.

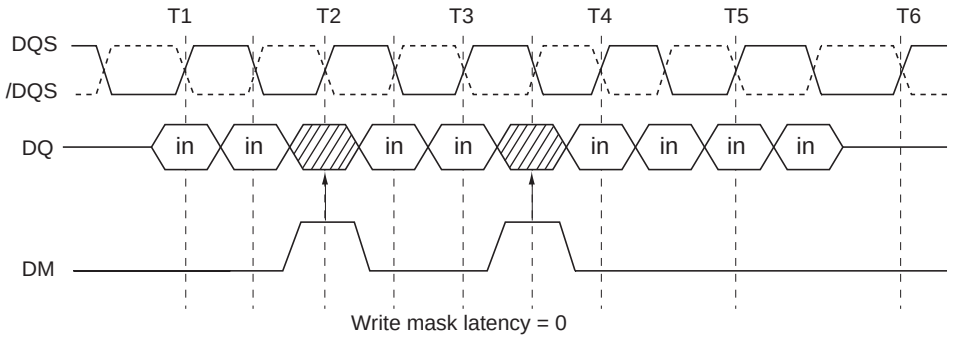
In the example (Figure Write Timing Parameters) the relevant strobe edges for write burst A are associated with the clock edges: T4, T4.5, T5, T5.5, T6, T6.5, T7, T7.5, T8, T8.5 and T9. Any timing requirements starting and ending on one of these strobe edges are T8, T8.5, T9, T9.5, T10, T10.5, T11, T11.5, T12, T12.5 and T13. Some edges are associated with both bursts.



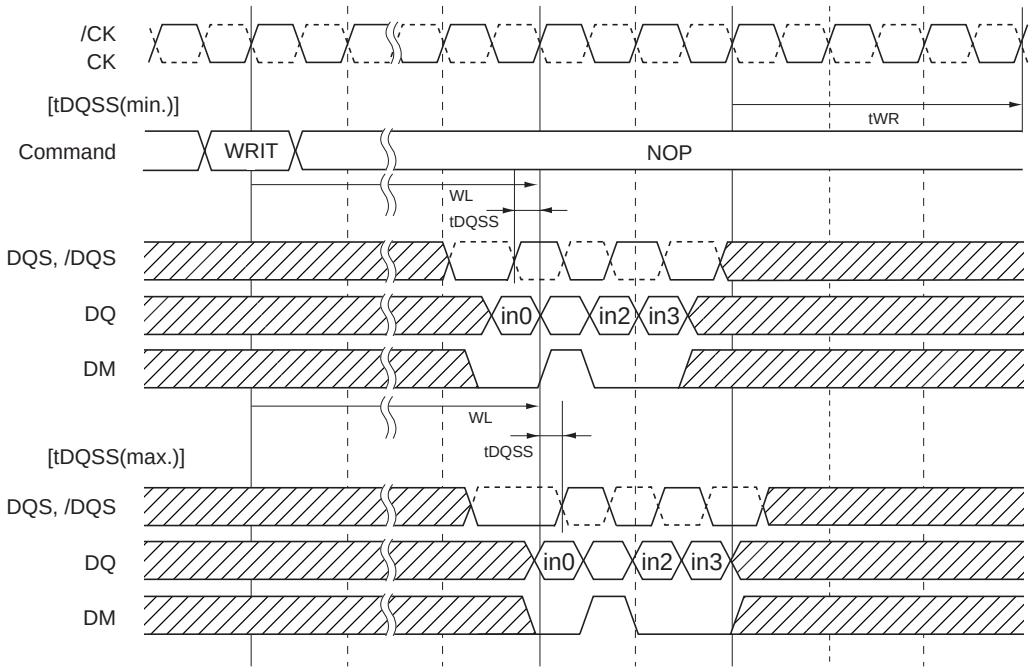
Write Timing Parameters

Write Data Mask

One write data mask (DM) pin for each 8 data bits (DQ) will be supported on DDR3 SDRAMs, Consistent with the implementation on DDR-I SDRAMs. It has identical timings on write operations as the data bits, and though used in a uni-directional manner, is internally loaded identically to data bits to ensure matched system timing. DM is not used during read cycles.



Data Mask Timing



Data Mask Function, WL = 5, AL = 0 shown

Precharge

The precharge command is used to precharge or close a bank that has been activated. The precharge command is triggered when /CS, /RAS and /WE are low and /CAS is high at the rising edge of the clock. The precharge command can be used to precharge each bank independently or all banks simultaneously. Four address bits A10, BA0, BA1 and BA2 are used to define which bank to precharge when the command is issued.

[Bank Selection for Precharge by Address Bits]

A10	BA0	BA1	BA2	Precharged Bank(s)
L	L	L	L	Bank 0 only
L	H	L	L	Bank 1 only
L	L	H	L	Bank 2 only
L	H	H	L	Bank 3 only
L	L	L	H	Bank 4 only
L	H	L	H	Bank 5 only
L	L	H	H	Bank 6 only
L	H	H	H	Bank 7 only
H	×	×	×	All banks 0 to 7

Remark: H: VIH, L: VIL, ×: VIH or VIL

Auto Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the precharge command or the auto precharge function. When a read or a write command is given to the DDR3 SDRAM, the /CAS timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the read or write Command is issued, then normal read or write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is high when the Read or Write Command is issued, then the auto precharge function is engaged. During auto precharge, a read Command will execute as normal with the exception that the active bank will begin to precharge on the rising edge which is /CAS latency (CL) clock cycles before the end of the read burst.

Auto precharge can also be implemented during Write commands. The precharge operation engaged by the Auto precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array.

This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon /CAS latency) thus improving system performance for random data access. The /RAS lockout circuit internally delays the Precharge operation until the array restore operation has been completed so that the auto precharge command may be issued with any read or write command.

Burst Read with Auto Precharge

If A10 is high when a Read Command is issued, the Read with Auto precharge function is engaged. The DDR3 SDRAM starts an auto precharge operation on the rising edge which is (AL + BL/2) cycles later from the read with AP command when tRAS (min.) is satisfied. If tRAS (min.) is not satisfied at the edge, the start point of auto precharge operation will be delayed until tRAS (min.) is satisfied. A new bank active (command) may be issued to the same bank if the following two conditions are satisfied simultaneously.

(1) The /RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.

(2) The /RAS cycle time (tRC) from the previous bank activation has been satisfied.

Burst Write with Auto precharge

If A10 is high when a write command is issued, the Write with auto precharge function is engaged. The DDR3 SDRAM automatically begins precharge operation after the completion of the burst writes plus write recovery time (tWR). The bank-undergoing auto precharge from the completion of the write burst may be reactivated if the following two conditions are satisfied.

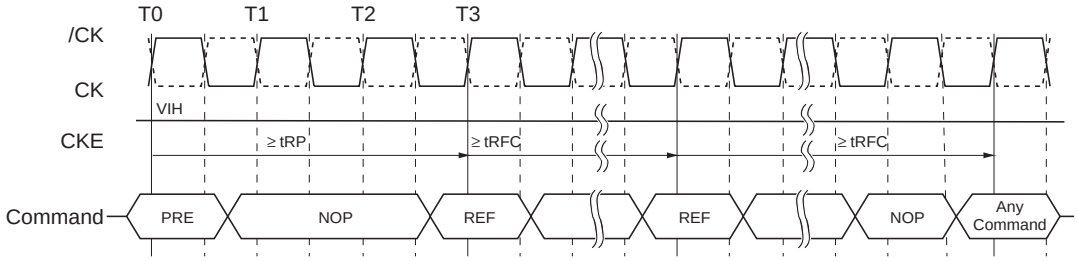
(1) The data-in to bank activate delay time (tWR + tRP) has been satisfied.

(2) The /RAS cycle time (tRC) from the previous bank activation has been satisfied.

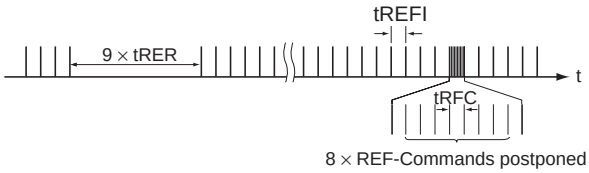
Auto-Refresh

The refresh command (REF) is used during normal operation of the DDR3 SDRAMs. This command is non persistent, so it must be issued each time a refresh is required. The DDR3 SDRAM requires refresh cycles at an average periodic interval of tREFI. When /CS, /RAS and /CAS are held low and /WE high at the rising edge of the clock, the chip enters a refresh cycle. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time tRP(min) before the refresh command can be applied. The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during a refresh command. An internal address counter supplies the addresses during the refresh cycle. No control of the external address bus is required once this cycle has started. When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the refresh command and the next valid command, except NOP or DESL, must be greater than or equal to the minimum refresh cycle time tRFC(min) as shown in the following figure. Note that the tRFC timing parameter depends on memory density.

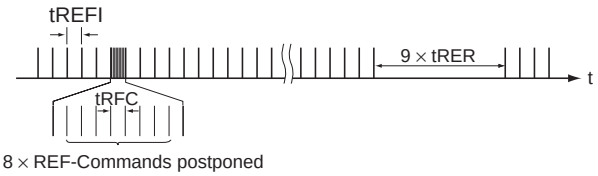
In general, a refresh command needs to be issued to the DDR3 SDRAM regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 refresh commands can be postponed during operation of the DDR3 SDRAM, meaning that at no point in time more than a total of 8 refresh commands are allowed to be postponed. In case that 8 refresh commands are postponed in a row, the resulting maximum interval between the surrounding refresh commands is limited to 9 × tREFI. A maximum of 8 additional refresh commands can be issued in advance ("pulled in"), with each one reducing the number of regular refresh commands required later by one. Note that pulling in more than 8 refresh commands in advance does not further reduce the number of regular refresh commands required later, so that the resulting maximum interval between two surrounding refresh commands is limited to 9 × tREFI. At any given time, a maximum of 16 REF commands can be issued within tREFI. Before entering self-refresh mode, all postponed refresh commands must be executed.



Refresh Command Timing



Postponing Refresh Command



Pulling-in Refresh Command

Self-Refresh

The self-refresh command can be used to retain data in the DDR3 SDRAM, even if the rest of the system is powered down. When in the self-refresh mode, the DDR3 SDRAM retains data without external clocking. The DDR3 SDRAM device has a built-in timer to accommodate self-refresh operation. The Self-Refresh Entry (SELF) command is defined by having /CS, /RAS, /CAS and CKE held low with /WE high at the rising edge of the clock.

Before issuing the self-refresh entry command, the DDR3 SDRAM must be idle with all bank precharge state with tRP satisfied. Also, on-die termination must be turned off before issuing Self-refresh entry command, by either registering ODT pin low "ODTL + 0.5tCK" prior to the self-refresh entry command or using MRS to MR1 command. Once the self-refresh entry command is registered, CKE must be held low to keep the device in self-refresh mode. The DLL is automatically disabled upon entering Self-refresh and is automatically enabled (including a DLL-Reset) upon exiting self-refresh.

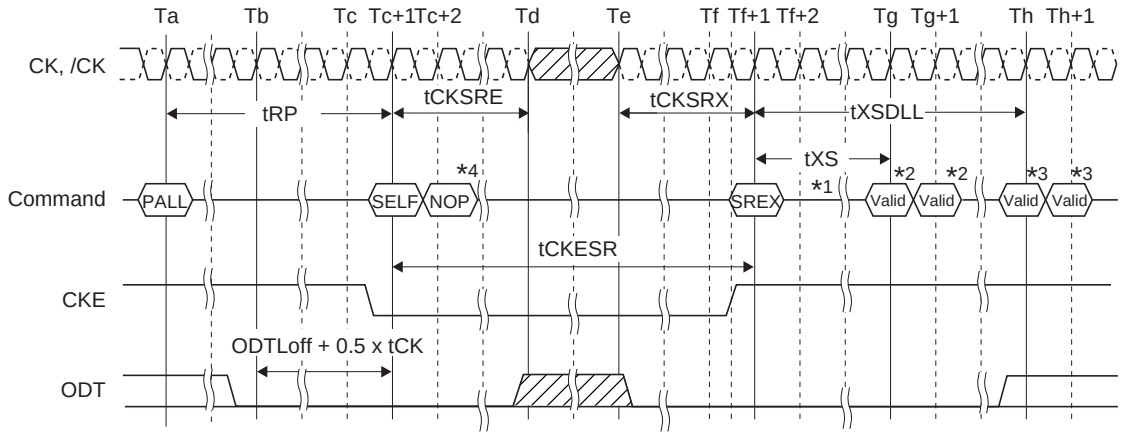
When the DDR3 SDRAM has entered self-refresh mode all of the external control signals, except CKE and /RESET, are "don't care". For proper self-refresh operation, all power supply and reference pins (VDD, VDDQ, VSS, VSSQ, VREFCA and VREFDQ) must be at valid levels. The DRAM initiates a minimum of one refresh command internally within tCKESR period once it enters self-refresh mode.

The clock is internally disabled during self-refresh operation to save power. The minimum time that the DDR3 SDRAM must remain in self-refresh mode is tCKESR. The user may change the external clock frequency or halt the external clock tCKSRE clock cycles after self-refresh entry is registered, however, the clock must be restarted and stable tCKSRX clock cycles before the device can exit self-refresh operation. To protect DRAM internal delay on CKE line to block the input signals, one NOP (or DESL) command is needed after self-refresh entry.

The procedure for exiting self-refresh requires a sequence of events. First, the clock must be stable tCKSRX prior to CKE going back high. Once a Self-Refresh Exit command (SREX, combination of CKE going high and either NOP or DESL on command bus) is registered, a delay of at least tXS must be satisfied before a valid command not requiring a locked DLL can be issued to the device to allow for any internal refresh in progress. Before a command which requires a locked DLL can be applied, a delay of at least tXSDLL and applicable ZQCAL function requirements (TBD) must be satisfied.

CKE must remain high for the entire self-refresh exit period tXSDLL for proper operation except for self-refresh reentry. Upon exit from self-refresh, the DDR3 SDRAM can be put back into Self-refresh mode after waiting at least tXS period and issuing one refresh command (refresh period of tRFC). NOP or DESL commands must be registered on each positive clock edge during the self-refresh exit interval tXS. ODT must be turned off during tXSDLL.

The use of Self-refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from self-refresh mode. Upon exit from self-refresh, the DDR3 SDRAM requires a minimum of one extra refresh command before it is put back into self-refresh mode.



Notes: 1. Only NOP or DESL commands.
2. Valid commands not requiring a locked DLL.
3. Valid commands requiring a locked DLL.
4. One NOP or DESL commands.

Self-Refresh Entry and Exit Timing

Power-Down Mode

Power-down is synchronously entered when CKE is registered low (along with NOP or DESL command). CKE is not allowed to go low while mode register set command, MPR operations, ZQCAL operations, DLL locking or read/write operation are in progress. CKE is allowed to go low while any of other operations such as row activation, precharge or auto precharge and refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.

The DLL should be in a locked state when power-down is entered for fastest power-down exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper read operation and synchronous ODT operation. DRAM design provides all AC and DC timing and voltage specification as well proper DLL operation with any CKE intensive operations as long as DRAM controller complies with DRAM specifications.

During power-down, if all banks are closed after any in-progress commands are completed, the device will be in precharge power-down mode; if any bank is open after in-progress commands are completed, the device will be in active power-down mode.

Entering power-down deactivates the input and output buffers, excluding CK, /CK, ODT, CKE and /RESET. To protect DRAM internal delay on CKE line to block the input signals, multiple NOP or DESL commands are needed during the CKE switch off and cycle(s) after this timing period are defined as tCPDED. CKE_low will result in deactivation of command and address receivers after tCPDED has expired.

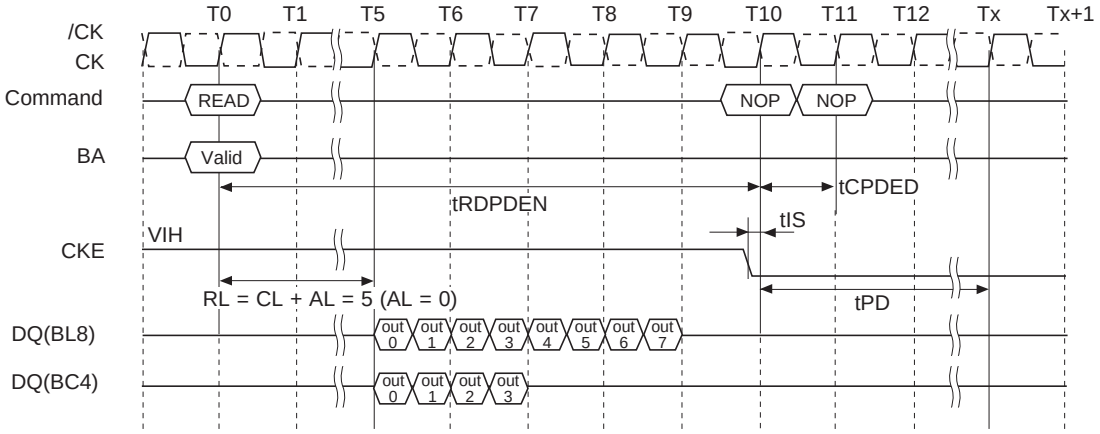
[Power-Down Entry Definitions]

Status of DRAM	MR0 bit A12	DLL	PD Exit	Relevant Parameters
Active (A bank or more Open)	Don't Care	On	Fast	tXP to any valid command
Precharged (All banks Precharged)	0	Off	Slow	tXP to any valid command. Since it is in precharge state, commands here will be ACT, AR, MRS, PRE or PALL . tXPDLL to commands who need DLL to operate, such as READ, READA or ODT control line.
Precharged (All Banks Precharged)	1	On	Fast	tXP to any valid command

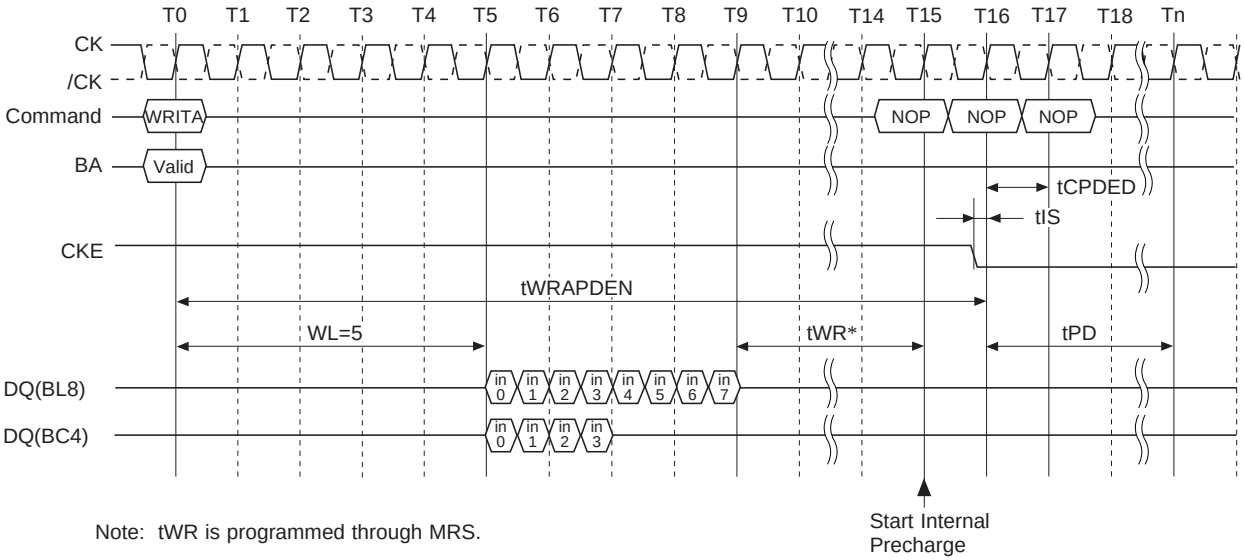
Also the DLL is disabled upon entering precharge power-down for slow exit mode, but the DLL is kept enabled during precharge power-down for fast exit mode or active power-down. In power-down mode, CKE low, RESET high and a stable clock signal must be maintained at the inputs of the DDR3 SDRAM, and ODT should be in a valid state but all other input signals are "Don't Care" (If RESET goes low during power-down, the DRAM will be out of PD mode and into reset state). CKE low must be maintained until tPD has been satisfied. Power-down duration is limited by 9 times tREFI of the device.

The power-down state is synchronously exited when CKE is registered high (along with a NOP or DESL command). CKE high must be maintained until tCKE has been satisfied. A valid, executable command can be applied with power-down exit latency, tXP and/or tXPDLL after CKE goes high. Power-down exit latency is defined at AC Characteristics table of this data sheet.

Timing Diagrams for Proposed CKE with Power-Down Entry, Power-Down Exit

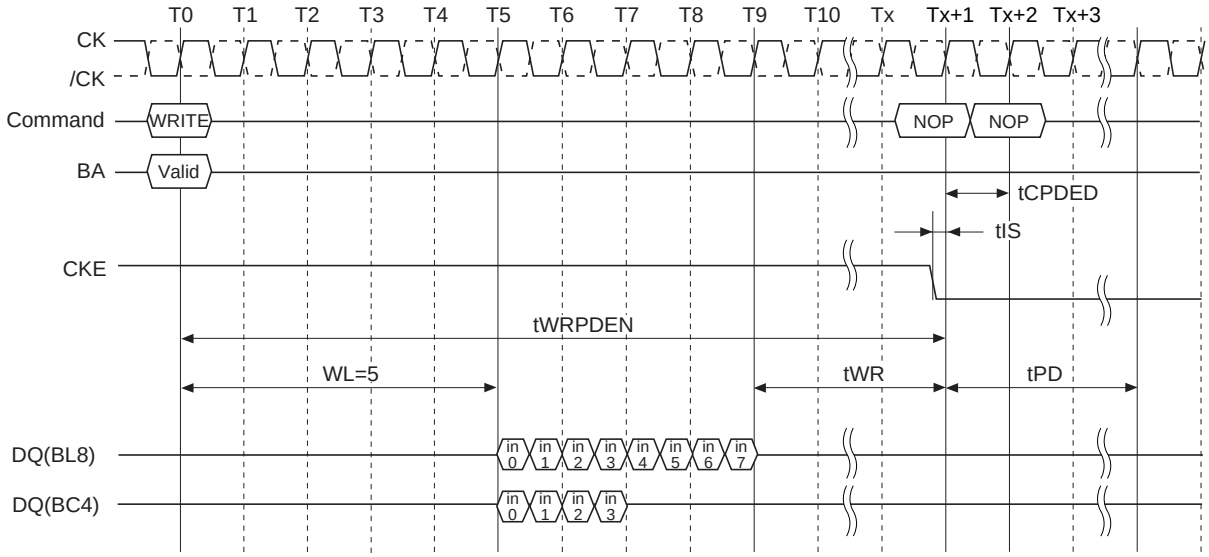


Power-Down Entry after Read and Read with Auto Precharge

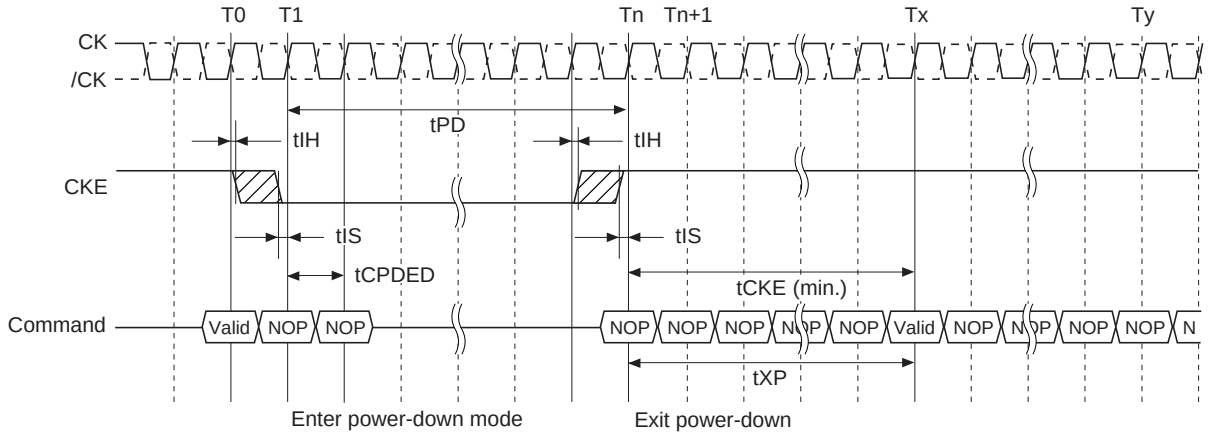


Note: tWR is programmed through MRS.

Power-Down Entry After Write with Auto Precharge

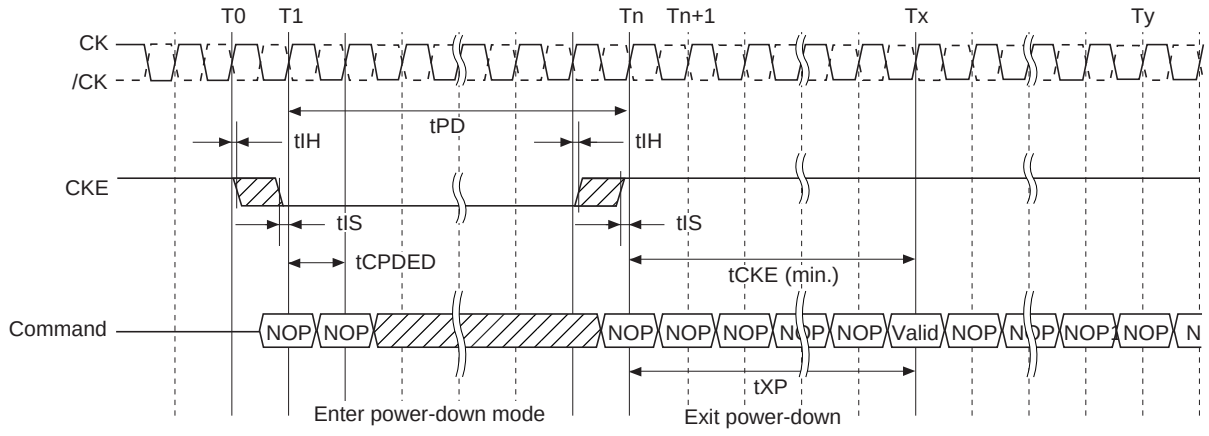


Power-Down Entry after Write

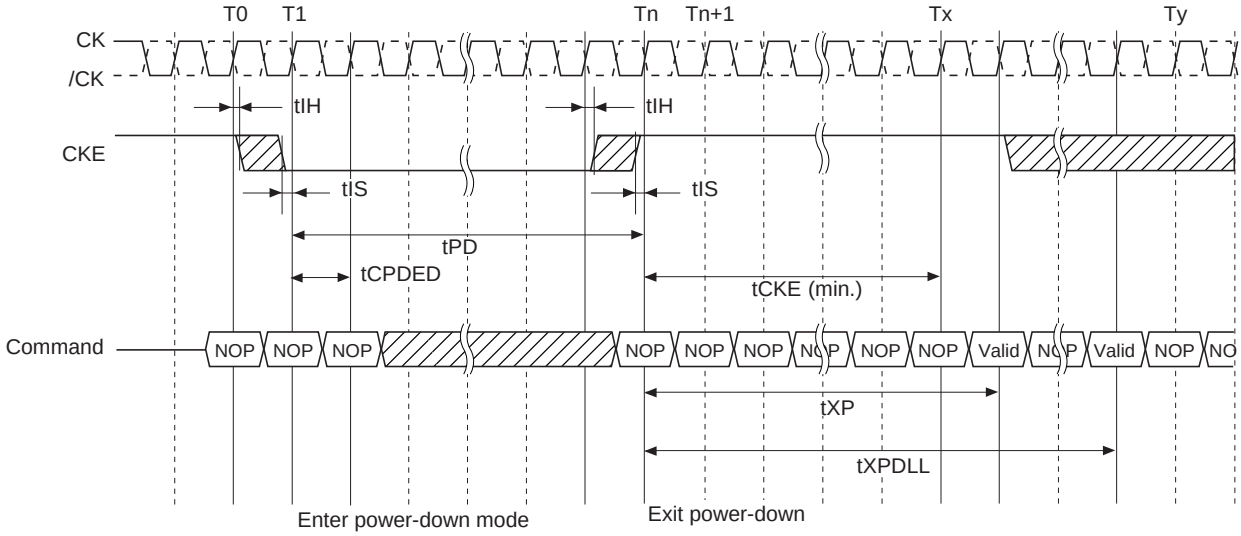


Note: Valid command at T0 is ACT, NOP, DESL or precharge with still one bank remaining open after completion of precharge command.

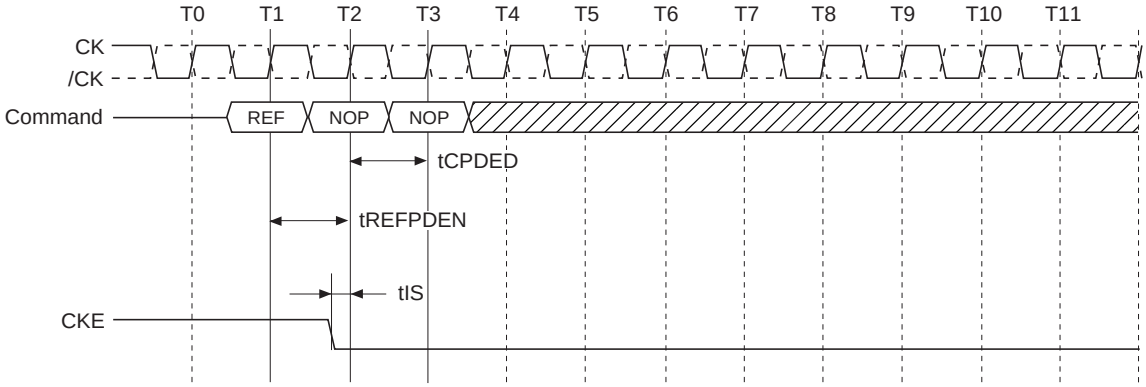
Active Power-Down Entry and Exit Timing Diagram



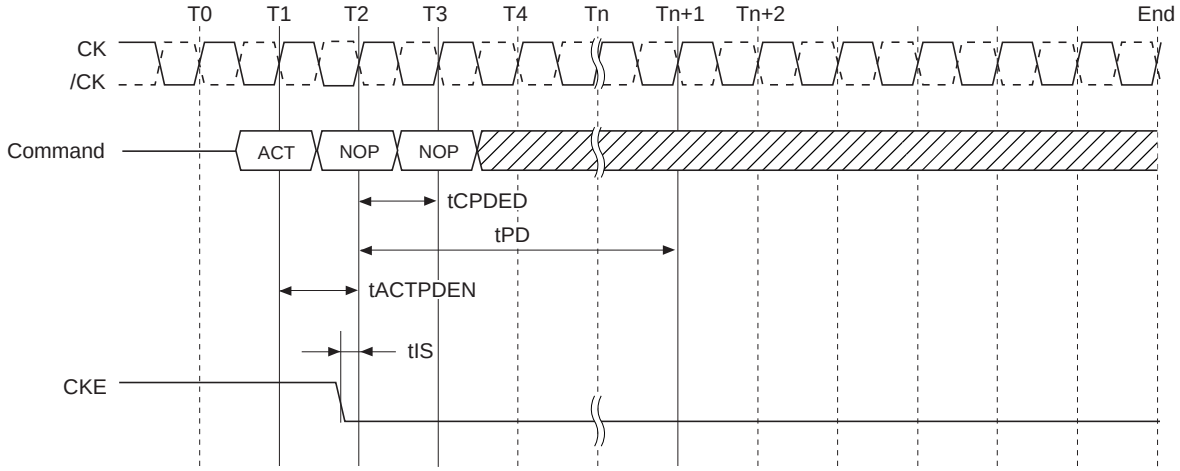
Precharge Power-Down (Fast Exit Mode) Entry and Exit



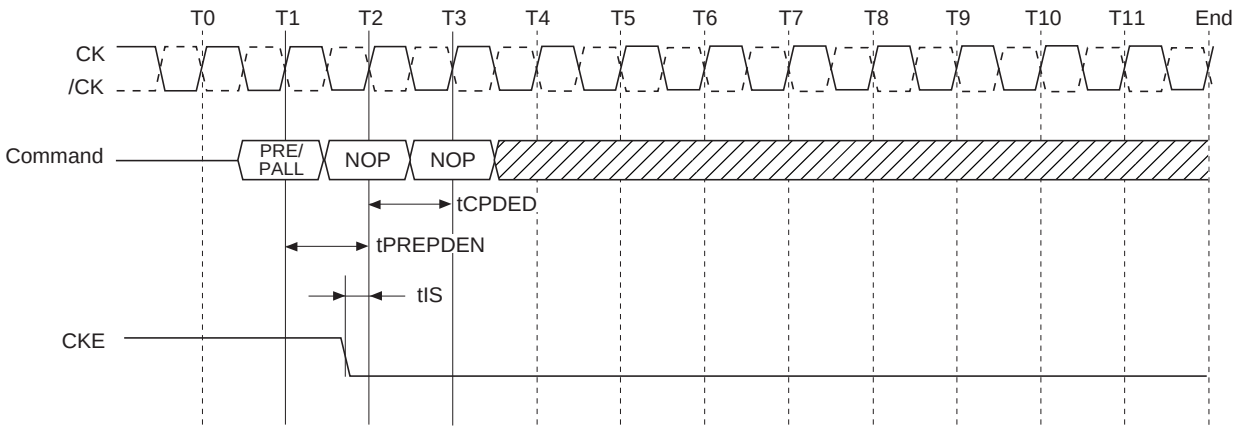
Precharge Power-Down (Slow Exit Mode) Entry and Exit



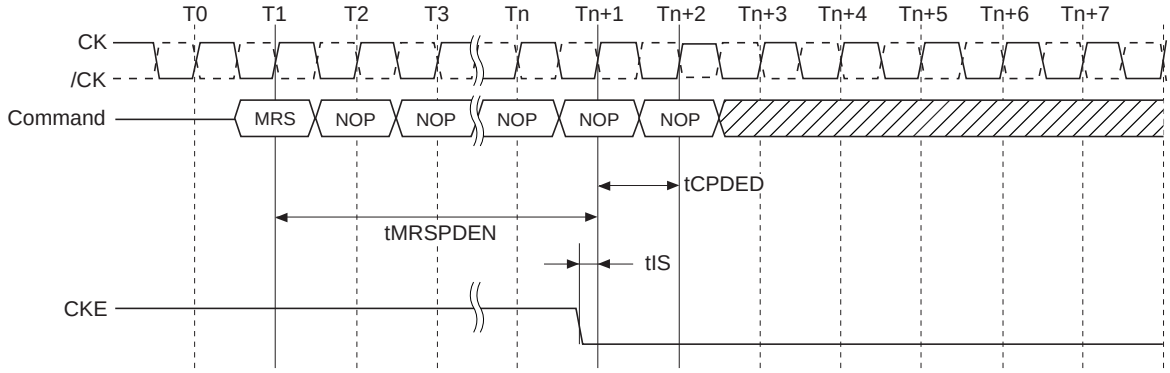
Refresh Command to Power-Down Entry



Active Command to Power-Down Entry



Precharge/Precharge All Command to Power-Down Entry



MRS Command to Power-Down Entry

Timing Values tXXXPDEN Parameters

Status of DRAM	Last Command before CKE_low	Parameter	Parameter Value	Unit
Idle or Active	Activate	tACTPDEN	1	nCK
Idle or Active	Precharge	tPRPDEN	1	nCK
Active	READ/READA	tRDPDEN	RL + 4 + 1	nCK
Active	WRIT for BL8MRS, BL8OTF, BC4OTF	tWRPDEN	WL + 4 + (tWR/tCK (avg)) *1	nCK
Active	WRIT for BC4MRS	tWRPDEN	WL + 2 + (tWR/tCK (avg))*1	nCK
Active	WRITA for BL8MRS, BL8OTF, BC4OTF	tWRAPDEN	WL + 4 + WR*2 + 1	nCK
Active	WRITA for BC4MRS	tWRAPDEN	WL + 2 + WR*2 + 1	nCK
Idle	Refresh	tREFPDEN	1	nCK
Idle	Mode Register Set	tMRSPDEN	tMOD	

Notes: 1. tWR is defined in ns, for calculation of tWRPDEN, it is necessary to round up tWR / tCK to next integer.
2. WR in clock cycles as programmed in mode register.

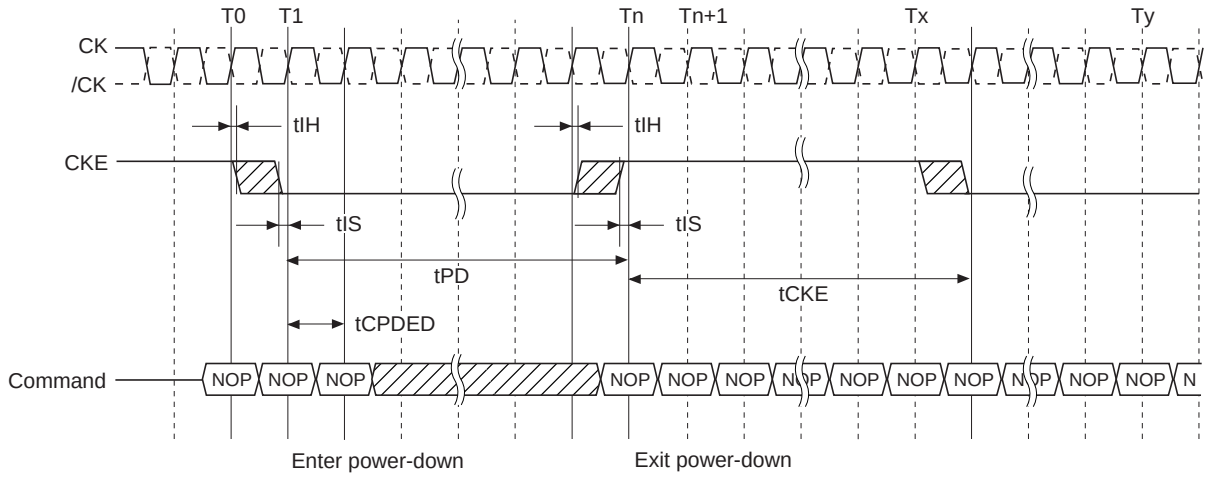
Power-Down Entry and Exit Clarification

Case 1:

When CKE registered low for power-down entry, tPD must be satisfied before CKE can be registered high for power-down exit.

Case 1a:

After power-down exit, tCKE must be satisfied before CKE can be registered low again.



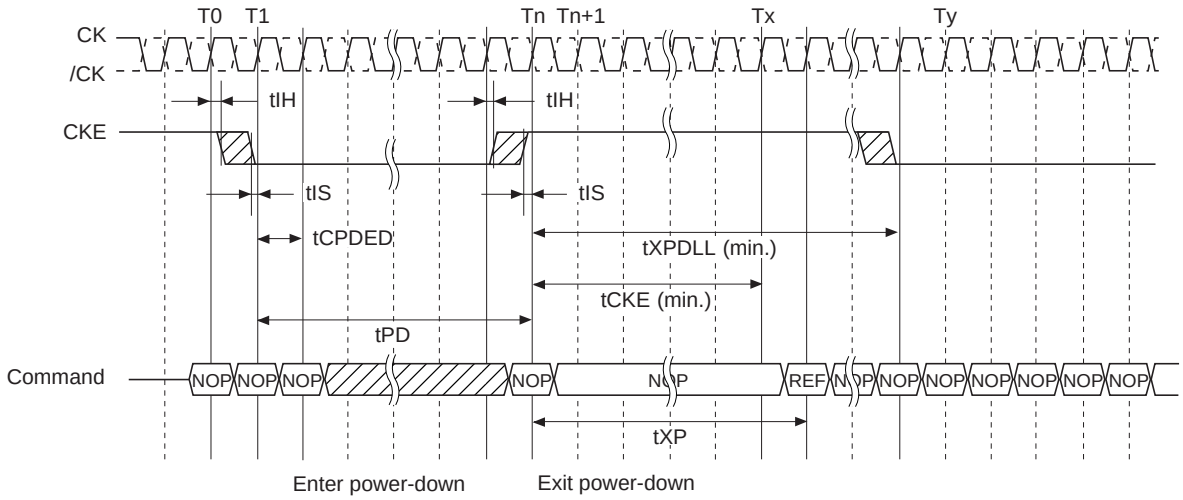
Power-Down Entry/Exit Clarifications (1)

Case 2:

For certain CKE intensive operations, for example, repeated "PD Exit - Refresh - PD Entry" sequence, the number of clock cycles between PD Exit and PD Entry may be insufficient to keep the DLL updated. Therefore the following conditions must be met in addition to tPD in order to maintain proper DRAM operation when Refresh commands is issued in between PD Exit and PD Entry.

Power-down mode can be used in conjunction with Refresh command if the following conditions are met:

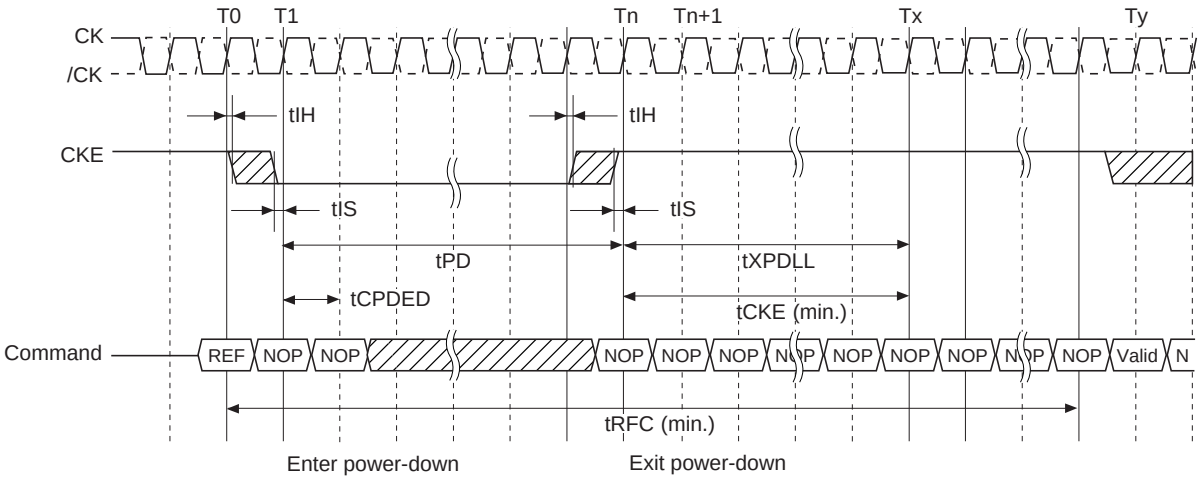
1. tXP must be satisfied before issuing the command
2. tXPDLL must be satisfied (referenced to registration of PD exit) before next power-down can be entered.



Power-Down Entry/Exit Clarifications (2)

Case 3:

If an early PD Entry is issued after Refresh command, once PD Exit is issued, NOP or DESL with CKE high must be issued until tRFC from the refresh command is satisfied. This means CKE cannot be de-asserted twice within tRFC window.



Note: * Synchronous ODT Timing starts at the end of tXPDLL (min.)

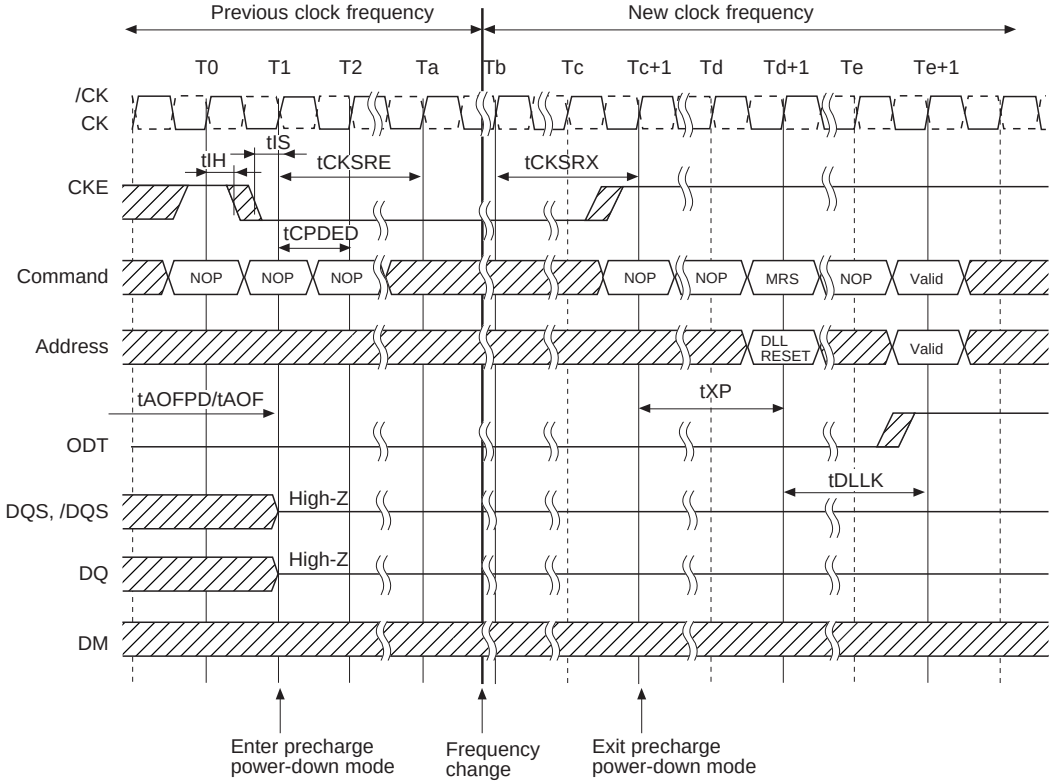
Power-Down Entry/Exit Clarifications (3)

Input Clock Frequency Change during Precharge Power-Down

Once the DDR3 SDRAM is initialized, the DDR3 SDRAM requires the clock to be “stable” during almost all states of normal operation. This means once the clock frequency has been set and is to be in the “stable state”, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (Spread Spectrum Clocking) specifications.

The input clock frequency can be changed from one stable clock rate to another stable clock rate under two conditions: (1) self-refresh mode and (2) precharge power-down mode. Outside of these two modes, it is illegal to change the clock frequency. For the first condition, once the DDR3 SDRAM has been successfully placed in to Self-Refresh mode and tCKSRE has been satisfied, the state of the clock becomes a don’t care. Once a don’t care, changing the clock frequency is permissible, provided the new clock frequency is stable prior to tCKSRX. When entering and exiting Self-Refresh mode for the sole purpose of changing the clock frequency, the self-refresh entry and exit specifications must still be met as outlined in Self-Refresh section.

The second condition is when the DDR3 SDRAM is in Precharge Power-down mode (either fast exit mode or slow exit mode.) ODT must be at a logic low ensuring RTT is in an off state prior to entering Precharge Power-down mode and CKE must be at a logic low. A minimum of tCKSRE must occur after CKE goes low before the clock frequency may change. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. During the input clock frequency change, ODT and CKE must be held at stable low levels. Once the input clock frequency is changed, stable new clocks must be provided to the DRAM tCKSRX before Precharge Power-down may be exited; after Precharge Power-down is exited and tXP has expired, the DLL must be RESET via MRS. Depending on the new clock frequency additional MRS commands may need to be issued to appropriately set the WR, CL, and CWL with CKE continuously registered high. During DLL relock period, ODT must remain low. After the DLL lock time, the DRAM is ready to operate with new clock frequency. This process is depicted in the figure Clock Frequency Change in Precharge Power-Down Mode.



Notes: 1. Applicable for both slow exit and fast exit precharge power-down.
2. tCKSRE and tCKSRX are self-refresh mode specifications but the values they represent are applicable here.
3. tAOFPD and tAOF must be satisfied and outputs high-z prior to T1; refer to ODT timing for exact requirements.

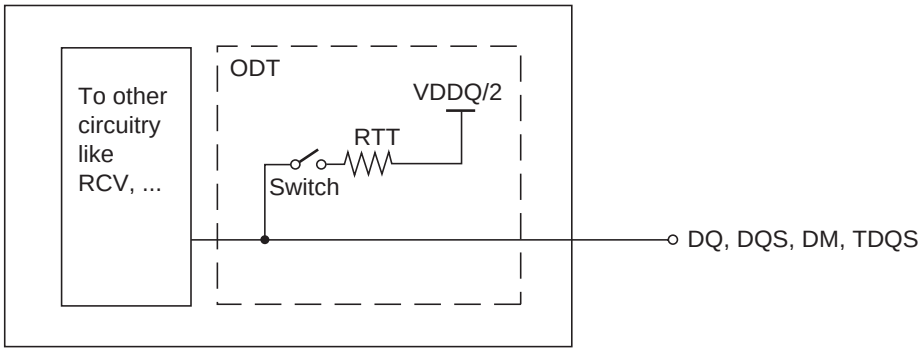
Clock Frequency Change in Precharge Power-Down Mode

On-Die Termination (ODT)

ODT (On-Die Termination) is a feature of the DDR3 SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS, /DQS and DM for ×4 and ×8 configuration (and TDQS, /TDQS for ×8 configuration, when enabled via A11=1 in MR1) via the ODT control pin. For ×16 configuration ODT is applied to each DQU, DQL, DQSU, /DQSU, DQSL, /DQSL, DMU and DML signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT feature is turned off and not supported in Self-Refresh mode.

A simple functional representation of the DRAM ODT feature is shown in figure Functional Representation of ODT.



Functional Representation of ODT

The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other control information, see below. The value of RTT is determined by the settings of Mode Register bits (see MR1 programming figure in the section Programming the Mode Register). The ODT pin will be ignored if the Mode Register MR1 is programmed to disable ODT and in self-refresh mode.

ODT Mode Register and ODT Truth Table

The ODT Mode is enabled if either of MR1 bits A2 or A6 or A9 are non-zero. In this case the value of RTT is determined by the settings of those bits.

Application: Controller sends WRIT command together with ODT asserted.

- One possible application: The rank that is being written to provide termination.
- DRAM turns ON termination if it sees ODT asserted (except ODT is disabled by MR)
- DRAM does not use any write or read command decode information
- The Termination Truth Table is shown in the Termination Truth Table

[Termination Truth Table]

ODT pin	DRAM Termination State
0	OFF
1	ON, (OFF, if disabled by MR1 bits A2, A6 and A9 in general)

Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked. Based on the power-down definition, these modes are:

- Active mode
- Idle mode with CKE high
- Active power-down mode (regardless of MR0 bit A12)
- Precharge power-down mode if DLL is enabled during precharge power-down by MR0 bit A12.

In synchronous ODT mode, RTT will be turned on or off ODTLon clock cycles after ODT is sampled high by a rising clock edge and turned off ODTLoff clock cycles after ODT is registered low by a rising clock edge. The ODT latency is tied to the write latency (WL) by: ODTLon = WL – 2; ODTLoff = WL – 2.

ODT Latency and Posted ODT

In Synchronous ODT mode, the Additive Latency (AL) programmed into the Mode Register (MR1) also applies to the ODT signal. The DRAM internal ODT signal is delayed for a number of clock cycles defined by the Additive Latency (AL) relative to the external ODT signal.

ODTLon = CWL + AL − 2; ODTLoff = CWL + AL − 2. For details, refer to DDR3 SDRAM latency definitions.

[ODT Latency Table]

Parameter	Symbol	Value	Unit
ODT turn-on Latency	ODTLon	WL – 2 = CWL + AL – 2	nCK
ODT turn-off Latency	ODTLoff	WL – 2 = CWL + AL – 2	nCK

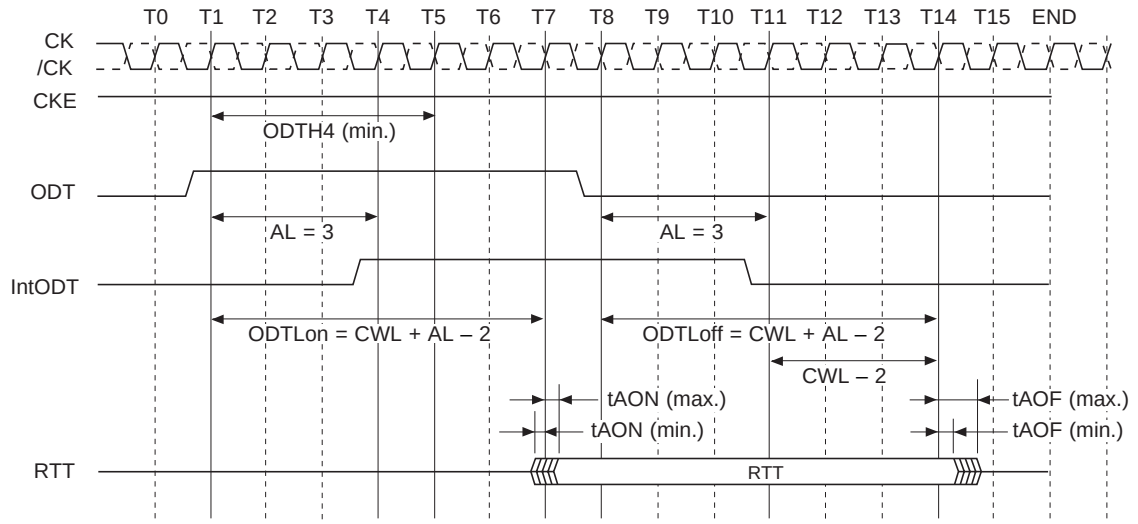
Synchronous ODT Timing Parameters

In synchronous ODT mode, the following timing parameters apply (see Synchronous ODT Timing Examples (1)): ODTLLow, ODTLLoff, tAON,(min.), (max.), tAOF,(min.),(max.) Minimum RTT turn-on time (tAON min) is the point in time when the device leaves high impedance and ODT resistance begins to turn on. Maximum RTT turn-on time (tAON max) is the point in time when the ODT resistance is fully on. Both are measured from ODTLon.

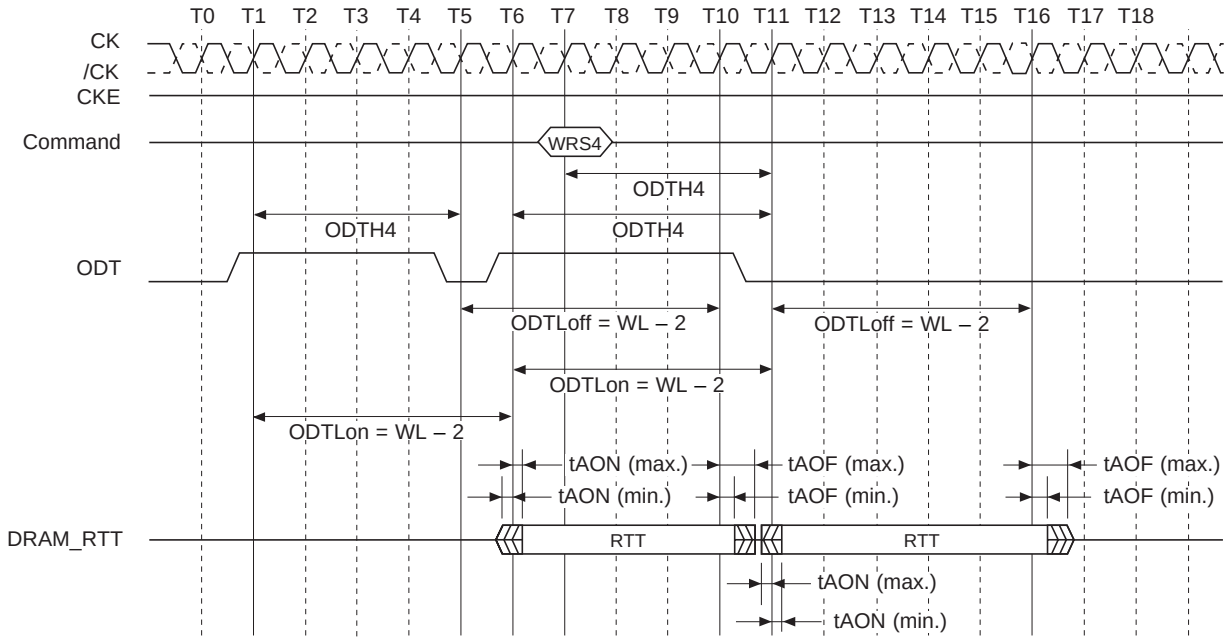
Minimum RTT turn-off time (tAOF min) is the point in time when the device starts to turn-off the ODT resistance.

Maximum RTT turn-off time (tAOF max) is the point in time when the on-die termination has reached high impedance. Both are measured from ODTLoff.

When ODT is asserted, it must remain high until ODTH4 is satisfied. If a Write command is registered by the SDRAM with ODT high, then ODT must remain high until ODTH4 (BL4) or ODTH8 (BL8) after the Write command (see figure Synchronous ODT Timing Examples (2)). ODTH4 and ODTH8 are measured from ODT registered high to ODT registered low or from the registration of a Write command until ODT is registered low.



Synchronous ODT Timing Examples (1): AL=3, CWL = 5;
ODTLon = AL + CWL - 2 = 6; ODTLoff = AL + CWL - 2 = 6



Synchronous ODT Timing Examples (2)*: BC4, WL = 7

ODT must be held high for at least ODTH4 after assertion (T1); ODT must be kept high ODTH4 (BC4) or ODTH8 (BL8) after write command (T7). ODTH is measured from ODT first registered high to ODT first registered low, or from registration of write command with ODT high to ODT registered low. Note that although ODTH4 is satisfied from ODT registered high at T6 ODT must not go low before T11 as ODTH4 must also be satisfied from the registration of the write command at T7.

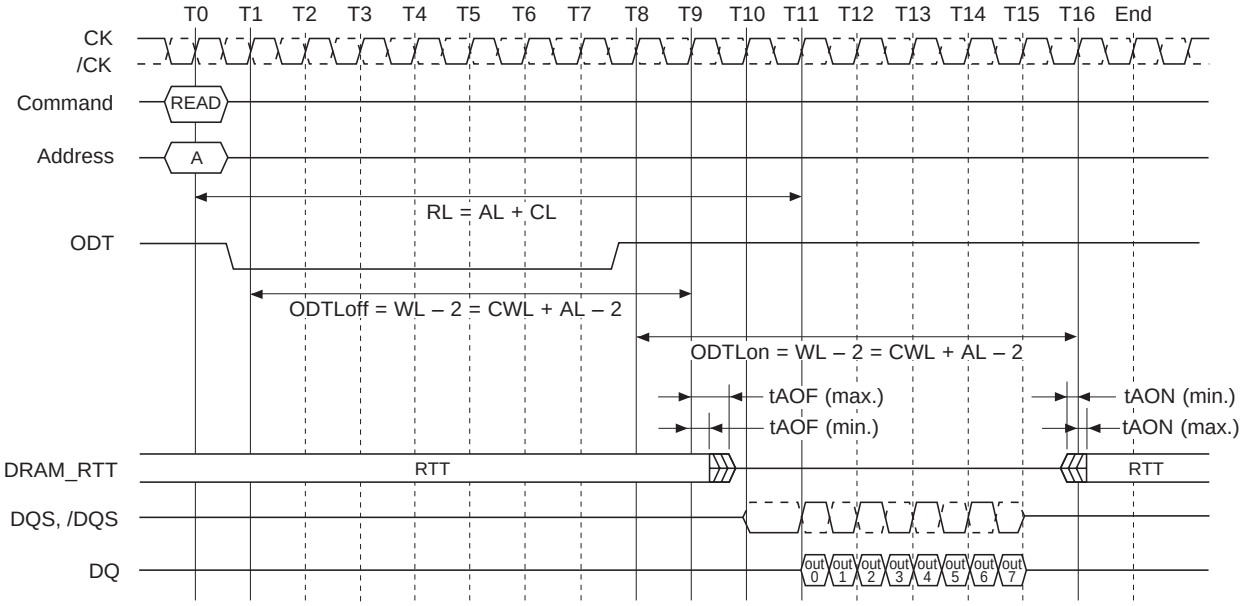
ODT during Reads

As the DDR3 SDRAM cannot terminate and drive at the same time, RTT must be disabled at least half a clock cycle before the read preamble by driving the ODT pin low appropriately. RTT may nominally not be enabled until one clock cycle after the end of the post-amble as shown in the example in the figure below.

Note that ODT may be disabled earlier before the Read and enabled later after the Read than shown in this example in the figure below.

ODT must be disabled externally during Reads by driving ODT low.

(example: CL = 6; AL = CL - 1 = 5; RL = AL + CL = 11; CWL = 5; ODTLon = CWL + AL -2 = 8; ODTLoff = CWL + AL - 2 = 8)



Example of ODT during Reads

Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. This requirement is supported by the "Dynamic ODT" feature as described as follows:

Functional Description:

The Dynamic ODT mode is enabled if bit A9 or A10 of MR2 is set to '1'. The function and is described as follows:

- Two RTT values are available: RTT_Nom and RTT_WR.
  - The value for RTT_Nom is pre-selected via bits A[9,6,2] in MR1
  - The value for RTT_WR is pre-selected via bits A[10,9] in MR2
- During operation without write commands, the termination is controlled as follows:
  - Nominal termination strength RTT_Nom is selected.
  - Termination on/off timing is controlled via ODT pin and latencies ODTLon and ODTLoff.
- When a write command (WRIT, WRITA, WRS4, WRS8, WRAS4, WRAS8) is registered, and if Dynamic ODT is enabled, the termination is controlled as follows:
  - A latency ODTLcnw after the write command, termination strength RTT_WR is selected.
  - A latency ODTLcwn8 (for BL8, fixed by MRS or selected OTF) or ODTLcwn4 (for BC4, fixed by MRS or selected OTF) after the write command, termination strength RTT_Nom is selected.
  - Termination on/off timing is controlled via ODT pin and ODTLon, ODTLoff.

Table Latencies and Timing Parameters Relevant for Dynamic ODT shows latencies and timing parameters, which are relevant for the on-die termination control in Dynamic ODT mode:

When ODT is asserted, it must remain high until ODTH4 is satisfied. If a write command is registered by the SDRAM with ODT high, then ODT must remain high until ODTH4 (BC4) or ODTH8 (BL8) after the write command (see the figure Synchronous ODT Timing Examples (2)). ODTH4 and ODTH8 are measured from ODT registered high to ODT registered low or from the registration of a write command until ODT is registered low.

[Latencies and Timing Parameters Relevant for Dynamic ODT]

Parameters	Symbols	Defined from	Defined to	Definition for all DDR3 speed bins	Unit
ODT turn-on Latency	ODTLon	Registering external ODT signal high	Turning termination on	ODTLon = WL – 2.0	nCK
ODT turn-off Latency	ODTLoff	Registering external ODT signal low	Turning termination off	ODTLoff = WL – 2.0	nCK
ODT latency for changing from RTT_Nom to RTT_WR	ODTLcnw	Registering external write command	Change RTT strength from RTT_Nom to RTT_WR	ODTLcnw = WL – 2.0	nCK
ODT latency for change from RTT_WR to RTT_Nom (BC4)	ODTLcwn4	Registering external write command	Change RTT strength from RTT_WR to RTT_Nom	ODTLcwn4 = 4 + ODTLoff	nCK
ODT latency for change from RTT_WR to RTT_Nom (BL8)	ODTLcwn8	Registering external write command	Change RTT strength from RTT_WR to RTT_Nom	ODTLcwn8 = 6 + ODTLoff	nCK
Minimum ODT high time after ODT assertion	ODTH4	registering ODT high	ODT registered low	ODTH4 (min.) = 4	nCK
Minimum ODT high time after Write (BC4)	ODTH4	registering Write with ODT high	ODT registered low	ODTH4 (min.) = 4	nCK
Minimum ODT high time after Write (BL8)	ODTH8	registering Write with ODT high	ODT registered low	ODTH8 (min.) = 6	nCK
RTT change skew	tADC	ODTLcnw ODTLcwn	RTT valid	0.3ns to 0.7ns	tCK (avg)

Mode Register Settings for Dynamic ODT Mode:

The table Mode Register for RTT Selection shows the Mode Register bits to select RTT_Nom and RTT_WR values.

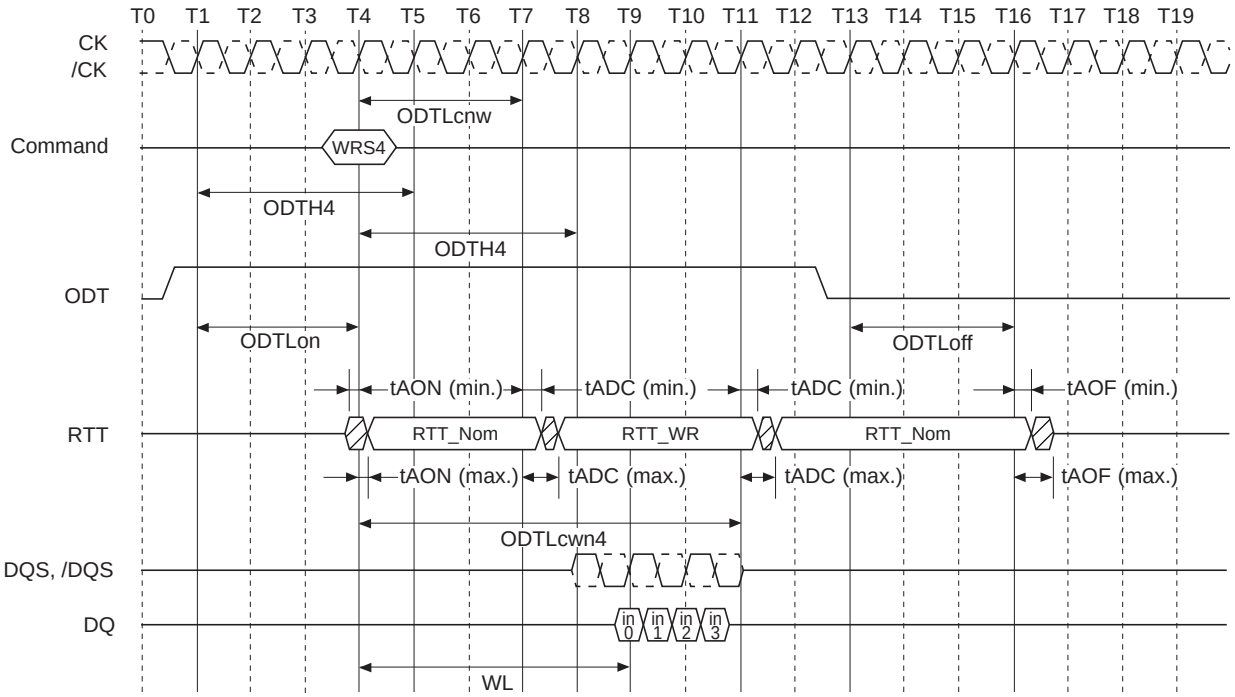
[Mode Register for RTT Selection]

MR1					MR2			
A9	A6	A2	RTT_Nom (RZQ)	RTT_Nom (Ω)	A10	A9	RTT_WR (RZQ)	RTT_WR*[1] (Ω)
0	0	0	off	off	0	0	Dynamic ODT OFF: Write does not affect RTT value	
0	0	1	RZQ/4	60	0	1	RZQ/4	60
0	1	0	RZQ/2	120	1	0	RZQ/2	120
0	1	1	RZQ/6	40	1	1	Reserved	Reserved
1	0	0	RZQ/12*[2]	20	—	—	—	—
1	0	1	RZQ/8*[2]	30	—	—	—	—
1	1	0	Reserved	Reserved	—	—	—	—
1	1	1	Reserved	Reserved	—	—	—	—

Notes: 1. RZQ = 240Ω.

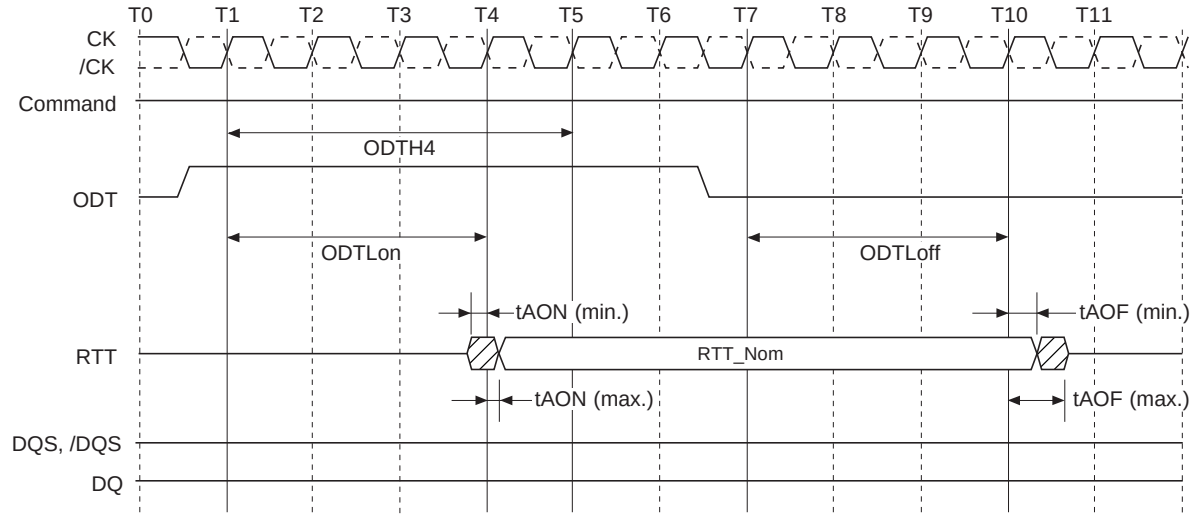
2. If RTT_Nom is used during WRITEs, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed.

ODT Timing Diagrams



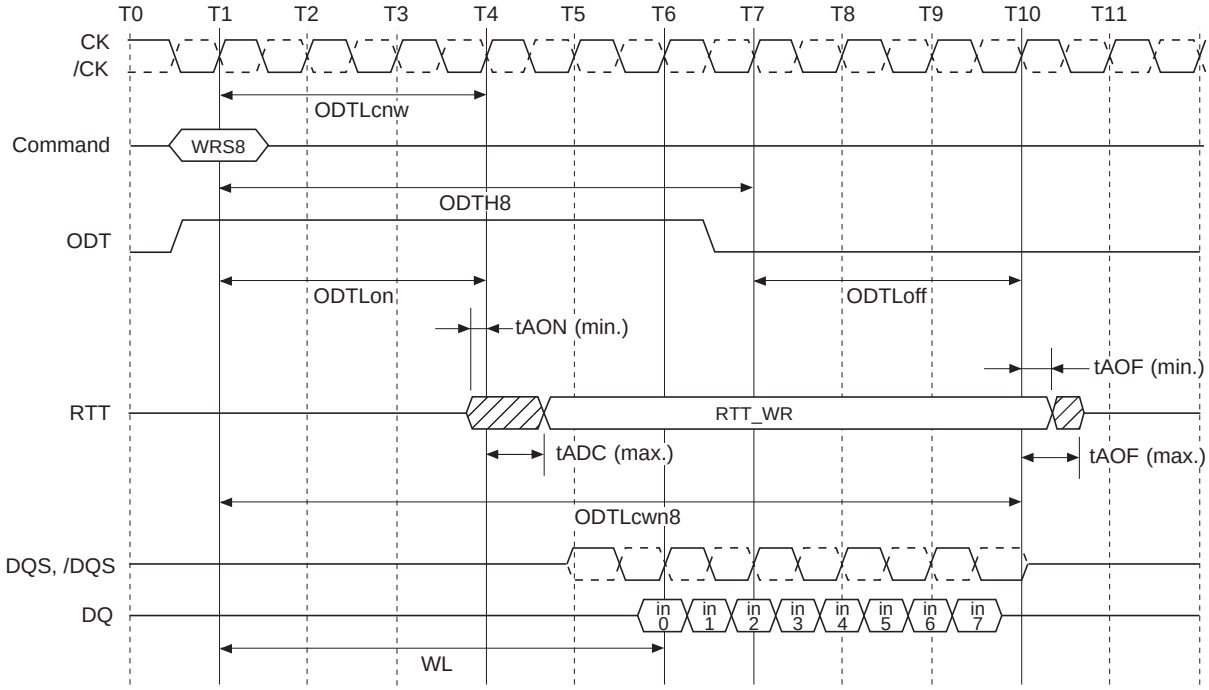
Dynamic ODT: Behavior with ODT Being Asserted Before and after the Write*

Note: Example for BC4 (via MRS or OTF), AL = 0, CWL = 5. ODTH4 applies to first registering ODT high and to the registration of the write command. In this example ODTH4 would be satisfied if ODT is low at T8 (4 clocks after the write command).



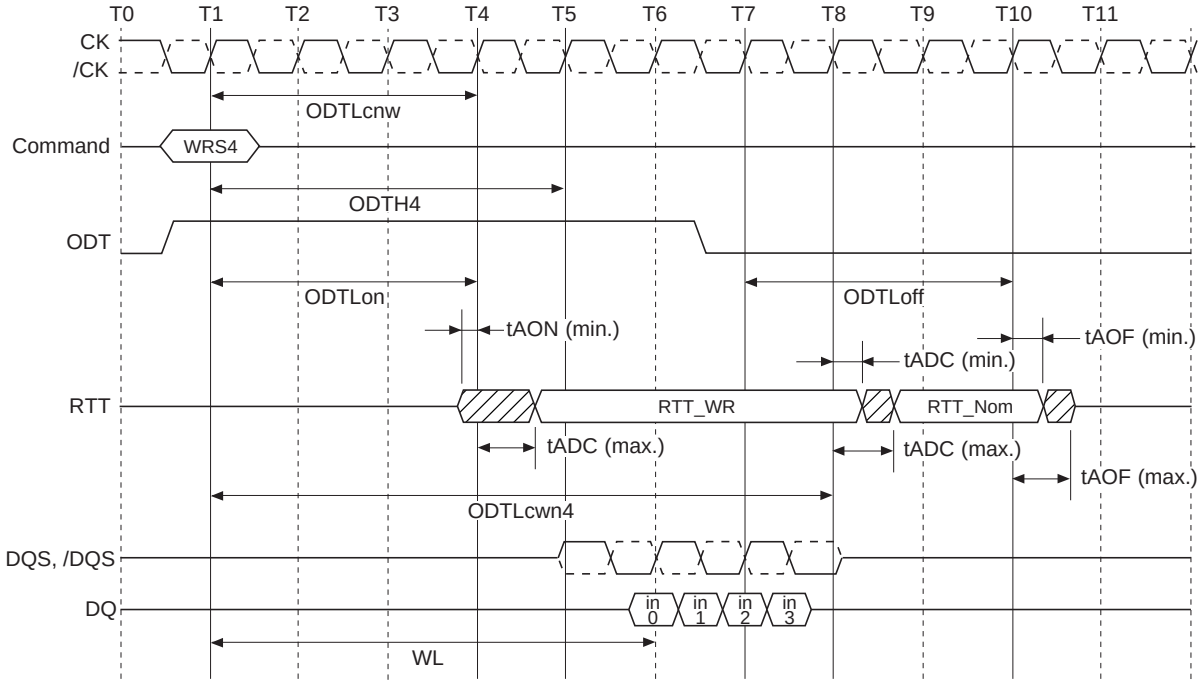
Dynamic ODT*: Behavior without Write Command; AL = 0, CWL = 5

Note: ODTH4 is defined from ODT registered high to ODT registered low, so in this example ODTH4 is satisfied; ODT registered low at T5 would also be legal.



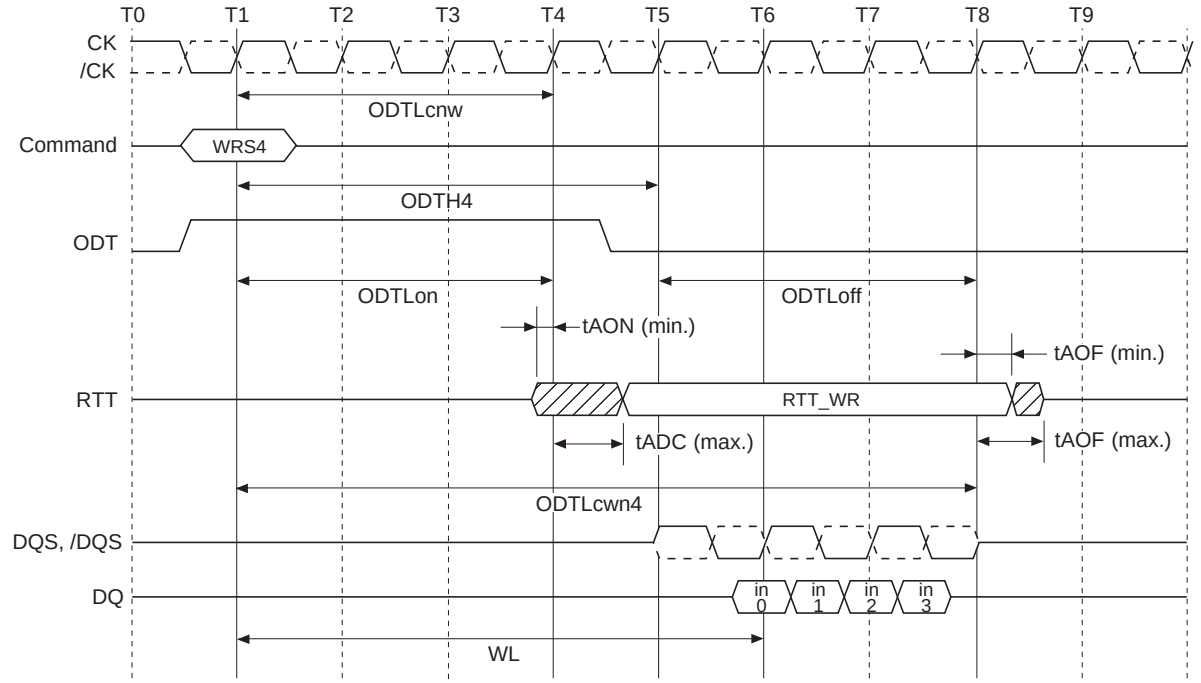
Dynamic ODT*: Behavior with ODT Pin Being Asserted Together with Write Command for Duration of 6 Clock Cycles

Note: Example for BL8 (via MRS or OTF), AL = 0, CWL = 5. In this example ODTH8 = 6 is exactly satisfied.



Dynamic ODT*: Behavior with ODT Pin Being Asserted Together with Write Command for a Duration of 6 Clock Cycles, Example for BC4 (via MRS or OTF), AL = 0, CWL = 5.

Note: ODTH4 is defined from ODT registered high to ODT registered low, so in this example ODTH4 is satisfied; ODT registered low at T5 would also be legal.



Dynamic ODT*: Behavior with ODT Pin Being Asserted Together with Write Command for Duration of 4 Clock Cycles

Note: Example for BC4 (via MRS or OTF), AL = 0, CWL = 5. In this example ODTH4 = 4 is exactly satisfied.

Asynchronous ODT Mode

Asynchronous ODT mode is selected when DRAM runs in DLL-on mode, but DLL is temporarily disabled (i.e. frozen) in precharge power-down (by MR0 bit A12).

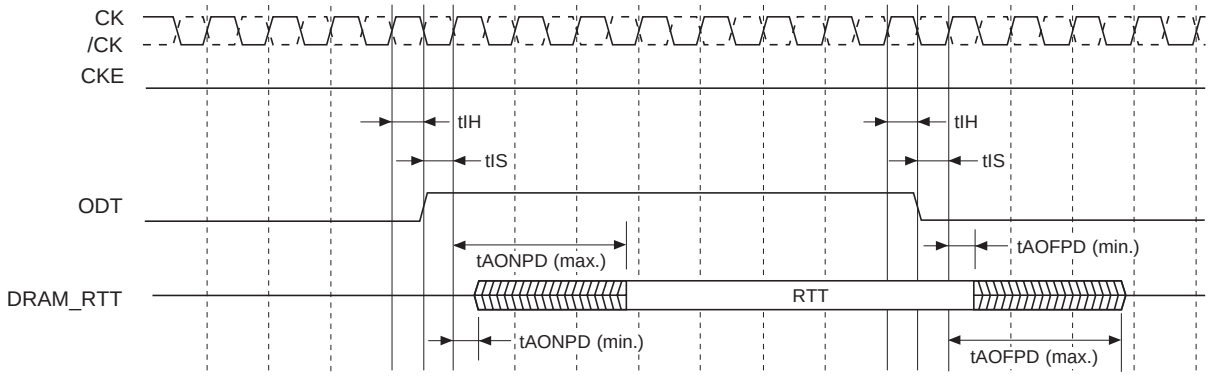
Precharge power-down mode if DLL is disabled during precharge power-down by MR0 bit A12.

In asynchronous ODT timing mode, internal ODT command is not delayed by Additive Latency (AL) relative to the external ODT command.

In asynchronous ODT mode, the following timing parameters apply (see figure Asynchronous ODT Timings): tAONPD (min.), (max.), tAOFPD (min.),(max.)

Minimum RTT turn-on time (tAONPD (min.)) is the point in time when the device termination circuit leaves high impedance state and ODT resistance begins to turn on. Maximum RTT turn-on time (tAONPD (max.)) is the point in time when the ODT resistance is fully on. tAONPD (min.) and tAONPD (max.) are measured from ODT being sampled high.

Minimum RTT turn-off time (tAOFPD (min.)) is the point in time when the devices termination circuit starts to turn off the ODT resistance. Maximum ODT turn-off time (tAOFPD (max.)) is the point in time when the on-die termination has reached high impedance. tAOFPD (min.) and tAOFPD (max.) are measured from ODT being sampled low.



Asynchronous ODT Timings on DDR3 SDRAM with Fast ODT Transition: AL is Ignored

In precharge power-down, ODT receiver remains active, however no read or write command can be issued, as the respective address/command receivers may be disabled.

[Asynchronous ODT Timing Parameters for All Speed Bins]

Symbol	Parameters	min.	max.	Unit
tAONPD	Asynchronous RTT turn-on delay (power-down with DLL frozen)	2	8.5	ns
tAOFPD	Asynchronous RTT turn-off delay (power-down with DLL frozen)	2	8.5	ns

[ODT for Power-Down (with DLL Frozen) Entry and Exit Transition Period]

Description	min.	max.
ODT to RTT turn-on delay	min {ODTLon × tCK + tAON(min.); tAONPD(min.) }	max {ODTLon × tCK + tAON(max.); tAONPD(max.) }
	min { (WL – 2.0) × tCK + tAON(min.); tAONPD(min.) }	max {(WL – 2.0) × tCK + tAON(max.); tAONPD(max.) }
ODT to RTT turn-off delay	min { ODTLoff × tCK +tAOF(min.); tAOFPD(min.) }	max { ODTLoff × tCK + tAOF(max.); tAOFPD(max.) }
	min { (WL – 2.0) × tCK +tAOF(min.); tAOFPD(min.) }	max {(WL – 2.0) × tCK + tAOF(max.); tAOFPD(max.) }
tANPD	WL – 1.0	

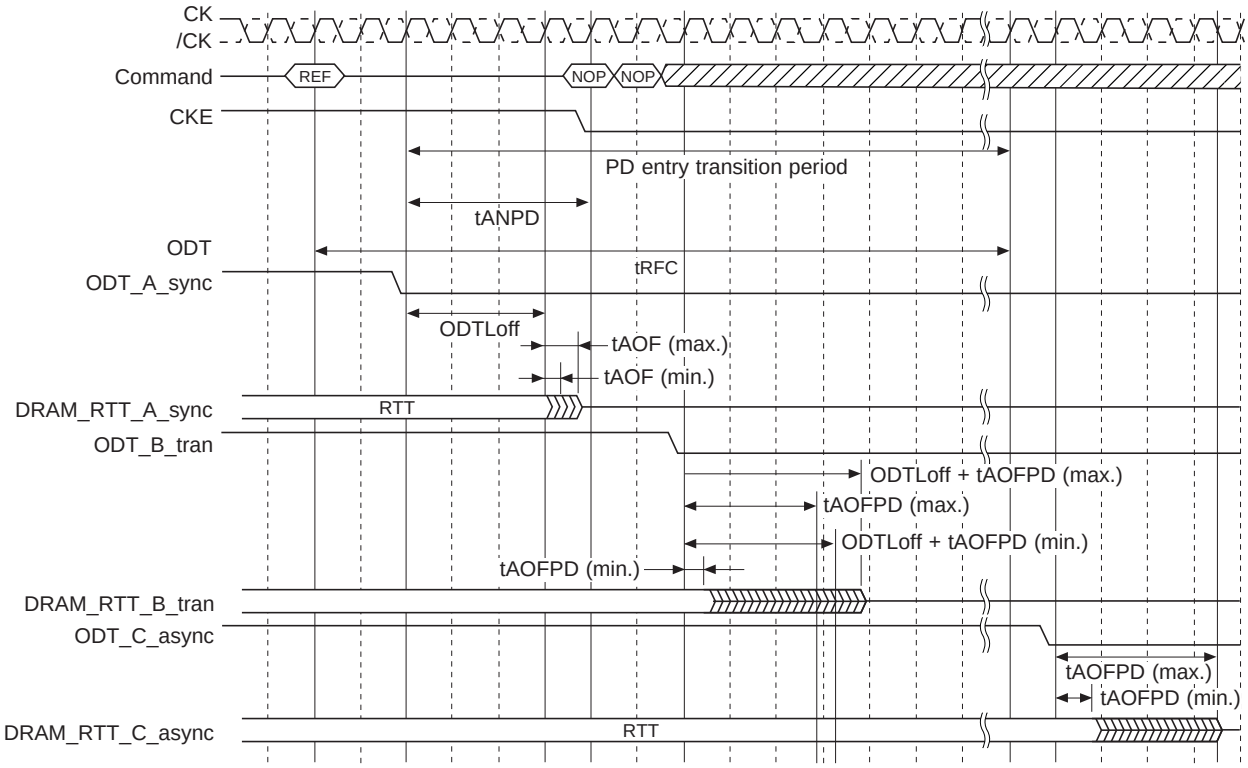
Synchronous to Asynchronous ODT Mode Transition during Power-Down Entry

If DLL is selected to be frozen in precharge power-down mode by the setting of bit A12 in MR0 to 0 there is a transition period around power-down entry, where the DDR3 SDRAM may show either synchronous or asynchronous ODT behavior.

This transition period ends when CKE is first registered low and starts tANPD before that. If there is a Refresh command in progress while CKE goes low, then the transition period ends tRFC after the refresh command. tANPD is equal to (WL – 1.0) and is counted (backwards) from the clock cycle where CKE is first registered low.

ODT assertion during the transition period may result in an RTT change as early as the smaller of tAONPD(min.) and (ODTLon × tCK + tAON(min.)) and as late as the larger of tAONPD(max.) and (ODTLon × tCK + tAON(max.)). ODT de-assertion during the transition period may result in an RTT change as early as the smaller of tAOFPD(min.) and (ODTLoff × tCK + tAOF(min.)) and as late as the larger of tAOFPD(max.) and (ODTLoff × tCK + tAOF(max.)). Note that, if AL has a large value, the range where RTT is uncertain becomes quite large.

The figure below shows the three different cases: ODT_A, synchronous behavior before tANPD; ODT_B has a state change during the transition period; ODT_C shows a state change after the transition period.



Synchronous to Asynchronous Transition During Precharge Power-Down (with DLL Frozen) Entry (AL = 0; CWL = 5; tANPD = WL – 1 = 4)

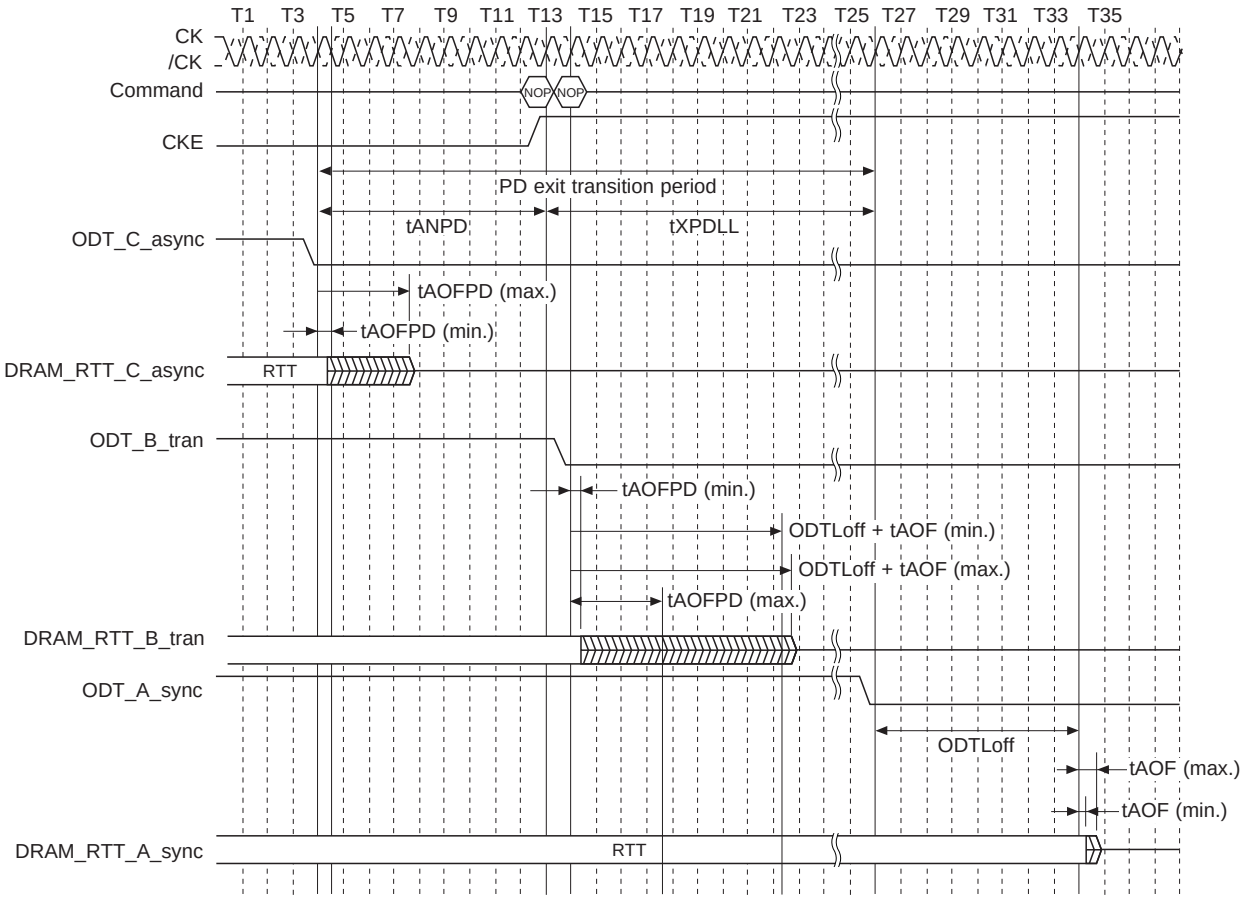
Asynchronous to Synchronous ODT Mode Transition during Power-Down Exit

If DLL is selected to be frozen in precharge power-down mode by the setting of bit A12 in MR0 to 0, there is also a transition period around power-down exit, where either synchronous or asynchronous response to a change in ODT must be expected from the DDR3 SDRAM.

This transition period starts tANPD before CKE is first registered high, and ends tXPDLL after CKE is first registered high. tANPD is equal to (WL – 1.0) and is counted backward from the clock cycle where CKE is first registered high.

ODT assertion during the transition period may result in an RTT change as early as the smaller of tAONPD(min.) and (ODTLon × tCK + tAON(min.)) and as late as the larger of tAONPD(max.) and (ODTLon × tCK + tAON(max.)). ODT de-assertion during the transition period may result in an RTT change as early as the smaller of tAOFPD(min.) and (ODTLoff × tCK + tAOF(min.)) and as late as the larger of tAOFPD(max.) and (ODTLoff × tCK + tAOF(max.)). See ODT for Power-Down (with DLL Frozen) Entry and Exit Transition Period table.

Note that, if AL has a large value, the range where RTT is uncertain becomes quite large. The figure below shows the three different cases: ODT_C, asynchronous response before tANPD; ODT_B has a state change of ODT during the transition period; ODT_A shows a state change of ODT after the transition period with synchronous response.



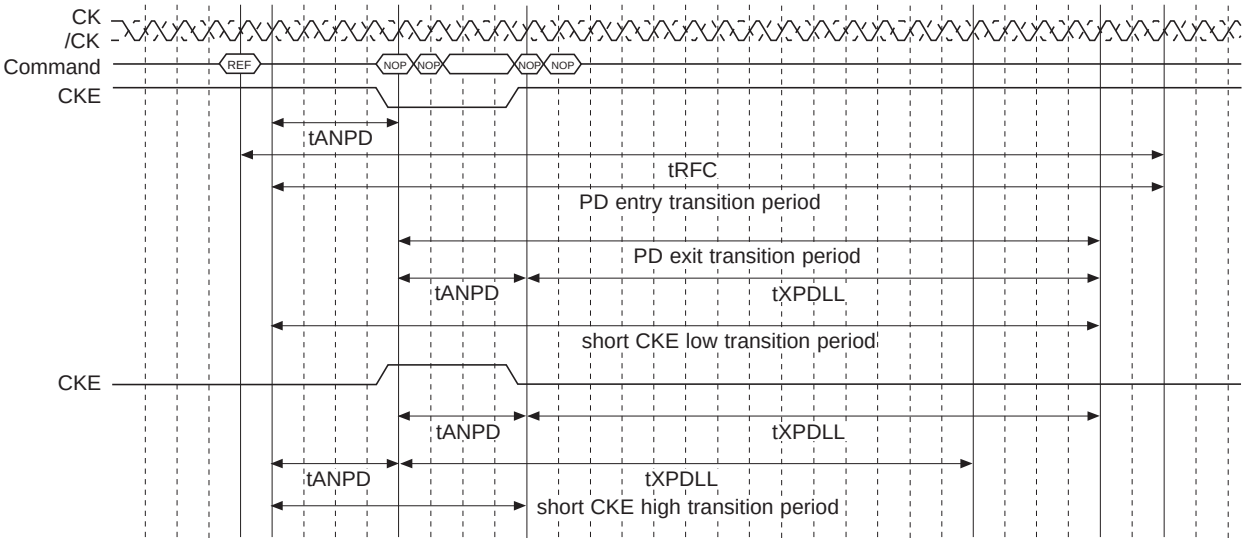
Asynchronous to Synchronous Transition during Precharge Power-Down (with DLL Frozen) Exit (CL = 6; AL = CL - 1; CWL = 5; tANPD= WL – 1 = 9)

Asynchronous to Synchronous ODT Mode during Short CKE high and Short CKE Low Periods

If the total time in precharge power-down state or idle state is very short, the transition periods for power-down entry and power-down exit may overlap. In this case the response of the DDR3 SDRAM RTT to a change in ODT state at the input may be synchronous OR asynchronous from the start of the power-down entry transition period to the end of the PD exit transition period (even if the entry period ends later than the exit period).

If the total time in idle state is very short, the transition periods for power-down exit and power-down entry may overlap. In this case the response of the DDR3 SDRAM RTT to a change in ODT state at the input may be synchronous OR asynchronous from the start of the power-down exit transition period to the end of the power-down entry transition period.

Note that in the bottom part of figure below it is assumed that there was no refresh command in progress when idle state was entered.



Transition Period for Short CKE Cycles with Entry and Exit Period Overlapping (AL = 0, WL = 5, tANPD = WL – 1 = 4)

ZQ Calibration

ZQ calibration command is used to calibrate DRAM RON and ODT values. DDR3 SDRAM needs longer time to calibrate RON and ODT at initialization and relatively smaller time to perform periodic calibrations.

ZQCL command is used to perform the initial calibration during power-up initialization sequence. This command may be issued at any time by the controller depending on the system environment. ZQCL command triggers the calibration engine inside the DRAM and once calibration is achieved the calibrated values are transferred from calibration engine to DRAM I/O which gets reflected as updated RON and ODT values.

The first ZQCL command issued after reset is allowed a timing period of tZQinit to perform the full calibration and the transfer of values. All other ZQCL commands except the first ZQCL command issued after RESET is allowed a timing period of tZQoper.

ZQCS command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter tZQCS.

One ZQCS command can effectively correct a minimum of 0.5% (ZQCorrection) of RON and RTT impedance error within 64nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(\text{Tsens} \times \text{Tdriftrate}) + (\text{Vsens} \times \text{Vdriftrate})}$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5%/°C, VSens = 0.15%/mV, Tdriftrate = 1°C/sec and Vdriftrate = 15mV/sec, then the interval between ZQCS commands is calculated as:

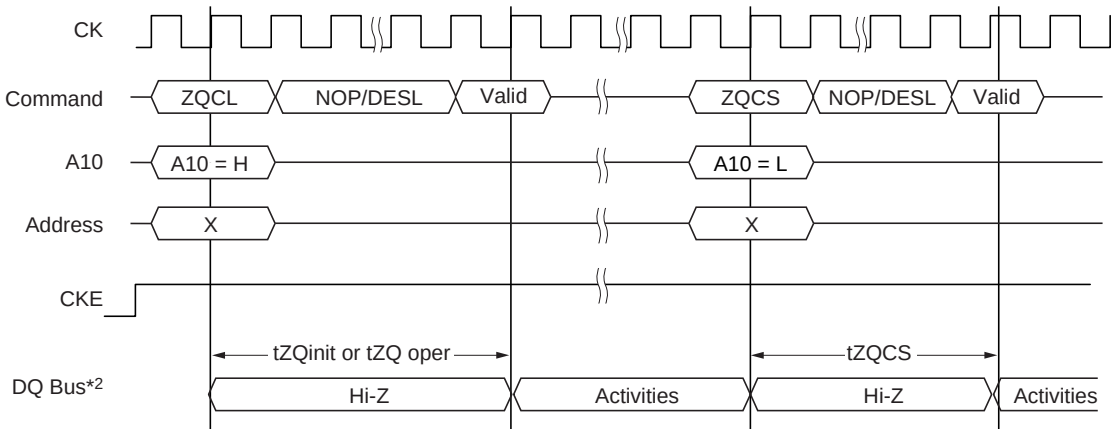
$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 = 128\text{ms}$$

No other activities should be performed on the DRAM channel by the controller for the duration of tZQinit, tZQoper or tZQCS. The quiet time on the DRAM channel allows in accurate calibration of RON and ODT. Once DRAM calibration is achieved the DRAM should disable ZQ current consumption path to reduce power.

All banks must be precharged and tRP met before ZQCL or ZQCS commands are issued by the controller.

ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self-refresh. Upon self-refresh exit, DDR3 SDRAM will not perform an IO calibration without an explicit ZQ calibration command. The earliest possible time for ZQ Calibration command (short or long) after self-refresh exit is tXS.

In dual rank systems that share the ZQ resistor between devices, the controller must not allow any overlap of tZQoper or tZQinit or tZQCS between ranks.



Notes: 1. ODT must be disabled via ODT signal or MRS during calibration procedure.
2. All device connected to DQ bus should be High impedance during calibration.

ZQ Calibration

ZQ External Resistor Value and Tolerance

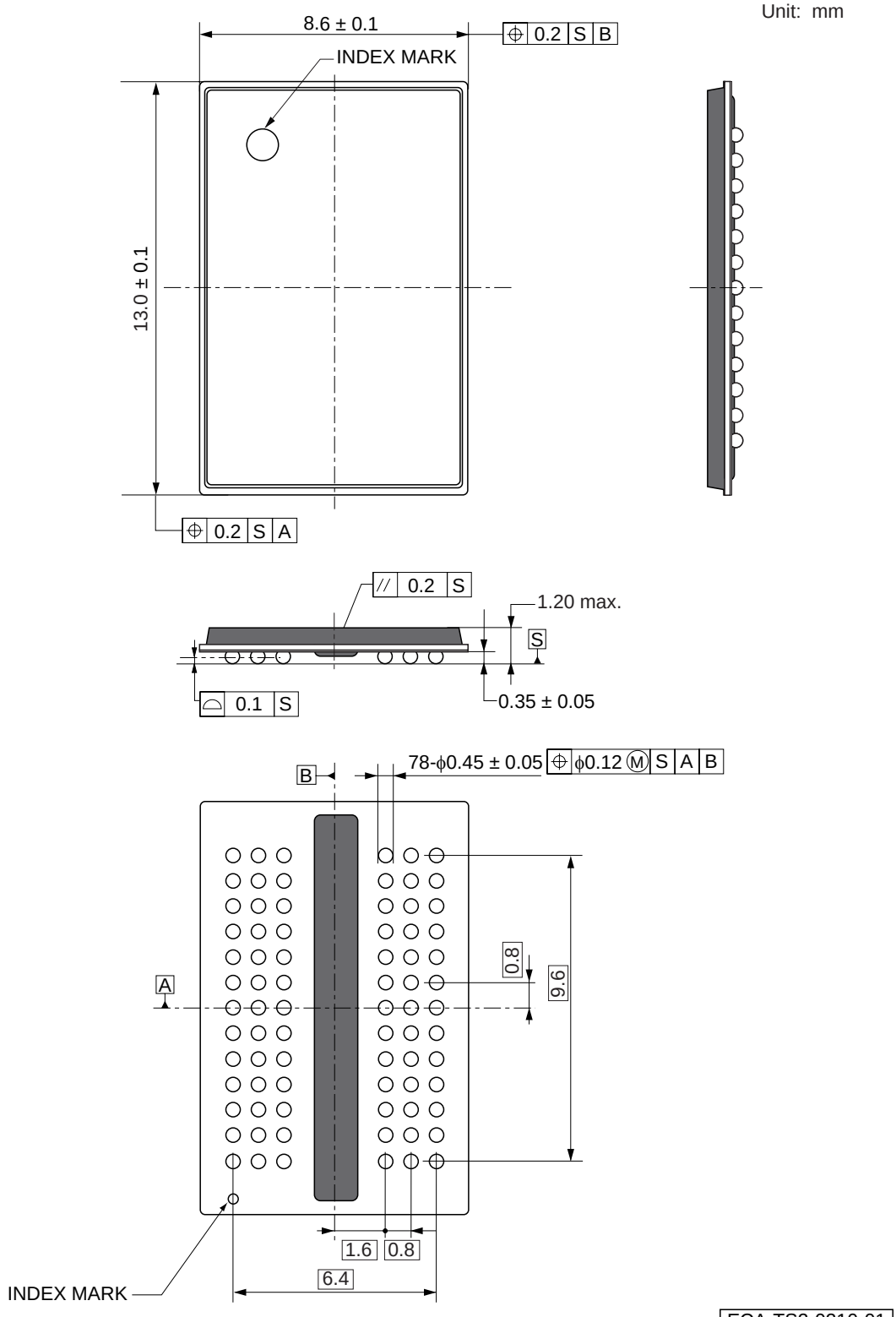
DDR3 SDRAM has a 240Ω, ±1% tolerance external resistor connecting from the DDR3 SDRAM ZQ pin to ground. The resister can be used as single DRAM per resistor.

Package Drawing

78-ball FBGA

Solder ball: Lead free (Sn-Ag-Cu)

Unit: mm

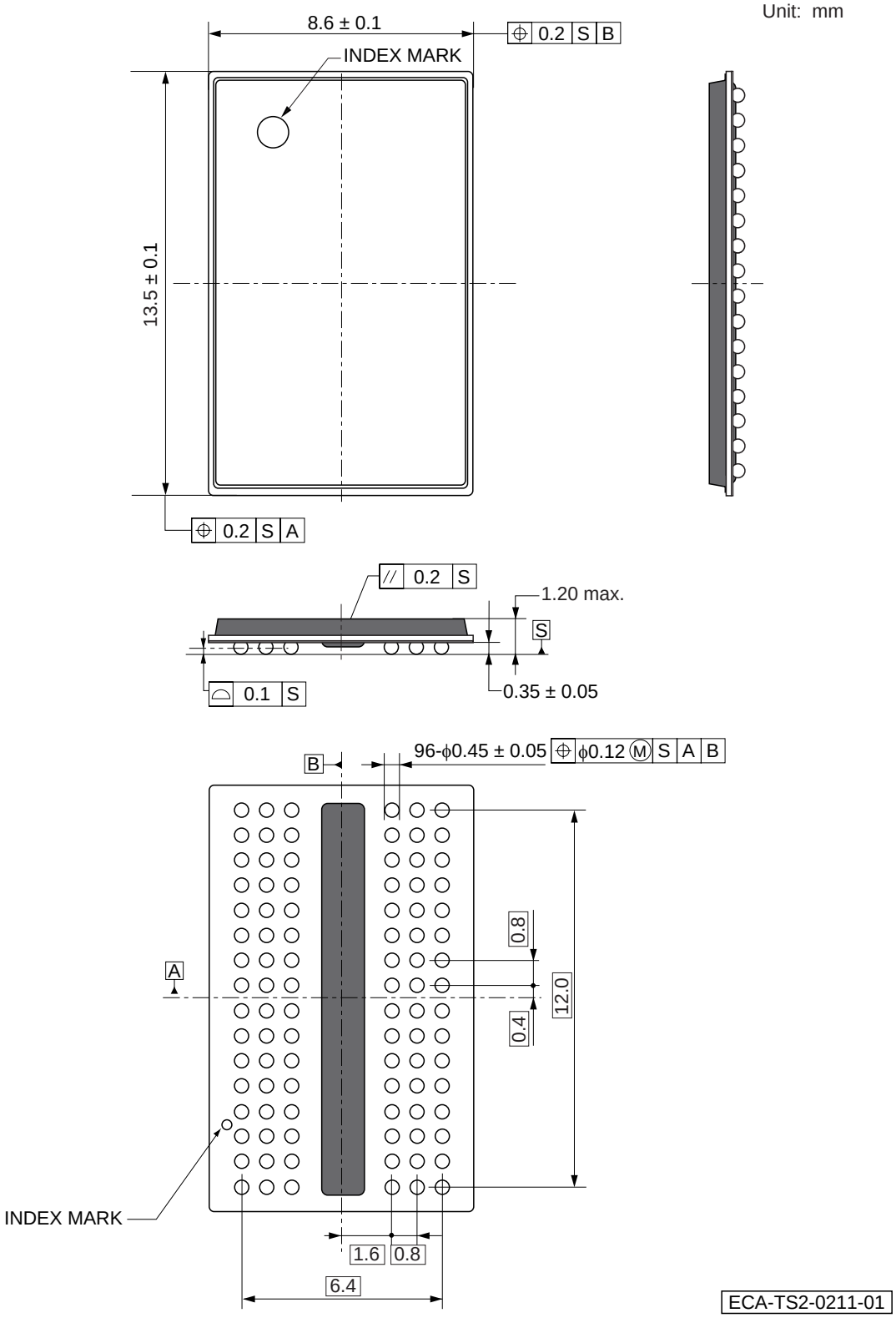


ECA-TS2-0210-01

96-ball FBGA

Solder ball: Lead free (Sn-Ag-Cu)

Unit: mm



ECA-TS2-0211-01

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the EDJ1104BASE, EDJ1108BASE, EDJ1116BASE.

Type of Surface Mount Device

EDJ1104BASE, EDJ1108BASE: 78-ball FBGA < Lead free (Sn-Ag-Cu) >
EDJ1116BASE: 96-ball FBGA < Lead free (Sn-Ag-Cu) >

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107

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[Product usage]
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[Usage environment]

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2) Usage in exposure to direct sunlight or the outdoors, or in dusty places.
3) Usage involving exposure to significant amounts of corrosive gas, including sea air, CL_2, H_2S, NH_3, SO_2, and NO_X.
4) Usage in environments with static electricity, or strong electromagnetic waves or radiation.
5) Usage in places where dew forms.
6) Usage in environments with mechanical vibration, impact, or stress.
7) Usage near heating elements, igniters, or flammable items.

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