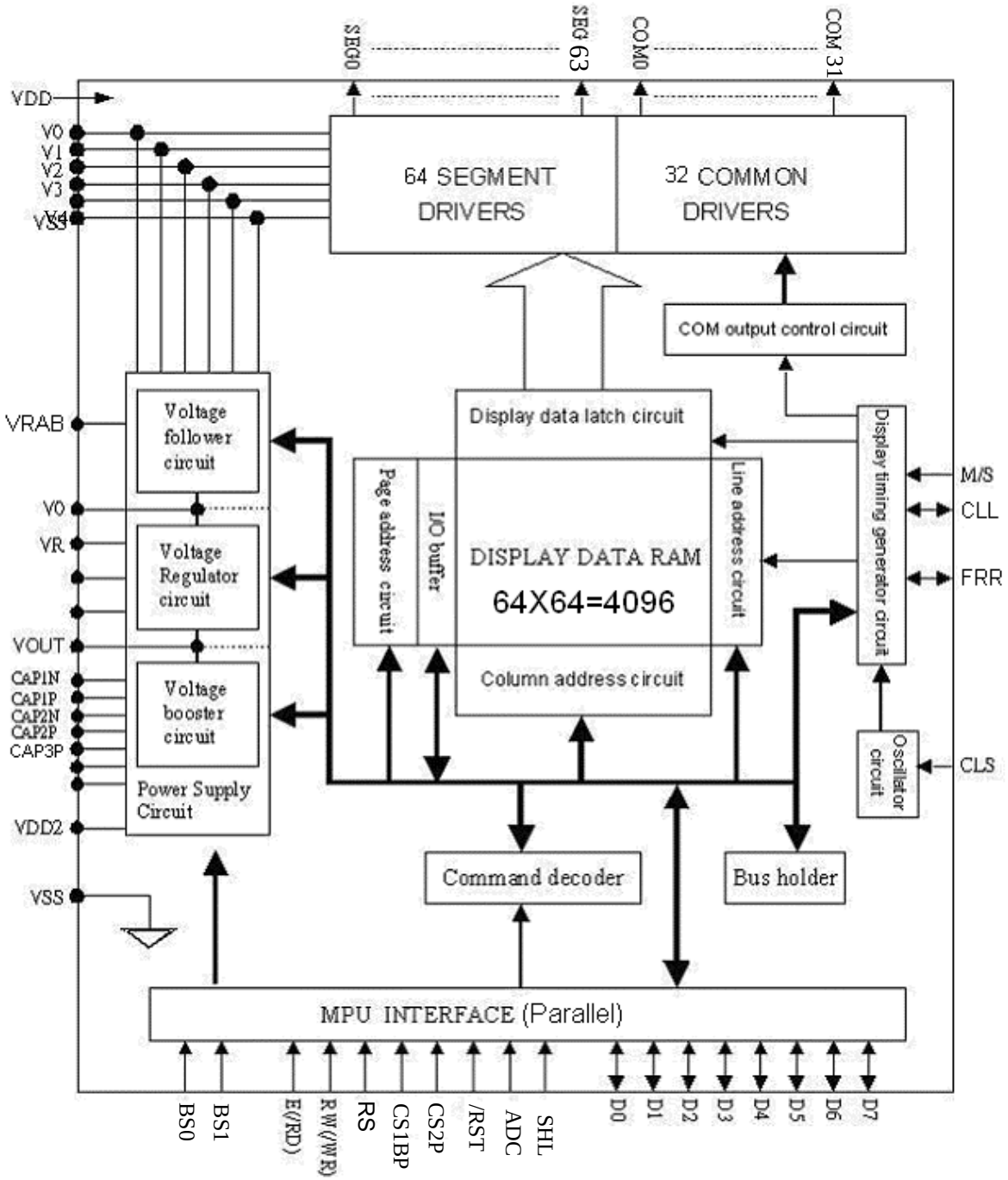
■ FEATURES

- Direct display of RAM data through the display data RAM.
- RAM capacity：64 x 64 = 4096 bits
- Display duty selectable by software
  1/64 duty：64common x 128segment (RW1065 x 2)
  64common x 192segment (RW1065 x 3)
  1/32 duty：32common x 128segment (RW1065 x 2)
  32common x 192segment (RW1065 x 3)
- High-speed 8-bit MPU interface (The chip can be connected directly to the 6800 series MPUs)
- Abundant command functions
  Display data Read/Write, display ON/OFF, Normal/Reverse display mode, page address set, display start line set, column address set, status read, display all point ON/OFF, read/modify/write, segment driver direction selects, power saver.
- Low-power liquid crystal display power supply circuit equipped internally.
- Bias set 1/5 1/6 1/8 1/9 by pin.
- Booster circuit (with Boost ratios of 2X/3X/4X, where the step-up voltage reference power supply can be input externally).
  V_0 voltage regulator resistors equipped externally, V_1 to V_4 voltage divider resistors equipped internally, voltage follower.
- CR oscillator circuit equipped internally (external clock can also be input)
- Low power consumption.
  Logic power supply $V_{DD} – V_{SS}$ = 2.7V to 5.5 V
  Boost reference voltage: $V_{DD2} – V_{SS}$ = 2.7V to 5.5V
  Booster maximum voltage limited V_{OUT}=17.0V
  Liquid crystal drive power supply:
  $V_0 – V_{SS}$ = 4.0V to 15.0 V
- Wide range of operating temperatures: –40 to 85°C
- CMOS process.
- Shipping forms include bare chip and COB.
- Software compatible to KS0108.

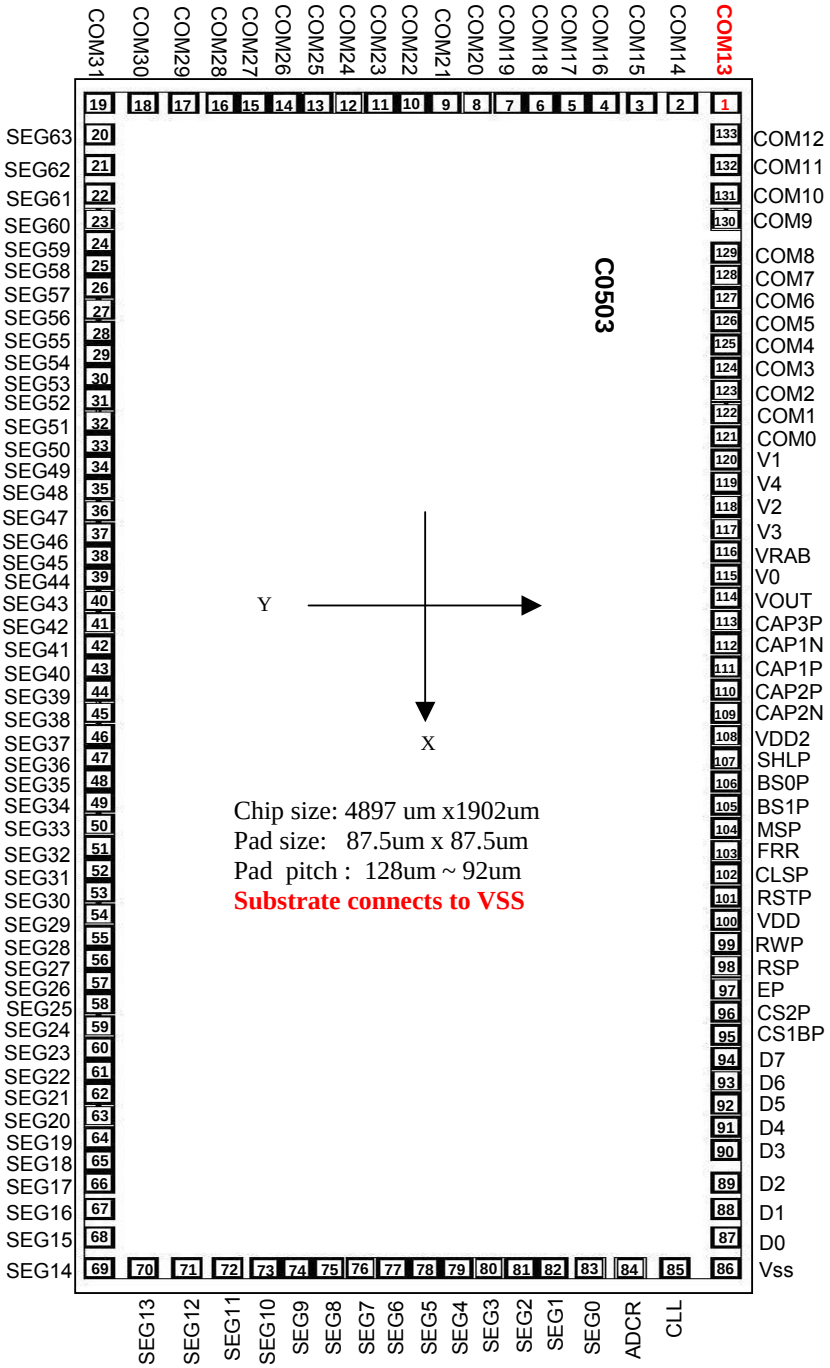
■ GENERAL DESCRIPTION

The RW1065 is a single-chip dot matrix LCD driver that can be connected directly to a microprocessor bus. 8-bit parallel display data sent from the microprocessor is stored in the internal display data RAM and the chip generates a LCD drive signal independent of the microprocessor. Because the chips in the RW1065 contain 64x64 bits of display data RAM and there is a 1-to-1 correspondence between the LCD panel pixels and the internal RAM bits, these chips enable displays with a high degree of freedom.
The RW1065 chips contain 32 common output circuits and 64 segment output circuits, so that two RW1065 chips can drive a 64x128 dot display (capable of displaying 8 columnsx4 rows of a 16x16 dot kanji font).
Moreover, the capacity of the display can be extended through the use of master/slave structures up to three RW1065 chips.
The chips are able to minimize power consumption because no external operating clock is necessary for the display data RAM read/write operation. Furthermore, because each chip is equipped internally with a low-power LCD driver power supply, and a display clock CR oscillator circuit, the RW1065 can be used to create the lowest power display system with the fewest components for high-performance portable devices.

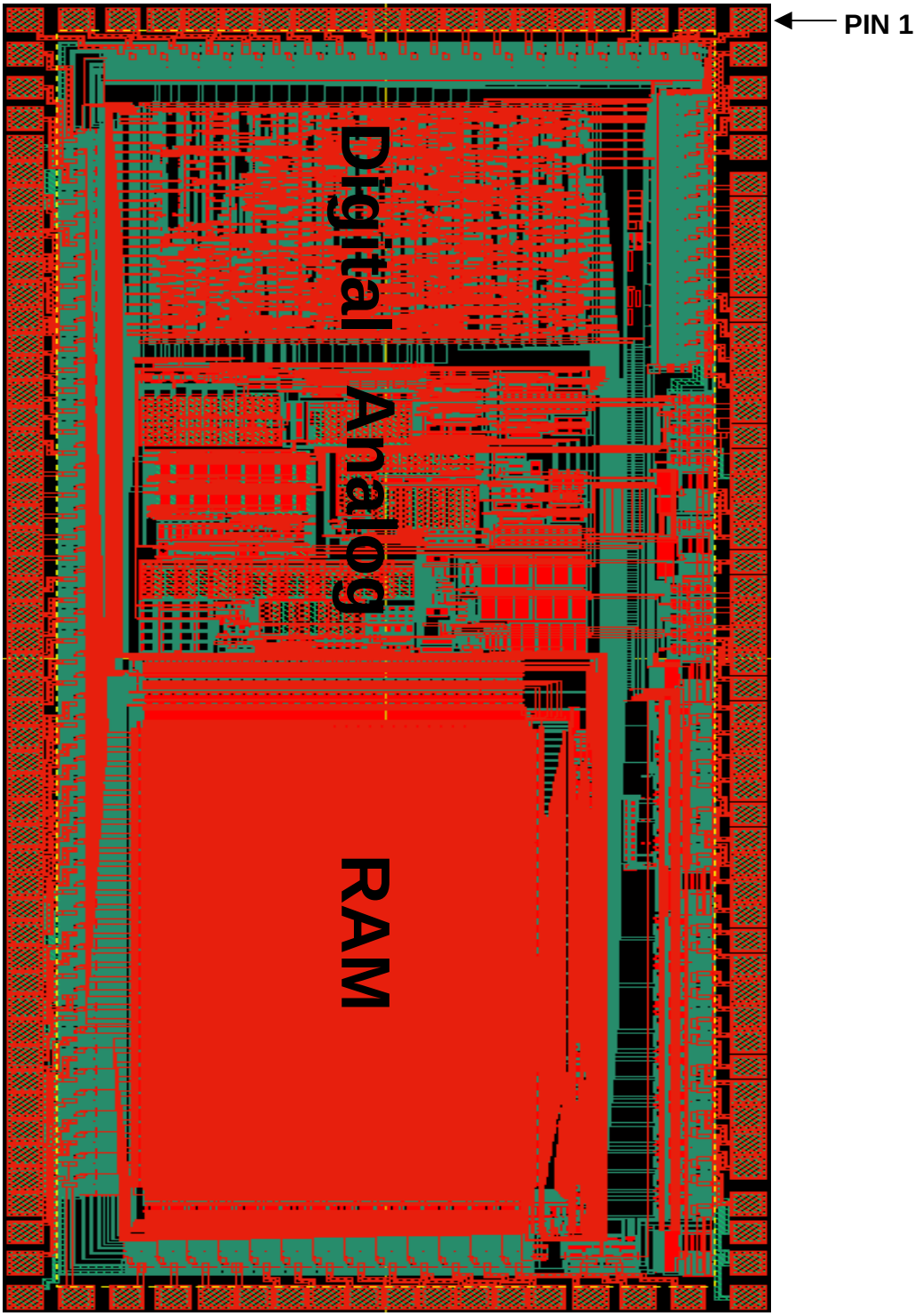
■ BLOCK DIAGRAM



■ PAD ARRANGEMENT



■ CHIP LAYOUT



■ Pin Description

(1)Power Pins

Name	I/O	Description
VDD	-	Connected to the +5V 0r +3V dc power. Common to the Vcc MPU power pin.
VDD2		This is the retevence power supply for the Step-up voltage circuit.
VSS	-	0V dc pin connected to the system ground.
CAP1P~3P CAP1N~2N	-	Capacitor connector pin for voltage booster.
V0~V4	-	Multi-level power supplies for LCD driving. The voltage determined for each liquid crystal cell is divided by resistance or it is converted in impedance by the op amp, and supplied. These voltages must satisfy the following: V0 ≧ V1 ≧ V2 ≧ V3 ≧V4 ≧ VSS

(2)System Bus Connection Pins

Name	I/O	Description
D7 to D0	I/O	The 8-bit bidirectional data buses to be connected to the 8- or 16- bit standard MCU Data busses.
RS	I	Usually connected to the low-order bit of the MPU address bus and used to identify the data or a command. RS=0: D0 to D7 are display control data. RS=1: D0 to D7 are display data.
CLS	I	CLS=1 : internal oscillator enable CLS=0 : external clock operation mode
ADCP	I	The pin selects the relationship between display data RAM column addresses and segment drivers. **ADCP=1: SEG0←column address 3FH,…..inverted** **ADCP=0: SEG0←column address 00H,…..normal**
SHLP	I	The pin selects the com output scan direction. **SHL=1: Reverse direction,com63→com0** **SHL=0: Normal com0→com63** **Both master and slave should set identical SHL value**
BS1P,BS0P	I	Select LCD Bias 1/5, 1/6, 1/8, 1/9 bias **BS1P=0, BS0P=0 : 1/5 bias** **BS1P=0, BS0P=1 : 1/6 bias** **BS1P=1, BS0P=0 : 1/8 bias** **BS1P=1, BS0P=1 : 1/9 bias**
$\overline{\text{RST}}$	I	Input low active. System reset.
CS1BP, CS2P	I	Input. When CS1BP = 0 and CS2P = 1 the chip select become active
E	I	● For 68-series MPU : Input. Active high. Used as an enable clock input of the 68-series MPU.
R/W	I	● For 68-series MPU : Input. Used as an input pin of read control signals (if R/W is high) or write control signals signals (if low).

(3)LCD Driver Circuit Signals

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>CLL</td><td>I/O</td><td>Input/output.
I/O selection
● M/S = “H” & CLS = “H” ：Output
● M/S = “L” & CLS = “H” ：Input
● M/S = “X” & CLS = “L” ：Input

This is a display data latch signal to count up the line counter and common counter at each signal falling and rising edges.</td></tr>
<tr><td>SEGn</td><td>O</td><td>Output.
A single level of V0, V2, V3 and VSS is selected by the combination of display RAM contents and FR signal.</td></tr>
<tr><td>COMn</td><td>O</td><td>Output.
The output pin for LCD common (row) driving. A single level of V0, V1, V4 and VSS is selected by the combination of common counter output and FR signal. The slave LSI has the reverse common output scan sequence than the master LSI.</td></tr>
<tr><td>FRR</td><td>I/O</td><td>Input/output.
This is the liquid crystal alternating current signal I/O terminal
I/O selection
● M/S = “H”：Output
● M/S = “L”：Input</td></tr>
<tr><td>VRAB</td><td>I</td><td>Provides the voltage between V0 and VSS through a resistive voltage divider.</td></tr>
<tr><td>M/S</td><td>I</td><td>Input.
The master or slave LSI operation select pin for the RW1065.
<table>
<tr><th>M/S</th><th>Operating Mode</th><th>FR</th><th>CL</th><th>V0~V4</th><th>Power Supply</th><th>Internal OSC</th><th>COMMON Output</th><th>SEG output</th></tr>
<tr><td>High</td><td>Master</td><td>Output</td><td>See CLS</td><td>On</td><td>On</td><td>See CLS</td><td>COM0-31</td><td>SEG0-63</td></tr>
<tr><td>Low</td><td>Slave</td><td>Input</td><td>Input</td><td>Off</td><td>Off</td><td>Off</td><td>COM32-63</td><td>SEG64-127</td></tr>
</table></td></tr>
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