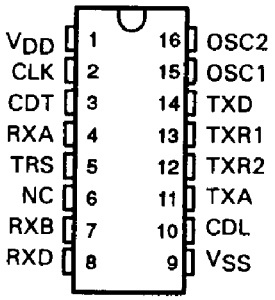
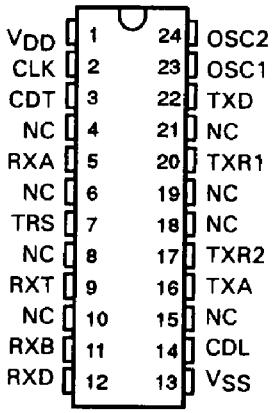
- Single-Chip Frequency-Shift-Keying (FSK) Modem
- Meets Both Bell 202 and CCITT V23 Specifications
- Transmit Modulation at 75, 150, 600, and 1200 Baud
- Receive Demodulation at 5, 75, 150, 600, and 1200 Baud
- Half-Duplex Operation Up to 1200 Baud Transmit and Receive
- Full-Duplex Operation Up to 1200 Baud Transmit and 150 Baud Receive
- On-Chip Group Delay Equalization and Transmit/Receive Filtering
- Carrier-Detect-Level Adjustment and Carrier-Fail Output
- Single 5-V Power Supply
- Low Power Consumption
- Reliable CMOS Silicon-Gate Technology

J OR N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC—No internal connection

D packages are available taped and reeled. Add "R" suffix to device type (e.g., TCM3105DWLR)

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

description

The TCM3105 is a single-chip asynchronous Frequency Shift Keying (FSK) voiceband modem that uses silicon gate CMOS technology to implement a switched capacitor architecture. It is pin selectable (TXR1, TXR2, and TRS inputs) for a wide range of transmit/receive baud rates and is compatible with the applicable BELL 202 or CCITT V23 standards. Operation is fully reversible, thereby allowing both forward and backward channels to be used simultaneously.

The transmitter is a programmable frequency synthesizer that provides two output frequencies (on TXA), representing the 'marks' and 'spaces' of the digital signal present on the TXD input.

The receive section is responsible for the demodulation of the analog signal appearing at the RXA input and is based on the principle of frequency-to-voltage conversion. This section contains a group delay equalizer (to correct phase distortion), automatic gain control, carrier detect level adjustment, and bias distortion adjustment, thereby optimizing performance and giving the lowest possible bit error rate.

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description (continued)

Carrier-detect information is given to the system by means of the carrier-detect circuits, which set a flag on the CDT output if the level of received in-band energy falls below a value set on the CDL input for a specified minimum duration.

The TCM3105DWE, TCM3105JE, and TCM3105NE are characterized for operation from −40°C to 85°C. The TCM3105DWL, TCM3105JL, and TCM3105NL are characterized for operation from 0°C to 70°C.

TERMINAL FUNCTIONS

PIN NAME	PIN NO. DW	PIN NO. J OR N	DESCRIPTION
CDL	14	10	Carrier Detect Level Adjust for external adjustment of carrier detect threshold
CDT	3	3	Carrier-Detect Output. A low-level output indicates carrier failure
CLK	2	2	Output for a continuous clock signal at 16 times the highest selected (transmit or receive) bit rate
NC	4, 6, 8, 10, 15, 18, 19, 21	6	No internal connection
OSC1	23	15	Oscillator connections. The crystal (typically 4.4336 MHz) is connected to these pins. If an external clock is used, OSC2 is left open and the clock is connected to OSC1.
OSC2	24	16	
RXA	5	4	Receive Analog Input to which the received line signal must be ac coupled
RXB	11	7	Receive Bias Adjust for external adjustment of the decision threshold of the final comparator to minimize bias distortion
RXD	12	8	Receiver Digital Output for the demodulated received data in positive logic. The high logic level is a mark and the low logic level is a space.
RXT	9	–	Receive test access. Output of limiter is available on this pin. (DW only)
TRS	7	5	Transmit/Receive Standard Select Input, which with TXR1 and TXR2, sets the standard bit rates and mark/space frequencies
TXA	16	11	Transmit Analog Output for the modulated signal, which must be ac coupled
TXD	22	14	Transmit Digital Input for input data to the transmitter in positive logic. The high logic level is a mark and the low logic level is a space. The data can be accepted at any speed from zero to the selected speed and may be totally asynchronous.
TXR1	20	13	Bit Rate Select 1 input, which, along with TXR2 and TRS, sets the bit rates and mark/space frequencies
TXR2	17	12	Bit Rate Select 2 input, which, along with TXR1 and TRS, sets the bit rates and mark/space frequencies
V_{DD}	1	1	Positive supply voltage
V_{SS}	13	9	Most negative supply voltage (normally ground); connected to substrate

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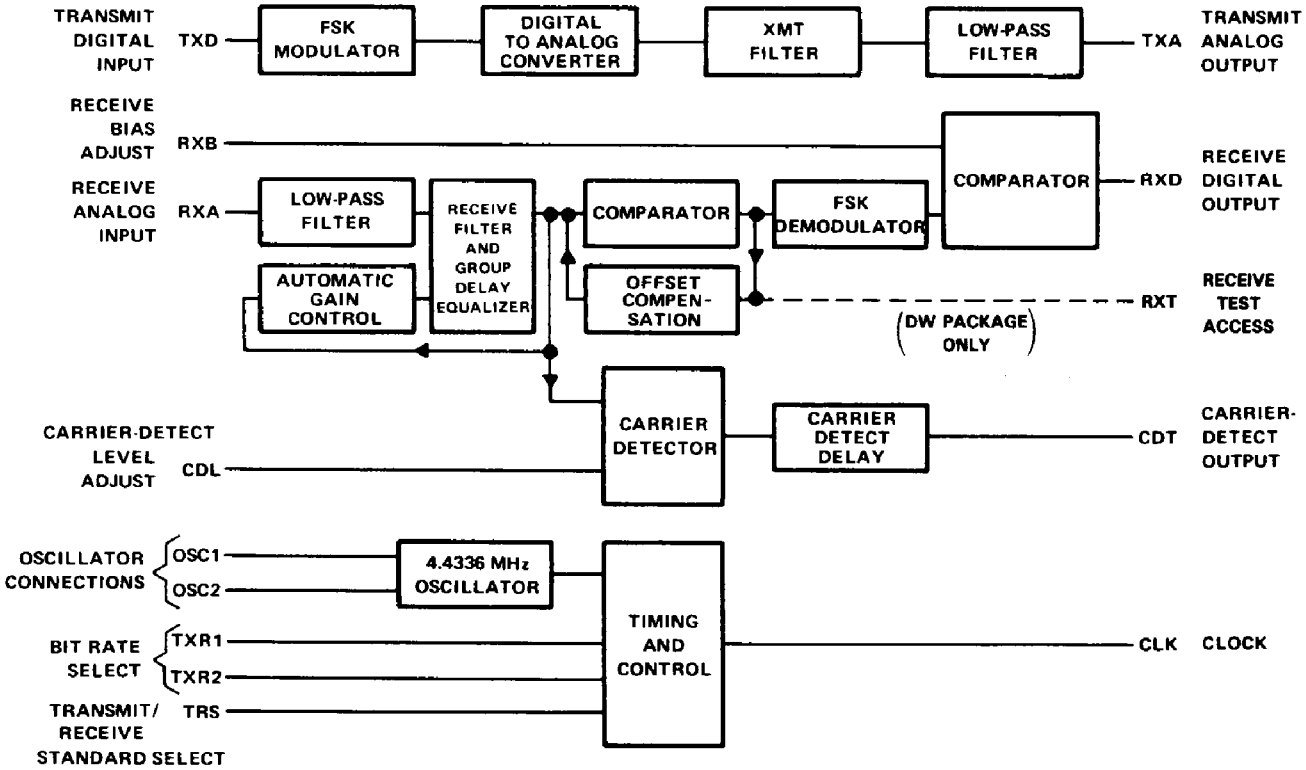
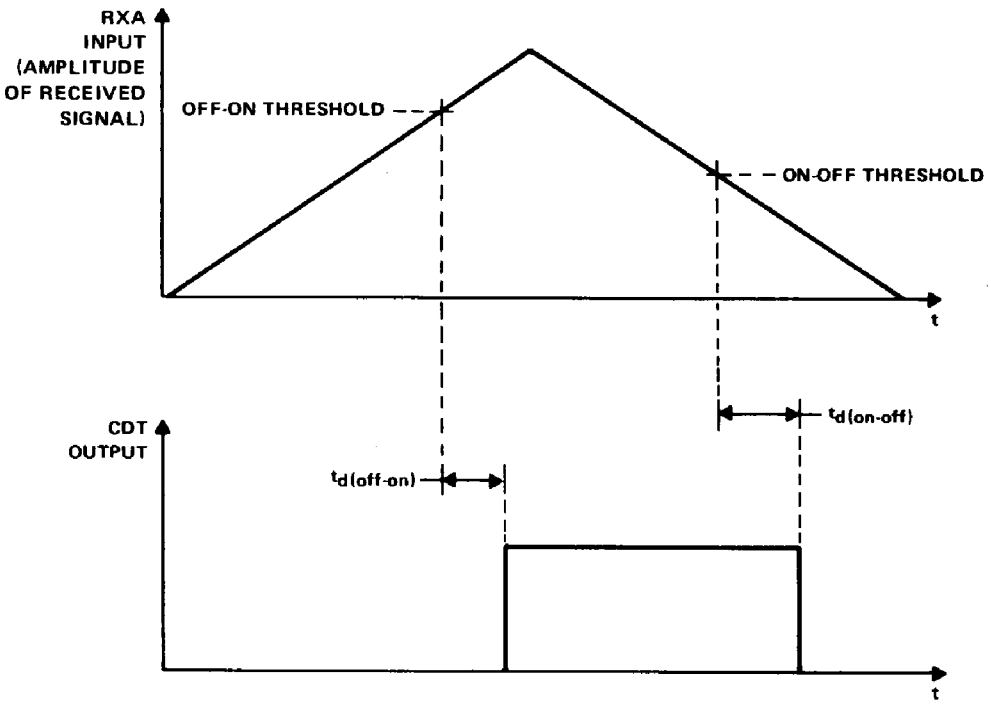
functional block diagram



timing diagram



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absolute maximum ratings over free-air operating temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . −0.3 V to 10 V
Input voltage, V_I (any input) . . . . . −0.3 to V_{DD}
Operating free-air temperature range: TCM3105DWL, TCM3105JL, TCM3105NL . . . . . −10°C to 70°C
TCM3105DWE, TCM3105JE, TCM3105NE . . . . . −55°C to 85°C
Storage temperature range . . . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

	TCM3105DWE TCM3105JE TCM3105NE			TCM3105DWL TCM3105JL TCM3105NL			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}	4	5	5.5	4	5	5.5	V
High-level input voltage, V_{IH}	2		V_{DD}	2		V_{DD}	V
Low-level input voltage, V_{IL}	0		0.8	0		0.8	V
Analog input level, peak-to-peak (ac coupled)		0.30	0.78		0.30	0.78	V
Clock frequency, f_{clock}	4.4334	4.4336	4.4338	4.4334	4.4336	4.4338	MHz
Analog load impedance at TXA	50			50			kΩ
Operating free-air temperature range, T_A	−40		85	0		70	°C

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		TCM3105DWE TCM3105JE TCM3105NE			TCM3105DWL TCM3105JL TCM3105NL			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	RXD, CDT, CLK	I_{OH} = −100 μA		2.4		V_{DD}	2.4		V_{DD}	V
V_{OL}	Low-level output voltage	RXD, CDT, CLK	I_{OL} = 1.6 mA		V_{SS}		0.4	V_{SS}		0.4	V
	Analog output voltage level, peak-to-peak	TXA	V_{DD} = 4 V	R_L = 50 kΩ, C_L = 100 pF		1.55			1.55		V
			V_{DD} = 5 V		1.4	1.9	2.3	1.4	1.9	2.3	
			V_{DD} = 5.5 V			2.1			2.1		
	Adjust voltage	RXB	V_{DD} = 5 V		2.3	2.7	3.1	2.3	2.7	3.1	V
		CDL			2.8	3.3	3.9	2.8	3.3	3.9	
	Analog output dc offset	TXA				$V_{DD}/2$			$V_{DD}/2$		V
	Digital input current	TXD, TRS, TXR1, TXR2	V_I = 0 to V_{DD}				±1			±1	μA
	Analog input current	RXA					±15			±15	μA
	Bias input current	RXB, CDL	V_I = 3 V				±150			±150	μA
I_{DD}	Supply current		V_{DD} = 4 V			3	6		3	5	mA
			V_{DD} = 5 V			5	10		5	8	
			V_{DD} = 5.5 V			8	16		8	12	
C_i	Input capacitance, all inputs		f = 1 MHz			10			10		pF
C_o	Output capacitance, all inputs		f = 1 MHz			10			10		pF
	Phase jitter						200			200	μs
	Bias distortion‡						±15%			±15%	
	Carrier detect threshold, off-on§				−45.5		−43	−45.5		−43	dBm
	Carrier detect threshold, on-off§				−48		−45.5	−48		−45.5	dBm
	Carrier detect hysteresis				2.5	2.8		2.5	2.8		dBm

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Bias distortion is the departure from a 50% duty cycle when a series of alternating mark and space tones is received.
§This is the threshold with the CDL input properly adjusted.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TCM3105DWE TCM3105JE TCM3105NE			TCM3105DWL TCM3105JL TCM3105NL			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{d(off-on)}$	Carrier detect off-to-on delay time	RX = 600 or 1200 b/s	12		25	12		25	ms
		RX = 5, 75, or 150 b/s	48		80	48		80	
$t_{d(on-off)}$	Carrier detect on-to-off delay time	RX = 600 or 1200 b/s	12		20	12		20	ms
		RX = 5, 75, or 150 b/s	48		75	48		75	
	Transmit frequency deviation from assignment (see Table 1)	f_{clock} = 4.4336 MHz		±1			±1		Hz

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

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PRINCIPLES OF OPERATION

The TCM3105 FSK modem is made up of four functional circuits. The circuits are the transmitter, the receiver, a carrier detector, and control and timing (See Figure 1).

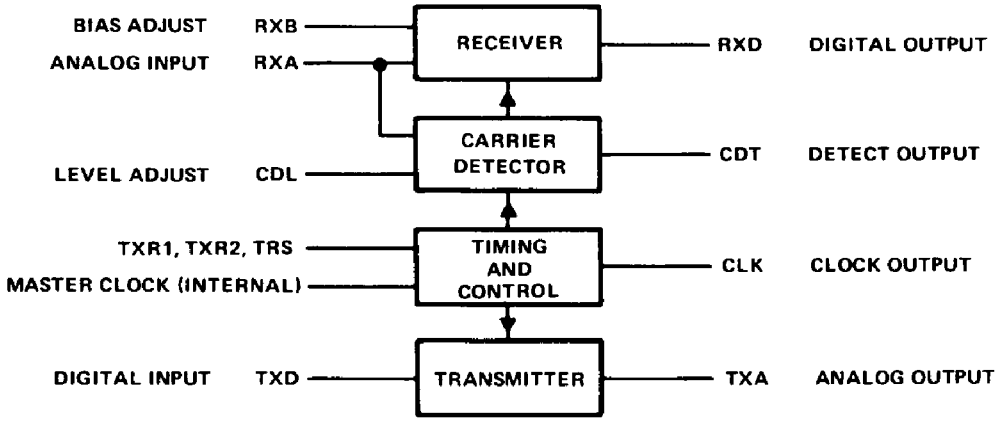

FIGURE 1. TCM3105 SYSTEM PARTITIONING

transmitter

The transmitter comprises a phase coherent FSK modulator, a transmit filter, and a transmit amplifier. The modulator is a programmable frequency synthesizer that drives the output frequencies by variable division of the oscillator frequency (4.4336 MHz). The division ratio is set by the states of the Transmit/Receive Standard input (TRS), the Bit Rate Select inputs (TXR1 and TXR2), and the Digital Data input (TXD).

A switched-capacitor low-pass filter limits the harmonics and noise outside the transmit band and the characteristics of this filter are set by the frequency select inputs as previously described. The harmonics introduced by the transmit filter clock are removed by a continuous low-pass filter.

The transmitter output level varies with power supply voltage and so must be compensated in the 2-wire to 4-wire converter to give a constant output level to the line.

receiver

A continuous low-pass anti-aliasing filter is followed by the receive amplifier, which automatically controls the gain to give a constant output level from the receive filter. The receive filter limits the bandwidth of the signal presented to the demodulator, reducing out-of-band interference, and has very high rejection of the transmit channel frequencies. These are typically present at much higher levels than the received signal.

The group delay equalizer is a switched-capacitor network that compensates the delay introduced by the receive filter and the network. The output from the equalizer is then limited to give an FSK modulated squarewave that is presented to the demodulator.

The demodulator is an edge-triggered multivibrator that triggers off positive and negative going edges. The output of the demodulator is, therefore, a stream of constant-length pulses at a frequency that is double the frequency of the limited input signal. The dc component of this signal is proportional to the received frequency and is extracted by a switched-capacitor, low-pass, post-demodulator filter.

The variation of dc level with received frequency is presented to a comparator that slices at a level externally fixed by the RXB bias adjustment pin. This voltage depends on received bit rate and internal offsets. The comparator output is then the received data at the RXD output.

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carrier detect

The carrier detect circuits comprise an energy detector and digital delay. The energy detector compares the total signal level at the output of the receive filter to an externally set threshold level on the CDL input. The comparator has a 2.5-dB hysteresis and a delay to allow for momentary signal loss and to prevent oscillation. The output of the detector is available on the CDT pin where a high level indicates that a carrier is present. The data output is clamped to a MARK condition when the carrier detect output switches off at the end of transmission.

control and timing

An on-chip oscillator runs from an external 4.4336-MHz crystal connected between the OSC1 and OSC2 pins or an external signal driving OSC1. A clock signal equal to 16 times the highest selected bit rate (transmit or receive) is available on the CLK output.

The single-supply rail means that all analog functions are referenced to an internally generated reference. All analog inputs and output must be ac coupled.

transmit and receive modes

The various modes of operation of the TCM3105 are given in Table 1. The data convention is that a logic high is a mark and a logic low is a space.

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TABLE 1. MODES OF OPERATION

STANDARD	TRS	TXR1	TXR2	TRANSMITTED BAUD RATE	RECEIVED BAUD RATE	TRANSMIT FREQUENCY ASSIGNMENTS (Hz)	RECEIVE FREQUENCY ASSIGNMENTS (Hz)	CLK FREQUENCY (kHz)
CCITT V.23	L	L	L	1200	1200	M 1300 S 2100	M 1300 S 2100	19.11
	H	L	L	1200	75	M 1300 S 2100	M 390 S 450	19.11
	L	L	H	600	75	M 1300 S 1700	M 390 S 450	9.56
	H	L	H	600	600	M 1300 S 1700	M 1300 S 1700	9.56
	L	H	L	75	1200	M 390 S 450	M 1300 S 2100	19.11
	H	H	L	75	600	M 390 S 450	M 1300 S 1700	9.56
	L	H	H	75	75	M 390 S 450	M 390 S 450	1.19
BELL 202	$\overline{CLK}$	L	L	1200	1200	M 1200 S 2200	M 1200 S 2200	19.11
	$\overline{CLK}$/8	L	H	1200	150	M 1200 S 2200	M 387 S 487	19.11
	$\overline{CLK}$/8	L	H	1200	5	M 1200 S 2200	M 387 S 0	19.11
	CLK	H	L	150	1200	M 387 S 487	M 1200 S 2200	19.11
	CLK	H	H	150	150	M 387 S 487	M 387 S 487	2.39
	CLK†	H†	L†	5	1200	M 387 S 0	M 1200 S 2200	19.11
	H†	H†	H†					
	H	H	H	Transmit Disabled	1200	Transmit Disabled	M 1200 S 2200	19.11

H = high level, L = low level
†In these modes, the modulation is controlled by the TRS and TXR2 pins. TXD is tied high.

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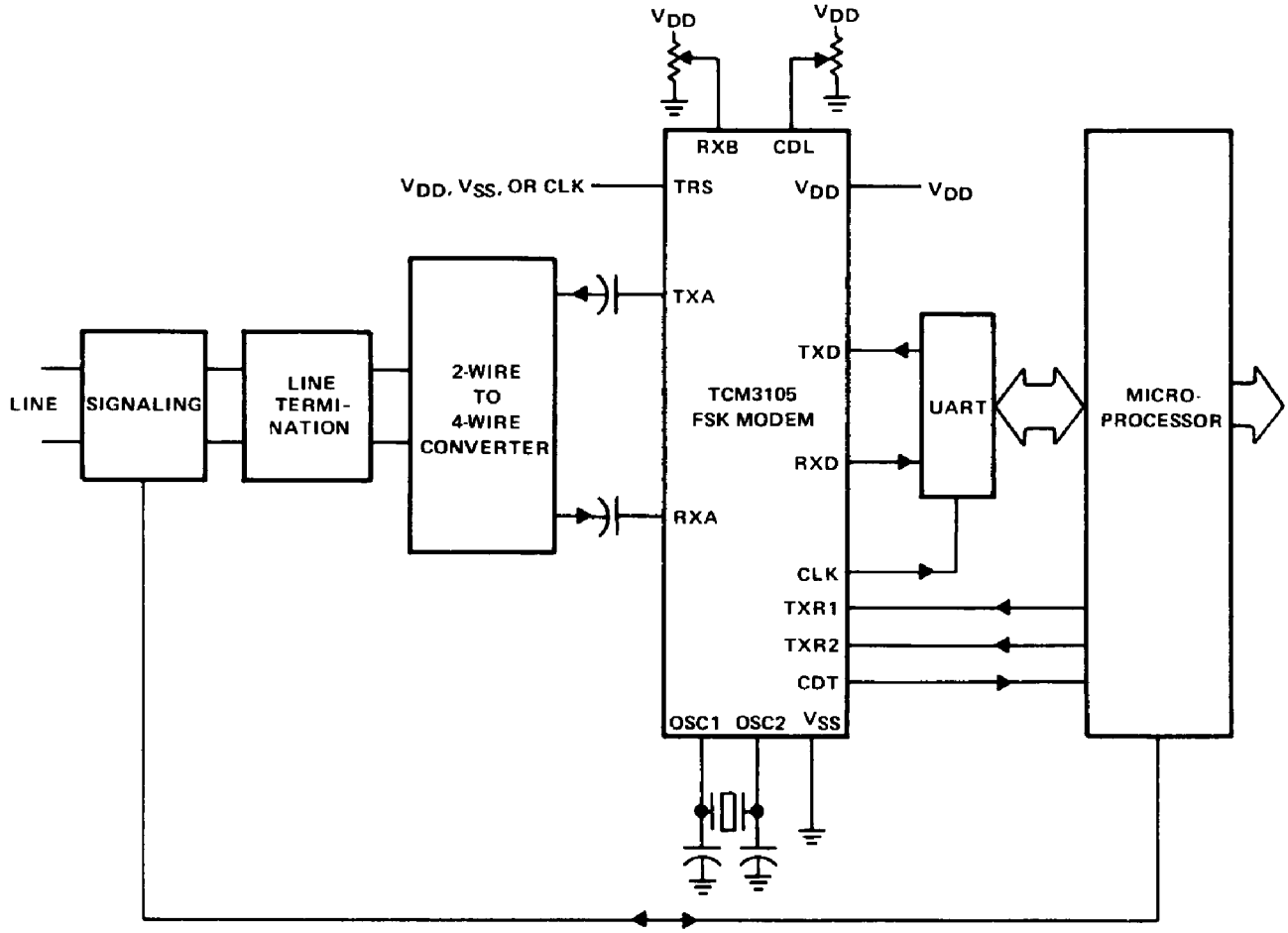

FIGURE 2. TYPICAL SYSTEM CONFIGURATION

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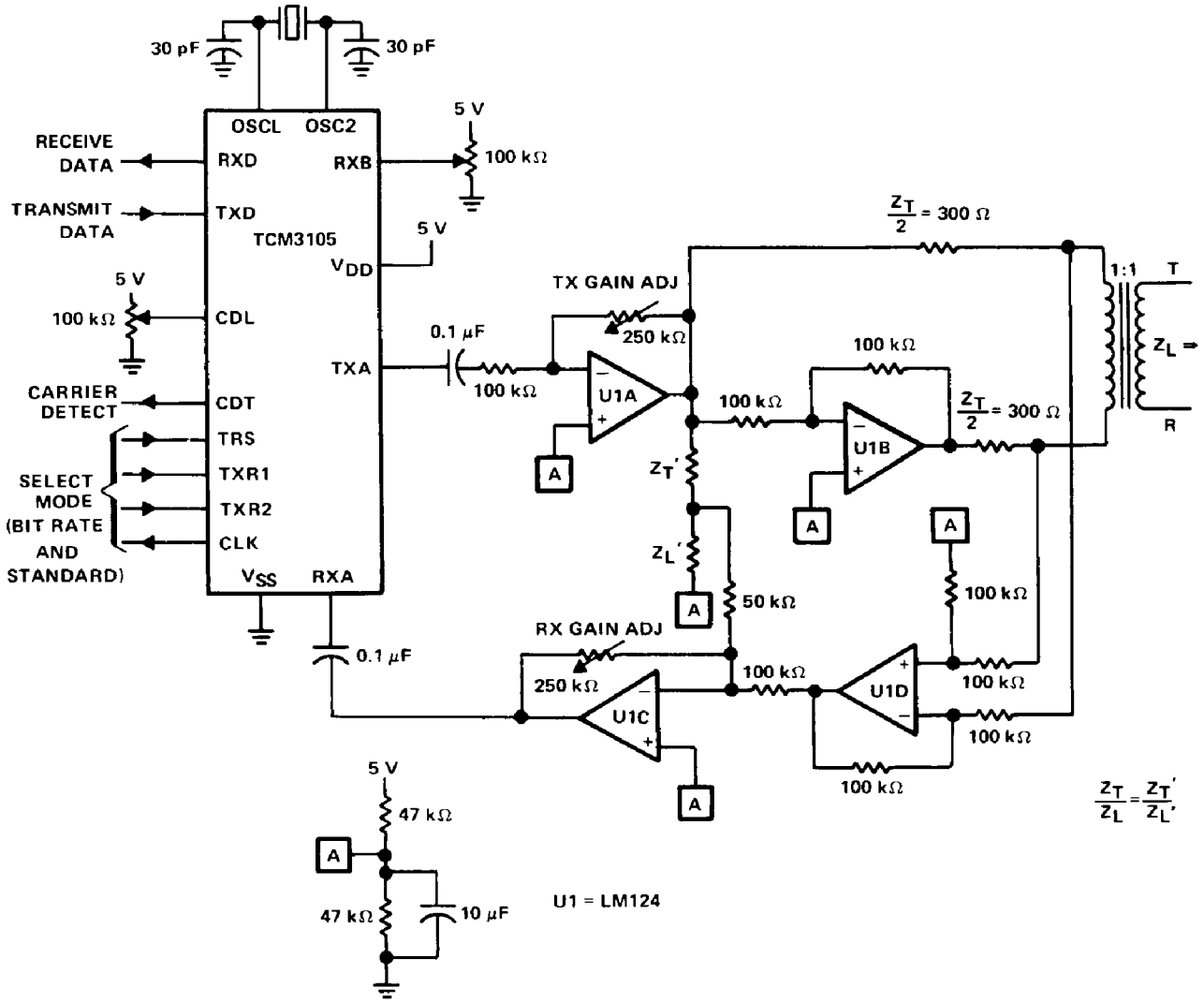

FIGURE 3. TELEPHONE LINE INTERFACE CIRCUIT

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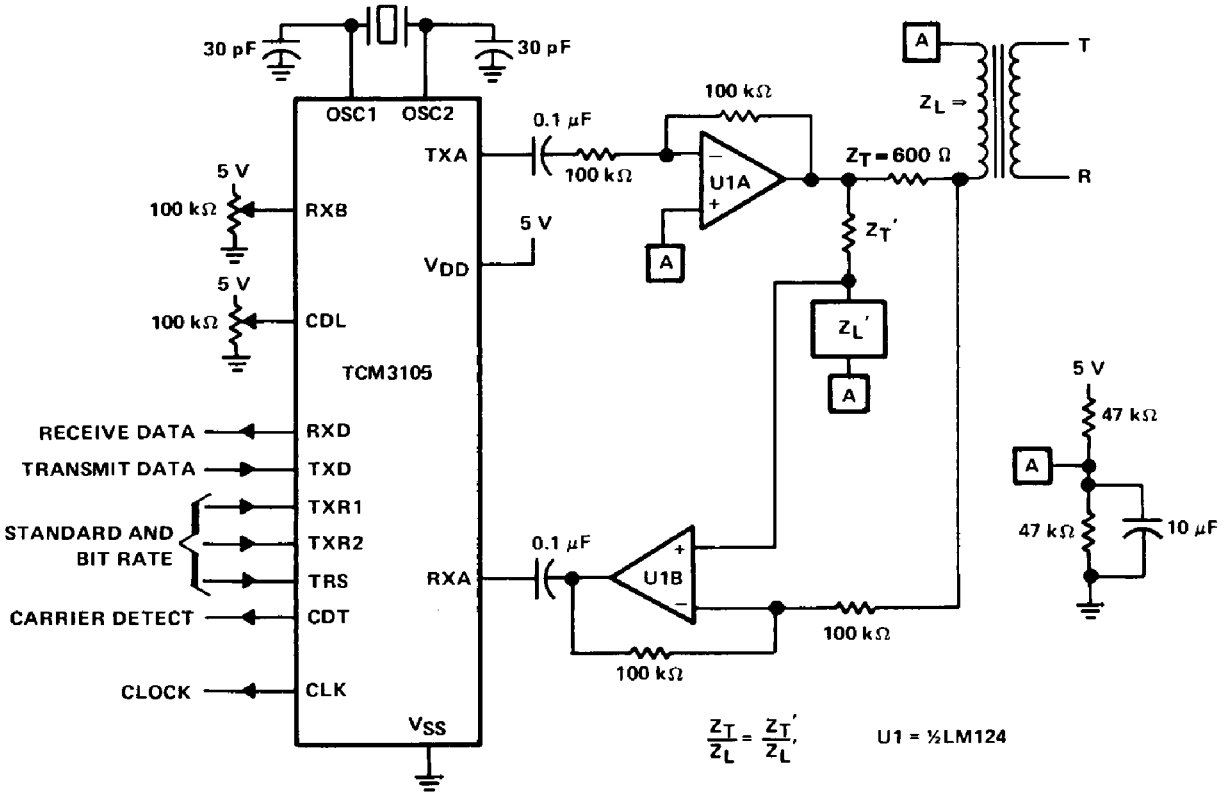

FIGURE 4. SIMPLIFIED TELEPHONE LINE INTERFACE CIRCUIT

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