HFA1130

850MHz, Output Limiting, Low Distortion Current Feedback Operational Amplifier

FN3369
Rev 5.00
April 25, 2013

The HFA1130 is a high speed wideband current feedback amplifier featuring programmable output limits. Built with Intersil's proprietary complementary bipolar UHF-1 process, it is the fastest monolithic amplifier available from any semiconductor manufacturer.

This amplifier is the ideal choice for high frequency applications requiring output limiting, especially those needing ultra fast overdrive recovery times. The output limiting function allows the designer to set the maximum positive and negative output levels, thereby protecting later stages from damage or input saturation. The sub-nanosecond overdrive recovery time quickly returns the amplifier to linear operation, following an overdrive condition.

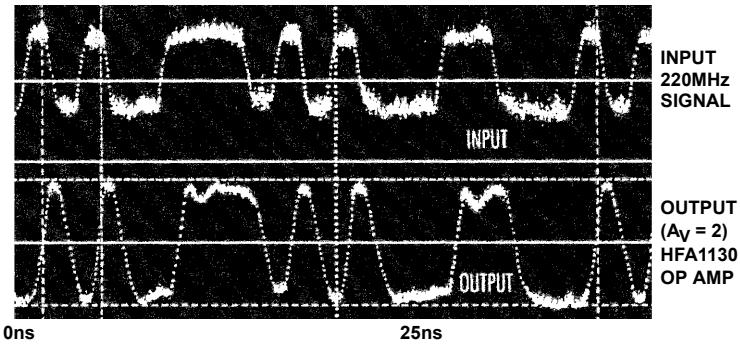
The HFA1130 offers significant performance improvements over the CLC500/501/502.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
HFA1130IBZ	1130 IBZ	-40 to +85	8 Ld SOIC	M8.15
HFA1130IBZ-T	1130 IBZ	-40 to +85	8 Ld SOIC	M8.15
HFA11XXEVAL	DIP Evaluation Board for High-Speed Op Amps			

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

The Op Amps with Fastest Edges



Features

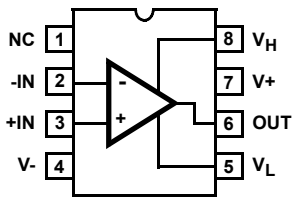
- User Programmable Output Voltage Limits
- Low Distortion (30MHz, HD2) . . . . . -56dBc
- -3dB Bandwidth 850MHz
- Very Fast Slew Rate. 2300V/µs
- Fast Settling Time (0.1%). 11ns
- Excellent Gain Flatness
  - (100MHz) 0.14dB
  - (50MHz) 0.04dB
  - (30MHz) 0.01dB
- High Output Current 60mA
- Overdrive Recovery . . . . . <1ns
- Pb-Free (RoHS Compliant)

Applications

- Residue Amplifier
- Video Switching and Routing
- Pulse and Video Amplifiers
- Wideband Amplifiers
- RF/IF Signal Processing
- Flash A/D Driver
- Medical Imaging Systems
- Related Literature
  - AN9420, Current Feedback Theory
  - AN9202, HFA11XX Evaluation Fixture

Pinout

HFA1130 (SOIC)
TOP VIEW



Absolute Maximum Ratings T_A = +25°C

Voltage Between V+ and V- 12V
Input Voltage . . . . . V_{SUPPLY}
Differential Input Voltage 5V
Output Current (50% Duty Cycle) 60mA

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package	170	N/A

Maximum Junction Temperature (Plastic Package). . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to T_A to 150°C
Pb-Free Reflow Profilesee link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEST LEVEL (Note 2)	TEMP. (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage (Note 3)		A	+25	-	2	6	mV
		A	Full	-	-	10	mV
Input Offset Voltage Drift		C	Full	-	10	-	µV/°C
V_{IO} CMRR	ΔV_{CM} = ±2V	A	+25	40	46	-	dB
		A	Full	38	-	-	dB
V_{IO} PSRR	ΔV_S = ±1.25V	A	+25	45	50	-	dB
		A	Full	42	-	-	dB
Non-Inverting Input Bias Current (Note 3)	+IN = 0V	A	+25	-	25	40	µA
		A	Full	-	-	65	µA
$+I_{BIAS}$ Drift		C	Full	-	40	-	nA/°C
$+I_{BIAS}$ CMS	ΔV_{CM} = ±2V	A	+25	-	20	40	µA/V
		A	Full	-	-	50	µA/V
Inverting Input Bias Current (Note 3)	-IN = 0V	A	+25	-	12	50	µA
		A	Full	-	-	60	µA
$-I_{BIAS}$ Drift		C	Full	-	40	-	nA/°C
$-I_{BIAS}$ CMS	ΔV_{CM} = ±2V	A	+25	-	1	7	µA/V
		A	Full	-	-	10	µA/V
$-I_{BIAS}$ PSS	ΔV_S = ±1.25V	A	+25	-	6	15	µA/V
		A	Full	-	-	27	µA/V
Non-Inverting Input Resistance		A	+25	25	50	-	kΩ
Inverting Input Resistance		C	+25	-	20	30	Ω
Input Capacitance (Either Input)		B	+25	-	2	-	pF
Input Common Mode Range		C	Full	±2.5	±3.0	-	V
Input Noise Voltage (Note 3)	100kHz	B	+25	-	4	-	$nV/\sqrt{Hz}$
+Input Noise Current (Note 3)	100kHz	B	+25	-	18	-	$pA/\sqrt{Hz}$
-Input Noise Current (Note 3)	100kHz	B	+25	-	21	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS A_V = +2, Unless Otherwise Specified							
Open Loop Transimpedance (Note 3)		B	+25	-	300	-	kΩ

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEST LEVEL (Note 2)	TEMP. (°C)	MIN	TYP	MAX	UNITS
-3dB Bandwidth (Note 3)	V_{OUT} = 0.2V_{P-P}, A_V = +1	B	+25	530	850	-	MHz
-3dB Bandwidth	V_{OUT} = 0.2V_{P-P}, A_V = +2, R_F = 360Ω	B	+25	-	670	-	MHz
Full Power Bandwidth	4V_{P-P}, A_V = -1	B	Full	-	300	-	MHz
Gain Flatness (Note 3)	To 100MHz	B	+25	-	±0.14	-	dB
Gain Flatness	To 50MHz	B	+25	-	±0.04	-	dB
Gain Flatness	To 30MHz	B	+25	-	±0.01	-	dB
Linear Phase Deviation (Note 3)	DC to 100MHz	B	+25	-	0.6	-	°
Differential Gain	NTSC, R_L = 75Ω	B	+25	-	0.03	-	%
Differential Phase	NTSC, R_L = 75Ω	B	+25	-	0.05	-	°
Minimum Stable Gain		A	Full	1	-	-	V/V
OUTPUT CHARACTERISTICS A_V = +2, Unless Otherwise Specified							
Output Voltage (Note 3)	A_V = -1	A	+25	±3.0	±3.3	-	V
		A	Full	±2.5	±3.0	-	V
Output Current	R_L = 50Ω, A_V = -1	A	+25, +85	50	60	-	mA
		A	-40	35	50	-	mA
DC Closed Loop Output Impedance (Note 3)		B	+25	-	0.07	-	Ω
2nd Harmonic Distortion (Note 3)	30MHz, V_{OUT} = 2V_{P-P}	B	+25	-	-56	-	dBc
3rd Harmonic Distortion (Note 3)	30MHz, V_{OUT} = 2V_{P-P}	B	+25	-	-80	-	dBc
3rd Order Intercept (Note 3)	100MHz	B	+25	20	30	-	dBm
1dB Compression	100MHz	B	+25	15	20	-	dBm
TRANSIENT RESPONSE A_V = +2, Unless Otherwise Specified							
Rise Time	V_{OUT} = 2.0V Step	B	+25	-	900	-	ps
Overshoot (Note 3)	V_{OUT} = 2.0V Step	B	+25	-	10	-	%
Slew Rate	A_V = +1, V_{OUT} = 5V_{P-P}	B	+25	-	1400	-	V/µs
	A_V = +2, V_{OUT} = 5V_{P-P}	B	+25	1850	2300	-	V/µs
0.1% Settling Time (Note 3)	V_{OUT} = 2V to 0V	B	+25	-	11	-	ns
0.2% Settling Time (Note 3)	V_{OUT} = 2V to 0V	B	+25	-	7	-	ns
POWER SUPPLY CHARACTERISTICS							
Supply Voltage Range		B	Full	±4.5	-	±5.5	V
Supply Current (Note 3)		A	+25	-	21	26	mA
		A	Full	-	-	33	mA
LIMITING CHARACTERISTICS A_V = +2, V_H = +1V, V_L = -1V, Unless Otherwise Specified							
Clamp Accuracy	V_{IN} = ±2V, A_V = -1	A	+25	-	60	±125	mV
Clamped Overshoot	V_{IN} = ±1V, Input t_R/t_F = 2ns	B	+25	-	4	-	%

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEST LEVEL (Note 2)	TEMP. (°C)	MIN	TYP	MAX	UNITS
Overdrive Recovery Time	V_{IN} = ±1V	B	+25	-	0.75	1.5	ns
Negative Clamp Range		B	+25	-	-5.0 to +2.0	-	V
Positive Clamp Range		B	+25	-	-2.0 to +5.0	-	V
Clamp Input Bias Current		A	+25	-	50	200	µA
Clamp Input Bandwidth	V_H or V_L = 100mV_{P-P}	B	+25	-	500	-	MHz

NOTES:

2. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.
3. See Typical Performance Curves for more information.

Application Information

Optimum Feedback Resistor (R_F)

The enclosed plots of inverting and non-inverting frequency response detail the performance of the HFA1130 in various gains. Although the bandwidth dependency on A_{CL} isn't as severe as that of a voltage feedback amplifier, there is an appreciable decrease in bandwidth at higher gains. This decrease can be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and the R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1130 design is optimized for a 510Ω R_F, at a gain of +1. Decreasing R_F in a unity gain application decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback causes the same problems due to the feedback impedance decrease at higher frequencies). At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth. The table below lists recommended R_F values for various gains, and the expected bandwidth.

A_{CL}	R_F (Ω)	BW (MHz)
+1	510	850
-1	430	580
+2	360	670
+5	150	520
+10	180	240
+19	270	125

Clamp Operation

General

The HFA1130 features user programmable output clamps to limit output voltage excursions. Clamping action is obtained by applying voltages to the V_H and V_L terminals (pins 8 and 5) of the amplifier. V_H sets the upper output limit, while V_L sets the lower clamp level. If the amplifier tries to drive the output above V_H, or below V_L, the clamp circuitry limits the output voltage at V_H or V_L (± the clamp accuracy), respectively. The low input bias currents of the clamp pins allow them to be driven by simple resistive divider circuits, or active elements such as amplifiers or DACs.

Clamp Circuitry

Figure 1 shows a simplified schematic of the HFA1130 input stage, and the high clamp (V_H) circuitry. As with all current feedback amplifiers, there is a unity gain buffer (Q_{X1} - Q_{X2}) between the positive and negative inputs. This buffer forces -IN to track +IN, and sets up a slewing current of (V_{-IN} - V_{OUT})/R_F. This current is mirrored onto the high impedance node (Z) by Q_{X3}-Q_{X4}, where it is converted to a voltage and fed to the output via another unity gain buffer. If no clamping is utilized, the high impedance node may swing within the limits defined by Q_{P4} and Q_{N4}. Note that when the output reaches it's quiescent value, the current flowing through -IN is reduced to only that small current ($-I_{BIAS}$) required to keep the output at the final voltage.

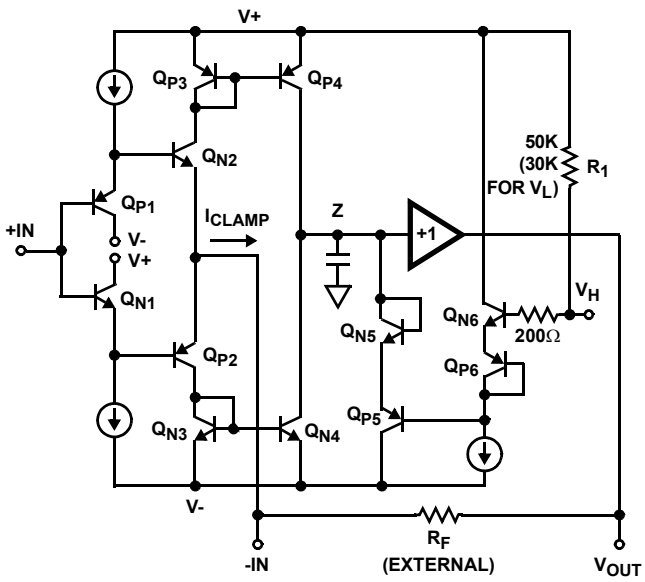


FIGURE 1. HFA1130 SIMPLIFIED V_H CLAMP CIRCUITRY

Tracing the path from V_H to Z illustrates the effect of the clamp voltage on the high impedance node. V_H decreases by $2V_{BE}$ (Q_{N6} and Q_{P6}) to set up the base voltage on Q_{P5}. Q_{P5} begins to conduct whenever the high impedance node reaches a voltage equal to Q_{P5}'s base + $2V_{BE}$ (Q_{P5} and Q_{N5}). Thus, Q_{P5} clamps node Z whenever Z reaches V_H. R_1 provides a pull-up network to ensure functionality with the clamp inputs floating. A similar description applies to the symmetrical low clamp circuitry controlled by V_L.

When the output is clamped, the negative input continues to source a slewing current (I_{CLAMP}) in an attempt to force the output to the quiescent voltage defined by the input. Q_{P5} must sink this current while clamping, because the -IN current is always mirrored onto the high impedance node. The clamping current is calculated as $(V_{-IN} - V_{OUT})/R_F$. As an example, a unity gain circuit with V_{IN} = 2V, V_H = 1V, and R_F = 510Ω would have I_{CLAMP} = (2-1)/510Ω = 1.96mA. Note that I_{CC} will increase by I_{CLAMP} when the output is clamp limited.

Clamp Accuracy

The clamped output voltage will not be exactly equal to the voltage applied to V_H or V_L. Offset errors, mostly due to V_{BE} mismatches, necessitate a clamp accuracy parameter which is found in the device specifications. Clamp accuracy is a function of the clamping conditions. Referring again to Figure 1, it can be seen that one component of clamp accuracy is the V_{BE} mismatch between the Q_{X6} transistors, and the Q_{X5} transistors. If the transistors always ran at the same current level there would be no V_{BE} mismatch, and no contribution to the inaccuracy. The Q_{X6} transistors are biased at a constant current, but as described earlier, the current through Q_{X5} is equivalent to I_{CLAMP}. V_{BE} increases as I_{CLAMP} increases, causing the clamped output voltage to increase as well. I_{CLAMP} is a function of the overdrive level (V_{-IN} -$V_{OUTCLAMPED}$) and R_F, so clamp accuracy degrades as the overdrive increases, or as R_F decreases. As an example, the specified accuracy of ±60mV for a 2X overdrive with R_F = 510Ω degrades to ±220mV for R_F = 240Ω at the same overdrive, or to ±250mV for a 3X overdrive with R_F = 510Ω.

Consideration must also be given to the fact that the clamp voltages have an effect on amplifier linearity. The "Nonlinearity Near Clamp Voltage" curve in the data sheet illustrates the impact of several clamp levels on linearity.

Clamp Range

Unlike some competitor devices, both V_H and V_L have usable ranges that cross 0V. While V_H must be more positive than V_L, both may be positive or negative, within the range restrictions indicated in the specifications. For example, the HFA1130 could be limited to ECL output levels by setting V_H = -0.8V and V_L = -1.8V. V_H and V_L may be connected to the same voltage (GND for instance) but the result won't be in a DC output voltage from an AC input signal. A 150 - 200mV AC signal will still be present at the output.

Recovery from Overdrive

The output voltage remains at the clamp level as long as the overdrive condition remains. When the input voltage drops below the overdrive level (V_{CLAMP}/A_{VCL}) the amplifier will return to linear operation. A time delay, known as the Overdrive Recovery Time, is required for this resumption of linear operation. The plots of "Unclamped Performance" and "Clamped Performance" highlight the HFA1130's subnanosecond recovery time. The difference between the unclamped and clamped propagation delays is the overdrive recovery time. The appropriate propagation delays are 4.0ns for the unclamped pulse, and 4.8ns for the clamped (2X overdrive) pulse yielding an overdrive recovery time of 800ps. The measurement uses the 90% point of the output transition to ensure that linear operation has resumed. Note: The propagation delay illustrated is dominated by the fixturing. The delta shown is accurate, but the true HFA1130 propagation delay is 500ps.

Use of Die in Hybrid Applications

This amplifier is designed with compensation to negate the package parasitics that typically lead to instabilities. As a result, the use of die in hybrid applications results in overcompensated performance due to lower parasitic capacitances. Reducing R_F below the recommended values for packaged units will solve the problem. For A_V = +2 the recommended starting point is 300Ω, while unity gain applications should try 400Ω.

PC Board Layout

The frequency performance of this amplifier depends a great deal on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value chip (0.1μF) capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Output capacitance, such as that resulting from an improperly terminated transmission line will degrade the frequency response of the amplifier and may cause oscillations. In most cases, the oscillation can be avoided by placing a resistor in series with the output.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to pin 2, and connections to pin 2 should be kept as short as possible.

An example of a good high frequency layout is the Evaluation Board shown below.

Evaluation Board

An evaluation board is available for the HFA1130, (Part Number HFA11XXEVAL). Please contact your local sales office for information.

Note: The SOIC version may be evaluated in the DIP board by using a SOIC-to-DIP adapter such as Aries Electronics Part Number 08-350000-10.

The layout and schematic of the board are shown here:

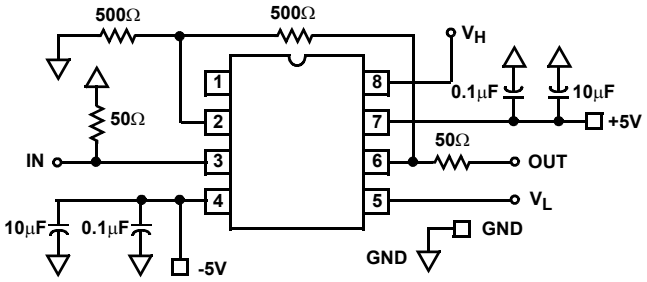
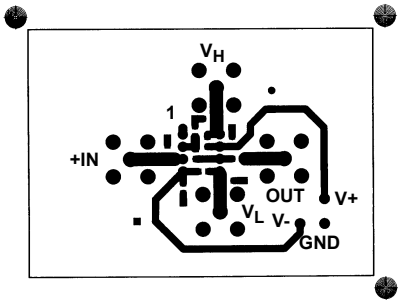
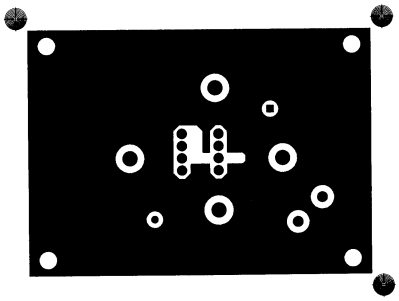


FIGURE 2. BOARD SCHEMATIC

TOP LAYOUT



BOTTOM LAYOUT



Typical Performance Curves

V_{SUPPLY} = ±5V, R_F = 510Ω, T_A = +25°C, R_L = 100Ω, Unless Otherwise Specified

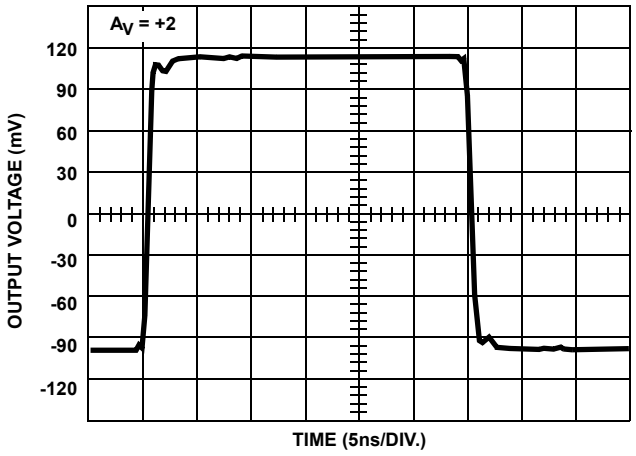


FIGURE 3. SMALL SIGNAL PULSE RESPONSE

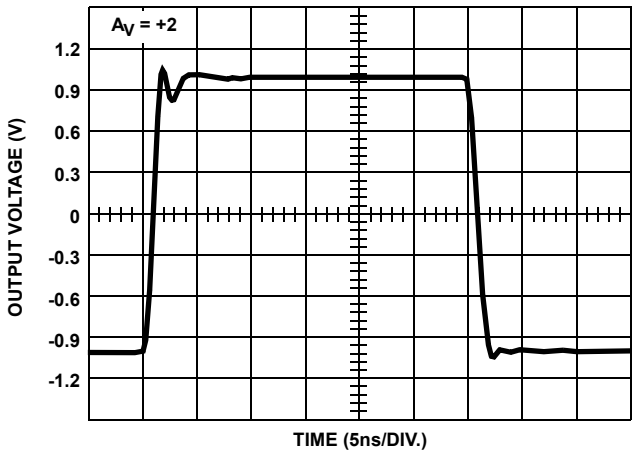


FIGURE 4. LARGE SIGNAL PULSE RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = +25°C$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

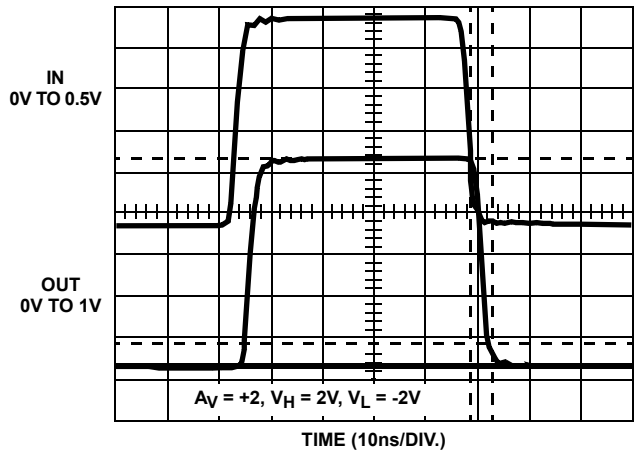


FIGURE 5. UNCLAMPED PERFORMANCE

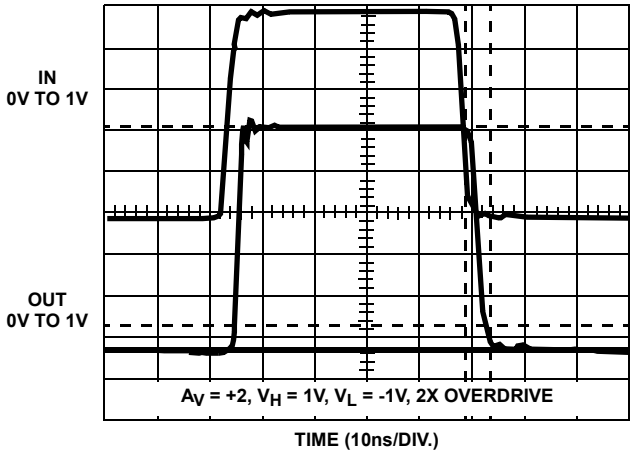


FIGURE 6. CLAMPED PERFORMANCE

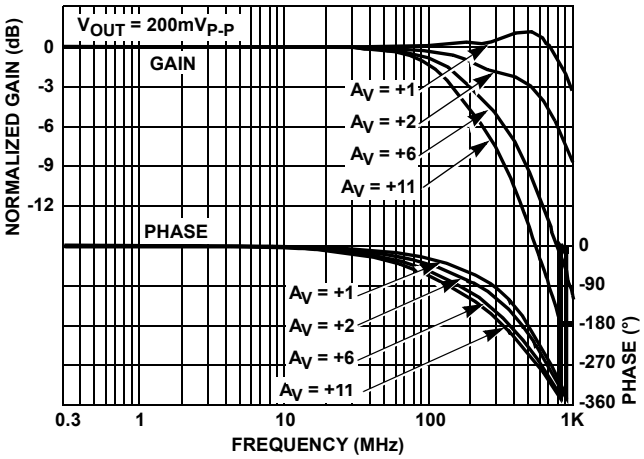


FIGURE 7. NON-INVERTING FREQUENCY RESPONSE

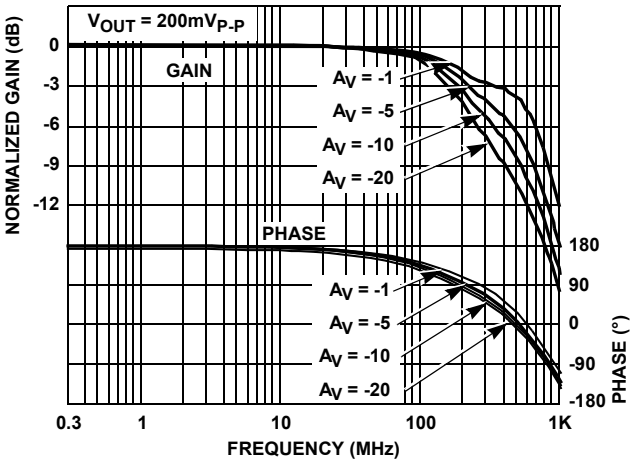


FIGURE 8. INVERTING FREQUENCY RESPONSE

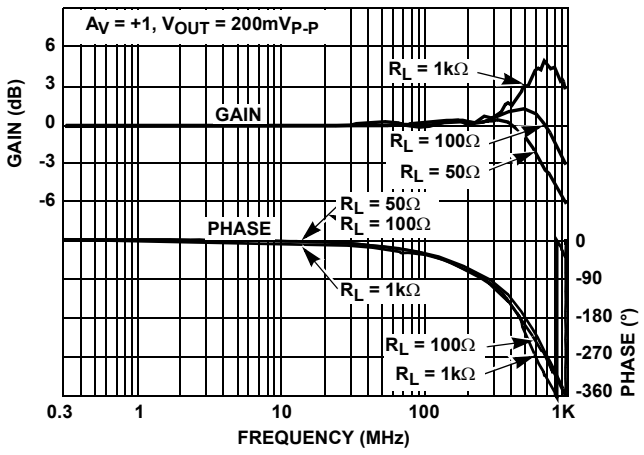


FIGURE 9. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

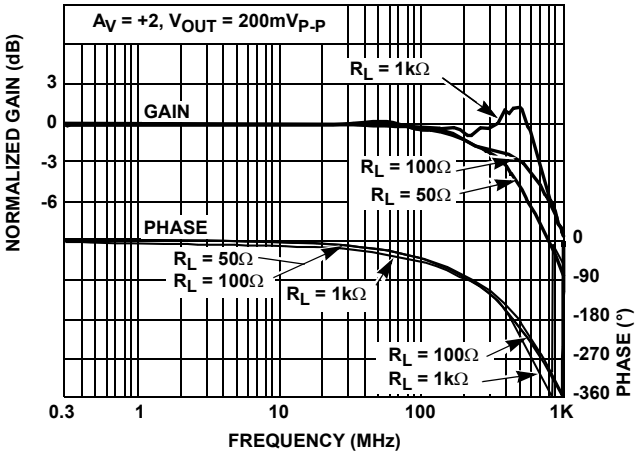


FIGURE 10. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

Typical Performance Curves V_{SUPPLY} = ±5V, R_F = 510Ω, T_A = +25°C, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

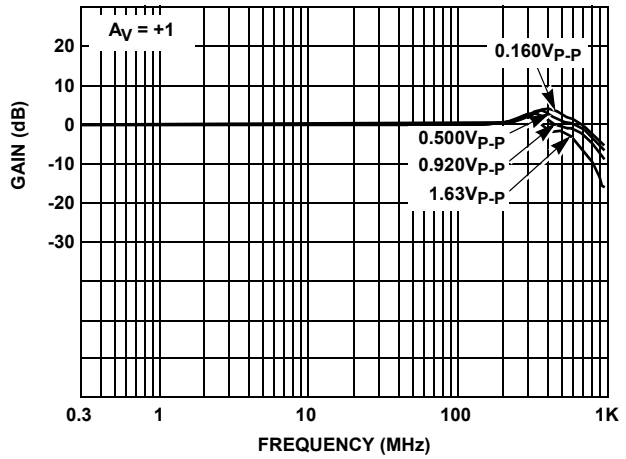


FIGURE 11. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

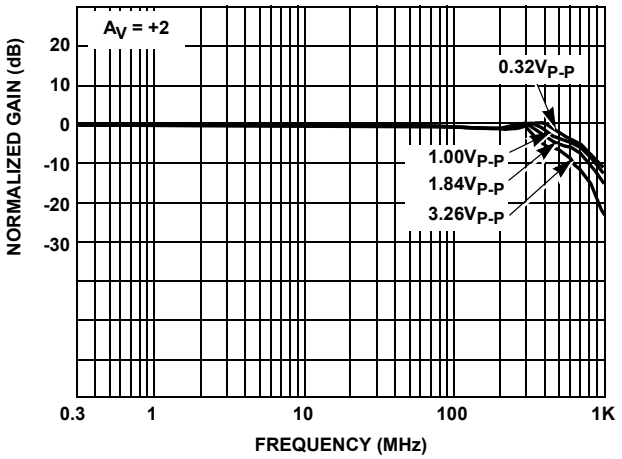


FIGURE 12. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

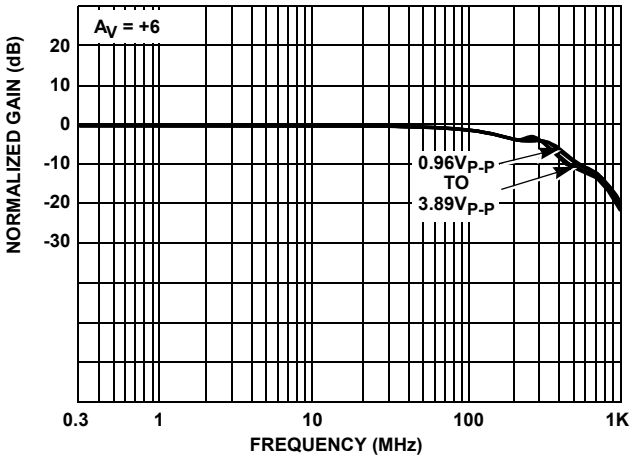


FIGURE 13. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

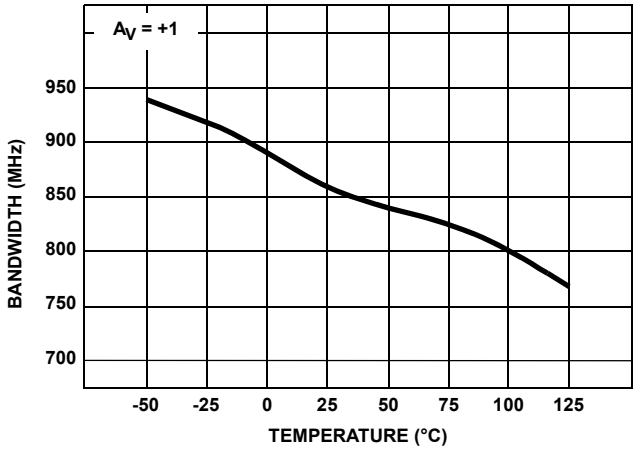


FIGURE 14. -3dB BANDWIDTH vs TEMPERATURE

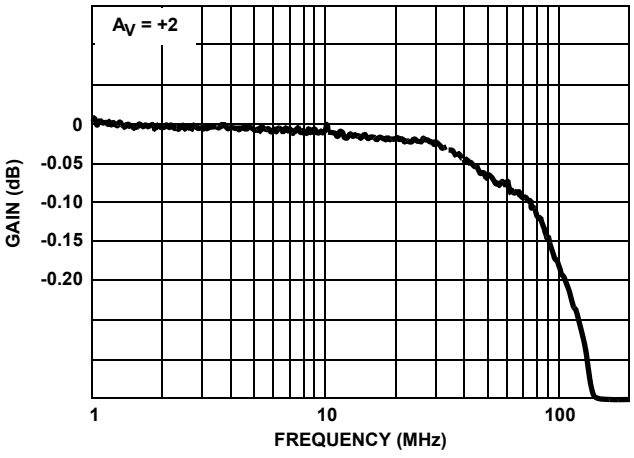


FIGURE 15. GAIN FLATNESS

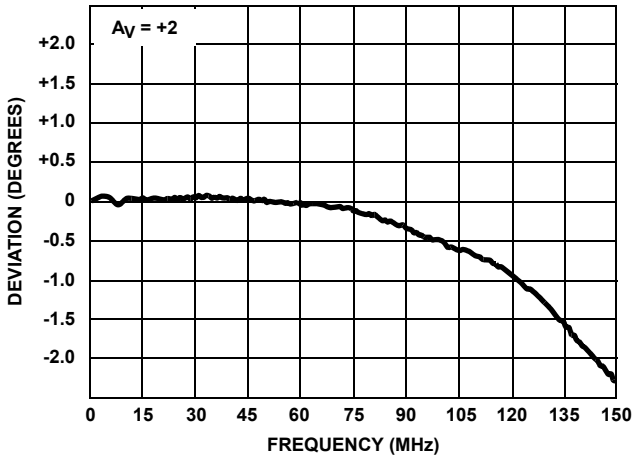


FIGURE 16. DEVIATION FROM LINEAR PHASE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = +25°C$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

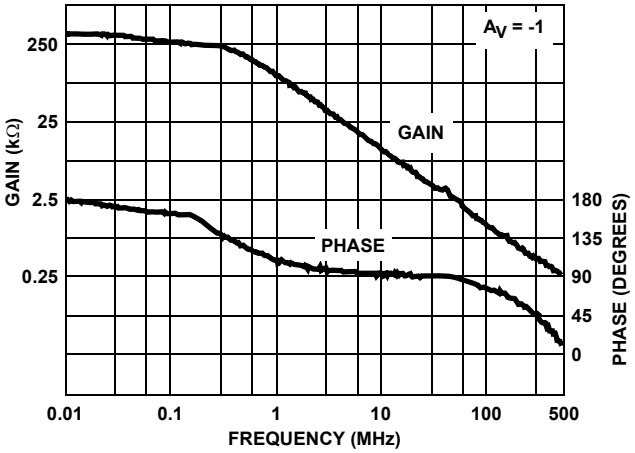


FIGURE 17. OPEN LOOP TRANSIMPEDANCE

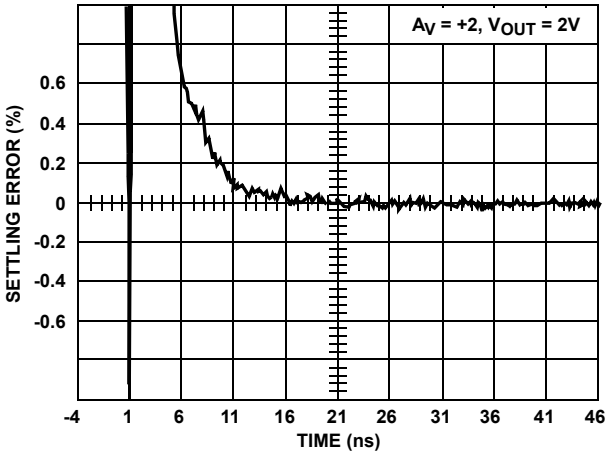


FIGURE 18. SETTLING RESPONSE

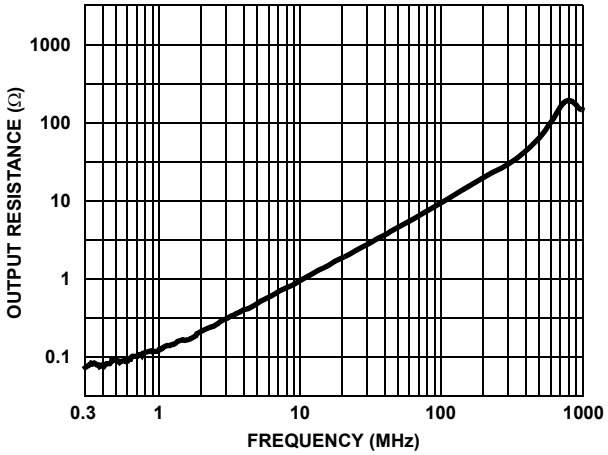


FIGURE 19. CLOSED LOOP OUTPUT RESISTANCE

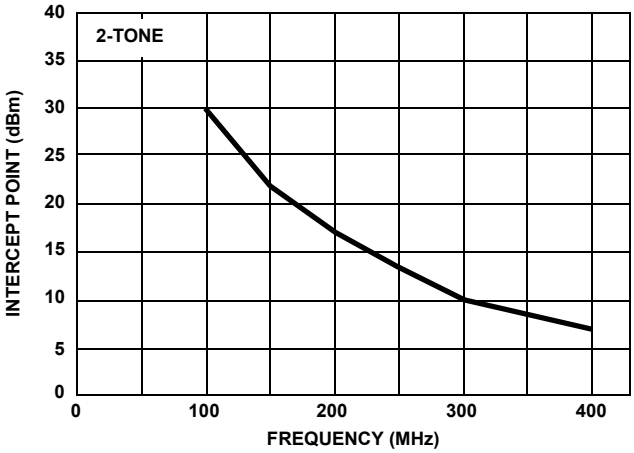


FIGURE 20. 3rd ORDER INTERMODULATION INTERCEPT

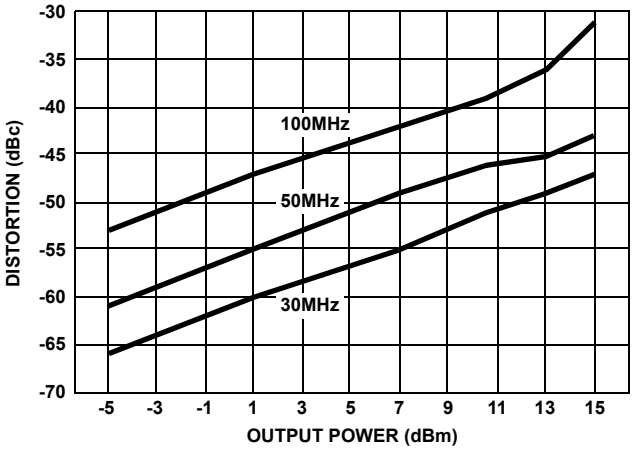


FIGURE 21. 2nd HARMONIC DISTORTION vs P_{OUT}

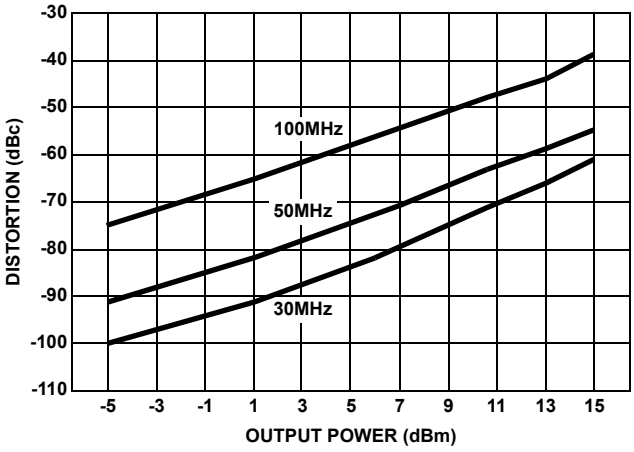


FIGURE 22. 3rd HARMONIC DISTORTION vs P_{OUT}

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = +25°C$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

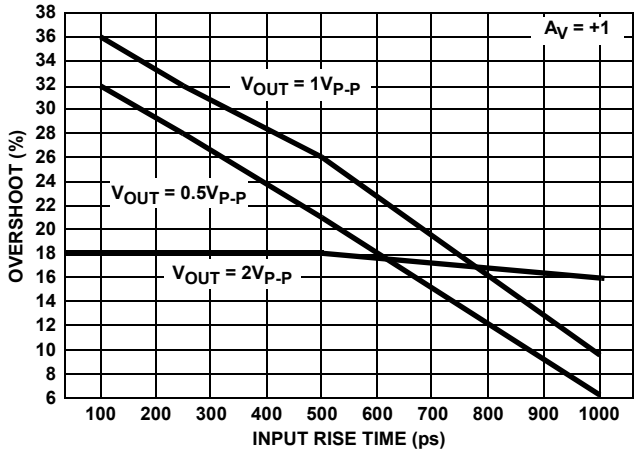


FIGURE 23. OVERSHOOT vs INPUT RISE TIME

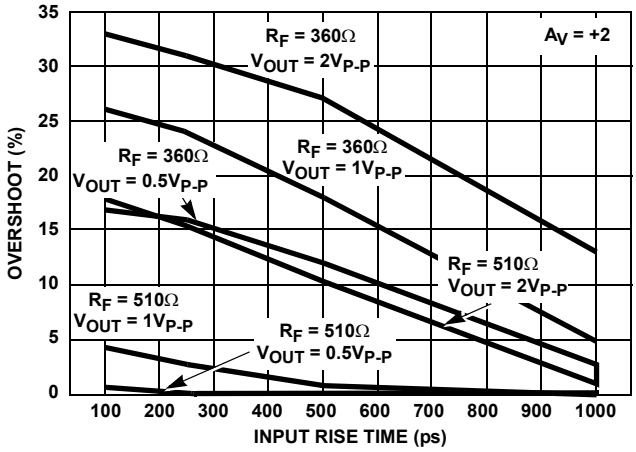


FIGURE 24. OVERSHOOT vs INPUT RISE TIME

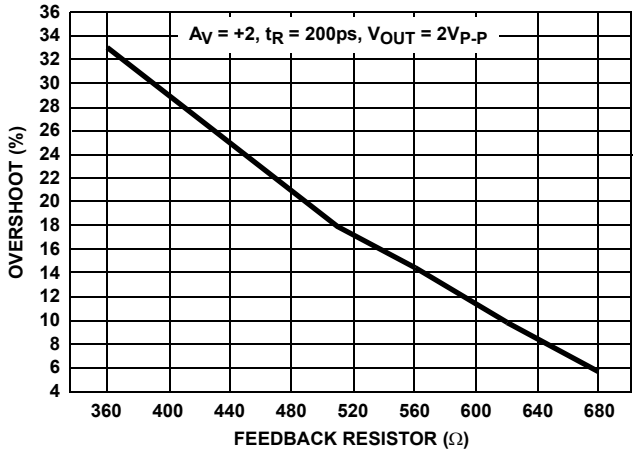


FIGURE 25. OVERSHOOT vs FEEDBACK RESISTOR

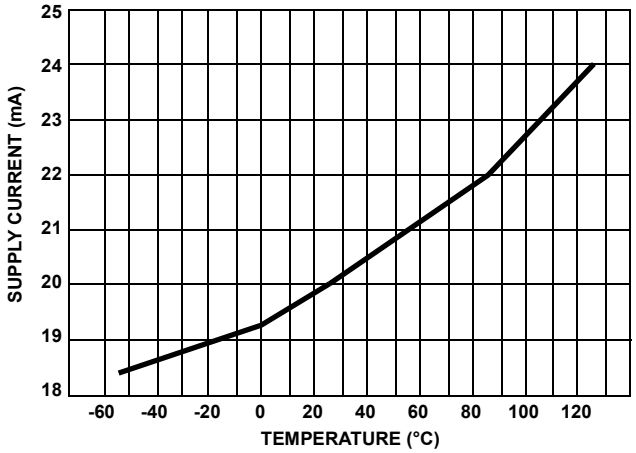


FIGURE 26. SUPPLY CURRENT vs TEMPERATURE

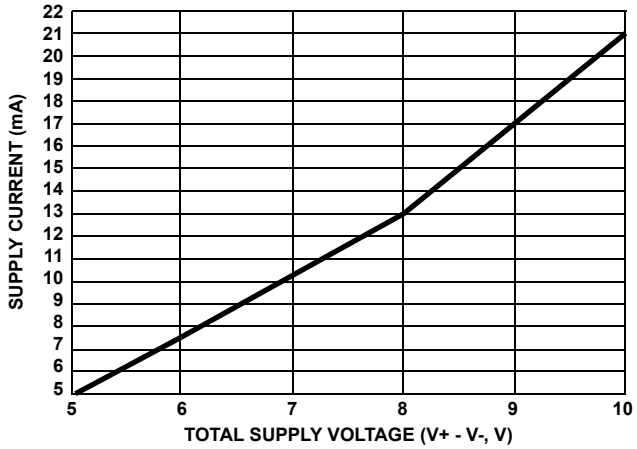


FIGURE 27. SUPPLY CURRENT vs SUPPLY VOLTAGE

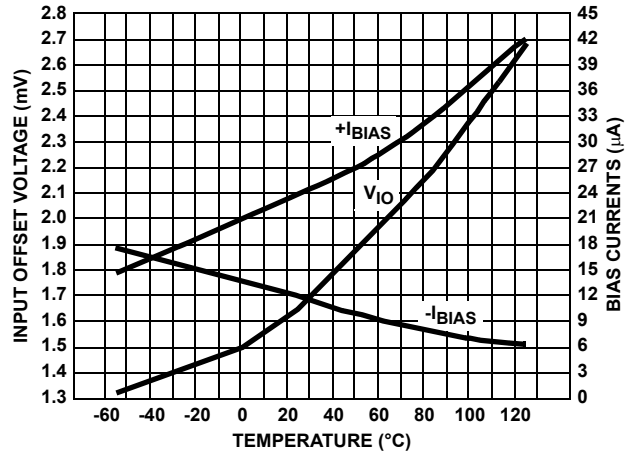


FIGURE 28. V_{IO} AND BIAS CURRENTS vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = +25°C$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

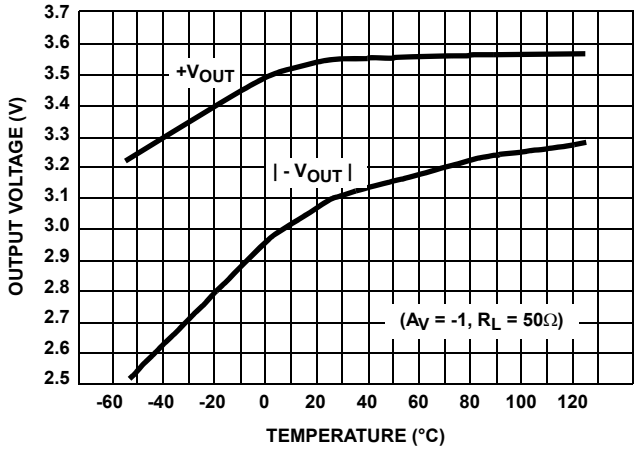


FIGURE 29. OUTPUT VOLTAGE vs TEMPERATURE

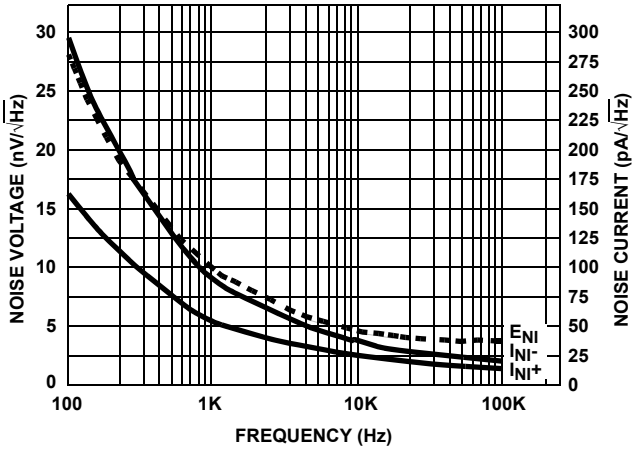


FIGURE 30. INPUT NOISE vs FREQUENCY

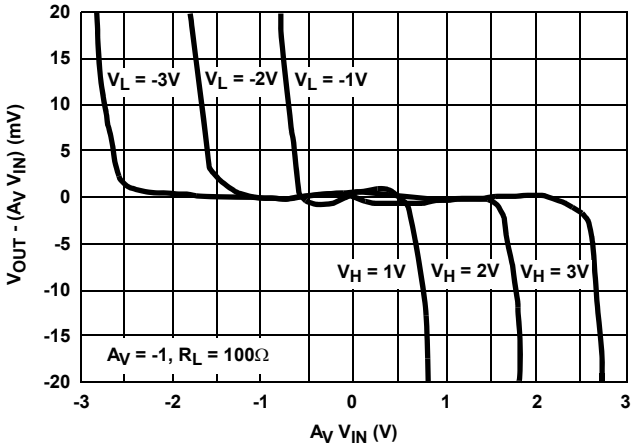


FIGURE 31. NON-LINEARITY NEAR CLAMP VOLTAGE

Die Characteristics

DIE DIMENSIONS:

63 mils x 44 mils x 19 mils
1600µm x 1130µm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: ALCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

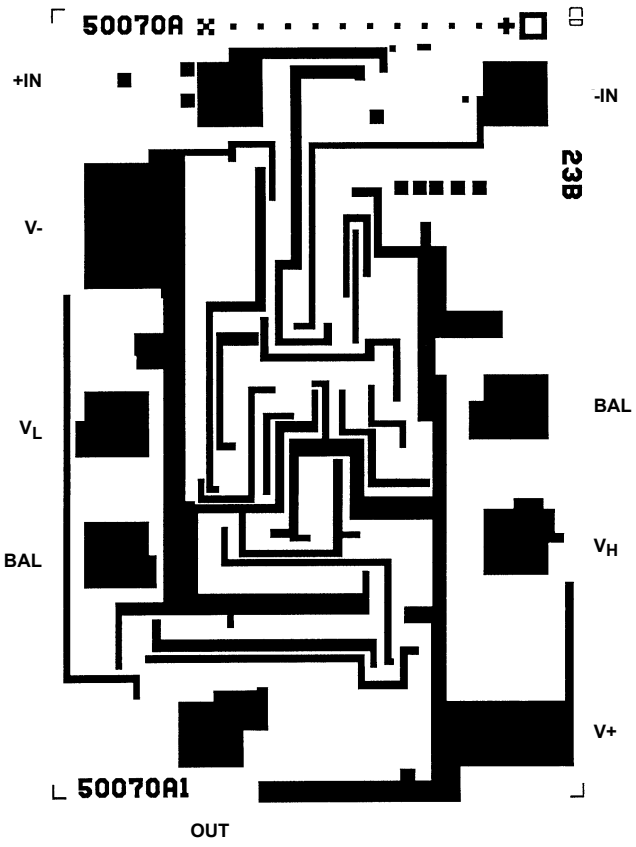
52

SUBSTRATE POTENTIAL (Powered Up):

Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1130

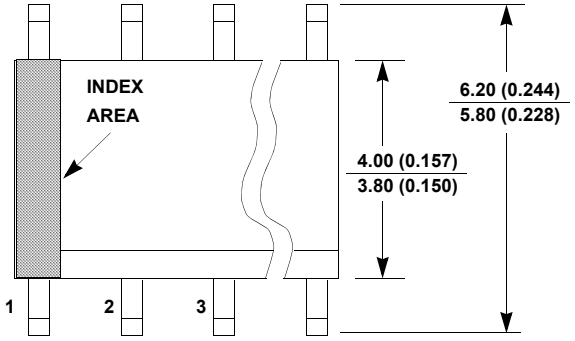


Package Outline Drawing

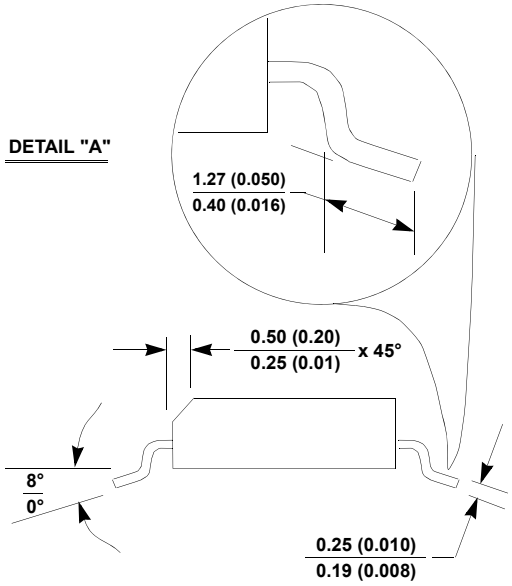
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

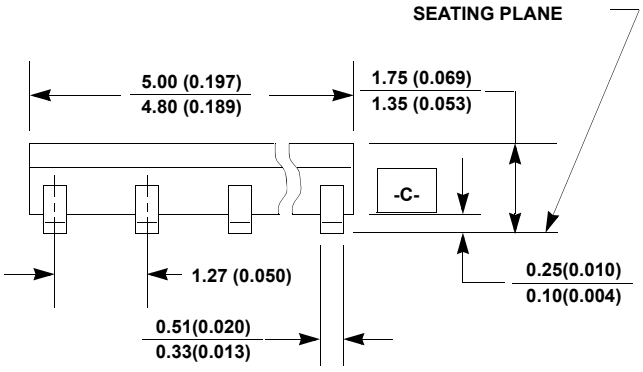
Rev 4, 1/12



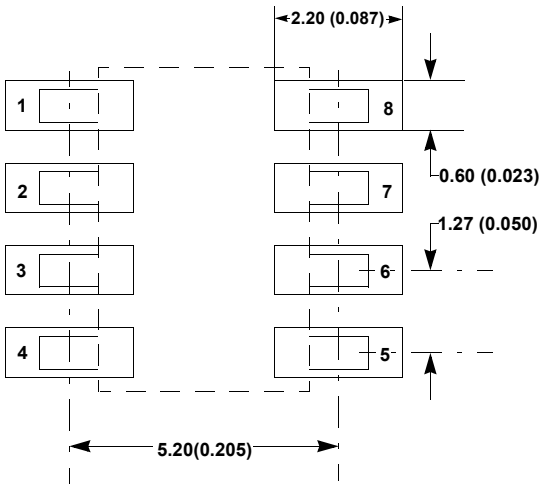
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.