

37-40GHz Integrated Down Converter

GaAs Monolithic Microwave IC in SMD leadless package

Description

The CHR3894-QEG is a multifunction monolithic receiver, which integrates a balanced cold FET mixer, a LO chain with buffers associated to a time two multiplier, and a RF low noise amplifier including gain control.

It is designed for a wide range of applications, from military to commercial communication systems.

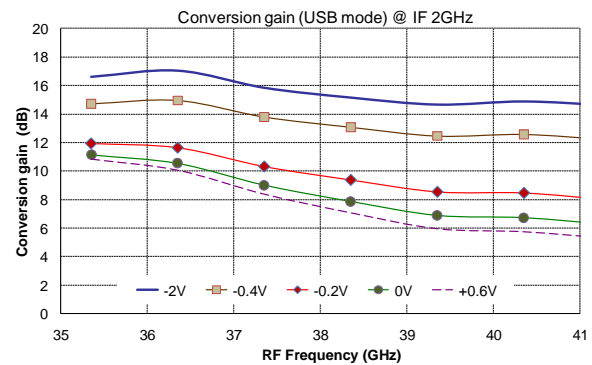
The circuit is manufactured with a pHEMT process, 0.15 μ m gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is supplied in RoHS compliant SMD package.



Main Features

- Broadband performances: 37-40GHz
- 13dB Conversion gain
- 15dBc Image Rejection
- 2dBm IIP3 without attenuation (GC=-2V)
- 8dB Gain Control range
- 4dB Noise Figure for IF>0.1GHz
- 0dBm LO input Power
- DC bias: Vd=4V @ Id=250mA
- 24L-QFN4x5
- MSL1



Main Electrical Characteristics

Tamb.= +25°C

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------------|-------------------------------------|------|-----|------|------|
| F _{RF} | RF frequency range | 37 | | 40 | GHz |
| F _{LO} | LO frequency range | 17.5 | | 21.0 | GHz |
| F _{IF} | IF frequency range | DC | | 3.5 | GHz |
| G | Conversion gain without attenuation | 10 | 13 | | dBm |

Electrical Characteristics

Tamb.= +25°C, VD = VD1 = +4V (1)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------------|--|------|------|------|------|
| F _{RF} | RF frequency range | 37 | | 40 | GHz |
| F _{LO} | LO frequency range | 17.5 | | 21.0 | GHz |
| F _{IF} | IF frequency range | DC | | 3.5 | GHz |
| G | Conversion gain without attenuation ⁽²⁾ | 10 | 13 | | dB |
| ΔG | Gain control range | | 8 | | dB |
| NF | Noise Figure for IF>0.1GHz | | 4 | 4.5 | dB |
| Im_rej | Image rejection ⁽²⁾ | 12 | 15 | | dBc |
| P _{LO} | LO Input power | | 0 | | dBm |
| IIP3 | Input IP3 without attenuation | 0 | 2 | | dBm |
| IIP3 | Input IP3 @ all attenuations | -2 | 0 | | dBm |
| LO RL | LO return loss | | -12 | | dB |
| RF RL | RF return loss | | -7 | | dB |
| VGL | LNA DC gate voltage | | -0.1 | | V |
| VGX | Multiplier DC gate voltage | | -0.9 | | V |
| GC | Gain control DC voltage | -2 | | +0.6 | V |
| IDt | Total Drain current (ID+ID1) ⁽³⁾ | | 250 | | mA |

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

(1) VD: LO-chain drain bias voltage. VD1: LNA drain bias voltage.

(2) An external combiner 90° is required on I / Q.

(3) ID: LO-chain drain current, typically 125mA.

(3) ID1: LNA drain current, typically 125mA, should be tuned with VGL.

Note: The total current (IDt) is not affected by the gain control voltage (GC).

Electrostatic discharge sensitive device observe handling precautions!

Absolute Maximum Ratings ⁽¹⁾T_{amb.} = +25°C

| Symbol | Parameter | Values | Unit |
|----------|---|--------------|------|
| VD, VD1 | Drain bias voltages | 4.5V | V |
| IDt | Drain bias current | 340 | mA |
| VGL, VGX | Gate bias voltages | -2 to +0.4 | V |
| GC | Gain Control voltage | -2.5 to +0.8 | V |
| P_RF | Maximum peak input power overdrive ⁽²⁾ | +15 | dBm |
| P_LO | Maximum LO input power | +15 | dBm |
| Tj | Junction temperature ⁽²⁾ | 175 | °C |
| Ta | Operating temperature range | -40 to +85 | °C |
| Tstg | Storage temperature range | -55 to +150 | °C |

⁽¹⁾ Operation of this device above anyone of these parameters may cause permanent damage.

⁽²⁾ Duration < 1s.

Typical Bias ConditionsT_{amb.} = +25°C

| Symbol | Pad N° | Parameter | Values | Unit |
|---------|--------|---------------------------------------|-----------|------|
| VD1, VD | 10, 11 | DC drain voltages (LNA and LO-chain) | 4 | V |
| ID1 | 10 | LNA drain current controlled with VGL | 125 | mA |
| VGL | 9 | LNA DC gate voltage | -0.1 | V |
| VGX | 12 | Multiplier DC gate voltage | -0.9 | V |
| GC | 8 | Gain control DC voltage | -2 to 0.6 | V |

Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (Tcase) as shown below. The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

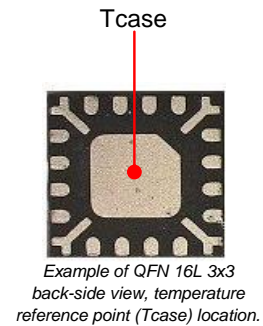
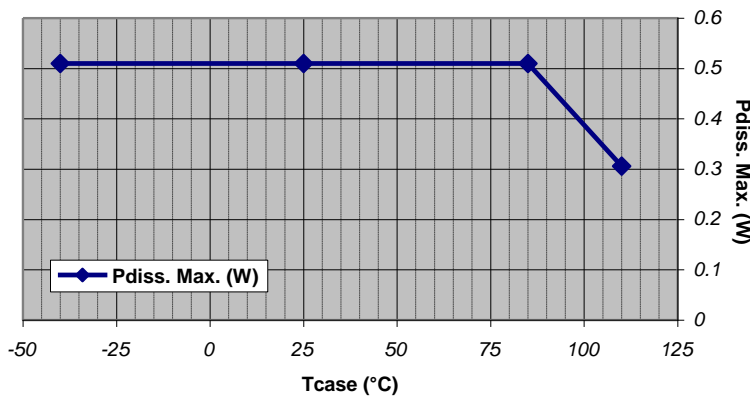
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below than the maximum temperature specified (see the curve P_{diss. Max}) in order to guarantee the nominal device life time (MTTF).

| DEVICE THERMAL SPECIFICATION : CHR3894-QEG | |
|--|-------------|
| Recommended max. junction temperature (T _j max) | : 147 °C |
| Junction temperature absolute maximum rating | : 175 °C |
| Max. continuous dissipated power @ T _{case} = 85 °C | : 0.51 W |
| => P _{diss} derating above T _{case} ⁽¹⁾ = 85 °C | : 8 mW/°C |
| Junction-Case thermal resistance (R _{th} J-C) ⁽²⁾ | : <122 °C/W |
| Min. package back side operating temperature ⁽³⁾ | : -40 °C |
| Max. package back side operating temperature ⁽³⁾ | : 85 °C |
| Min. storage temperature | : -55 °C |
| Max. storage temperature | : 150 °C |

(1) Derating at junction temperature constant = T_j max

(2) R_{th} J-C is calculated for a worst case where the **hotter junction** of the MMIC is considered.

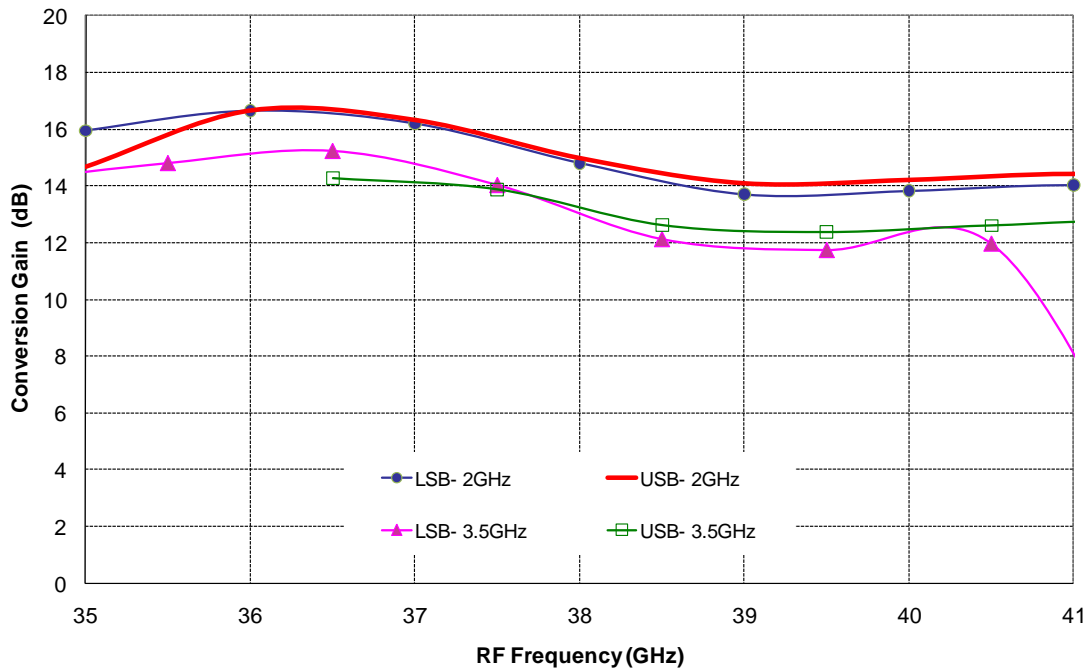
(3) T_{case}=Package back side temperature measured under the die-attach-pad (see the drawing below).



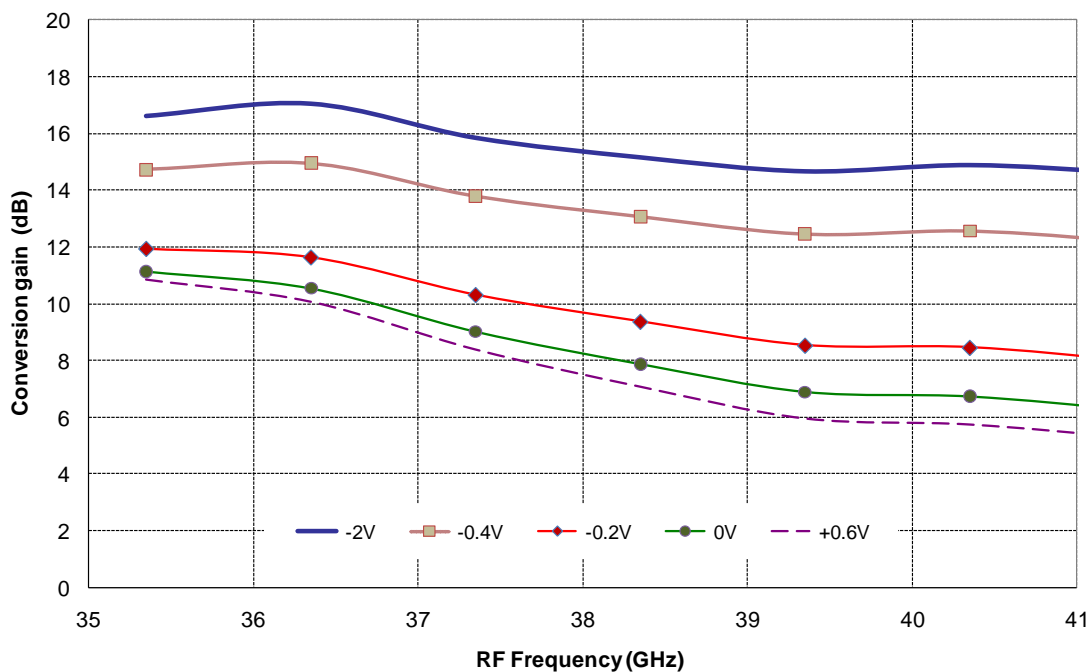
Typical Board Measurements

Tamb.= +25°C, VD = VD1 =+4V, VGL = -0.1V, VGX = -0.9V, P_LO = 0dBm (IDt = 250mA)
 These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board". Data given in the package access planes.

Conversion Gain versus RF & IF frequency (USB & LSB modes)
 without attenuation: GC= -2V



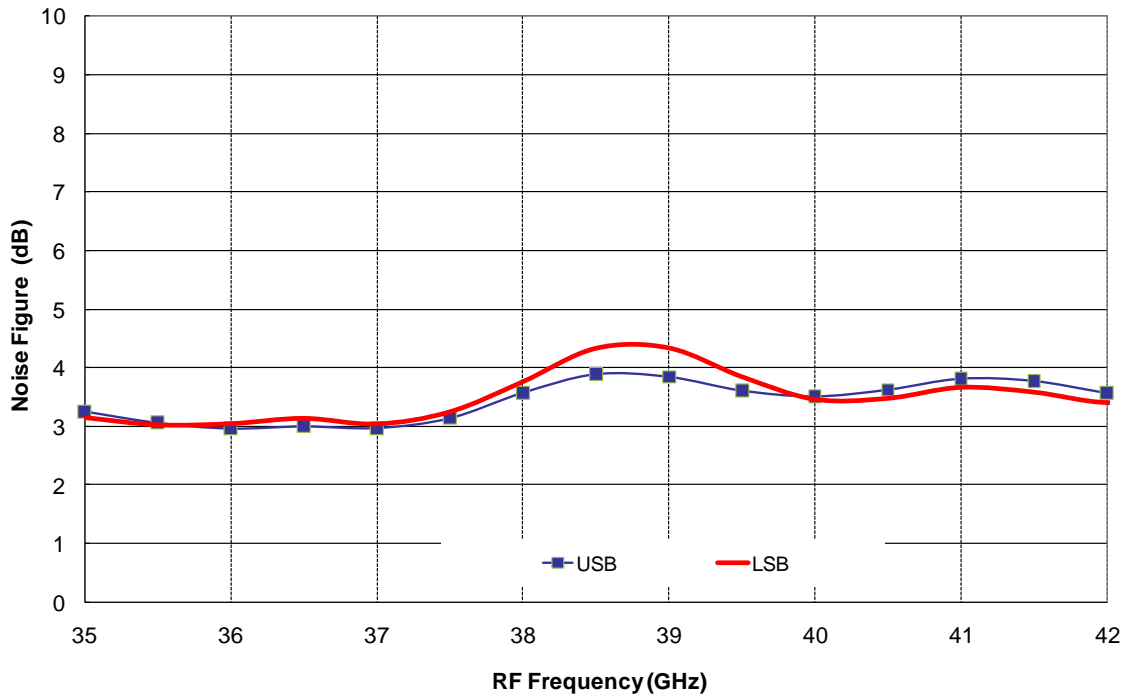
Conversion Gain versus RF frequency and gain control voltage
 (IF 2GHz, USB mode)



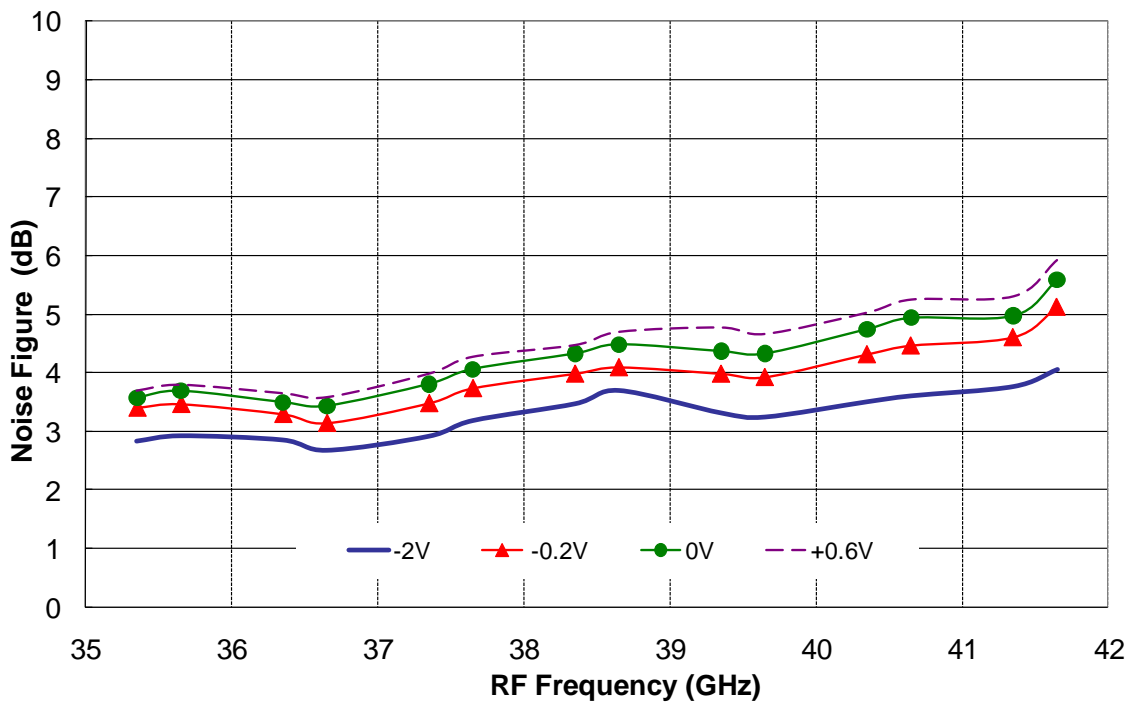
Typical Board Measurements

Tamb.= +25°C, VD = VD1 = +4V, VGL = -0.1V, VGX = -0.9V, P_LO = 0dBm (IDt = 250mA)

Noise figure versus RF frequency at IF 2GHz (USB & LSB modes)
without attenuation: GC= -2V



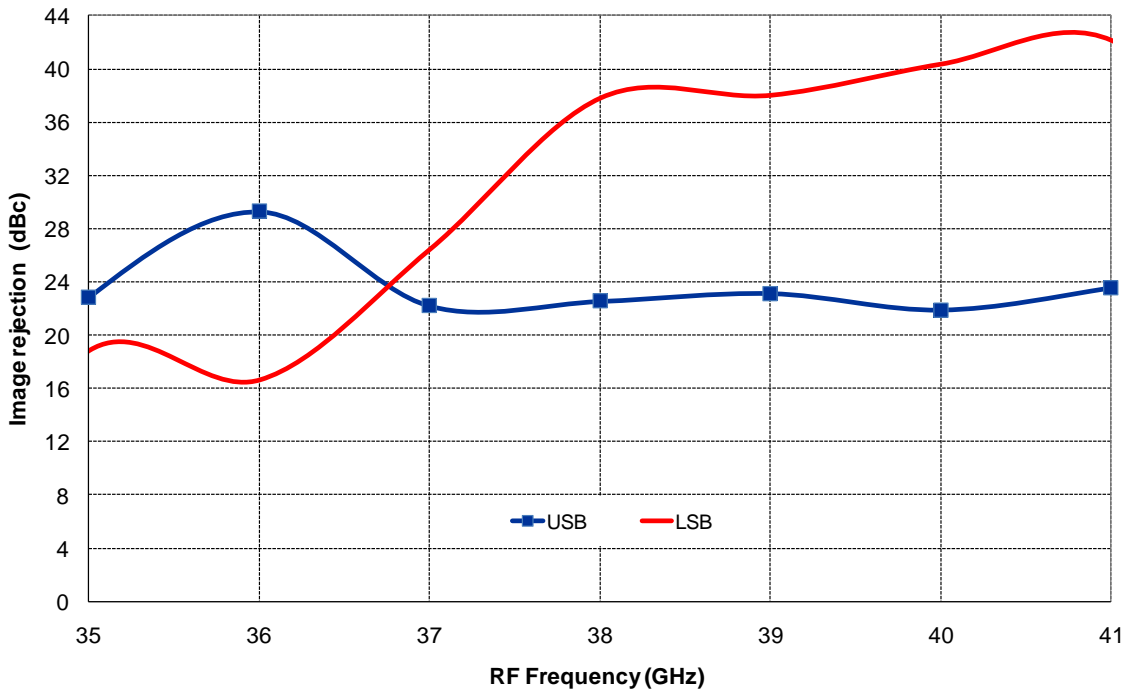
Noise figure versus gain control range (IF 2GHz, USB mode)



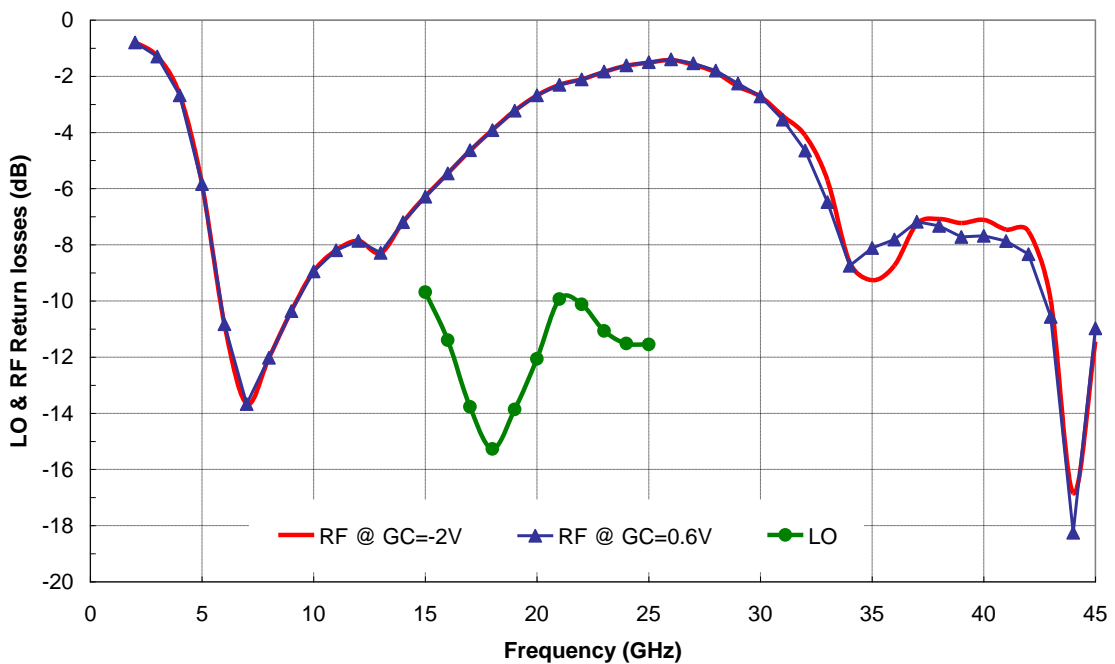
Typical Board Measurements

Tamb.= +25°C, VD = VD1 = +4V, VGL = -0.1V, VGX = -0.9V, P_LO = 0dBm (IDt = 250mA)

Image rejection versus RF frequency at IF 2GHz (USB & LSB modes)
without attenuation: GC= -2V



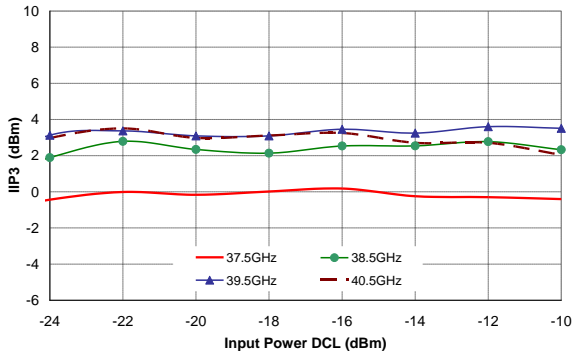
Return Losses (LO & RF) versus frequency and gain control voltage



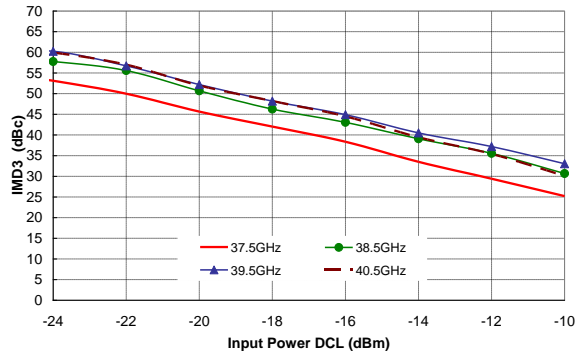
Typical Board Measurements

Tamb.= +25°C, VD = VD1 = +4V, VGL = -0.1V, VGX = -0.9V, P_LO = 0dBm (IDt = 250mA)

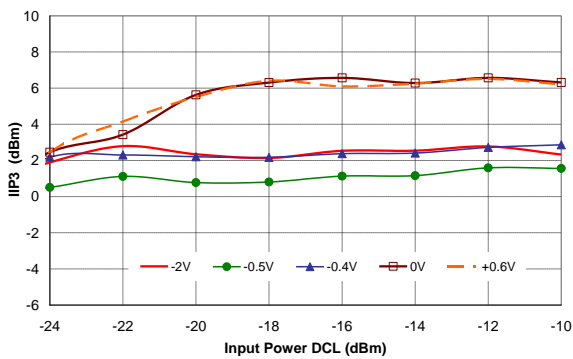
Input IP3 vs RF frequency at IF 3.5GHz
without attenuation: GC= -2V



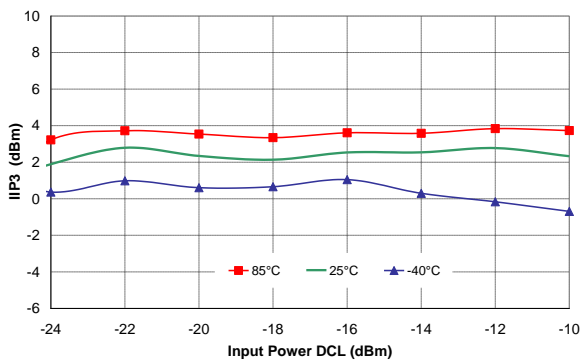
IMD3 vs RF frequency at IF 3.5GHz
without attenuation: GC= -2V



Input IP3 vs gain control at 38.5GHz



Input IP3 vs temperature at 38.5GHz
without attenuation: GC= -2V

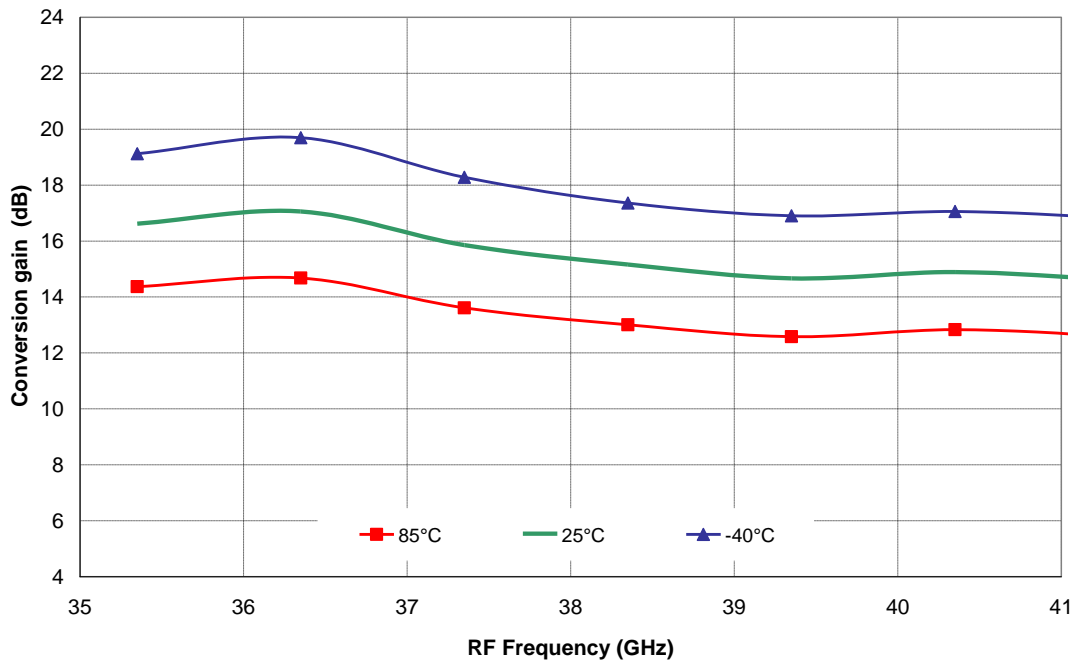


Typical Board Measurements

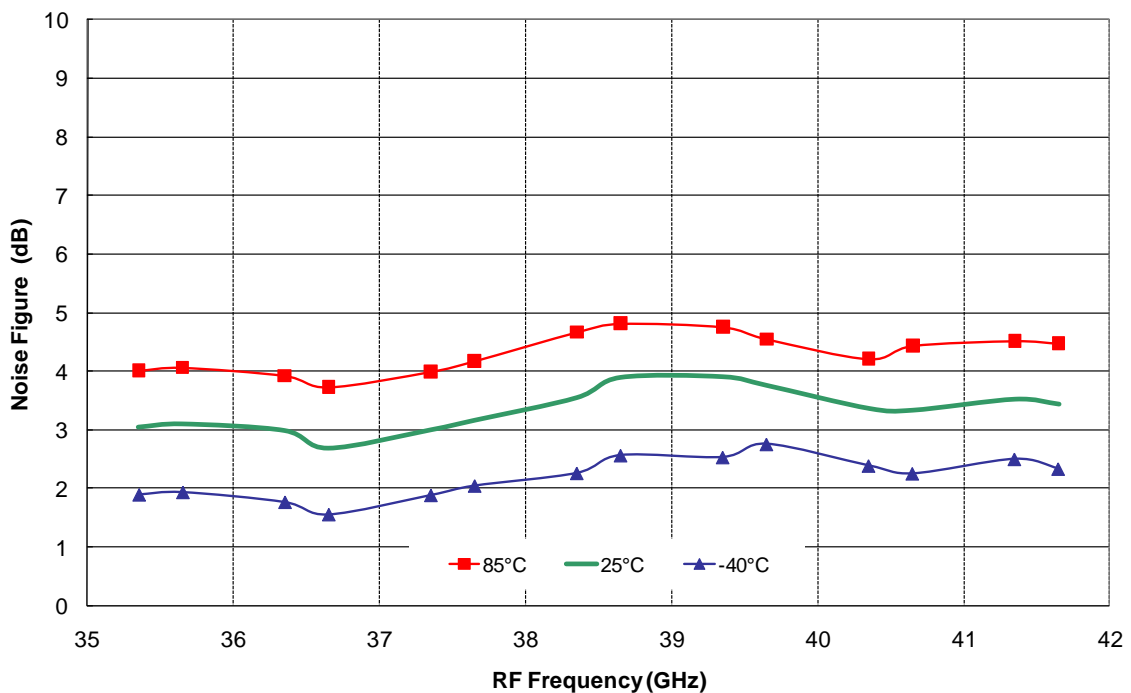
Tamb = +25°C, Tcold = -40°C, Thot = +85°C

VD = VD1 = +4V, VGL = -0.1V, VGX = -0.9V, P_LO = 0dBm

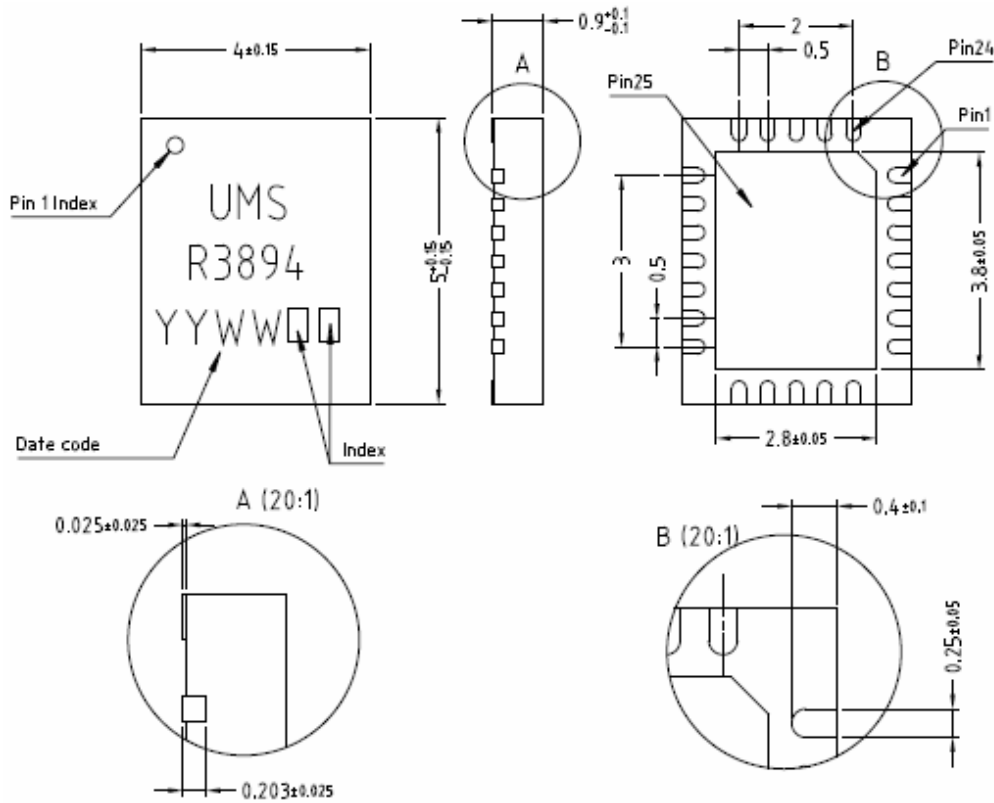
Conversion Gain versus temperature at IF 2GHz (USB mode)
without attenuation: GC= -2V



Noise figure versus temperature at IF 2GHz (USB mode)
without attenuation: GC= -2V



Package outline ⁽¹⁾



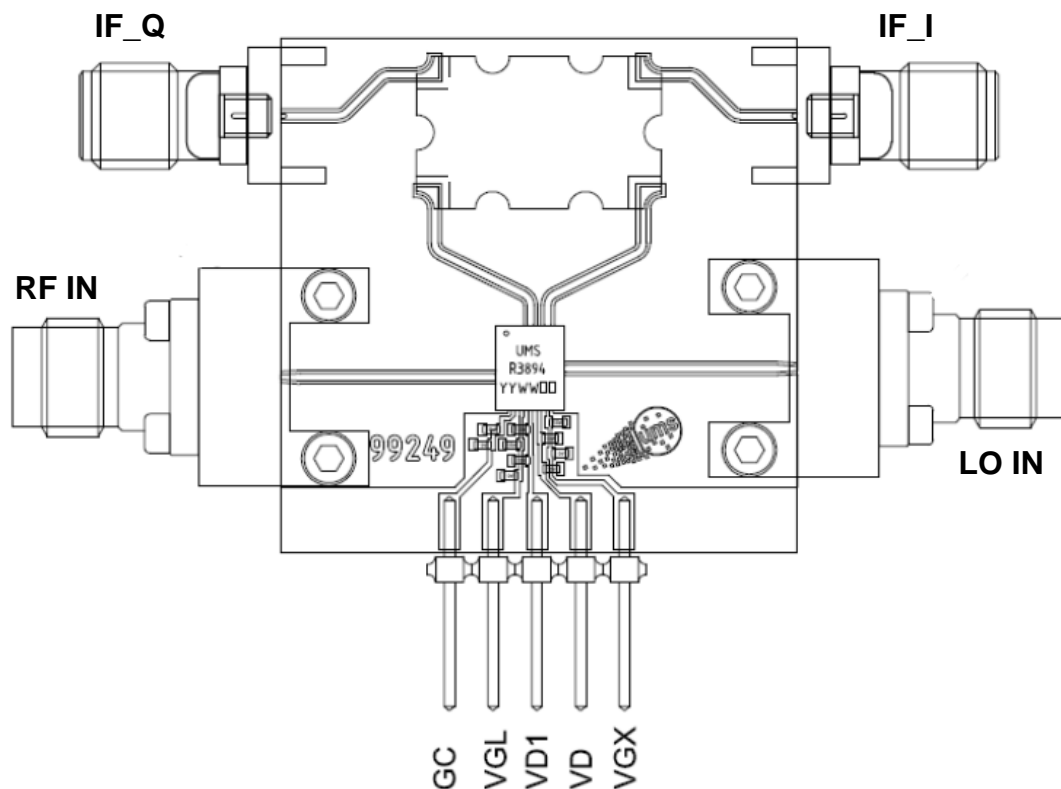
| | | | |
|----------------------------------|-----------------------|------------------------|------------------------|
| Matt tin, Lead Free (Green) | 1- Nc | 9- VGL | 17- Gnd ⁽²⁾ |
| Units : mm | 2- Nc | 10- VD1 | 18- Nc |
| From the standard : JEDEC MO-220 | 3- Nc | 11- VD | 19- Nc |
| (VGGD) | 4- Gnd ⁽²⁾ | 12- VGX | 20- IF_I |
| 25- GND | 5- RF in | 13- Nc | 21- Gnd ⁽²⁾ |
| | 6- Gnd ⁽²⁾ | 14- Nc | 22- IF_Q |
| | 7- Nc | 15- Gnd ⁽²⁾ | 23- Nc |
| | 8- GC | 16- LO in | 24- Nc |

⁽¹⁾ The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (<http://www.ums-gaas.com>) for exact package dimensions.

⁽²⁾ It is strongly recommended to ground all pins marked "Gnd" through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

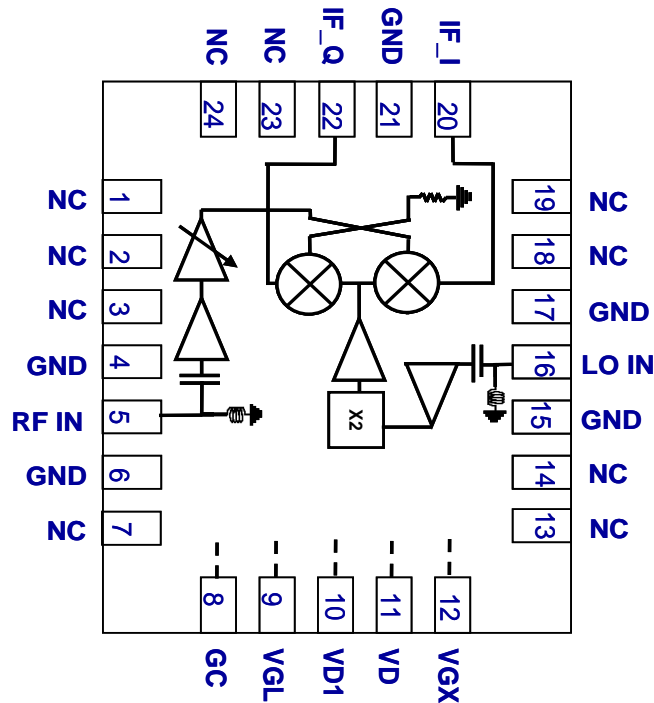
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF \pm 10% are recommended for all DC accesses.
- See application note AN0017 for details.
- Hybrid coupler 90° for 2-4GHz.



Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.

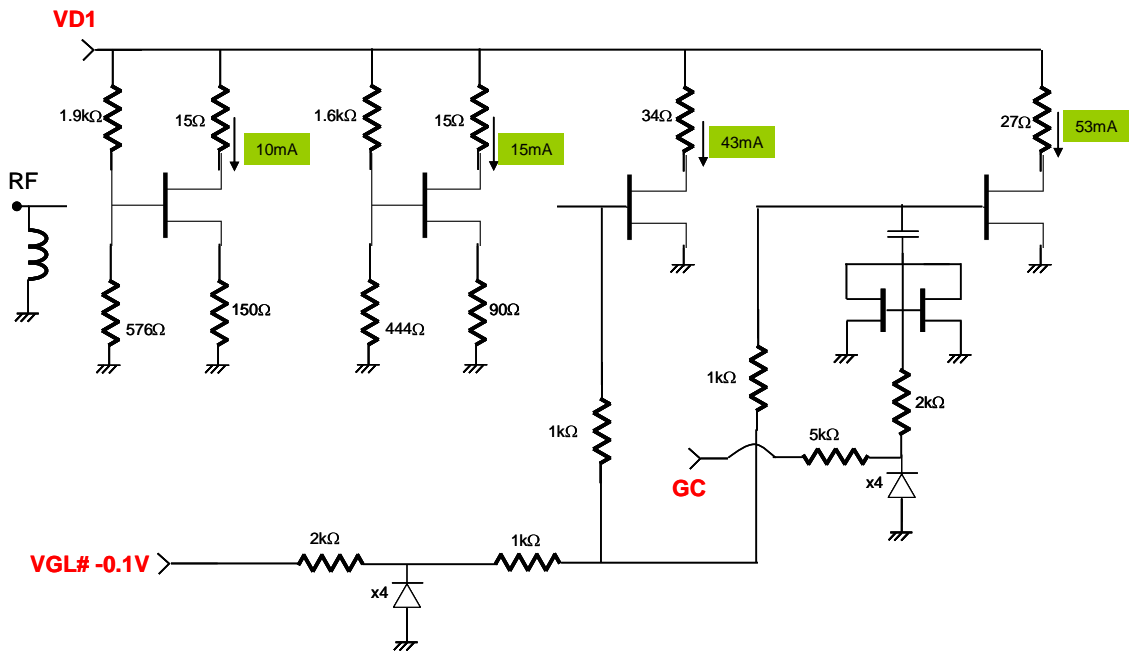


ESD protections are also implemented on gate and control accesses.

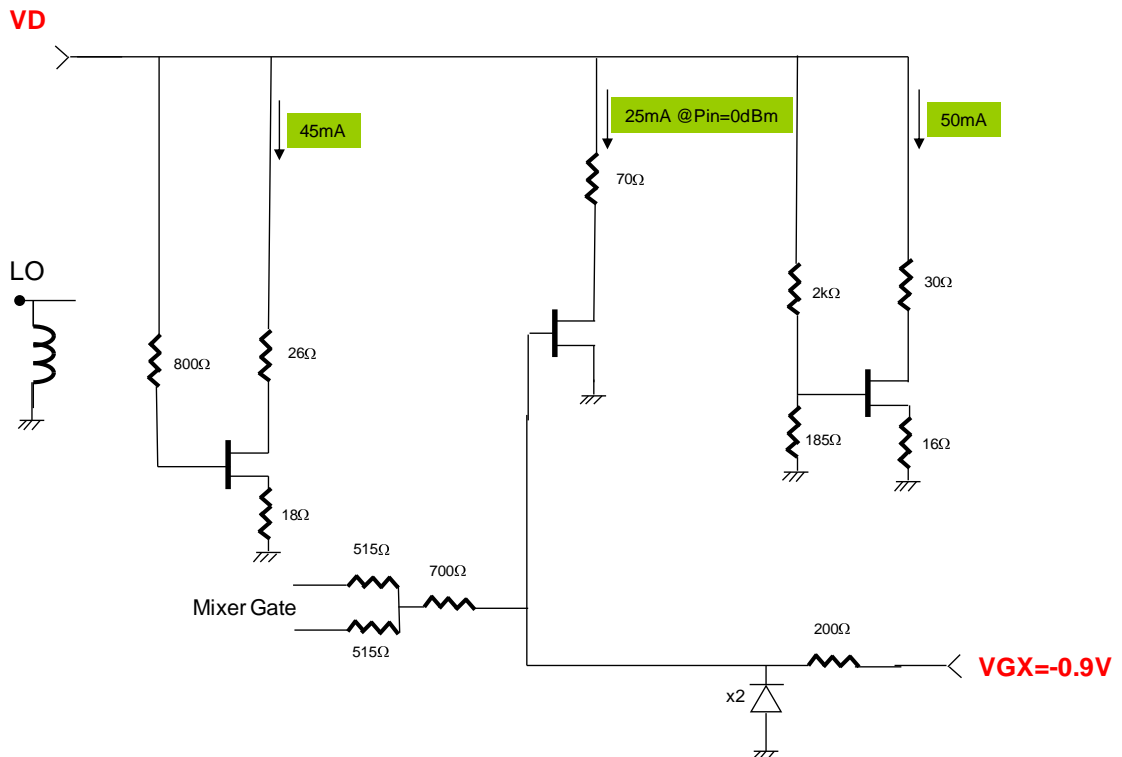
The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (10nF) on the PC board, as close as possible to the package.

DC Schematic

LNA: 4V, 125mA



LO chain: 4V, 125mA



Recommended package footprint

Refer to the application note AN0017 available at <http://www.ums-gaas.com> for package footprint recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <http://www.ums-gaas.com>.

Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 package:

CHR3894-QEG/XY

Stick: XY = 20

Tape & reel: XY = 21

Information furnished is believed to be accurate and reliable. However **United Monolithic Semiconductors S.A.S.** assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of **United Monolithic Semiconductors S.A.S.** Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. **United Monolithic Semiconductors S.A.S.** products are not authorised for use as critical components in life support devices or systems without express written approval from **United Monolithic Semiconductors S.A.S.**