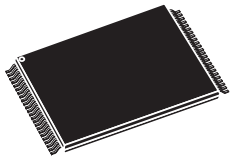
M39832

Single Chip 8 Mbit (1Mb x8 or 512Kb x16) Flash and 256 Kbit Parallel EEPROM Memory

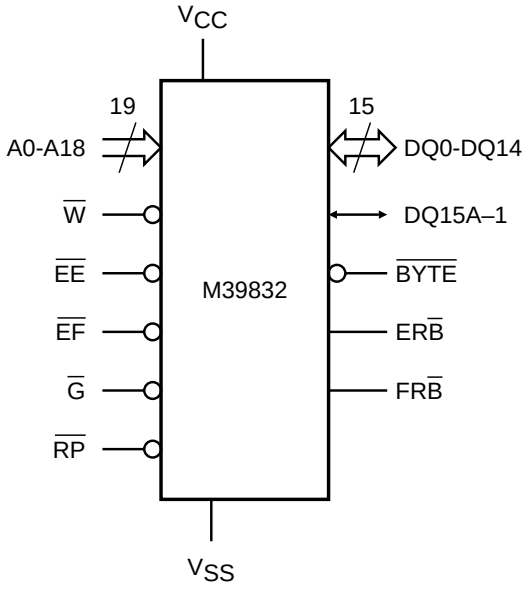
PRELIMINARY DATA

- 2.7V to 3.6V SUPPLY VOLTAGE for PROGRAM, ERASE and READ OPARATIONS
- FLASH ARRAY
  - Boot block (Top or Bottom location)
  - Parameter and Main blocks
  - Selectable x8/x16 Data Bus ($\overline{BYTE}$ pin).
- EEPROM ARRAY
  - x8 Data Bus only.
- 120ns ACCESS TIME (Flash and EEPROM array)
- WRITE, PROGRAM and ERASE STATUS BITS
- CONCURRENT MODE (Read Flash while writing to EEPROM)
- 100,000 ERASE/WRITE CYCLES
- 10 YEARS DATA RETENTION
- LOW POWER CONSUMPTION
  - Stand-by mode: 100µA
  - Automatic Stand-by mode
- 64 bytes ONE TIME PROGRAMMABLE MEMORY (x8 Data Bus only)
- STANDARD EPROM/OTP MEMORY PACKAGE
- EXTENDED TEMPERATURE RANGES



TSOP48 (NE)
12 x 20 mm

Figure 1. Logic Diagram



DESCRIPTION

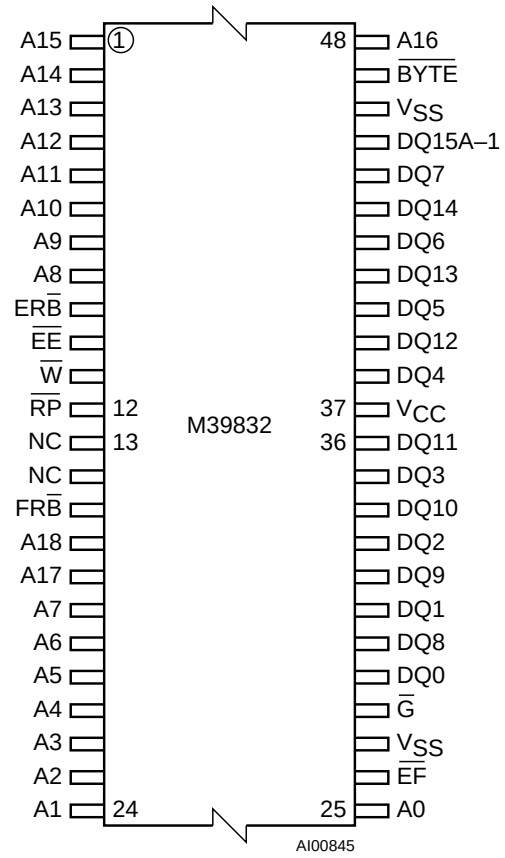
The M39832 is a memory device combining Flash and EEPROM into a single chip and using single supply voltage. The memory is mapped in two arrays: 8 Mbit of Flash memory and 256 Kbit of EEPROM memory. Each space is independant for writing, in concurrent mode the Flash Memory can be read while the EEPROM is being written.

An additional 64 bytes of EPROM are One Time Programmable.

The M39832 EEPROM memory array is organized in byte only (regardless on the $\overline{BYTE}$ pin). It may be written by byte or by page of 64 bytes and the integrity of the data can be secured with the help of the Software Data Protection (SDP).

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

Figure 2. TSOP Pin Connections



Warning: NC = Not Connected.

Table 1. Signal Names

A0-A18	Address Inputs
DQ0-DQ7	Data Input/Outputs, Commands Input
DQ8-DQ14	Data Input/Outputs
DQ15A–1	Data Input/Outputs or Address Input
$\overline{EE}$	EEPROM Array Enable
$\overline{EF}$	Flash Array Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Block Temporary Unprotect
ER$\overline{B}$	EEPROM Ready/Busy Output
FR$\overline{B}$	Flash Ready/Busy Output
$\overline{BYTE}$	Flash Array Byte/Word Organization
V_{CC}	Supply Voltage
V_{SS}	Ground

DESCRIPTION (cont'd)

The M39832 Flash Memory array can be configured as 1Mb x8 or 512Kb x16 with the $\overline{BYTE}$ input pin. The M39832-T and M39832-B feature asymetrically blocked architecture providing system memory integration. Both M39832-B and M39832-T devices have a Flash array of 19 blocks, one Boot Block of 16 KBytes or 8 KWords, two Parameter Blocks of 8 KBytes or 4 KWords, one Main Block of 32 KBytes or 16 KWords and fifteen Main Blocks of 64 KBytes or 32 KWords. The M39832-T has the Boot Block at the top of the memory address space and the M39832-B locates the Boot Block starting at the bottom. The memory maps are showed in Figures 3A and 3B. Each block can be erased separately,any combination of blocks can be specified for multi-block erase or the entire chip may be erased. The Erase operations are managed automatically. The block erase operation can be suspended in order to read from or program to any block not being ersased, and then resumed. Block protection provides additional data security. Each block can be separately protected or unprotected against Program or Erase on programming equipment. All previously protected blocks can be temporarily unprotected in the application. The Flash memory array is functionally compatible with the M29W800 Single Voltage Flash Memory device.

During a Program or Erase cycle in the Flash array or during a Write in the EEPROM array, status bits available on certain DQn pins provide information on the M39832 internal logic.

PIN DESCRIPTION

Byte/Word Organization Select ($\overline{BYTE}$). The $\overline{BYTE}$ input selects the output configuration for the Flash array: Byte-wide (x8) mode or Word-wide (x16) mode. The EEPROM array and the 64 Bytes OTP Row are always accessed Byte-wide (x8).

When $\overline{BYTE}$ is High, the Word-wide mode is selected for the Flash array (x16) and the data are read and programmed on DQ0-DQ15. The Flash array is accessed with A0-A18 Adrress lines. In this mode, data in the EEPROM array (x8) are read and programmed on DQ0-DQ7 and the array is accessed with A0-A14. The 64 bytes OTP are read and programmed on DQ0-DQ7 and are accessed with A0-A5 and A6 = 0.

When $\overline{BYTE}$ is Low, the Byte-wide mode is selected for the Flash array (x8) and the data are read and

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 85	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages	–0.6 to 5	V
V_{CC}	Supply Voltage	–0.6 to 5	V
V_{A9}, V_G, V_{EF} (2)	A9, $\overline{G}$, $\overline{EF}$ Voltage	–0.6 to 13.5	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to –2V during transition and for less than 20ns.

programmed on DQ0-DQ7. In this mode, DQ8-DQ14 are at high impedance and DQ15A–1 is the LSB address bit, making the Flash array to be accessed with A–1-A18 Adress lines. In this mode, data in the EEPROM array (x8) are read and programmed on DQ0-DQ7 and the array is accessed with A–1-A13. The 64 bytes OTP are read and programmed on DQ0-DQ7 and are accessed with A-1 - A4 and A6 = 0.

Address Inputs (A0-A18). The address inputs for the memory array are latched during a write operation on the falling edge at Chip Enable ($\overline{EE}$ or $\overline{EF}$) or Write Enable $\overline{W}$. In Word-wide organisation the address lines are A0-A18, in Byte-wide organisation DQ15A–1 acts as an additional LSB address line. When A9 is raised to V_{ID}, either a Read Electronic Signature Manufacturer or Device Code, Block Protection Status or a Write Block Protection or Block Unprotection is enabled depending on the combination of levels on A0, A1, A6, A12 and A15.

Data Input/Output (DQ0-DQ7). These Inputs/Outputs are used in the Byte-wide and Word-wide organisations. The input is data to be programmed in the memory array or a command to be written. Both are latched on the rising edge of Chip Enable ($\overline{EE}$ or $\overline{EF}$) or Write Enable $\overline{W}$. The output is data from the Memory Array, the Electronic Signature Manufacturer or Device codes, the Block Protection Status or the Status register Data Polling bit DQ7, the Toggle Bits DQ6 and DQ2, the Error bit DQ5 or the Erase Timer bit DQ3. Outputs are valid when Chip Enable ($\overline{EE}$ or $\overline{EF}$) and Output Enable $\overline{G}$ are active. The output is high impedance when the chip is deselected or the outputs are disabled and when $\overline{RP}$ is at a Low level.

Data Input/Outputs (DQ8-DQ14 and DQ15A–1). These Inputs/Outputs are additionally used in the Word-wide organisation. When $\overline{BYTE}$ is High DQ8-DQ14 and DQ15A–1 act as the MSB of the Data Input or Output, functioning as described for DQ0-DQ7 above, and DQ8 - DQ15 are 'don't care' for command inputs or status outputs. When $\overline{BYTE}$ is Low, DQ8-DQ14 are high impedance, DQ15A–1 is the Address A–1 input.

Memory Array Enable ($\overline{EE}$ and $\overline{EF}$). The Memory Array Enable ($\overline{EE}$ or $\overline{EF}$) activates the memory control logic, input buffers, decoders and sense amplifiers. When the $\overline{EE}$ input is driven high, the EEPROM memory array is not selected; when the $\overline{EF}$ input is driven high, the Flash memory array is not selected. Attempts to access both EEPROM and Flash arrays ($\overline{EE}$ low and $\overline{EF}$ low) are forbidden. Switching between the two memory array enables ($\overline{EE}$ and $\overline{EF}$) must not be made on the same clock cycle, a delay of greater than t_{EHFL} must be inserted.
The M39832 is in standby when both $\overline{EF}$ and $\overline{EE}$ are High (when no internal Erase or programming is running). The power consumption is reduced to the standby level and the outputs are in the high impedance state, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

After 150ns of inactivity and when the addresses are driven at CMOS levels, the chip automatically enters a pseudo standby mode where consumption is reduced to the CMOS standby value, while the outputs continue to drive the bus.

Output Enable ($\overline{G}$). The Output Enable gates the outputs through the data buffers during a read operation. The data outputs are in the high impedance state when the Output Enable $\overline{G}$ is High.

During Block Protect and Block Unprotect operations, the $\overline{G}$ input must be forced to V_{ID} level (12V + 0.5V) (for Flash memory array only).

Figure 3A. Top Boot Block Memory Map and Block Address Table

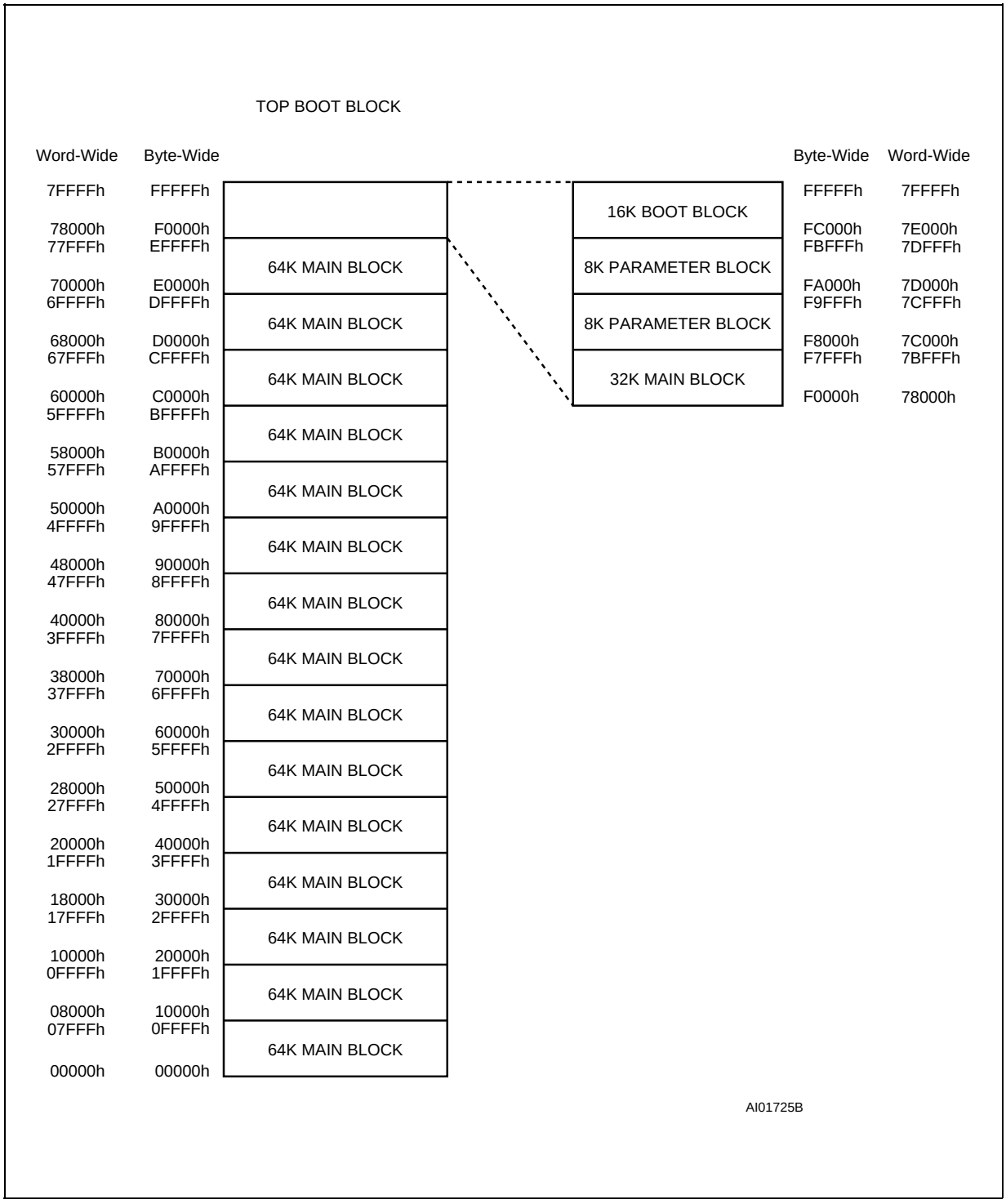


Figure 3B. Bottom Boot Block Memory Map and Block Address Table

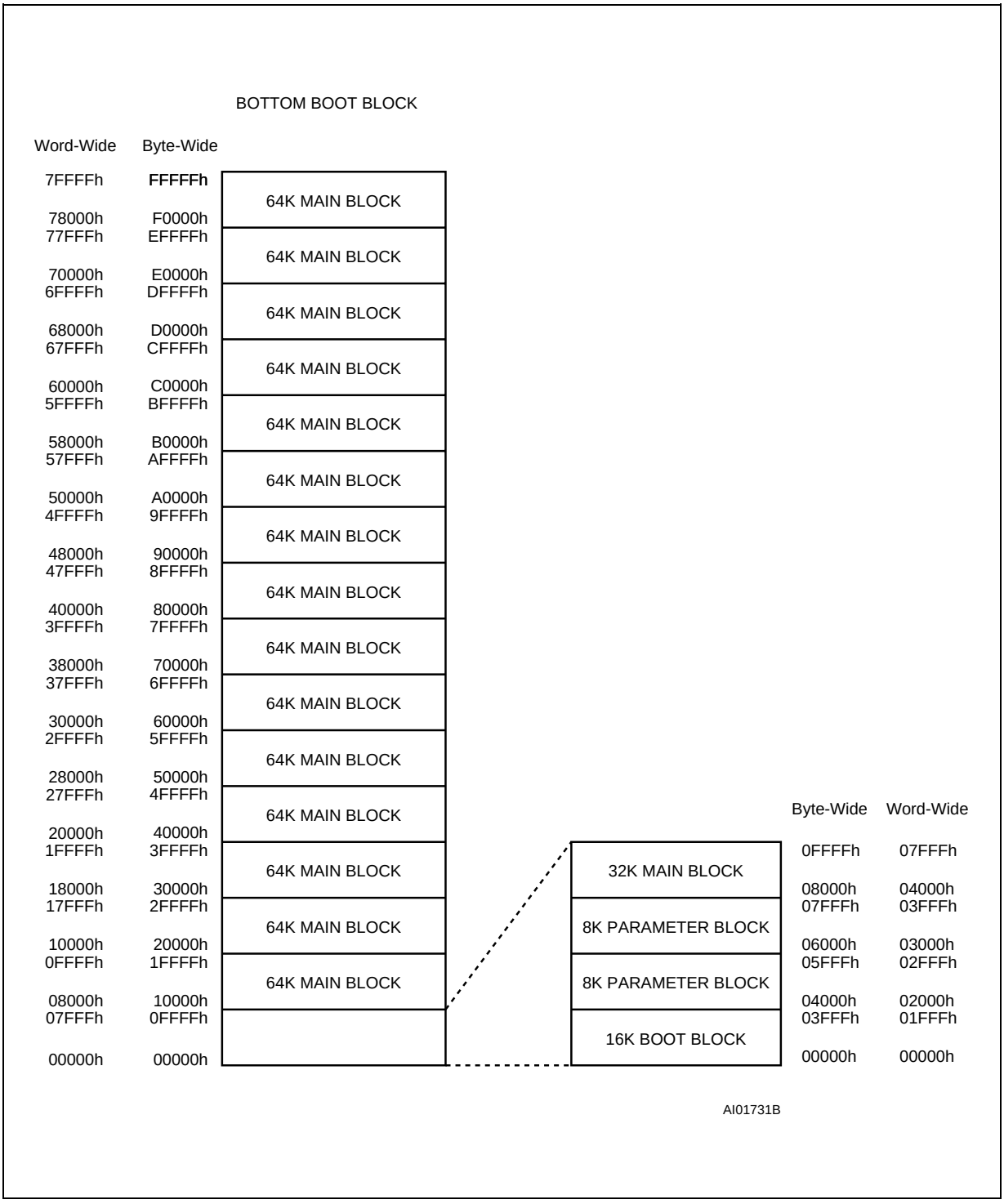


Table 3A. M39832-T Block Address Table

Address Range (x8)	Address Range (x16)	A18	A17	A16	A15	A14	A13	A12
00000h-0FFFFh	00000h-07FFFh	0	0	0	0	X	X	X
10000h-1FFFFh	08000h-0FFFFh	0	0	0	1	X	X	X
20000h-2FFFFh	10000h-17FFFh	0	0	1	0	X	X	X
30000h-3FFFFh	18000h-1FFFFh	0	0	1	1	X	X	X
40000h-4FFFFh	20000h-27FFFh	0	1	0	0	X	X	X
50000h-5FFFFh	28000h-2FFFFh	0	1	0	1	X	X	X
60000h-6FFFFh	30000h-37FFFh	0	1	1	0	X	X	X
70000h-7FFFFh	38000h-3FFFFh	0	1	1	1	X	X	X
80000h-8FFFFh	40000h-47FFFh	1	0	0	0	X	X	X
90000h-9FFFFh	48000h-4FFFFh	1	0	0	1	X	X	X
A0000h-AFFFFh	50000h-57FFFh	1	0	1	0	X	X	X
B0000h-BFFFFh	58000h-5FFFFh	1	1	1	1	X	X	X
C0000h-CFFFFh	60000h-67FFFh	1	1	0	0	X	X	X
D0000h-DFFFFh	68000h-6FFFFh	1	1	0	1	X	X	X
E0000h-EFFFFh	70000h-77FFFh	1	1	1	0	X	X	X
F0000h-F7FFFh	78000h-7BFFFh	1	1	1	1	0	X	X
F8000h-F9FFFh	7C000h-7CFFFh	1	1	1	1	1	0	0
FA000h-FBFFFh	7D000h-7DFFFh	1	1	1	1	1	0	1
FC000h-FFFFFh	7E000h-7FFFFh	1	1	1	1	1	1	X

Table 3B. M39832-B Block Address Table

Address Range (x8)	Address Range (x16)	A18	A17	A16	A15	A14	A13	A12
00000h-03FFFh	00000h-01FFFh	0	0	0	0	0	0	X
04000h-05FFFh	02000h-02FFFh	0	0	0	0	0	1	0
06000h-07FFFh	03000h-03FFFh	0	0	0	0	0	1	1
08000h-0FFFFh	04000h-07FFFh	0	0	0	0	1	X	X
10000h-1FFFFh	08000h-0FFFFh	0	0	0	1	X	X	X
20000h-2FFFFh	10000h-17FFFh	0	0	1	0	X	X	X
30000h-3FFFFh	18000h-1FFFFh	0	0	1	1	X	X	X
40000h-4FFFFh	20000h-27FFFh	0	1	0	0	X	X	X
50000h-5FFFFh	28000h-2FFFFh	0	1	0	1	X	X	X
60000h-6FFFFh	30000h-37FFFh	0	1	1	0	X	X	X
70000h-7FFFFh	38000h-3FFFFh	0	1	1	1	X	X	X
80000h-8FFFFh	40000h-47FFFh	1	0	0	0	X	X	X
90000h-9FFFFh	48000h-4FFFFh	1	0	0	1	X	X	X
A0000h-AFFFFh	50000h-57FFFh	1	0	1	0	X	X	X
B0000h-BFFFFh	58000h-5FFFFh	1	0	1	1	X	X	X
C0000h-CFFFFh	60000h-67FFFh	1	1	0	0	X	X	X
D0000h-DFFFFh	68000h-6FFFFh	1	1	0	1	X	X	X
E0000h-EFFFFh	70000h-77FFFh	1	1	1	0	X	X	X
F0000h-FfFFFh	78000h-7FFFFh	1	1	1	1	X	X	X

Table 4. Basic Operations

$\overline{EF}$	$\overline{EE}$	$\overline{G}$	$\overline{W}$	Operation
V_{IL}	V_{IH}	V_{IL}	V_{IH}	Read in Flash Array
V_{IH}	V_{IL}	V_{IL}	V_{IH}	Read in EEPROM Array
V_{IL}	V_{IH}	V_{IH}	V_{IL}	Write in Flash Array
V_{IH}	V_{IL}	V_{IH}	V_{IL}	Write in EEPROM Array
V_{IL}	V_{IH}	V_{IH}	V_{IH}	Output Disable, DQn = Hi-Z
V_{IH}	V_{IL}	V_{IH}	V_{IH}	Output Disable, DQn = Hi-Z
V_{IH}	V_{IH}	X	X	Standby, DQn = Hi-Z

Note: X = V_{IL} or V_{IH}.

Write Enable ($\overline{W}$). Addresses are latched on the falling edge of $\overline{W}$, and Data Inputs are latched on the rising edge of $\overline{W}$.

EEPROM Ready/Busy (ER$\overline{B}$). The EEPROM Ready/Busy pin outputs the status of the device when the EEPROM memory array is under the write condition

– ER$\overline{B}$ = '0': internal writing is in process,

– ER$\overline{B}$ = '1': no internal writing in in process.

This status pin can be used when reading (or fetching opcodes) in the Flash memory array.

The EEPROM Ready/Busy output uses an open drain transistor, allowing therefore the use of the M39832 in multi-memory applications with all Ready/Busy outputs connected to a single Ready/Busy line (OR-wired with an external pull-up resistor).

Flash Ready/Busy (FR$\overline{B}$). Flash Ready/Busy is an open-drain output and gives the internal state of Flash array. When FR$\overline{B}$ is Low, the Flash array is Busy with a Program or Erase operation and it will not accept any additional program or erase instructions except the Erase Suspend instruction. When FR$\overline{B}$ is High, the Flash array is ready for any Read, Program or Erase operation. The FR$\overline{B}$ will also be High when the Flash array is put in Erase Suspend or Standby modes.

Reset/Block Temporary Unprotect Input ($\overline{RP}$). The $\overline{RP}$ Input provides hardware reset of the Flash array and temporary unprotection of the protected Flash block(s). Reset of the Flash array is acheived by pulling $\overline{RP}$ to V_{IL} for at least t_{PLPX}. When the reset pulse is given while the Flash array is in Read or Standby modes, it will be available for new operations in t_{PHEL} after the rising edge of $\overline{RP}$. If the Flash array is in Erase, Erase Suspend or Program modes the reset will take t_{PLYH} during which the FR$\overline{B}$ signal will be held at VIL. The end of the Flash array reset will be indicated by the rising edge of FR$\overline{B}$. A hardware reset during an Erase or Program operation will corrupt the data being programmed or the block(s) being erased. See Table 14 and Figure 9. Temporary block unprotection is made by holding $\overline{RP}$ at V_{ID}. In this condition, previously protected blocks can be programmed or erased. The transition of $\overline{RP}$ from V_{IH} to V_{ID} must be slower than t_{PHPHH}. See Table 15 and Figure 9. When $\overline{RP}$ is returned from V_{ID} to V_{IH} all blocks temporarily unprotected will be again protected.

OPERATIONS

An operation is defined as the basic decoding of the logic level applied to the control input pins ($\overline{EF}$, $\overline{EE}$, $\overline{G}$, $\overline{W}$) and the specified voltages applied on the relevant address pins. These operations are detailed in Table 3.

Read. Both Chip Enable and Output Enable (that is $\overline{EF}$ and $\overline{G}$ or $\overline{EE}$ and $\overline{G}$) must be low in order to read the output of the memory.

Read operations are used to output the contents from the Flash or EEPROM array, the Manufacturer identifier, the Flash Block protection Status, the Flash Identifier, the EEPROM identifier or the OTP row content.

Notes:

– The Chip Enable input mainly provides power control and should be used for device selection. The Output Enable input should be used to gate data onto the output in combination with active $\overline{EF}$ or $\overline{EE}$ input signals.

– The data read depends on the previous instruction entered into the memory.

Table 5A. Flash Instructions ($\overline{EF}$=0, $\overline{EE}$=1)

Mne.	Instr.	Cyc.			1st Cyc.	2nd Cyc.	3rd Cyc.	4th Cyc.	5th Cyc.	6th Cyc.	7th Cyc.
RD (2,4)	Read/Reset Memory Array	1+	**Addr.** (3,7)		X	Read Memory Array until a new write cycle is initiated.					
			Data		F0h						
		3+	**Addr.** (3,7)	**Byte**	AAAAh	5555h	AAAAh	Read Memory Array until a new write cycle is initiated.			
				Word	5555h	2AAAh	5555h				
			Data		AAh	55h	F0h				
AS (4)	Auto Select	3+	**Addr.** (3,7)	**Byte**	AAAAh	5555h	AAAAh	Read Electronic Signature or Block Protection Status until a new write cycle is initiated. See Note 5 and 6.			
				Word	5555h	2AAAh	5555h				
			Data		AAh	55h	90h				
PG	Program	4	**Addr.** (3,7)	**Byte**	AAAAh	5555h	AAAAh	Program Address	Read Data Polling or Toggle Bit until Program completes.		
				Word	5555h	2AAAh	5555h				
			Data		AAh	55h	A0h	Program Data			
BE	Block Erase	6	**Addr.** (3,7)	**Byte**	AAAAh	5555h	AAAAh	AAAAh	5555h	Block Address	Additional Block (8)
				Word	5555h	2AAAh	5555h	5555h	2AAAh		
			Data		AAh	55h	80h	AAh	55h	30h	30h
FAE	Flash Array Erase	6	**Addr.** (3,7)	**Byte**	AAAAh	5555h	AAAAh	AAAAh	5555h	AAAAh	Note 9
				Word	5555h	2AAAh	5555h	5555h	2AAAh	5555h	
			Data		AAh	55h	80h	AAh	55h	10h	
ES (10)	Erase Suspend	1	**Addr.** (3,7)		X	Read until Toggle stops, then read all the data needed from any Block(s) not being erased then Resume Erase.					
			Data		B0h						
ER	Erase Resume	1	**Addr.** (3,7)		X	Read Data Polling or Toggle Bits until Erase completes or Erase is suspended another time					
			Data		30h						

Notes: 1. Commands not interpreted in this table will default to read array mode.
2. A wait of t_{PLYH} is necessary after a Read/Reset command if the memory was in an Erase or Program mode before starting any new operation (see Table 14 and Figure 9).
3. X = Don't Care.
4. The first cycles of the RD or AS instructions are followed by read operations. Any number of read cycles can occur after the command cycles.
5. Signature Address bits A0, A1, at V_{IL} will output Manufacturer code (20h). Address bits A0 at V_{IH} and A1, at V_{IL} will output Flash code.
6. Block Protection Address: A0, at V_{IL}, A1 at V_{IH} and A15-A18 within the Block will output the Block Protection status.
7. For Coded cycles address inputs A11-A18 are don't care.
8. Optional, additional Blocks addresses must be entered within the erase timeout delay after last write entry, timeout status can be verified through DQ3 value (see Erase Timer Bit DQ3 description). When full command is entered, read Data Polling or Toggle bit until Erase is completed or suspended.
9. Read Data Polling, Toggle bits or $\overline{FRB}$ until Erase completes.
10. During Erase Suspend, Read and Data Program functions are allowed in blocks not being erased.

Table 5B. EEPROM Instructions ($\overline{EE}$=0, $\overline{EF}$=1)

Mne.	Instr.	Cyc.			1st Cyc.	2nd Cyc.	3rd Cyc.	4th Cyc.	5th Cyc.	6th Cyc.	7th Cyc.
WOTP (2)	Write OTP Row	>3	**Addr.**	Byte	5555h	2AAAh	5555h	Addr 1	Addr 2	Addr 3	Addr 4
				Word	5555h	2AAAh	5555h				
			Data		AAh	55h	B0h	Byte 1	Byte 2	Byte 3	Byte 4
ROTP (2)	Read OTP Row	>3	**Addr.**	Byte	5555h	2AAAh	5555h	Addr 1	Addr 2	Addr 3	Addr 4
				Word	5555h	2AAAh	5555h				
			Data		AAh	55h	90h	Byte 1	Byte 2	Byte 3	Byte 4
RT	Return from OTP Read	1	**Addr.**		X (1)						
			Data		F0h						
SSDP (4)	SDP Enable	≥3	**Addr.**	**Byte**	5555h	2AAAh	5555h				
				Word	5555h	2AAAh	5555h				
			Data		AAh	55h	A0h				
SSDP (5)	SDP Disable	6	**Addr.**	**Byte**	5555h	2AAAh	5555h	5555h	2AAAh	5555h	
				Word	5555h	2AAAh	5555h	5555h	2AAAh	5555h	
			Data		AAh	55h	80h	AAh	55h	20h	

Notes: 1. X = Don't Care.
2. Once the WOTP has been initiated (first 3 Cycles), from 1 up to 64 bytes can be written in one single write cycle (See Write OTP chapter in following pages).
3. Once the ROTP has been initiated (first 3 Cycles), from 1 up to 64 bytes of the OTP can be read (See Read OTP chapter in following pages). The RT (Return) instruction MUST be sent to the device to exit ROTP mode.
4. Once SDP is set (SSDP instruction sent once), it is necessary to send SSDP prior to any byte or page to be written in the EEPROM array (See Figure 4 and EEPROM array Software Data Protection chapter in following pages).
5. See Figure 5 and EEPROM array Software Data Protection chapter in following pages.

Table 6. User Bus Operations (1)

Operation	$\overline{EE}$	$\overline{EF}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	$\overline{BYTE}$	A0	A1	A6	A9	A12	A15	DQ15 A–1	DQ8-DQ14	DQ0-DQ7
Block Protection(2,4)	V_{IH}	V_{IL}	V_{ID}	V_{IL} Pulse	V_{IH}	X	X	X	X	V_{ID}	X	X	X	X	X
Blocks Unprotection(4)	V_{IH}	V_{ID}	V_{ID}	V_{IL} Pulse	V_{IH}	X	X	X	X	V_{ID}	V_{IH}	V_{IH}	X	X	X
Block Protection Verify(2,4)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	V_{IL}	V_{ID}	A12	A15	X	X	Block Protect Status (3)
Block Unprotection Verify(2,4)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	V_{IH}	V_{ID}	A12	A15	X	X	Block Protect Status (3)
Block Temporary Unprotection	V_{IH}	X	X	X	V_{ID}	X	X	X	X	X	X	X	X	X	X
Write the EEPROM Identifier (5)	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	A0	A1	V_{IL}	V_{ID}	X	X	A–1	X	64 Bytes User Defined
			V_{IH}	V_{IL}	V_{IH}	V_{IH}	A0	A1	V_{IL}	V_{ID}	X	X	X	X	64 Bytes User Defined
Read the EEPROM Identifier (5)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	A0	A1	V_{IL}	V_{ID}	X	X	A–1	X	64 Bytes User Defined
			V_{IL}	V_{IH}	V_{IH}	V_{IH}	A0	A1	V_{IL}	V_{ID}	X	X	X	X	64 Bytes User Defined

Notes: 1. X = V_{IL} or V_{IH}
2. Block Address must be given on A12-A18 bits.
3. See Table 8.
4. Operation performed on programming equipment.
5. The 65 Bytes User defined EEPROM Identifier are accessed on DQ0-DQ7 with A0 to A5 when $\overline{BYTE}$ = 1 (x16) or with A–1 to A4 when $\overline{BYTE}$ = 0 (x8)

Table 7. Read Electronic Signature (following AS instruction or with A9 = V_{ID})

Org.	Code	Device	$\overline{EE}$	$\overline{EF}$	$\overline{G}$	$\overline{W}$	$\overline{BYTE}$	A0	A1	Other Addresses	DQ15 A–1	DQ8-DQ14	DQ0-DQ7
Word-wide	Manufacturer		V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	Don't Care	0	00h	20h
	Flash	M39832-T	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	Don't Care	0	00h	D7h
		M39832-B	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	Don't Care	0	00h	5Bh
Byte-wide	Manufacturer		V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Don't Care	Don't Care	Hi-Z	20h
	Flash	M39832-T	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Don't Care	Don't Care	Hi-Z	D7h
		M39832-B	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Don't Care	Don't Care	Hi-Z	5Bh

Table 8. Read Block Protection with AS Instruction ($\overline{EF}$ = 0, $\overline{EE}$ = 1)

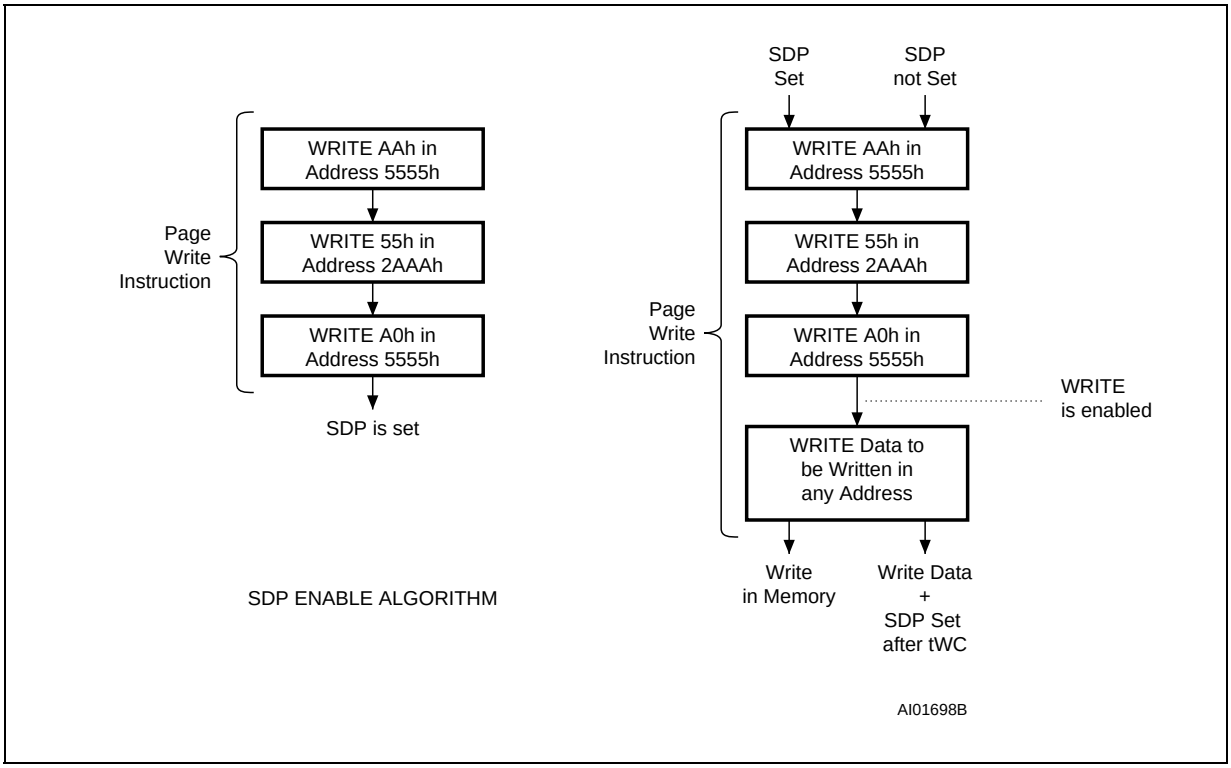
Code	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A1	A12-A18	Other Addresses	DQ0-DQ7
Protected Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Block Address	Don't Care	01h
Unprotected Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Block Address	Don't Care	00h

Table 9. Status Bit

DQ	Name	Logic Level	Definition	Note
7	Data Polling	'1'	Erase Complete or erase block in Erase Suspend	Indicates the P/E.C. status, check during Program or Erase, and on completion before checking bits DQ5 for Program or Erase Success.
		'0'	Erase On-going	
		DQ	Program Complete or data of non erase block during Erase Suspend	
		$\overline{DQ}$	Program On-going	
6	Toggle Bit	'-1-0-1-0-1-0-1-'	Erase or Program On-going	Successive reads output complementary data on DQ6 while Programming or Erase operations are on-going. DQ6 remains at constant level when P/E.C. operations are completed or Erase Suspend is acknowledged.
		DQ	Program Complete	
		'-1-1-1-1-1-1-1-'	Erase Complete or Erase Suspend on currently addressed block	
5	Error Bit	'1'	Program or Erase Error	This bit is set to '1' in the case of Programming or Erase failure.
		'0'	Program or Erase On-going	
4	Reserved			
3	Erase Time Bit	'1'	Erase Timeout Period Expired	P/E.C. Erase operation has started. Only possible command entry is Erase Suspend (ES).
		'0'	Erase Timeout Period On-going	An additional block to be erased in parallel can be entered to the P/E.C.
2	Toggle Bit	'-1-0-1-0-1-0-1-'	Chip Erase, Erase or Erase Suspend on the currently addressed block. Erase Error due to the currently addressed block (when DQ5 = '1').	Indicates the erase status and allows to identify the erased block
		1	Program on-going, Erase on-going on another block or Erase Complete	
		DQ	Erase Suspend read on non Erase Suspend block	
1	Reserved			
0	Reserved			

Notes: Logic level '1' is High, '0' is Low. -0-1-0-0-0-1-1-1-0- represent bit value in successive Read operations.

Figure 4. EEPROM SDP Enable Flowcharts



Write. A Write operation can be used for two goals:

– either write data in the EEPROM memory array

– or enter a sequence of bytes or word composing an instruction.

The reader should note that Programming a Flash byte or word is an instruction (see Instructions paragraph).

Writing data requires:

– the Chip Enable (either $\overline{EE}$ or $\overline{EF}$) to be Low

– the Write Enable ($\overline{W}$) to be Low with Output Enable (G) High.

Addresses in Flash array (or EEPROM array) are latched on the falling edge of $\overline{W}$ or $\overline{EF}$ ($\overline{EE}$) whichever occurs last; the data to be written in Flash array (EEPROM array) is latched on the rising edge of $\overline{W}$ or $\overline{EF}$ ($\overline{EE}$) whichever occurs first.

Specific Read and Write Operations. Device specific data is accessed through operations decoding the V_{ID} level applied on A9 and the logic levels applied on address inputs (A0, A1, A6). These specific operations are:

– Read the Manufacturer identifier

– Read the Flash identifier

– Define and Read the Flash Block protection status

– Read the EEPROM identifier

– Write the EEPROM identifier

Note: The OTP row (64 bytes) is accessed with a specific software sequence detailed in the paragraph "Write in OTP row".

Instructions

An instruction is defined as a sequence of specific Write operations. Each received byte or word is sequentially decoded (and not executed as standard Write operations) and the instruction is executed when the correct number of bytes or word are properly received and the time between two consecutive bytes or words is shorter than the time-out value.

The sequencing of any instruction must be followed exactly, any invalid combination of instruction bytes or word or time-out between two consecutive bytes or word will reset the device logic into a Read memory state (when addressing the Flash array) or directly decoded as a single operation when addressing the EEPROM array.

For efficient decoding of the instruction, the two first bytes or words of an instruction are the coded cycles and are followed by a command confirmation byte or word.

Figure 5. EEPROM SDP disable Flowchart

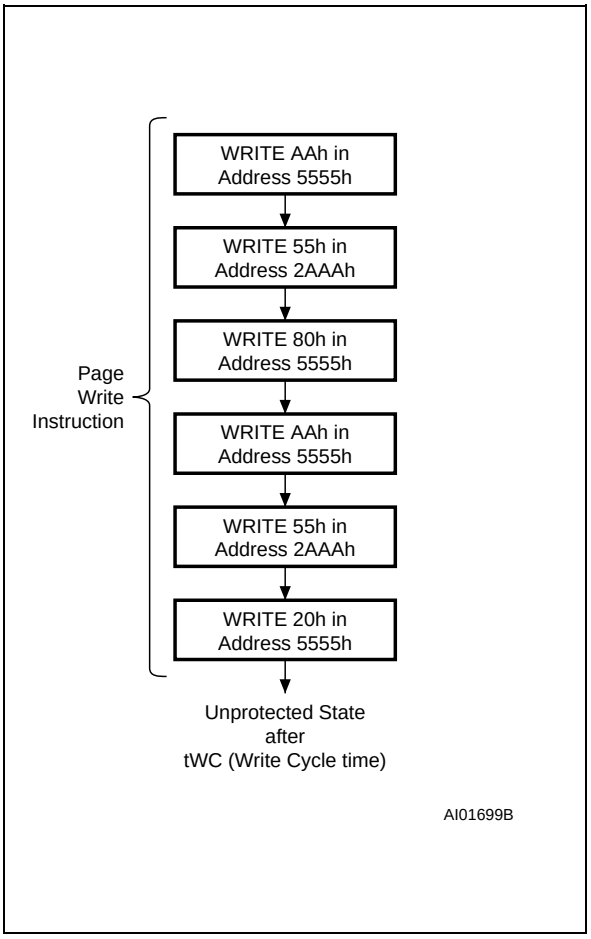
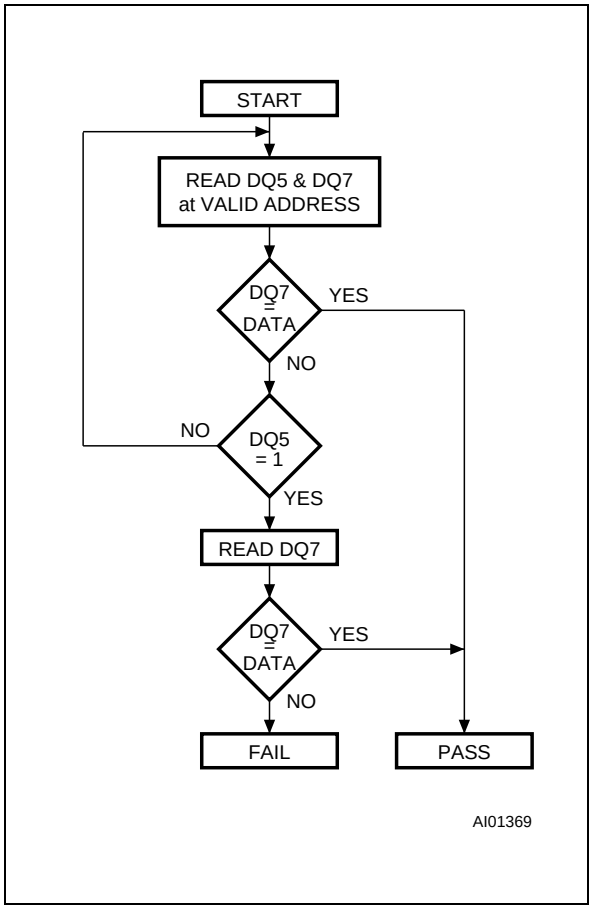


Figure 6. EEPROM and Flash Data Polling Flowchart



READ

Read operations and instructions can be used to:

– read the contents of the Memory Array (Flash and EEPROM)

– read the status bits and identifiers.

Read data (Flash and EEPROM)

Both Chip Enable $\overline{EF}$ (or $\overline{EE}$) and Output Enable ($\overline{G}$) must be low in order to read the data from the memory.

Read the Manufacturer Identifier

The manufacturer's identifier can be read with two methods: a Read operation or a Read instruction.

Read Operation. The manufacturer's identifier can be read with a Read operation with specific logic levels applied on A0, A1, A6 and the V_{ID} level on A9 (See Table 7).

Read Instruction. The manufacturer's identifier can also be read with a single read operation immediatly following the AS instruction (See Table 5A and Table 7).

Read the Flash Identifier

The Flash identifier can be read with two methods: a Read operation or a Read instruction.

Read Operation. The Flash identifier can be read with a single Read operation with specific logic levels applied on A0, A1, A6 and the V_{ID} level on A9 (See Table 7).

Read Instruction. The Flash identifier can also be read with a single read operation immediatly following the AS instruction (See Table 5A and Table 7).

Read the EEPROM Identifier

The EEPROM identifier (64 bytes, user defined) can be read with a single Read operation with A6 = '0' and A9 = V_{ID} (See Table 6).

When accessing the 64 Bytes of EEPROM Identifier, the only LSB addresses are decoded. The LSB addresses are A0 to A5 when $\overline{BYTE}$ = '1' (x16) and A–1 to A4 when $\overline{BYTE}$ = '0' (x8). Each Byte of the EEPROM identifier can be individually accessed in read or write mode.

Read the OTP Row

The OTP row is mapped in the EEPROM array ($\overline{EE}$ = '0', $\overline{EF}$ = '1'). Read of the OTP row (64 bytes) is by an instruction (ROTP) composed of three specific Write operations of data bytes at three specific memory locations (each location in a different page) before reading the OTP row content (See Table 5B).

When accessing the OTP row, only the LSB addresses are decoded and A6 must be '0'. The LSB addresses are A0 to A5 when $\overline{BYTE}$ = '1' (x16) and A–1 to A4 when $\overline{BYTE}$ = '0' (x8).

Each Read of the OTP row has to be followed by the (RT) Return instruction (See Table 5B).

Read the Flash Block Protection Status

Reading the Flash block protection status is by a read operation immediatly following the AS instruction (See Table 5A and Table 8). A12-A18 define the Flash block whose protection has to be verified. This Read operation will output a 01h if the Flash block is protected and a 00h if the Flash block is not protected.

The Flash block protection status can also be verified with a single Read operation (see chapter: Flash array specific features), with V_{ID} on A9 (See Table 6 and Table 8).

Read the Status Bits

The M39832 provides several Write operation status flags which may be used to minimize the application write (or erase or program) time. These signals are available on the I/O port bits when programming (or erasing) are in progress. It should be noted that the Ready/Busy pins also reflects the status of the EEPROM Write and the Flash Programming/Erasing.

Data Polling flag, DQ7. When Erasing or Programming into the Flash block (or when Writing into the EEPROM block), bit DQ7 outputs the complement of the bit being entered for Programming/Writing on DQ7. Once the Program instruction or the Write operation is performed, the true logic value is read on DQ7 (in a Read operation).

Flash memory block specific features:

– Data Polling is effective after the fourth W pulse (for programming) or after the sixth W pulse (for Erase). It must be performed at the address being programmed or at an address within the Flash sector being erased.

– During an Erase instruction, DQ7 outputs a '0'. After completion of the instruction, DQ7 will output the last bit programmed (that is a '1' after erasing).

– if the byte to be programmed is in a protected Flash sector, the instruction is ignored.

– If all the Flash sectors to be erased are protected, DQ7 will be set to '0' for about 100µs, and then return to the previous addressed byte. No erasure will be performed.

– if all sectors are protected, a Bulk Erase instruction is ignored.

Toggle flag, DQ6. The M39832 also offers another way for determining when the EEPROM write or the Flash memory Program instruction is completed. During the internal Write operation, the DQ6 will toggle from '0' to '1' and '1' to '0' on subsequent attempts to read any byte of the memory, when either $\overline{G}$, $\overline{EE}$ or $\overline{EF}$ is low.

When the internal cycle is completed the toggling will stop and the data read on DQ0-DQ7 is the addressed memory byte. The device is now accessible for a new Read or Write operation. The operation is completed when two successive reads yield the same output data.

Flash memory block specific features:

a. The Toggle bit is effective after the fourth $\overline{W}$ pulse (for programming) or after the sixth $\overline{W}$ pulse (for Erase).

b. If the byte to be programmed belongs to a protected Flash sector, the instruction is ignored and:

– if all the Flash sectors selected for erasure are protected, DQ6 will toggle to '0' for about 100µs, and then return to the previous addressed byte.

– if all sectors are protected, the Bulk Erase instruction is ignored.

Figure 7A. Data Toggle Flowchart

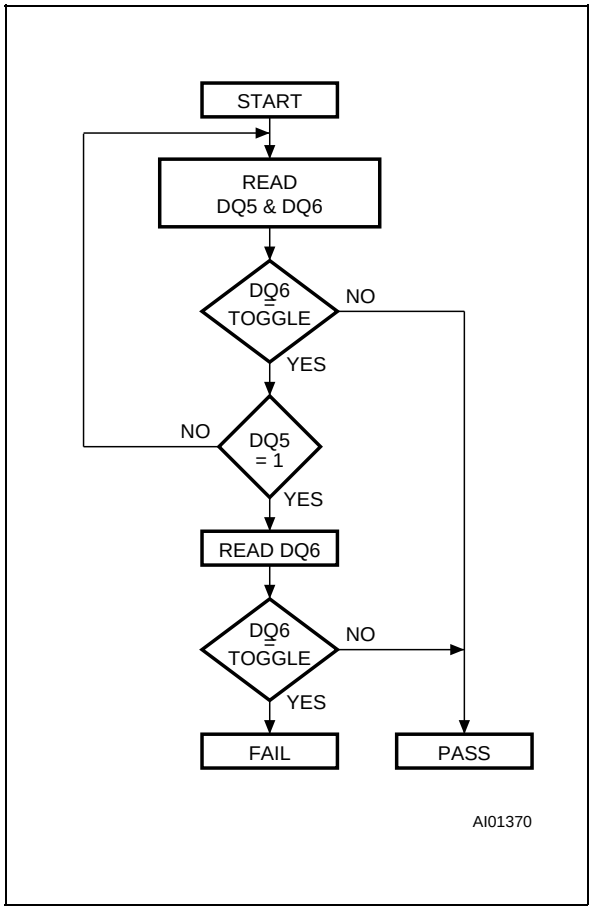
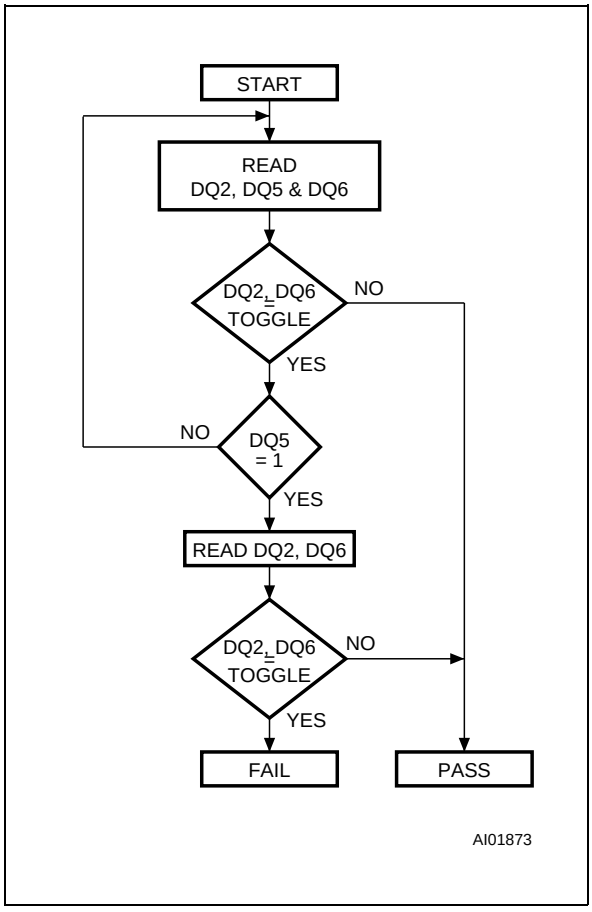


Figure 7B. Flash ata Toggle Flowchart



Toggle Bit, DQ2 (Flash array only). This toggle bit, together with DQ6, can be used to determine the device status during the Erase operations. It can also be used to identify the block being erased. During Erase or Erase Suspend a read from a block being erased will cause DQ2 to toggle. A read from a block not being erased will set DQ2 to '1' during erase and to DQ2 during Erase Suspend. During Flash Array Erase, a read operation will cause DQ2 to toggle as all blocks are being erased. DQ2 will be set to '1' during program operation and when erase is complete. After erase completion and if the error bit DQ5 is set to '1', DQ2 will toggle if the faulty block is addressed.

Error flag, DQ5 (Flash block only). This bit is set to '1' by the internal logic when there is a failure of programming, block erase, or chip erase that results in invalid data in the memory block. In case of an error in block erase or program, the block in which the error occured or to which the programmed data belongs, must be discarded. The DQ5 failure condition will also appear if a user tries to program a '1' to a location that is previously programmed to '0'. Other Blocks may still be used. The error bit resets after a Read/Reset (RD) instruction. In case of success of Program or Erase, the error bit will be set to '0' . when A0 is High with A1 Low.

Erase Timer Bit, DQ3 (Flash array only). This bit is set to '0' by internal logic when the last block Erase command has been entered to the Command Interface and it is awaiting the Erase start. When the erase timeout period is finished, after 50ms to 90ms, DQ3 returns to '1'.

WRITE a BYTE (or a PAGE) in EEPROM

It should be noticed that writing in the EEPROM array is an operation, it is not an instruction (as for Programming a byte in the Flash array).

Write a Byte in EEPROM Array

A write operation is initiated when Chip Enable $\overline{E}$ is Low and Write Enable $\overline{W}$ is Low with Output

Enable $\overline{G}$ High. Addresses are latched on the falling edge of $\overline{W}$, $\overline{EE}$ whichever occurs last.

Once initiated, the write operation is internally timed until completion, that is during a time t_W.

The status of the write operation can be found by reading the Data Polling and Toggle bits (as detailed in the READ chapter) or the $\overline{ERB}$ output. This Ready/Busy output is driven low from the write of the byte being written until the completion of the internal Write sequence.

Write a Page in EEPROM Array

The Page write allows up to 64 bytes within the same EEPROM page to be consecutively latched into the memory prior to initiating a programming cycle. All bytes must be located in a single page address, that is A6-A14 when $\overline{BYTE}$ is high (x16) or A5-A13 when $\overline{BYTE}$ is low (x8) must be the same for all bytes. Once initiated, the Page write operation is internally timed until completion, that is during a time t_{WC}.

The status of the write operation can be seen by reading the Data Polling and Toggle bits (as detailed in the READ chapter) or the $\overline{ERB}$ output. This Ready/Busy output is driven low from the write of the first byte to be written until the completion of the internal Write sequence.

A Page write is composed of successive Write operations which must be sequenced within a time period (between two consecutive Write operations) that is smaller than the t_{WLWL} value. If this period of time exceeds the t_{WLWL} value, the internal programming cycle will start.

EEPROM Array Software Data Protection

A protection instruction allows the user to inhibit all write modes to the EEPROM array: the Software Data Protection (referenced as SDP in the following). The SDP feature is useful for protecting the EEPROM memory from inadvertent write cycles that may occur during uncontrolled bus conditions.

The M39832 is shipped as standard in the unprotected state meaning that the EEPROM memory contents can be changed by the user. After the SDP enable instruction, the device enters the Protect Mode where no further write operations have any effect on the EEPROM memory contents.

The device remains in this mode until a valid SDP disable instruction is received whereby the device reverts to the unprotected state.

To enable the Software Data Protection, the device has to be written (with a Page Write) with three specific data bytes at three specific memory locations (each location in a different page) as shown in Figure 4 and Table 5B. This sequence provides an unlock key to enable the write action, and, at the same time, SDP continues to be set. Any further Write in EEPROM when the SDP is set will use this same sequence of three specific data bytes at three specific memory locations followed by the bytes to write. The first SDP enable sequence can be directly followed by the bytes to written.

Similarly, to disable the Software Data Protection the user has to write specific data bytes into six different locations with a Page Write addressing different bytes in different pages, as shown in Figure 5 and Table 5B.

The Software Data Protection state is non-volatile and is not changed by power on/off sequences. The SDP enable/disable instructions set/reset an internal non-volatile bit and therefore will require a write time t_{WC}, This Write operation can be monitored only on the Toggle bit (status bit DQ6) and the $\overline{ERB}$ pin. The Ready/Busy output is driven low from the first byte to be written (that is the first Write AAh, @5555h of the SDP set/reset sequence) until the completion of the internal Write sequence.

Write OTP Row

Writing (only one time) in the OTP row (64 bytes) is enabled by an instruction (WOTP). This instruction is composed of three specific Write operations of data bytes at three specific memory locations (each location in a different page) followed by the the data to store in the OTP row (refer to Table 5B).

When accessing the OTP row, the only LSB addresses are decoded and A6 must be '0'. The LSB addresses are A0 to A5 when $\overline{BYTE}$ = '1' (x16) and A–1 to A4 when $\overline{BYTE}$ = '0' (x8). Once at least one Byte of the OTP row has been written (even with FFh), the whole row becomes Read only.

Write the EEPROM Block Identifier

The EEPROM block identifier (64 Bytes) can be written with a single Write operation with A6 = '0' and the V_{ID} level on A9 (see Table 6). When accessing the 64 Bytes of EEPROM Identifier, the only LSB addresses are decoded. The LSB addresses are A0 to A5 when $\overline{BYTE}$ = '1' (x16) and A-1 to A4 when $\overline{BYTE}$ = '0' (x8). Each Byte of the EEPROM identifier can be individually accessed in read or write mode.

PROGRAM in the Flash ARRAY

It should be noted that writing data into the EEPROM array and the Flash array is not performed in a similar way: the Flash memory requires an instruction (see Instruction chapter) for Erasing and another instruction for Programming one (or more) byte(s) or word(s), the EEPROM memory is directly written with a simple operation (see Operation chapter).

Program (PG) Instruction. This instruction uses four write cycles. Both for Byte-wide configuration and for Word-wide configuration. The Program command A0h is written to address AAAAh in the Byte-wide configuration or to address 5555h in the Word-wide configuration on the third cycle after two Coded cycles. A fourth write operation latches the Address on the falling edge of $\overline{W}$ or $\overline{EF}$ and the Data to be written on the rising edge and starts the internal operation. Read operations output the Status Register bits after the programming has started. Memory programming is made only by writing '0' in place of '1'. Status bits DQ6 and DQ7 determine if programming is on-going and DQ5 allows verification of any possible error. Programming at an address not in blocks being erased is also possible during erase suspend. In this case, DQ2 will toggle at the address being programmed.

Auto Select (AS) Instruction. This instruction uses the two Coded cycles followed by one write cycle giving the command 90h to address AAAAh in the Byte-wide configuration or address 5555h in the Word-wide configuration for command set-up. A subsequent read will output the manufacturer code and the device code or the block protection status depending on the levels of A0 and A1. The manufacturer code is output when the addresses lines A0 and A1 are Low, the Flash code for Top Boot or Bottom Boot is output when A0 is High with A1 Low.

The AS instruction allows access to the block protection status. After giving the AS instruction, A0 is set to V_{IL} with A1 at V_{IH}, while A12-A18 define the address of the block to be verified. A read in these conditions will output a 01h if the block is protected and a 00h if the block is not protected.

The ERASE in the Flash ARRAY

Flash Array Erase (FAE) Instruction. This instruction uses six write cycles. The Erase Set-up command 80h is written to address AAAAh in the Byte-wide configuration or the address 5555h in the Word-wide configuration on the third cycle after the two Coded cycles. The Flash Array Erase Confirm command 10h is similarly written on the sixth cycle after another two Coded cycles. If the second command given is not an erase confirm or if the Coded cycles are wrong, the instruction aborts and the device is reset to Read Array. It is not necessary to program the array with 00h first as it will be done automatically before erasing it to FFh. Read operations after the sixth rising edge of $\overline{W}$ or $\overline{EF}$ output the Status Register bits. During the execution of the erase, Data Polling bit DQ7 returns '0', then '1' on completion. The Toggle bits DQ2 and DQ6 toggle during erase operation and stop when erase is completed. After completion, the Status Bit DQ5 returns '1' if there has been an Erase Failure.

Block Erase (BE) Instruction. This instruction uses a minimum of six write cycles. The Erase Set-up command 80h is written to address AAAh in the Byte-wide configuration or address 5555h in the Word-wide configuration on third cycle after the two Coded cycles. The Block Erase Confirm command 30h is similarly written on the sixth cycle after another two Coded cycles. During the input of the second command an address within the block to be erased is given and latched into the memory. Additional block Erase Confirm commands and block addresses can be written subsequently to erase other blocks in parallel, without further Coded cycles. The erase will start after the erase timeout period (see Erase Timer Bit DQ3 description). Thus, additional Erase Confirm commands for other blocks must be given within this delay. The input of a new Erase Confirm command will restart the timeout period. The status of the internal timer can be monitored through the level of DQ3, if DQ3 is '0' the Block Erase Command has been given and the timeout is running, if DQ3 is '1', the timeout has expired and the Block(s) are being erased. If the second command given is not an erase confirm or if the Coded cycles are wrong, the instruction aborts, and the device is reset to Read Array. It is not necessary to program the block with 00h as it will be done automatically before erasing it to FFh. Read operations after the sixth rising edge of $\overline{W}$ or $\overline{EF}$ output the Status Register bits.

During the execution of the erase , the memory accepts only the Erase Suspend ES and Read/Reset RD instructions. Data Polling bit DQ7 returns '0' while the erasure is in progress and '1' when it has completed. The Toggle bit DQ2 and DQ6 toggle during the erase operation. They stop when erase is completed. After completion the Status bit DQ5 returns '1' if there has been an erase failure. In such a situation, the Toggle bit DQ2 can be used to determine which block is not correctly erased. In the case of erase failure, a Read/Reset RD instruction is necessary in order to reset the memory.

Figure 8. Block Protection Flowchart

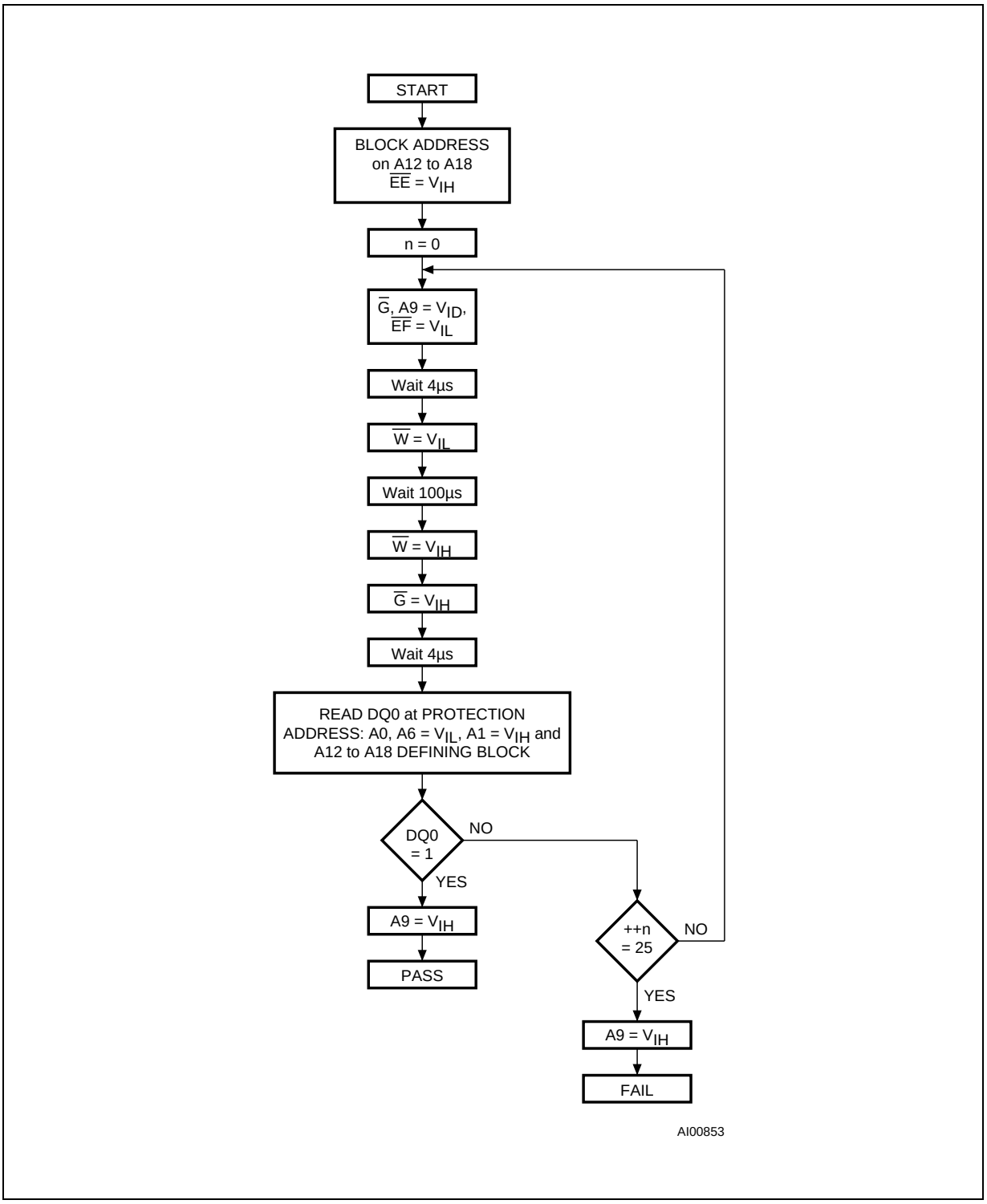
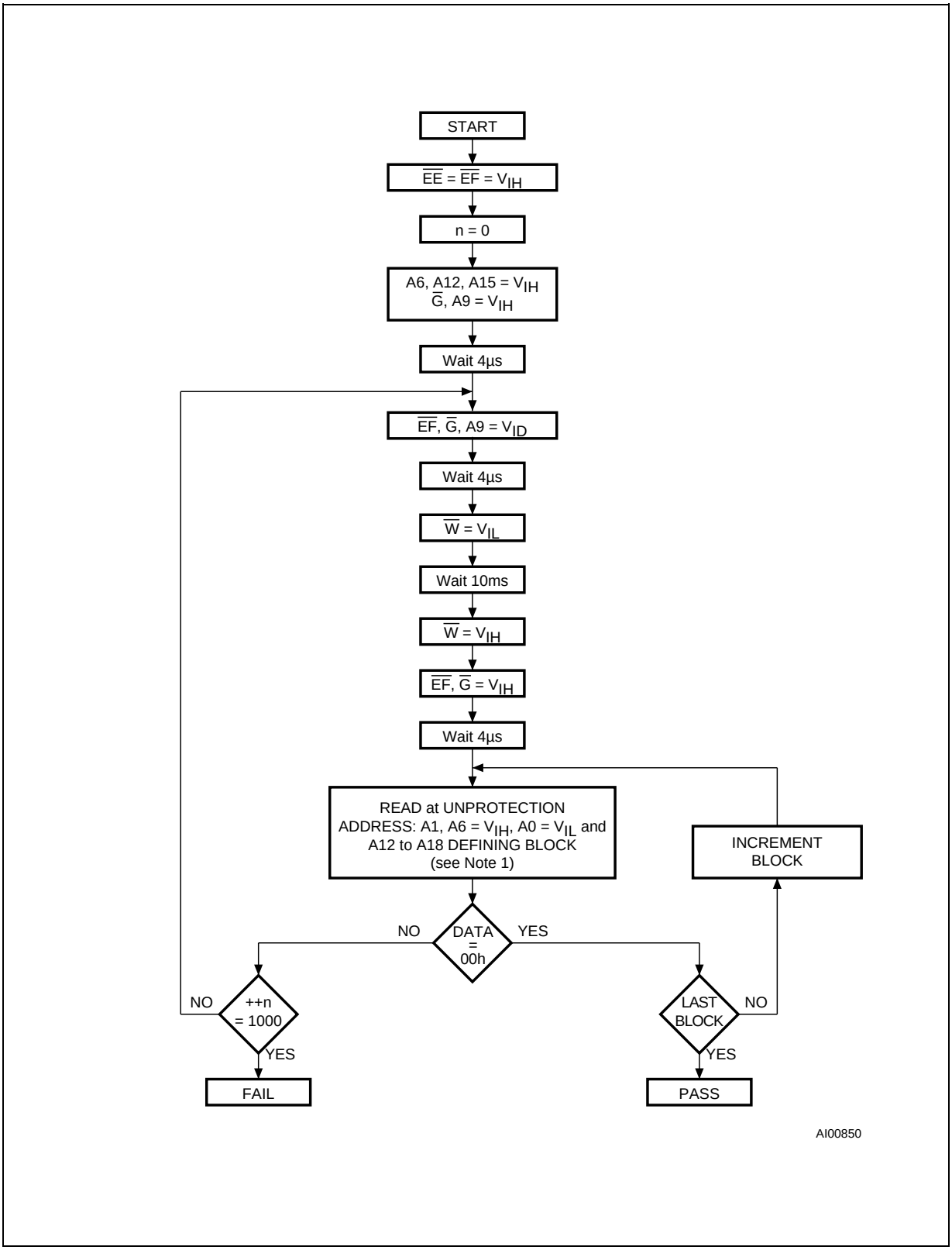


Figure 9. Block Unprotecting Flowchart



Note: 1. A6 is kept at V_{IH} during unprotection algorithm in order to secure best unprotection verification. During all other protection status reads, A6 must be kept at V_{IL}.

Table 10. AC Measurement Conditions

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0.V to V_{CC}
Input and Output Timing Ref. Voltages	V_{CC} / 2

Figure 10. AC Testing Input Output Waveform

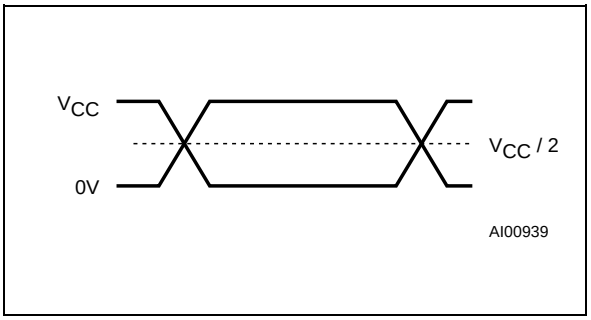


Figure 11. Output AC Testing Load Circuit

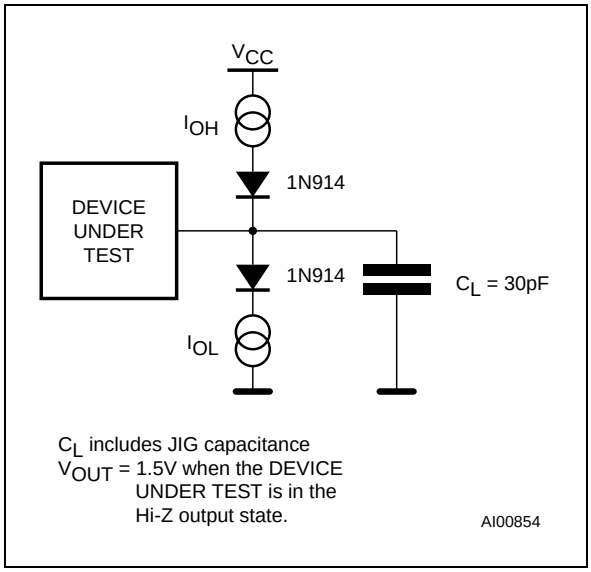


Table 11. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Erase Suspend (ES) Instruction. The Block Erase operation may be suspended by this instruction which consists of writing the command B0h without any specific address. No Coded cycles are required. It permits reading of data from another block and programming in another block while an erase operation is in progress. Erase suspend is accepted only during the Block Erase instruction execution. Writing this command during Erase timeout will, in addition to suspending the erase, terminate the timeout. The Toggle bit DQ6 stops toggling when erase is suspended. The Toggle bits will stop toggling between 0.1ms and 15ms after the Erase Suspend (ES) command has been written. The device will then automatically be set to Read Memory Array mode. When erase is suspended, a Read from blocks being erased will output DQ2 toggling and DQ6 at '1'. A Read from a block not being erased returns valid data. During suspension the memory will respond only to the Erase Resume ER and the Program PG instructions.

A Program operation can be initiated during erase suspend in one of the blocks not being erased. It will result in both DQ2 and DQ6 toggling when the data is being programmed. A Read/Reset command will definitively abort erasure and result in invalid data in the blocks being erased.

Erase Resume (ER) Instruction. If an Erase Suspend instruction was previously executed, the erase operation may be resumed by giving the command 30h, at any address, and without any Coded cycles.

FLASH ARRAY SPECIFIC FEATURES

Block Protection (See Figure 8). Each block can be separately protected against Program or Erase on programming equipment. Block protection provides additional data security, as it disables all program or erase operations. This mode is activated when both A9 and G are raised to V_{ID} and an address in the block is applied on A12-A18. Block protection is initiated on the edge of W falling to V_{IL}. Then after a delay of 100ms, the edge of W rising to V_{IH} ends the protection operations. Block protection verify is achieved by bringing G, $\overline{EF}$, A0 and A6 to V_{IL} and A1 to V_{IH}, while W is at V_{IH} and A9 at V_{ID}.

Under these conditions, reading the data output will yield 01h if the block defined by the inputs on A12-A18 is protected. Any attempt to program or erase a protected block will be ignored by the device.

Remarks:

– The Verify operation is a read with a simulated worst case conditions. This allows a guarantee of the retention of the Protection status

– During the application life, the block protection status can be accessed with a regular Read instruction without applying a "high voltage" V_{ID} on A9. This instruction is detailed in Table 5 and Table 8.

Blocks Unprotection (See Figure 9). All protected blocks can be unprotected simultaneously on programming equipment to allow updating of bit contents. All blocks must first be protected before the unprotection operation. Block unprotection is activated when A9, $\overline{G}$ and $\overline{E}$ are at V_{ID} and A12, A15 at V_{IH}. Unprotection is initiated by the edge of $\overline{W}$ falling to V_{IL}. After a delay of 10ms, the unprotection operation will end. Unprotection verify is achieved by bringing $\overline{G}$ and $\overline{E}$ to V_{IL} while A0 is at V_{IL}, A6 and A1 are at V_{IH} and A9 remains at V_{ID}. In these conditions, reading the output data will yield 00h if the block defined by the inputs A12-A18 has been succesfully unprotected. Each block must be separately verified by giving its address in order to ensure that it has been unprotected.

Remarks:

– The Verify operation is a read with a simulated worst case conditions. This allows a guarantee of the retention of the Protection status

– During the application life, the Block protection status can be accessed with a regular Read instruction without "high voltage" V_{ID} on A9. This instruction is detailed in Table 5 and Table 8.

Block Temporary Unprotection. Any previously protected block can be temporarily unprotected in order to change stored data. The temporary unprotection mode is activated by bringing RP to V_{ID}. During the temporary unprotection mode the previously protected blocks are unprotected. A block can be selected and data can be modified by executing the Erase or Program instruction with the RP signal held at V_{ID}. When RP is returned to VIH, all the previously protected blocks are again protected.

Read/Reset (RD) Instruction. The Read/Reset instruction consists of one write cycle giving the command F0h. It can be optionally preceded by the two Coded cycles. Subsequent read operations will read the memory array addressed and output the data read. A wait state of 10ms is necessary after Read/Reset prior to any valid read if the memory was in an Erase mode when the RD instruction is given.

GLOSSARY

Array: EEPROM array (256 Kbit) or Flash array (8 Mbit)

Block: part of the Flash array (See Figure 3A and 3B).

Page: 64 bytes of EEPROM

Write and Program: Writing (into the EEPROM array) and programming (the Flash array is not performed in a similar way:

– the Flash memory requires an instruction (see Instruction chapter) for Erasing and another instruction for Programming one (or more) byte(s) or word(s)

– the EEPROM memory is directly written with a simple operation (see Operation chapter).

SDP: Software Data Protection. Used for protecting the EEPROM array against false Write operations (as in noisy environments).

POWER SUPPLY and CURRENT CONSUMPTION

Power Up. The M39832 internal logic is reset upon a power-up condition to Read memory status. Any Write operation in EEPROM is inhibited during the first 5 ms following the power-up.

Either $\overline{EF}$, $\overline{EE}$ or $\overline{W}$ must be tied to V_{IH} during Power-up for the maximum security of the data contents and to remove the possibility of a byte being written on the first rising edge of $\overline{EF}$, $\overline{EE}$ or $\overline{W}$. Any write cycle initiation is locked when Vcc is below V_{LKO}.

Supply Rails. Normal precautions must be taken for supply voltage decoupling, each device in a system should have the V_{CC} rail decoupled with a 0.1µF capacitor close to the V_{CC} and V_{SS} pins. The printed circuit board trace width should be sufficient to carry the V_{CC} program and erase currents required.

Table 12. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.7 to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC1} (1)	Supply Current (Read Flash)	$\overline{EE} = V_{IH}$, $\overline{EF} = V_{IL}$, $\overline{G} = V_{IH}$, f = 6MHz		10	mA
I_{CC2}	Supply Current (Read EEPROM)	$\overline{EE} = V_{IL}$, $\overline{EF} = V_{IH}$, $\overline{G} = V_{IH}$, f = 6MHz		10	mA
I_{CC3}	Supply Current (Standby)	$\overline{EF} = \overline{EE} = V_{CC} \pm 0.2V$		100	µA
I_{CC4}	Supply Current (Flash Block Program or Erase)	Byte program, Sector or Chip Erase in progress		20	mA
I_{CC5}	Supply Current (EEPROM Write)	During t_{WC}		20	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}	VCC + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.8mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –100µA	V_{CC} –0.4		V
V_{ID}	A9 High Voltage		11.5	12.5	V
I_{ID}	V_{ID} Current	A9 = V_{ID}		100	µA
V_{LKO}	V_{CC} Minimum for Write, Erase and Program		1.9	2.3	V

Note: 1. When reading the Flash block when an EEPROM byte(s) is under a write cycle, the supply current is $I_{CC1} + I_{CC5}$.

Figure 12. Read Mode AC Waveforms

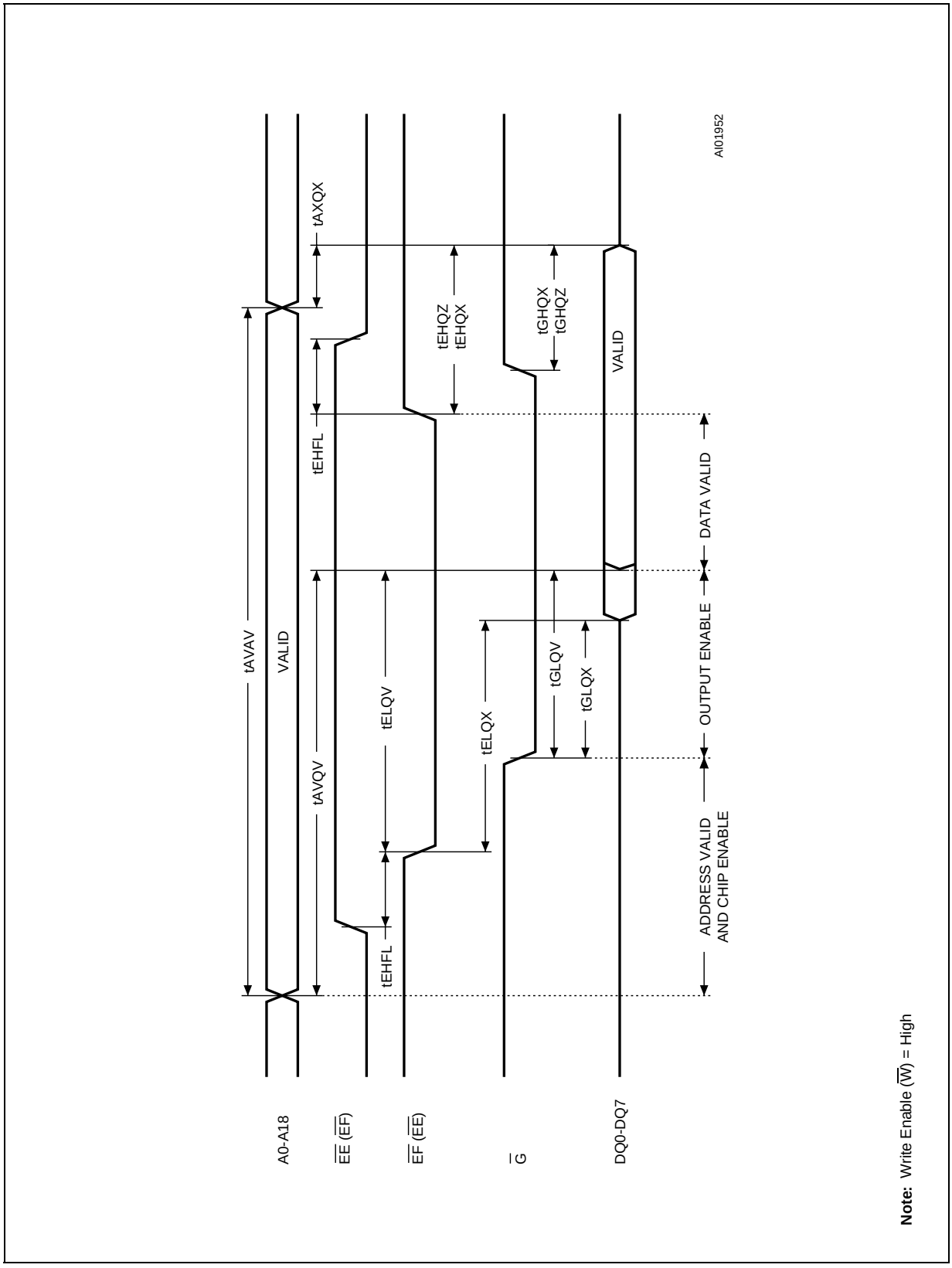
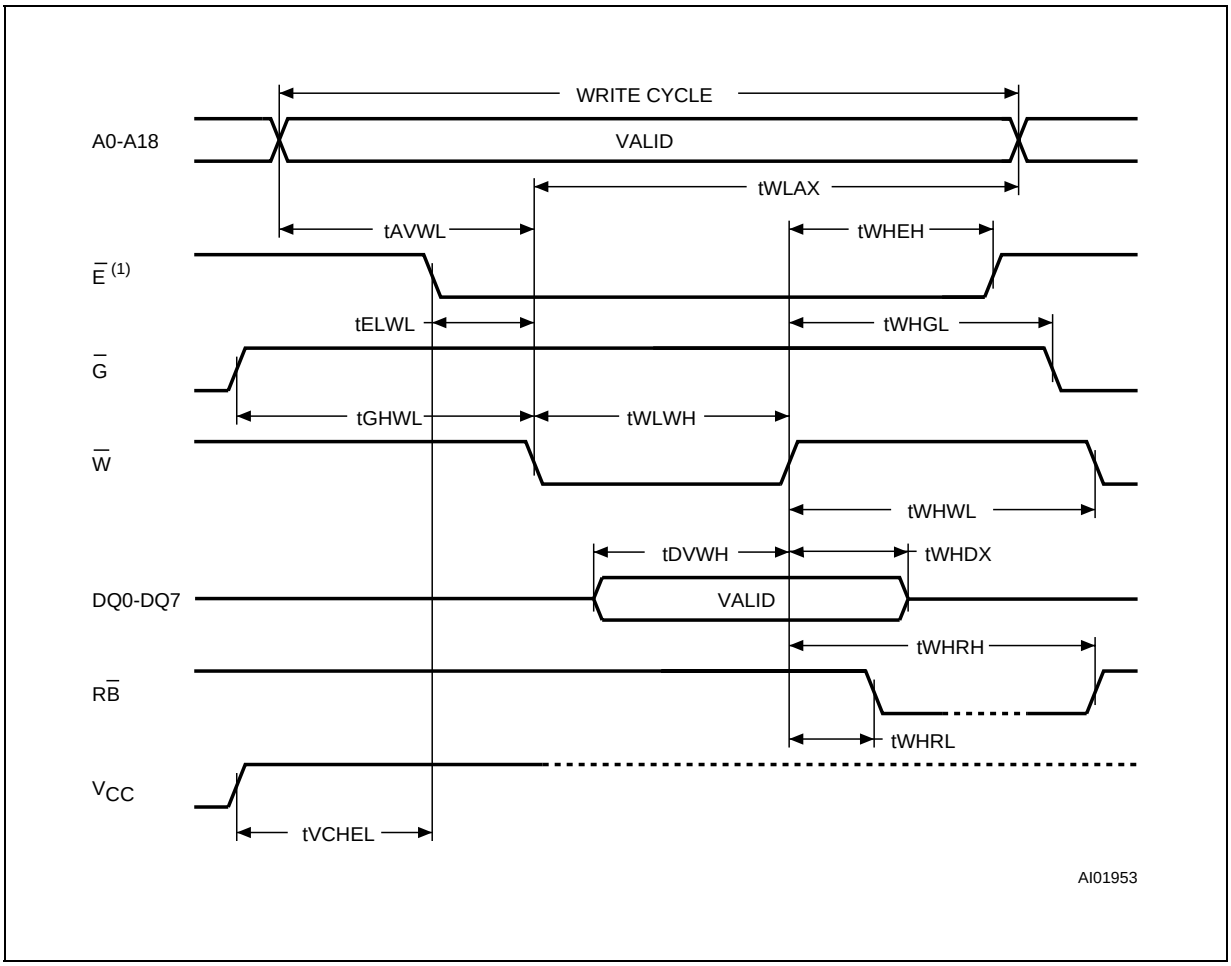


Table 13. Read AC Characteristics
(T_A = 0 to 70°C or –20 to 85°C; V_{CC} = 3.3V ± 0.3V)

Symbol	Alt	Parameter	Test Condition	M39832				Unit
				-120		-150		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(EE, \overline{EF}) = (V_{IH}, V_{IL})$, $\overline{G} = V_{IL}$	120		150		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(EE, \overline{EF}) = (V_{IH}, V_{IL})$, $\overline{G} = V_{IL}$		120		150	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		120		150	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(EE, EF) = (V_{IH}, V_{IL})$	0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(EE, EF) = (V_{IH}, V_{IL})$		55		55	ns
t_{EHQX}	t_{OH}	Chip Enable High to Output Transition	$\overline{G} = V_{IL}$	0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$		40		40	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(EE, EF) = (V_{IH}, V_{IL})$	0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(EE, EF) = (V_{IH}, V_{IL})$		40		40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(EE, \overline{EF}) = (V_{IH}, V_{IL})$, $\overline{G} = V_{IL}$	0		0		ns
t_{EHFL}	t_{CED}	$\overline{EE}$ ($\overline{EF}$) Active to $\overline{EF}$ ($\overline{EE}$)		100		100		ns

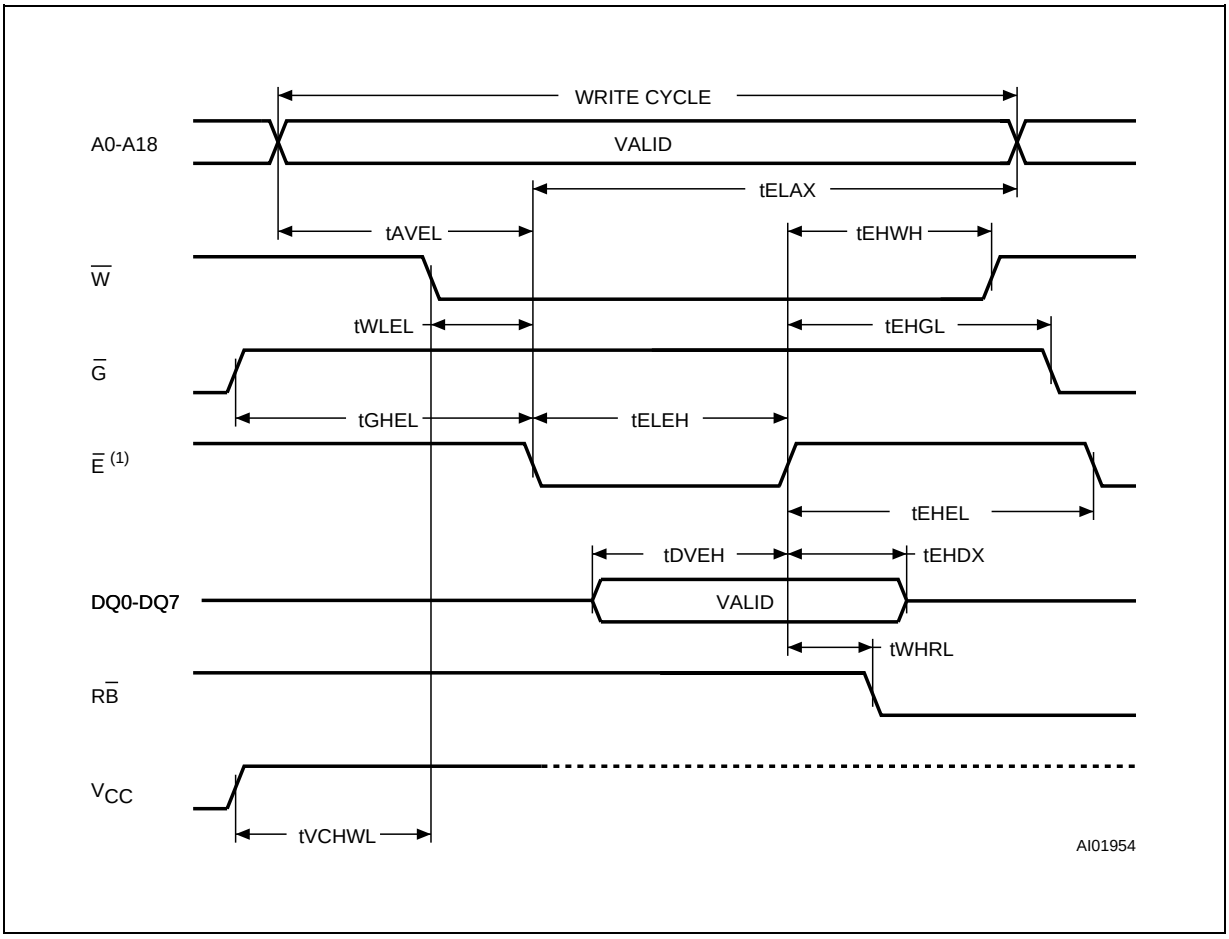
Notes: 1. Sampled only, not 100% tested.
2. $\overline{G}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{EE}$ (or $\overline{EF}$) without increasing t_{ELQV}.

Figure 13. Write AC Waveforms, $\overline{W}$ Controlled



Notes: Address are latched on the falling edge of $\overline{W}$, Data is latched on the rising edge of $\overline{W}$.
$\overline{E}$ is either $\overline{EF}$ when $\overline{EE}$ = V_{IH} or $\overline{EE}$ when $\overline{EF}$ = V_{IH}.

Figure 14. Write AC Waveforms, $\overline{E}$ Controlled



Notes: Address are latched on the falling edge of $\overline{E}$, Data is latched on the rising edge of $\overline{E}$.
$\overline{E}$ is either $\overline{EF}$ when $\overline{EE}$ = V_{IH} or $\overline{EE}$ when $\overline{EF}$ = V_{IH}.

Table 14. Write AC Characteristics, Write Enable Controlled
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.7V to 3.6V)

Symbol	Alt	Parameter	M39832				Unit
			-120		-150		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	120		150		ns
t_{ELWL} (2)	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50		65		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		65		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		ns
t_{WHEH} (2)	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	30		35		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	50		65		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	50		50		µs
t_{WHQV1} (1)		Write Enable High to Output Valid (Program)	15		15		µs
t_{WHQV2} (1)		Write Enable High to Output Valid (Sector Erase)	2.0	30	2.0	30	sec
t_{WHWL0}		Time Out between 2 consecutive Section Erase		80		80	µs
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	0		0		ns
t_{WHRL} (3)	t_{DB}	Write Enable High to Ready/Busy Output Low		150		150	ns

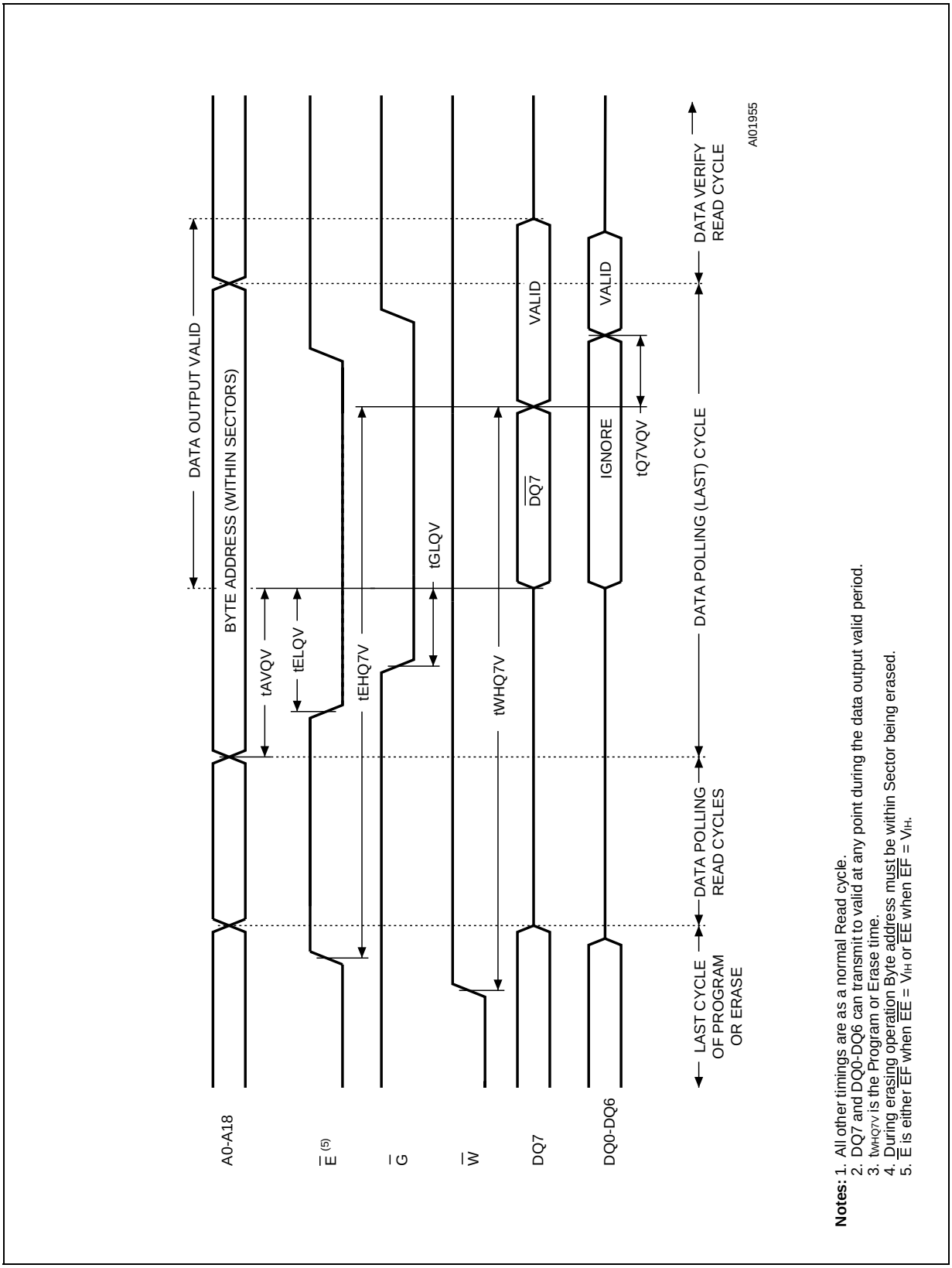
Notes: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQ7V} + t_{Q7VQV}$
2. Chip Enable means ($\overline{EE}$, $\overline{EF}$) = (V_{IL}, V_{IH}) or ($\overline{EE}$, $\overline{EF}$) = (V_{IH}, V_{IL}).
3. With a 3.3KΩ pull-up resistor.

Table 15. Write AC Characteristics, $\overline{EE}$ or $\overline{EF}$ Controlled
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.7V to 3.6V)

Symbol	Alt	Parameter	M39832				Unit
			-120		-150		
			Min	Max	Min	Max	
t_{WLWL}	t_{BLC}	Byte Load Cycle (EEPROM)	0.2	150	0.2	150	µs
t_{WHRH}	t_{WC}	Write Cycle Time (EEPROM)		10		10	ms
t_{AVAV}		Address Valid to Next Address Valid	120		150		ns
t_{WLEL}	t_{WS}	Write Enable Low to Memory Block Enable Low	0		0		ns
t_{ELEH}	t_{CP}	Memory Block Enable Low to Memory Block Enable High	50		65		ns
t_{DVEH}	t_{DS}	Input Valid to Memory Block Enable High	50		65		ns
t_{EHDX}	t_{DH}	Memory Block Enable High to Input Transition	0		0		ns
t_{EHWH}	t_{WH}	Memory Block Enable High to Write Enable High	0		0		ns
t_{EHEL}	t_{CPH}	Memory Block Enable High to Memory Block Enable Low	30		35		ns
t_{AVEL}	t_{AS}	Address Valid to Memory Block Enable Low	0		0		ns
t_{ELAX}	t_{AH}	Memory Block Enable Low to Address Transition	50		65		ns
t_{GHEL}		Output Enable High to Memory Block Enable Low	0		0		ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	50		50		µs
t_{EHQV1} (1)		Memory Block Enable High to Output Valid (Program)	15		15		µs
t_{EHQV2} (1)		Memory Block Enable High to Output Valid (Sector Erase)	2.0	30	2.0	30	sec
t_{EHGL}	t_{OEH}	Memory Block Enable High to Output Enable Low	0		0		ns
t_{EHRL} (2)	t_{DB}	EEPROM Block Enable High to Ready/Busy Output Low		150		150	ns

Notes: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQ7V} + t_{Q7VQV}$.
2. With a 3.3KΩ pull-up resistor.

Figure 15. Data Polling DQ7 AC Waveforms



Notes: 1. All other timings are as a normal Read cycle.
2. DQ7 and DQ0-DQ6 can transmit to valid at any point during the data output valid period.
3. t_{WHQ7V} is the Program or Erase time.
4. During erasing operation Byte address must be within Sector being erased.
5. $\overline{E}$ is either $\overline{EF}$ when $\overline{EE} = V_{IH}$ or $\overline{EE}$ when $\overline{EF} = V_{IH}$.

Table 16. Data Polling and Toggle Bit AC Characteristics (1)
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	M39832				Unit
		-120		-150		
		Min	Max	Min	Max	
t_{WHQ7V1} (2)	Write Enable High to DQ7 Valid (Program, W Controlled)	10		10		µs
t_{WHQ7V2} (2)	Write Enable High to DQ7 Valid (Sector Erase, W Controlled)	1.5	30	1.5	30	sec
t_{EHQ7V1} (2)	Flash Block Enable High to DQ7 Valid (Program, EF Controlled)	10		10		µs
t_{EHQ7V2} (2)	Flash Block Enable High to DQ7 Valid (Sector Erase, EF Controlled)	1.5	30	1.5	30	sec
t_{Q7VQV}	Q7 Valid to Output Valid (Data Polling)		50		55	ns

Notes: 1. All other timings are defined in Read AC Characteristics table.
2. t_{WHQ7V} is the Program or Erase time.

Table 17. Program, Erase Times and Program, Erase Endurance Cycles (Flash Block)
(T_A = 0 to 70°C; V_{CC} = 2.7V to 3.6V)

Parameter	M39832				Unit
	Min	Typ	Typical after 100k W/E Cycles	Max	
Flash array Erase (Preprogrammed)		5	5		sec
Flash array Erase		12	12		sec
Flash array Block Erase		2.4			sec
Parameter Block Erase		2.3			sec
Main Block (32Kb) Erase		2.7			sec
Main Block (64Kb) Erase		3.3		15	sec
Chip Program (Byte)		8	8		sec
Byte Program		10	10		µs
Word Program		20	20		µs
Program/Erase Cycles (per Block)	100,000				cycles

Figure 16. Data Toggle DQ6 AC Waveforms

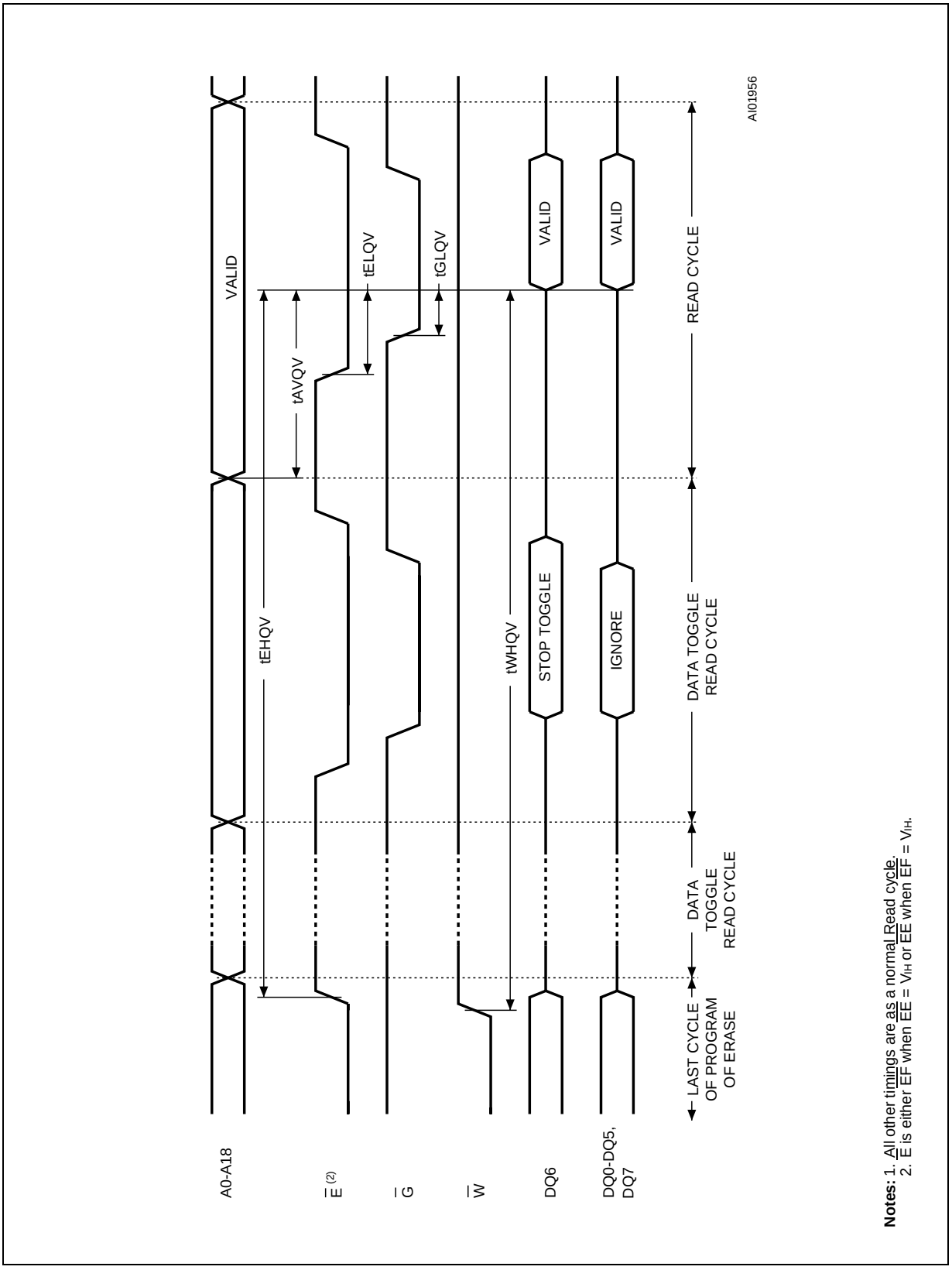
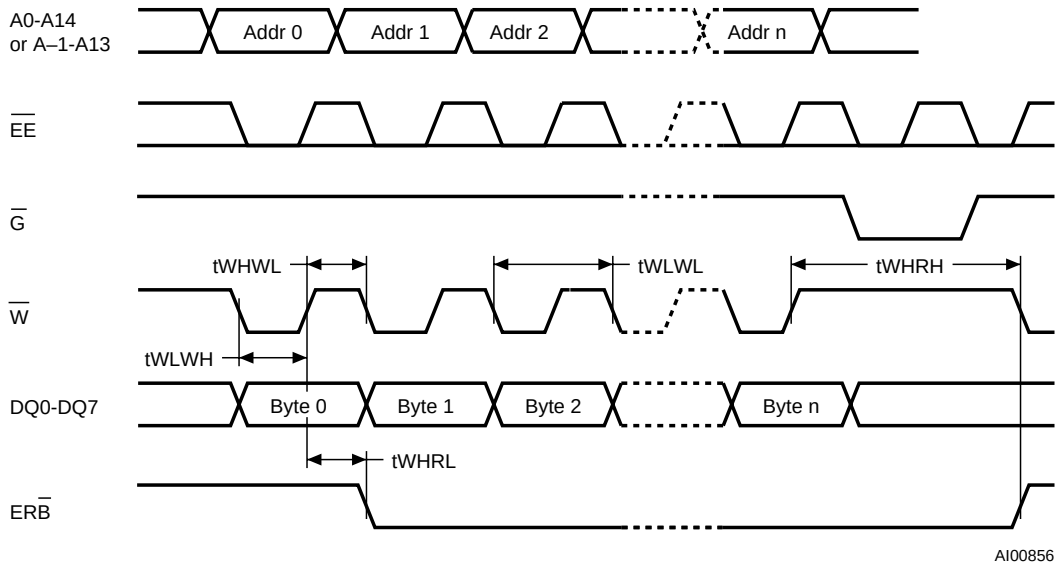
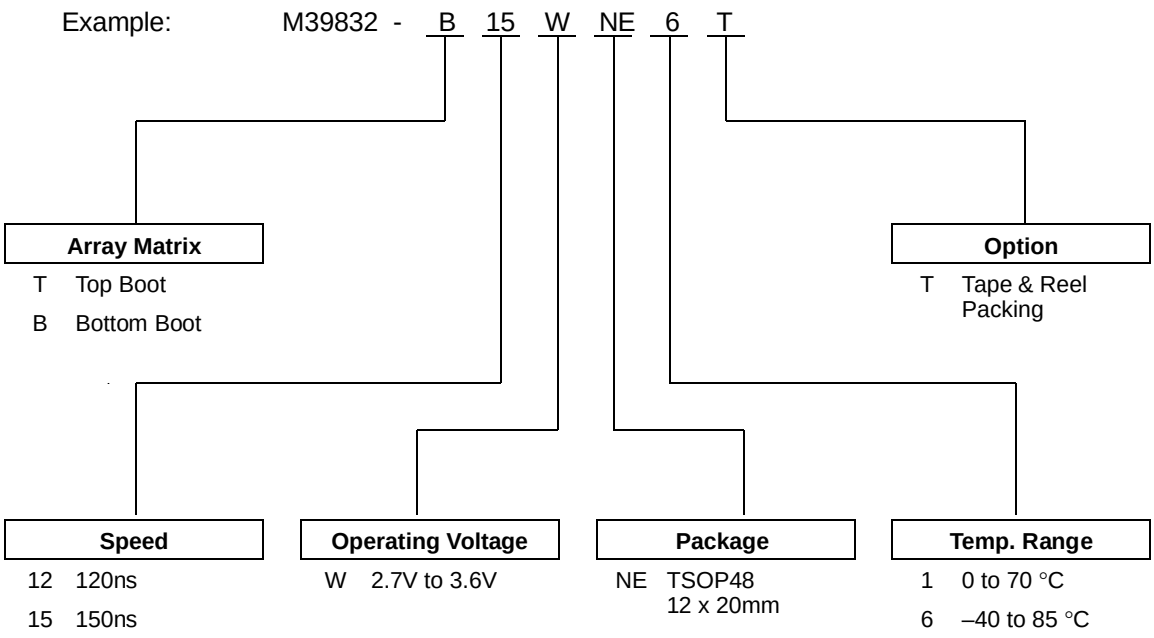


Figure 17. EEPROM Page Write Mode AC Waveforms, $\overline{W}$ Controlled



ORDERING INFORMATION SCHEME

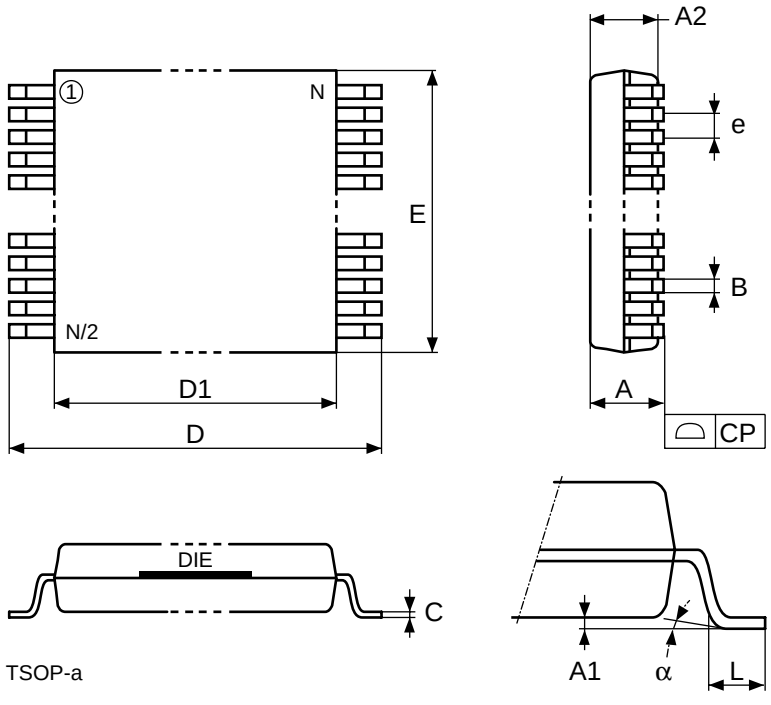


Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

TSOP48 - 48 lead Plastic Thin Small Outline, 12 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		11.90	12.10		0.469	0.476
e	0.50	-	-	0.020	-	-
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	48			48		
CP			0.10			0.004



TSOP-a

Drawing is not to scale.

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