40V 400mA Step-Down Switching Regulator with Dual Fault Protected LDOs

FEATURES

- **Triple Output Supply from a Single Input Requires Only One Inductor**
- **I_Q = 50µA at 12V_{IN} to 5V, 3.3V and 2.5V with No Load**
- **Buck Regulator:**
  - **Low Ripple (<15mV_{P-P}) Burst Mode® Operation**
  - **400mA Output with Internal Power Switch**
  - **4.3V to 40V Input Operation Range (60V Max)**
- **Dual Low Dropout Linear Regulators**
  - **200mA Outputs with Programmable Current Limits**
  - **1.6V to 45V Input Range**
  - **Fault Protected to ±45V**
- Adjustable 250kHz to 2.2MHz Switching Frequency
- Synchronizable Between 300kHz and 2.2MHz
- Programmable Undervoltage Lockout
- Power Good Indicators
- Available in a Thermally-Enhanced 16-Lead MSOP and 24-Lead (3mm × 5mm) QFN Packages

APPLICATIONS

- Automotive Battery Regulation
- Power for Portable Instrumentation
- Industrial Supplies
- Fault-Protected Sensor Supply

DESCRIPTION

The LT®3667 is a monolithic triple power supply composed of a 400mA buck switching regulator and two 200mA low dropout linear regulators (LDOs).

The buck regulator includes a high efficiency switch, a boost diode, and the necessary oscillator, control and logic circuitry. Current mode topology is used for fast transient response and good loop stability. Low ripple Burst Mode operation maintains high efficiency at low output currents while keeping output ripple below 15mV in a typical application.

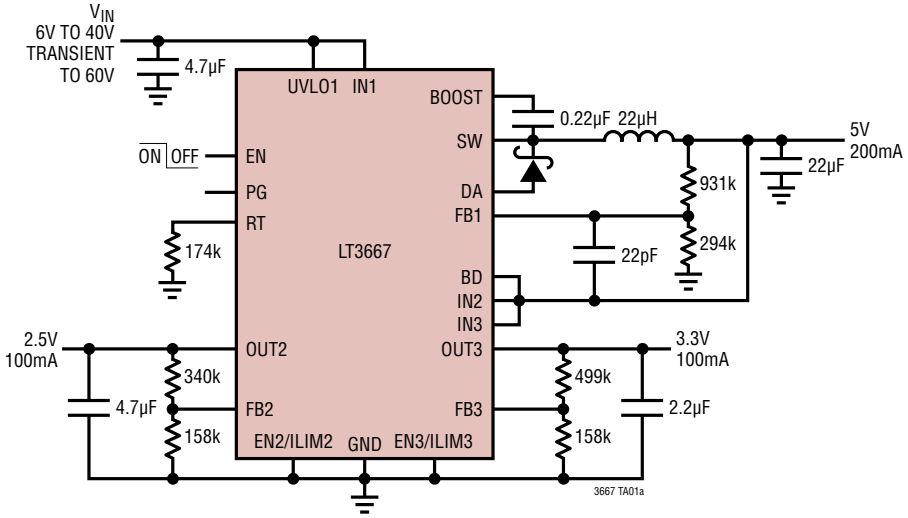
Each LDO supplies 200mA of output current with a typical dropout voltage of 340mV, and each LDO has an accurate resistor programmable current limit.

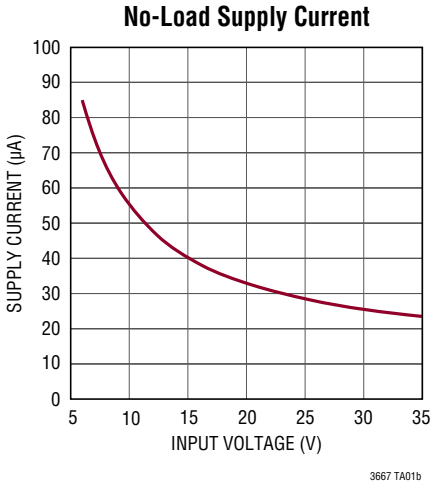
Internal protection circuitry includes reverse-battery protection, current limiting, thermal limiting and reverse current protection.

The LT3667 is available in a thermally-enhanced 16-Lead MSOP and a 24-Pin 3mm x 5mm QFN package with exposed pad for low thermal resistance.

, LT, LTC, LTM, Burst Mode, Linear Technology and the Linear logo are registered trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners.

TYPICAL APPLICATION

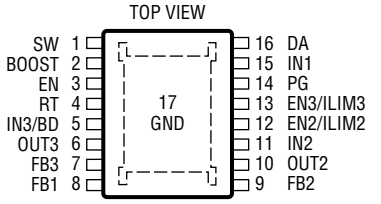




ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

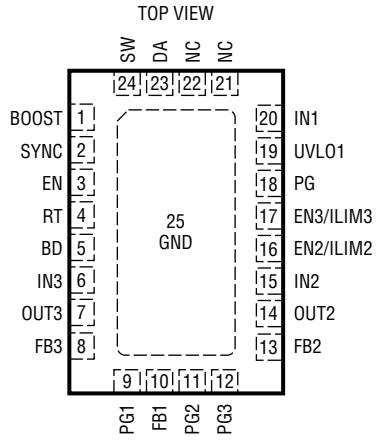
FB2, FB3 Voltage ..... ±45V
OUT2, OUT3 Voltage ..... ±45V
IN2, IN3 (QFN) Voltage ..... ±45V
OUT2 – IN2 Differential Voltage ..... ±45V
OUT3 – IN3/BD Differential Voltage (MSOP) ..... ±45V
OUT3 – IN3 Differential Voltage (QFN) ..... ±45V
IN1, EN, UVLO1 (QFN) Voltage (Note 3) 60V
IN1 Reverse Voltage ..... –0.3V
EN Pin Current ..... –1mA
IN3/BD (MSOP) Voltage 30V
BD (QFN) Voltage 30V
BOOST Pin Voltage 50V
BOOST Pin Above SW Pin 30V
RT Voltage 2V
FB1 Voltage 6V
EN2/ILIM2, EN3/ILIM3 Voltage 4V
PG Voltage 30V
PG1, PG2, PG3 Voltage (QFN) 30V
SYNC Voltage (QFN) 6V
Operating Junction Temperature Range (Notes 4, 5)
E-, I-Grades ..... –40°C to 125°C
H-Grades ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MSOP Package Only ..... 300°C

PIN CONFIGURATION



MSE PACKAGE
16-LEAD PLASTIC MSOP

θ_{JA} = 40°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB



UDD PACKAGE
24-LEAD (3mm × 5mm) PLASTIC QFN

θ_{JA} = 46°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3667EMSE#PBF	LT3667EMSE#TRPBF	3667	16-Lead Plastic MSOP	–40°C to 125°C
LT3667IMSE#PBF	LT3667IMSE#TRPBF	3667	16-Lead Plastic MSOP	–40°C to 125°C
LT3667HMSE#PBF	LT3667HMSE#TRPBF	3667	16-Lead Plastic MSOP	–40°C to 150°C
LT3667EUDD#PBF	LT3667EUDD#TRPBF	LGFH	24-Lead (3mm × 5mm) Plastic QFN	–40°C to 125°C
LT3667IUDD#PBF	LT3667IUDD#TRPBF	LGFH	24-Lead (3mm × 5mm) Plastic QFN	–40°C to 125°C
LT3667HUDD#PBF	LT3667HUDD#TRPBF	LGFH	24-Lead (3mm × 5mm) Plastic QFN	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN1} = 12V unless otherwise noted. (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN1} Undervoltage Lockout (Note 6)	V_{IN2} = 0V, V_{IN3} = 0V	●		4	4.3	V
V_{IN1} Overvoltage Lockout		●	40	42	44	V
V_{IN2} Undervoltage Lockout (Note 6)	V_{IN1} = 3.5V, V_{IN3} = 0V	●		4	4.3	V
UVLO1 Threshold Voltage	Pin Voltage Falling	●	0.95	1	1.05	V
UVLO1 Pin Hysteresis				75		mV
UVLO1 Pin Current	V_{UVLO1} = 1V			1	30	nA
Quiescent Current from IN1	V_{EN} = 0.3V V_{EN} = 12V, V_{IN2} = 0V, Not Switching	 ●		0.01 13	1 30	µA µA
Quiescent Current from IN2	V_{EN} = 0.3V V_{EN} = 12V, V_{IN1} = 0V, V_{IN2} = 5V	 ●		0.01 38	1 80	µA µA
Quiescent Current from IN1 + IN2	V_{EN} = 0.3V, V_{IN2} = 5V V_{EN} = 12V, V_{IN2} = 5V, Not Switching	 ●		0.01 40	1 90	µA µA
Quiescent Current from IN3	V_{EN} = 0.3V, V_{IN3} = 5V V_{EN} = 12V, V_{IN3} = 5V	 ●		0.01 25	1 60	µA µA
EN Pin Current	V_{EN} = 12V			0.6	2	µA
EN Input Threshold			0.3		1.1	V
Power Good Pins PG (MSOP), PG1, PG2, PG3 (QFN)						
Leakage Current	V_{PG} = 5V, $V_{PG1/2/3}$ = 5V			0.1	1	µA
Output Voltage Low	I_{PG} = 40µA, $I_{PG1/2/3}$ = 40µA	●		0.2	0.3	V
Threshold as % of V_{FB} (FB1, FB2, FB3)	Pin Voltage Falling Pin Voltage Rising		88 108	90 110	92 112	% %
PG1 Threshold Hysteresis	Measured at FB1 Pin			30		mV
PG2/PG3 Threshold Hysteresis	Measured at FB2/FB3 Pin			20		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN1} = 12V unless otherwise noted. (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Regulator						
Switching Frequency	R_T = 37.4k R_T = 102k R_T = 487k	● ● ●	1.8 0.8 220	2.0 0.94 243	2.1 1.1 275	MHz MHz kHz
Minimum Switch Off-Time		●		120	170	ns
Switch Current Limit (Note 7)	5% Duty Cycle, V_{IN} = 5V, V_{FB1} = 0V 90% Duty Cycle, V_{IN} = 5V, V_{FB1} = 0V	● ●	600 450	750 550	950 750	mA mA
Switch V_{CESAT}	I_{SW} = 200mA			300		mV
DA Pin Current to Stop Switching		●	420	500	650	mA
Switch Leakage Current	V_{SW} = 0V			0.05	2	µA
Boost Schottky Diode Forward Voltage	$I_{BOOSTDIODE}$ = 50mA, V_{IN} = NC, V_{BOOST} = 0V			900		mV
Boost Schottky Diode Reverse Leakage	$V_{REVERSE}$ = 12V, V_{IN} = NC			0.04	4	µA
Minimum Boost Voltage (Note 8)		●		1.7	2.5	V
BOOST Pin Current	I_{SW} = 200mA, V_{BOOST} = 15V			10	16	mA
Feedback Voltage (FB1)		 ●	1.188 1.176	1.2 1.2	1.212 1.224	V mV
FB1 Pin Bias Current	Pin Voltage = 1.2V	●		0.1	20	nA
Reference Voltage Line Regulation	4.2V < V_{IN1} < 40V			0.001	0.005	%/V
SYNC High Level Input Voltage SYNC Low Level Input Voltage		● ●	1.2		 0.5	V V
SYNC Input Frequency			0.3		2.2	MHz
Each LDO Regulator						
Minimum Input Voltage	I_{LOAD} = 200mA	●		1.6	2.2	V
Feedback Voltage (FB2/FB3)	V_{IN} = 2.2V, I_{LOAD} = 1mA 2.2V < V_{IN} < 15V, 1mA < I_{LOAD} < 200mA	 ●	792 784	800	808 816	mV mV
Load Regulation (Note 12)	V_{IN} = 2.2V, I_{LOAD} = 1mA to 200mA	●		0.2	5	mV
Reference Voltage Line Regulation (Note 12)	2.2V < $V_{IN2,3}$ < 45V			0.005	0.01	%/V
Dropout Voltage (Notes 9, 10), V_{IN} = $V_{OUT(NOMINAL)}$	I_{LOAD} = 1mA I_{LOAD} = 1mA	 ●		70	165 210	mV mV
	I_{LOAD} = 50mA I_{LOAD} = 50mA	 ●		230	300 400	mV mV
	I_{LOAD} = 100mA I_{LOAD} = 100mA	 ●		280	400 450	mV mV
	I_{LOAD} = 200mA I_{LOAD} = 200mA	 ●		340	650 750	mV mV
GND Pin Current, V_{IN} = $V_{OUT(NOMINAL)}$ + 0.6V (Notes 10, 11)	I_{LOAD} = 0mA I_{LOAD} = 50mA I_{LOAD} = 200mA	● ● ●		40 1 5	90 2 10	µA mA mA
Quiescent Current I_{IN2} with LDO2 Disabled Quiescent Current I_{IN3} with LDO3 Disabled (QFN) Quiescent Current $I_{IN3/BD}$ with LDO3 Disabled (MSOP)	V_{IN1} = 0V, V_{IN2} = 12V, $V_{EN2/ILIM2}$ = 2V V_{IN1} = 16V, V_{IN3} = 12V, $V_{EN3/ILIM3}$ = 2V V_{IN1} = 16V, $V_{IN3/BD}$ = 12V, $V_{EN3/ILIM3}$ = 2V			13 0.2 1.2	20 1 2	µA µA µA
FB2 Pin Bias Current (Note 12) FB3 Pin Bias Current (Note 12)	V_{IN2} = 12V V_{IN3} = 12V	● ●		–3 –3	±40 ±40	nA nA
Ripple Rejection (Note 12)	V_{IN} – V_{OUT} = 2V (Avg), V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} =200mA		60	85		dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN1} = 12V unless otherwise noted. (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reverse Output Current (Note 13)	V_{OUT2} = 1.2V, V_{IN1} = V_{IN2} = V_{IN3} = 0V V_{OUT3} = 1.2V, V_{IN1} = V_{IN2} = V_{IN3} = 0V			5 5	40 40	µA µA
Input Reverse Leakage Current LDO2 Input Reverse Leakage Current LDO3 (QFN)	V_{IN2} = –45V, V_{IN1} = V_{IN3} = V_{OUT2} = 0V V_{IN3} = –45V, V_{IN1} = V_{IN2} = V_{OUT3} = 0V	● ●			300 300	µA µA
Internal Current Limit (Note 12)	V_{IN2} = 2.2V, V_{OUT2} = 0V, EN2/ILIM2 Pin Grounded			300		mA
	ΔV_{OUT2} = –5%	●	220			mA
	V_{IN3} = 2.2V, V_{OUT3} = 0V, EN3/ILIM3 Pin Grounded			300		mA
	ΔV_{OUT3} = –5%	●	220			mA
Externally Programmed Current Limit	$R_{EN/ILIM}$ = 31.6k, $V_{OUT2/3}$ = 5V, $V_{IN2/3} \geq$ 5.6V $R_{EN/ILIM}$ = 6.19k, $V_{OUT2/3}$ = 5V, $V_{IN2/3} \geq$ 5.6V $R_{EN/ILIM}$ = 6.19k, $V_{OUT2/3}$ = 5V, 5.6V ≤ $V_{IN2/3}$ ≤ 15V $R_{EN/ILIM}$ = 1.54k, $V_{OUT2/3}$ = 5V, 5.6V ≤ $V_{IN2/3}$ ≤ 15V	● ● ● ●	9.5 47 48.45 176	10 51 51 197	10.5 55 53.55 230	mA mA mA mA
LDO Disable Threshold	$V_{EN/ILIM}$ Rising		0.9	1	1.2	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Positive currents flow into pins, negative currents flow out of pins. Minimum and maximum values refer to absolute values.

Note 3: Absolute maximum voltage at the IN1, UVLO1 and EN pins is 60V for nonrepetitive 1 second transients, and 40V for continuous operation.

Note 4: The LT3667E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3667I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3667H is guaranteed over the full –40°C to 150°C operating junction temperature range.

Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 6: This is the voltage necessary to keep the internal bias circuitry in regulation.

Note 7: Current limit guaranteed by design and/or correlation to static test. Slope compensation reduces current limit at higher duty cycles.

Note 8: This is the minimum voltage across the boost capacitor needed to guarantee full saturation of the switch.

Note 9: Dropout voltage is the minimum input-to-output voltage differential needed for an LDO to maintain regulation at a specified output current. When an LDO is in dropout, its output voltage will be equal to $V_{IN} – V_{DROP}$.

Note 10: To satisfy minimum input voltage requirements, the LT3667 is tested and specified for these conditions with an external resistor divider (80.6k bottom, 422k top) which sets V_{OUT} to 5V. The external resistor divider adds 9.93µA of DC load on the output. This external current is not factored into GND pin current.

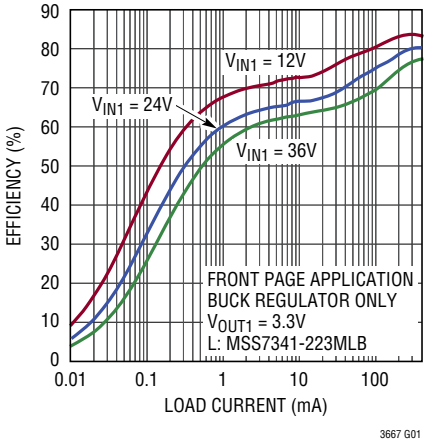
Note 11: GND pin current is tested with $V_{IN} = V_{OUT(NOMINAL)}$ + 0.6V and a current source load. GND pin current increases in dropout.

Note 12: The LT3667 is tested and specified for these conditions with FB2 (FB3) pin connected to the OUT2 (OUT3) pin.

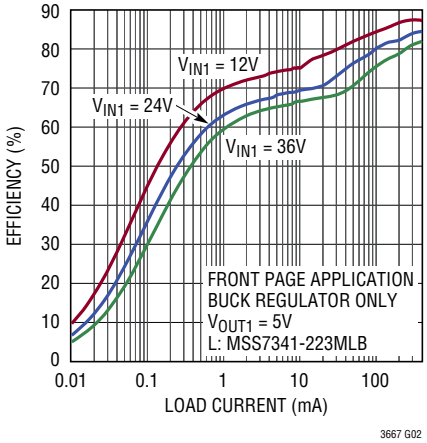
Note 13: Reverse output current is tested with the IN2 (IN3) pin grounded and the OUT2 (OUT3) pin forced to the rated output voltage. This current flows into the OUT2 (OUT3) pin and out of the GND pin.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

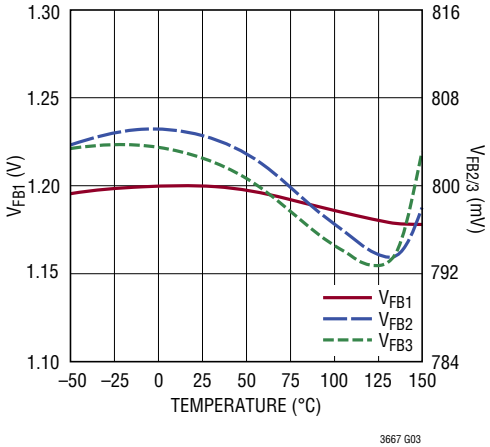
Efficiency, V_{OUT} = 3.3V



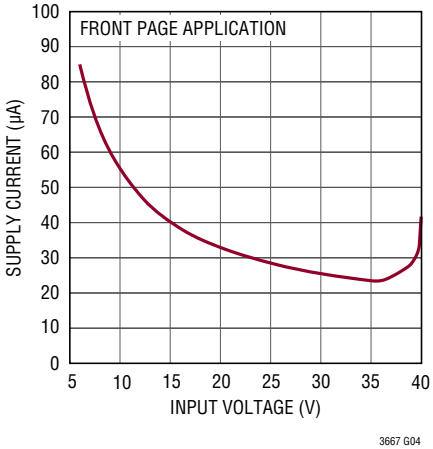
Efficiency, V_{OUT} = 5V



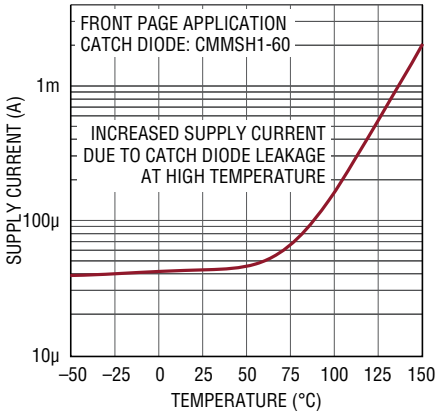
$V_{FB1/2/3}$ vs Temperature



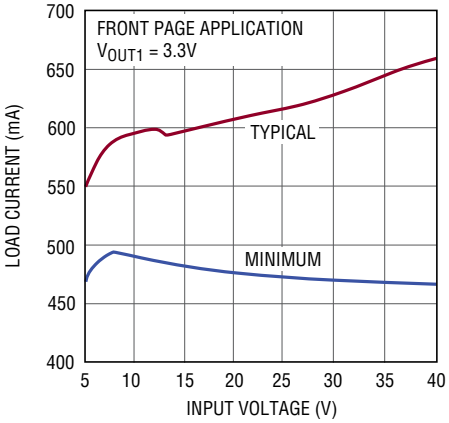
No-Load Supply Current



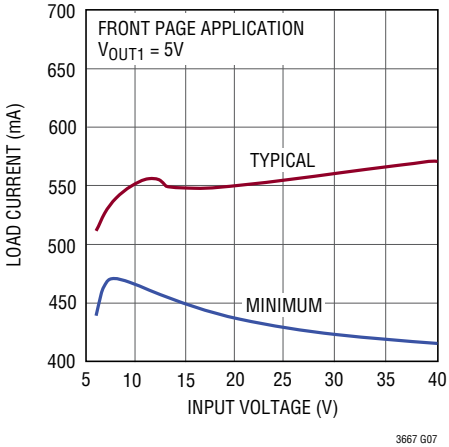
No-Load Supply Current



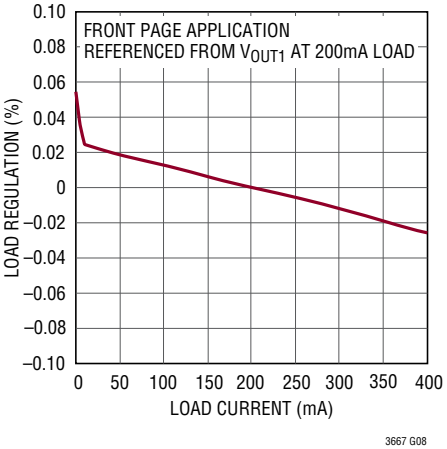
Maximum Load Current



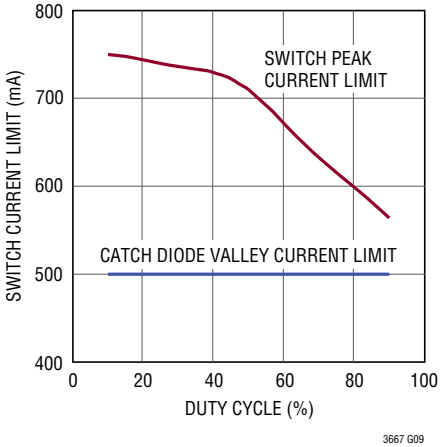
Maximum Load Current



Switching Regulator Load Regulation

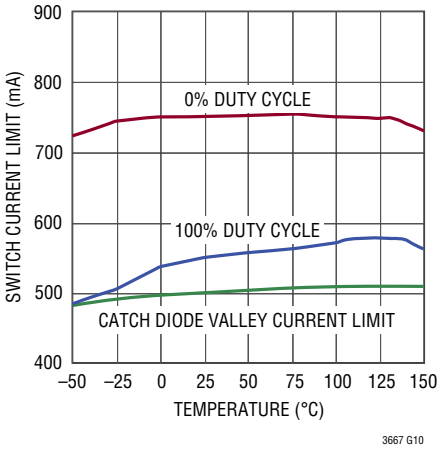


Switch Current Limit

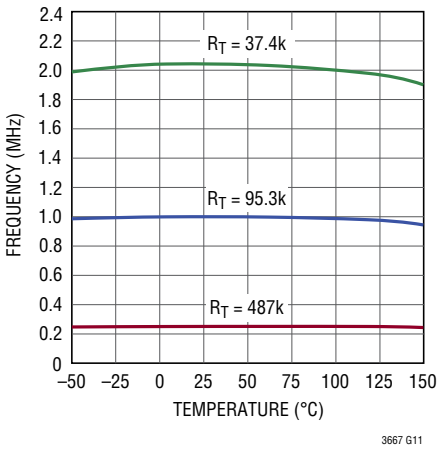


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

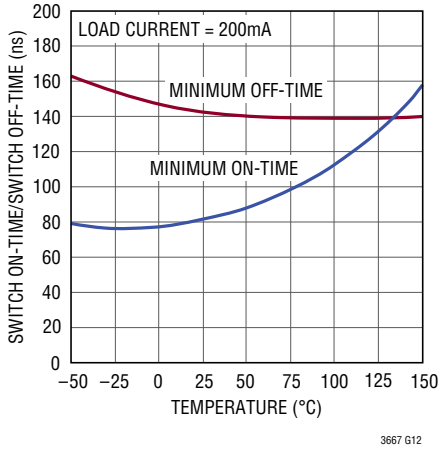
Switch Current Limit



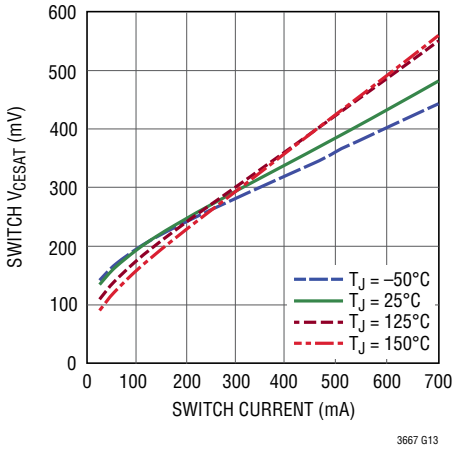
Switching Frequency



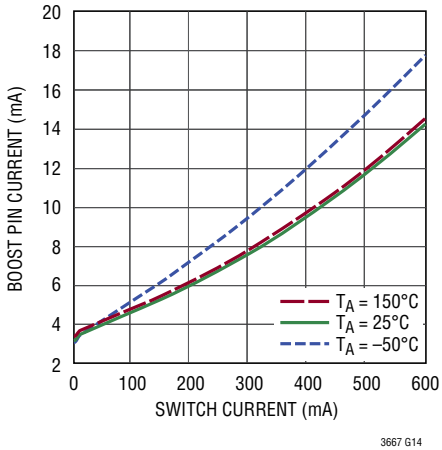
Minimum Switch On-Time/ Switch-Off Time



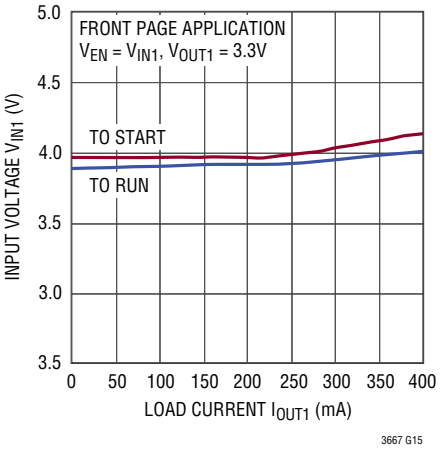
Switch V_{CESAT}



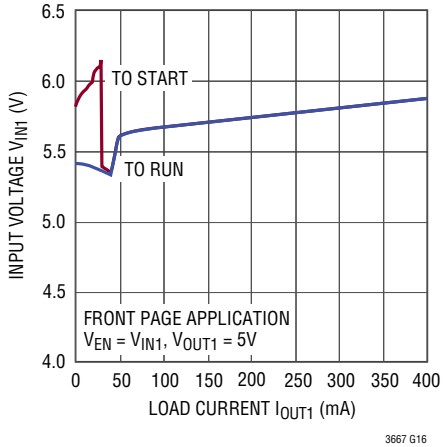
BOOST Pin Current



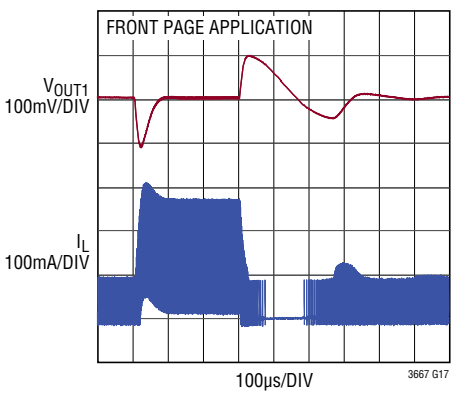
Minimum Input Voltage, V_{OUT} = 3.3V



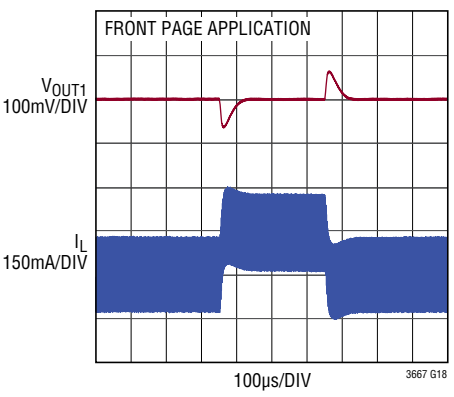
Minimum Input Voltage, V_{OUT} = 5V



Transient Load Response, Load Step 10mA to 140mA

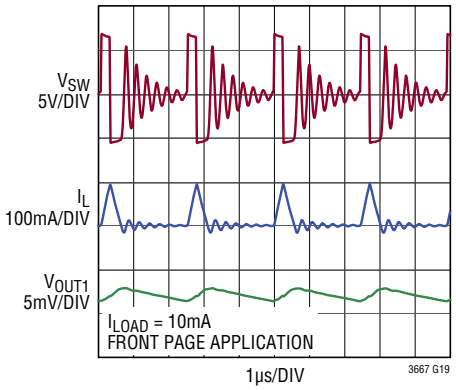


Transient Load Response Load Step 150mA to 300mA

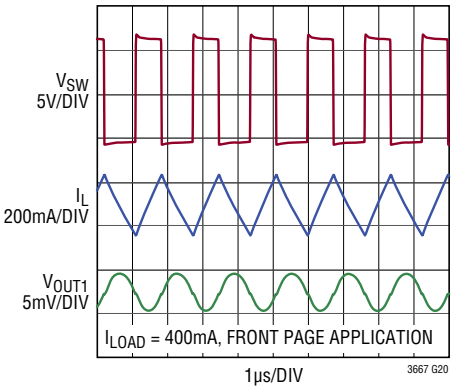


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

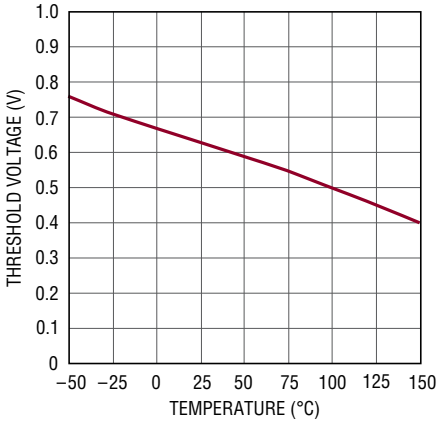
Switching Waveforms, Burst Mode Operation



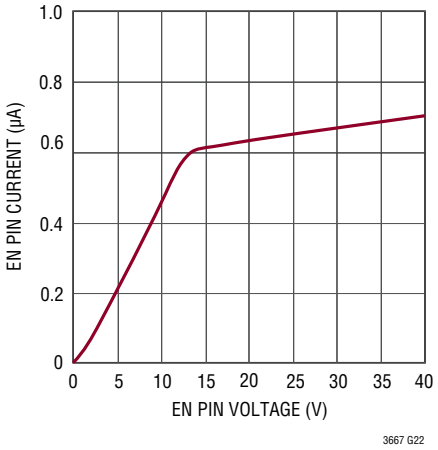
Switching Waveforms, Full Frequency Continuous Operation



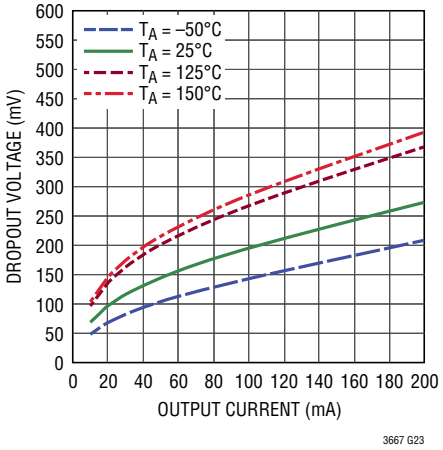
EN Threshold



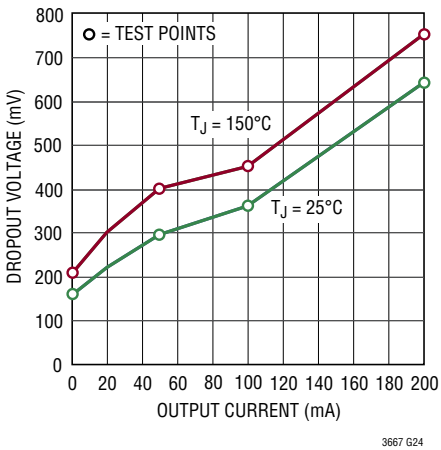
EN Pin Current



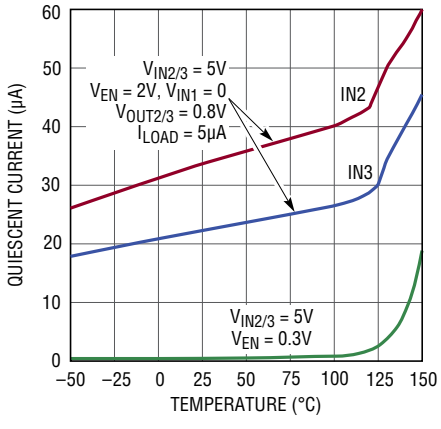
LDOs: Typical Dropout Voltage



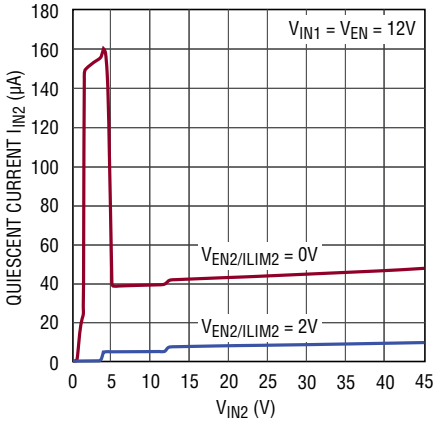
LDOs: Guaranteed Dropout Voltage



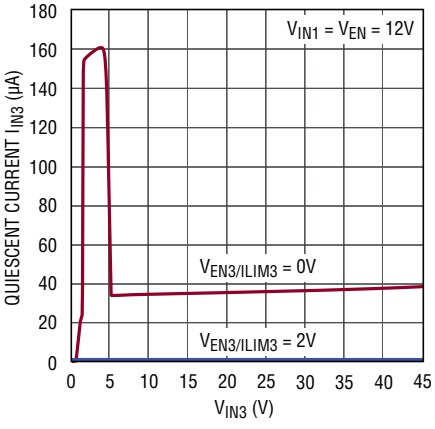
LDOs: IN2, IN3 Quiescent Current



LDOs: 5V Quiescent Current IN2

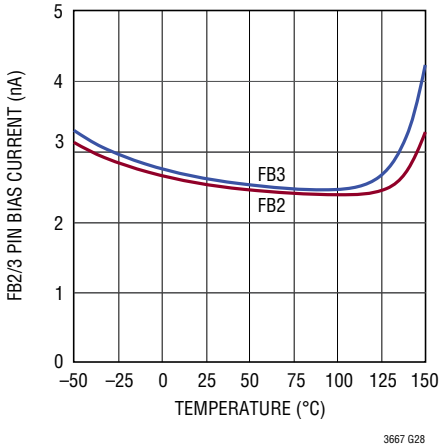


LDOs: 5V Quiescent Current IN3

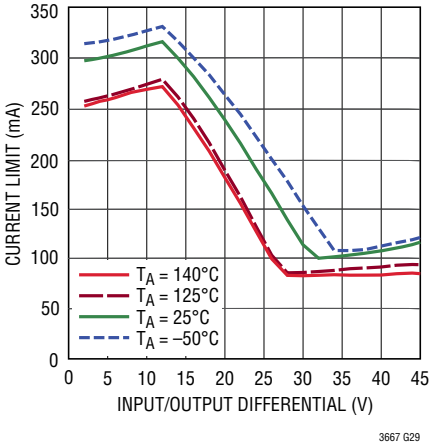


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

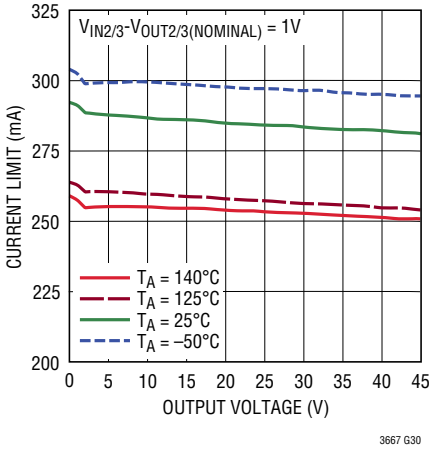
FB2, FB3 Pin Bias Current



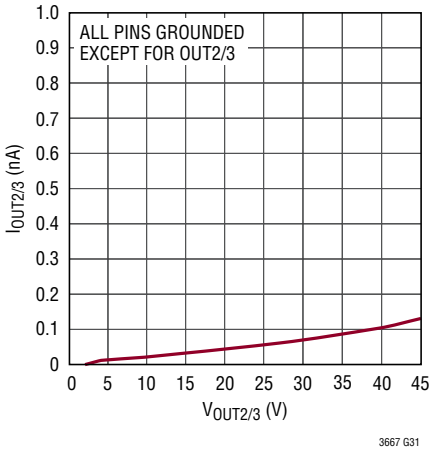
LDOs: Internal Current Limit



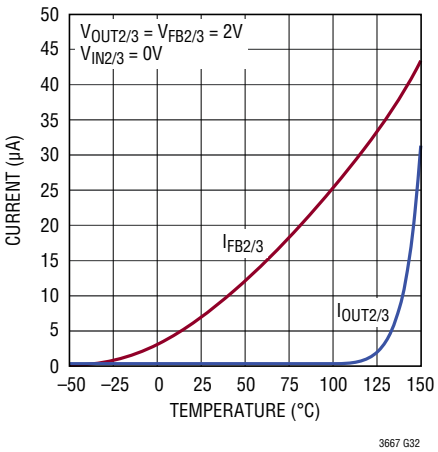
LDOs: Internal Current Limit



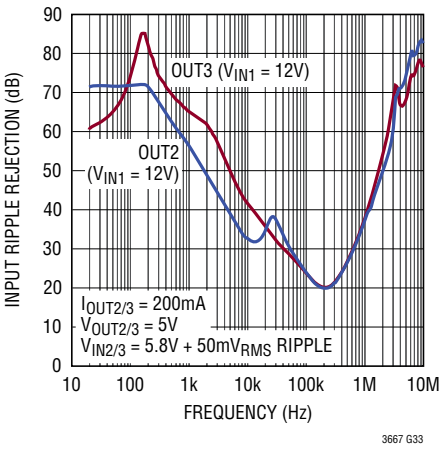
LDOs: Reverse Output Current



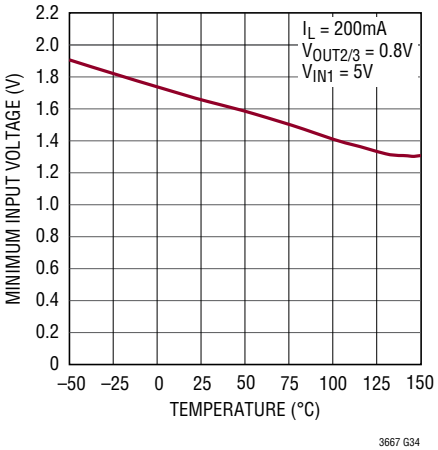
LDOs: Reverse Output Current



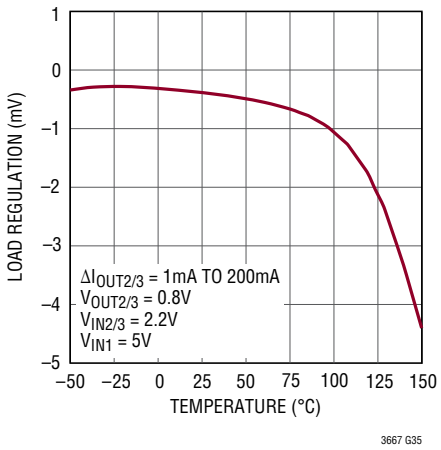
LDOs: Input Ripple Rejection



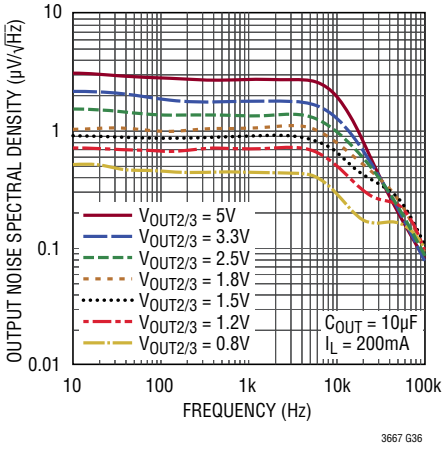
LDOs: Minimum Input Voltage



LDOs: Load Regulation

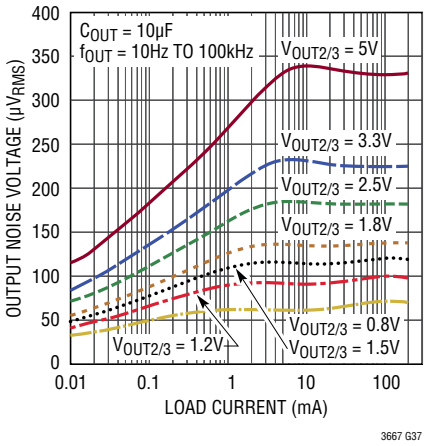


LDOs: Output Noise Spectral Density

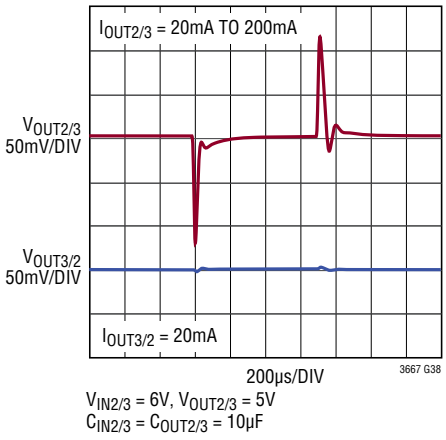


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

LDOs: RMS Output Noise

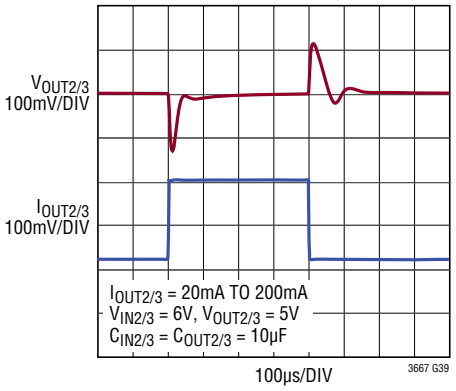


LDOs: Channel-to-Channel Isolation

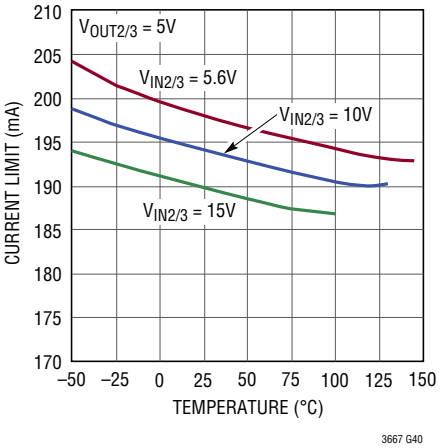


$V_{IN2/3}$ = 6V, $V_{OUT2/3}$ = 5V
$C_{IN2/3}$ = $C_{OUT2/3}$ = 10µF

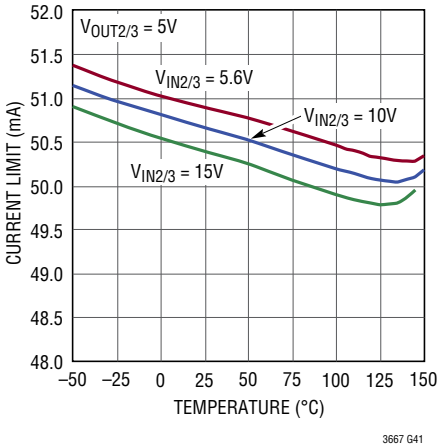
LDOs: Transient Response



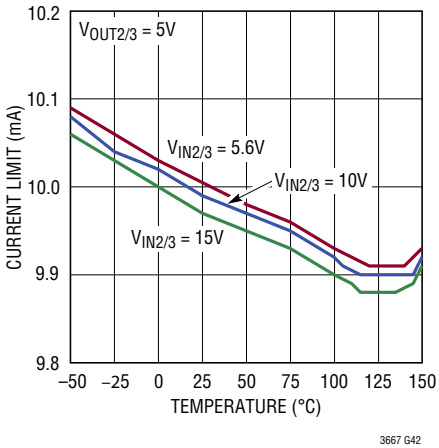
LDOs: External Current Limit, $R_{EN/ILIM}$ = 1.54k



LDOs: External Current Limit, $R_{EN/ILIM}$ = 6.19k



LDOs: External Current Limit, $R_{EN/ILIM}$ = 31.6k



PIN FUNCTIONS (MSOP/QFN)

SW (Pin 1/Pin 24): The SW pin is the output of the internal power switch. Connect this pin to the inductor, the catch diode and the boost capacitor.

BOOST (Pin 2/Pin 1): This pin is used to provide a drive voltage, higher than the input voltage, to the internal bipolar NPN power switch of the switching regulator. Connect a capacitor (typically 0.22µF) between BOOST and SW.

SYNC (Pin 2, QFN Only): This is the external clock synchronization input. Ground this pin for low ripple Burst Mode operation at low output loads. Tie to a clock source for synchronization. Refer to Synchronization section in Applications Information for more details.

EN (Pin 3/Pin 3): The EN pin is used to put the LT3667 in shutdown mode. Tie to ground to shut down the LT3667. Tie to 1V or more for normal operation. If the EN pin is to be pulled below ground, use a series resistor to limit the pin current to 1mA.

RT (Pin 4/Pin 4): Oscillator Resistor Input. Connect a resistor from this pin to ground to set the switching frequency.

BD (Pin 5, QFN Only): This pin connects to the anode of the internal boost diode. This pin also supplies current to the LT3667's internal regulator when BD is above 3.2V.

OUT3 (Pin 6/Pin 7), OUT2 (Pin 10/Pin 14): These are the outputs of the two LDOs. Stability requirements demand a minimum 2.2µF ceramic output capacitor to prevent oscillations.

FB3 (Pin 7/Pin 8), FB2 (Pin 9/Pin 13): The two LDOs of the LT3667 regulate the FB2 and FB3 pins to 0.8V. Connect the feedback resistor divider taps to these pins.

FB1 (Pin 8/Pin 10): The switching regulator of the LT3667 regulates the FB1 pin to 1.2V. Connect the feedback resistor divider tap to this pin.

PG1 (Pin 9, QFN Only): The PG1 pin is the open-drain output of an internal window comparator. PG1 remains low until the FB1 pin is within ±10% of its final regulation voltage. PG1 output is valid when V_{IN1} or V_{IN2} are above the minimum input voltage and EN is high.

IN2 (Pin 11/Pin 15), IN3/BD (Pin 5, MSOP), IN3 (Pin 6, QFN): These pins are the inputs of the two LDOs. IN3/BD also connects to the anode of the internal boost diode and also supplies current to the LT3667's internal regulator when IN3/BD is above 3.2V.

PG2 (Pin 11, QFN Only): The PG2 pin is the open-drain output of an internal window comparator. PG2 remains low until the FB2 pin is within ±10% of its final regulation voltage. PG2 output is valid when V_{IN1} or V_{IN2} are above the minimum input voltage and EN is high.

EN2/ILIM2 (Pin 12/Pin 16), EN3/ILIM3 (Pin 13/Pin 17): Precision current limit programming pins. They connect to collectors of current mirror PNPs which are 1/799th the size of the output power PNPs of the two LDOs. These pins are also the inputs to the current limit amplifiers. Current limit thresholds are set by connecting resistors between the EN2/ILIM2 pin and GND and between the EN3/ILIM3 pin and GND. Stability requirements demand 47nF capacitors in parallel to these resistors. For detailed information on how to set the pin resistor values, see the Operation section. If any of these pins is not used, tie it to GND. To disable an LDO, pull its EN/ILIM pin above 1.2V.

PG3 (Pin 12, QFN Only): The PG3 pin is the open-drain output of an internal window comparator. PG3 remains low until the FB3 pin is within ±10% of its final regulation voltage. PG3 output is valid when V_{IN1} or V_{IN2} are above the minimum input voltage and EN is high.

PG (Pin 14/Pin 18): The PG pin is the open-drain output of an internal window comparator. PG remains low until the FB1, FB2, and FB3 pin are within ±10% of their final regulation voltages. PG output is valid when V_{IN1} or V_{IN2} are above the minimum input voltage and EN is high.

PIN FUNCTIONS (MSOP/QFN)

IN1 (Pin 15/Pin 20): The IN1 pin supplies current to the internal regulator and to the internal power switch. This pin must be locally bypassed.

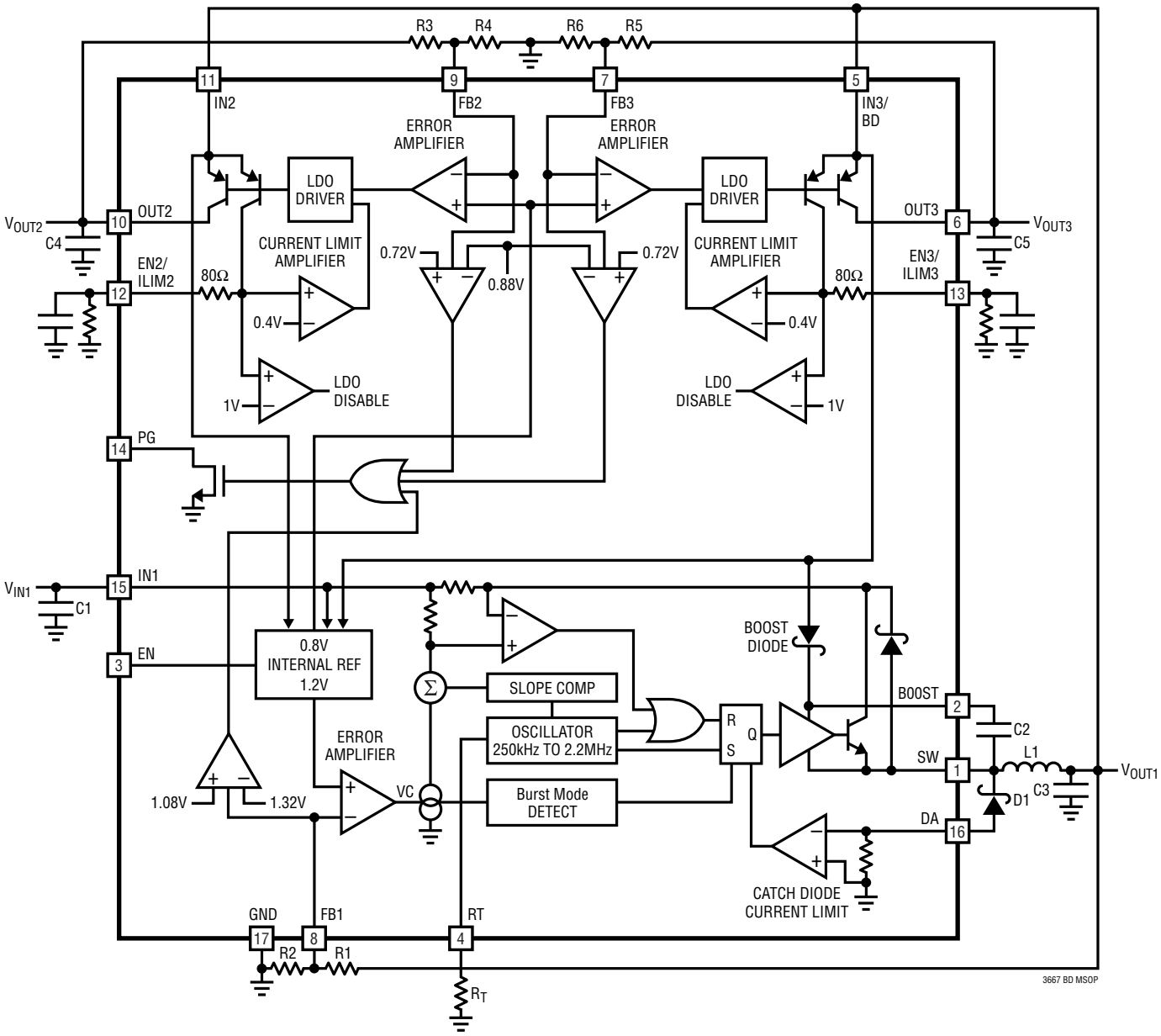
DA (Pin 16/Pin 23): Connect the anode of the catch diode (D1 in Block Diagrams) to this pin. Internal circuitry senses the current through the catch diode providing frequency foldback in overload conditions.

GND (Exposed Pad Pin 17/Exposed Pad Pin 25): This is the ground of all internal circuitry, as well as the power ground used by the catch diode (D1). The exposed pad must be soldered to the PCB.

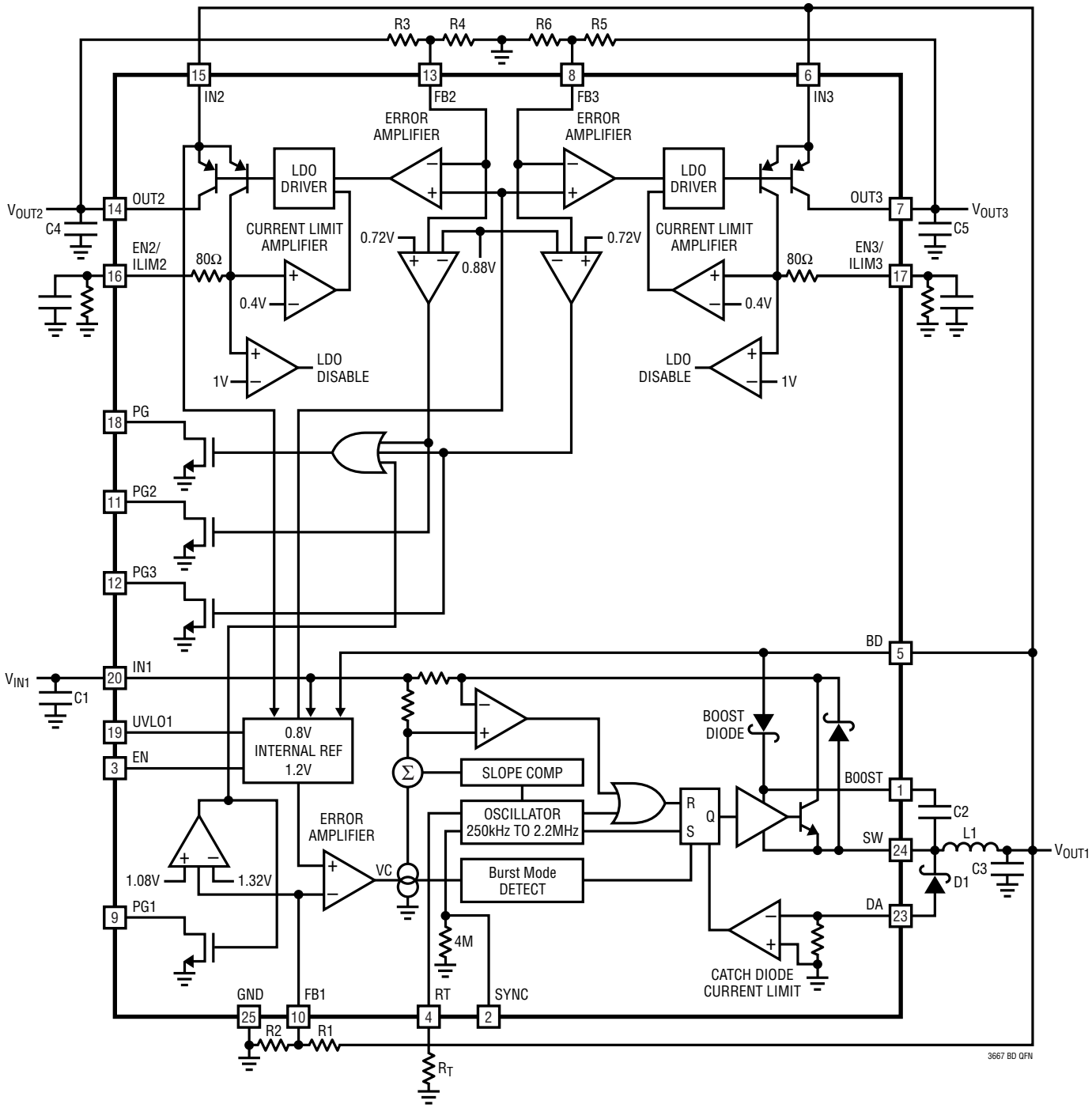
UVLO1 (Pin 19, QFN Only): The precise 1V threshold voltage of this pin can function as an accurate undervoltage lockout (UVLO). The switching regulator only operates when the voltage at the UVLO1 pin exceeds this threshold. The LDOs are not affected by this pin.

NC (Pins 21, 22, QFN only): These pins are not connected internally and can be left floating or tied to ground.

BLOCK DIAGRAM (MSOP)



BLOCK DIAGRAM (QFN)



OPERATION

The LT3667 combines a 400mA buck switching regulator and two 200mA low dropout linear regulators. Operation is best understood by referring to the Block Diagrams.

The buck regulator part is a constant frequency, current mode step-down regulator. An oscillator, with frequency set by R_T, sets an RS flip-flop, turning on the internal power switch. An amplifier and comparator monitor the current flowing between the IN1 and SW pins, turning the switch off when this current reaches a level determined by the voltage at VC. An error amplifier measures the output voltage through an external resistor divider tied to the FB1 pin and servos the VC node. If the error amplifier's output increases, more current is delivered to the output; if it decreases, less current is delivered.

Another comparator monitors the current flowing through the catch diode and reduces the operating frequency when the current exceeds the 500mA bottom current limit. This foldback in frequency helps to control the output current in fault conditions such as a shorted output with high input voltage. Maximum deliverable current to the output is therefore limited by both switch current limit and catch diode current limit.

An internal regulator provides power to the control circuitry. The bias regulator normally draws power from the IN1 pin, but if the IN3/BD (MSOP) or BD (QFN) pin is connected to an external voltage higher than 3.2V, bias power will be drawn from the external source (typically the regulated output voltage). This improves efficiency.

The switch driver operates from either IN1 or from the BOOST pin. An external capacitor is used to generate a voltage at the BOOST pin that is higher than the input supply. This allows the driver to fully saturate the internal NPN power switch for efficient operation.

To further optimize efficiency, the LT3667 automatically switches to Burst Mode operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the input supply current to 50µA (including the current drawn by the LDOs).

The switching regulator has an overvoltage protection feature which disables switching action when IN1 goes above 42V (typical) during transients. It can then safely sustain transient input voltages up to 60V.

The switching regulator can also be separately shut down via the UVLO1 pin, which can be used to implement a programmable undervoltage lockout with an external resistive divider.

The LDO blocks are micropower, low noise 200mA linear regulators with low dropout voltage and current limit, which provide fast transient response with minimum low ESR 2.2µF ceramic output capacitors. Each output current limit can be programmed individually with a single resistor, and pulling the EN2/ILIM2 or EN3/ILIM3 pin high shuts down the corresponding LDO. Internal protection circuitry includes reverse-battery protection, reverse-output protection, reverse-current protection, and current limit with foldback.

The internal reference voltage circuitry is supplied by the IN1 and IN2 pins. This allows the LDO at IN2 to run independently and supply the switching regulator with its output OUT2.

The EN pin is used to place the LT3667 in shutdown, thereby reducing the input current to less than 1µA.

The LT3667 contains three power good window comparators that indicate whether the output voltages are within ±10% of their nominal value. The outputs of these comparators are open-drain transistors which are off when their corresponding output is in regulation, allowing external resistors to pull the power good pins high. The PG pin provides a combined power good signal, while the QFN package additionally allows access to the individual power good signals through pins PG1, PG2 and PG3. Power good is valid if the LT3667 is enabled and IN1 or IN2 are above their minimum input voltages.

Internal thermal limiting protects the LT3667 during overload conditions.

APPLICATIONS INFORMATION

SWITCHING REGULATOR

FB1 Resistor Network

The switching regulator output voltage of the LT3667 is programmed with a resistor divider between the output of the switching regulator and the FB1 pin. Choose the resistor values according to:

$$R1 = R2\left(\frac{V_{OUT1}}{1.2V} - 1\right)$$

Reference designators refer to the Block Diagram of the LT3667. 1% resistors are recommended to maintain output voltage accuracy. Note that choosing larger resistors will decrease the quiescent current of the application circuit.

Setting the Switching Frequency

The LT3667 regulator uses a constant frequency PWM architecture that can be programmed to switch from 250kHz to 2.2MHz by using a resistor tied from the RT pin to ground. Table 1 shows the necessary R_T value for a desired switching frequency.

Table 1: Switching Frequency vs R_T Value

SWITCHING FREQUENCY (MHz)	R_T VALUE (kΩ)
0.25	475
0.3	383
0.4	274
0.5	215
0.6	174
0.8	124
1	95.3
1.2	75
1.4	61.9
1.6	51.1
1.8	43.2
2	37.4
2.2	32.4

Operating Frequency Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, minimum dropout voltage, and maximum input voltage. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency, lower maximum input voltage, and higher dropout voltage. The highest acceptable switching frequency ($f_{SW(MAX)}$) for a given application can be calculated as follows:

$$f_{SW(MAX)} = \frac{V_{OUT1} + V_D}{t_{ON(MIN)}\left(V_{IN1} - V_{SW} + V_D\right)}$$

where V_{IN1} is the typical input voltage, V_{OUT1} is the output voltage, V_D is the catch diode drop (~0.5V) and V_{SW} is the internal switch drop (~0.5V at max load). This equation shows that slower switching frequency is necessary to accommodate high V_{IN1}/V_{OUT1} ratio.

Lower frequency also allows a lower dropout voltage. Input voltage range depends on the switching frequency because the LT3667 switch has finite minimum on and off times. The switch can turn on for a minimum of ~150ns and turn off for a minimum of ~170ns (note that the minimum on-time is a strong function of temperature). The minimum and maximum duty cycles that can be achieved taking minimum on and off times into account are:

$$DC_{MIN} = f_{SW} \bullet t_{ON(MIN)}$$

$$DC_{MAX} = 1 - f_{SW} \bullet t_{OFF(MIN)}$$

where f_{SW} is the switching frequency, $t_{ON(MIN)}$ is the minimum switch on-time (~150ns), and $t_{OFF(MIN)}$ is the minimum switch off-time (~170ns). These equations show that the duty cycle range increases when the switching frequency is decreased.

A good choice of switching frequency should allow an adequate input voltage range (see Input Voltage Range section) and keep the inductor and capacitor values small.

APPLICATIONS INFORMATION

Input Voltage Range

The minimum input voltage is determined by either the LT3667's minimum operating voltage of 4.3V or by its maximum duty cycle (as discussed in the previous section). The minimum input voltage due to duty cycle is:

$$V_{IN1(MIN)} = \frac{V_{OUT1} + V_D}{1 - f_{SW} \bullet t_{OFF(MIN)}} - V_D + V_{SW}$$

where $V_{IN(MIN)}$ is the minimum input voltage, V_{OUT1} is the output voltage, V_D is the catch diode drop (~0.5V), V_{SW} is the internal switch drop (~0.5V at maximum load), f_{SW} is the switching frequency, and $t_{OFF(MIN)}$ is the minimum switch off-time (~170ns). Note that a higher switching frequency will increase the minimum input voltage. If a lower dropout voltage is desired, a lower switching frequency should be used.

The highest allowed V_{IN1} during normal operation ($V_{IN1(OP-MAX)}$) is limited by minimum duty cycle and is given by:

$$V_{IN1(OP-MAX)} = \frac{V_{OUT1} + V_D}{f_{SW} \bullet t_{ON(MIN)}} - V_D + V_{SW}$$

where V_{OUT1} is the output voltage, V_D is the catch diode drop (~0.5V), V_{SW} is the internal switch drop (~0.5V at maximum load), f_{SW} is the switching frequency, and $t_{ON(MIN)}$ is the minimum switch on-time (~150ns).

However, the LT3667 will tolerate inputs up to the absolute maximum ratings of the V_{IN1} and BOOST pins, regardless of the chosen switching frequency. During such transients where V_{IN1} is higher than $V_{IN1(OP-MAX)}$, the part will skip pulses to maintain output regulation. The output voltage ripple and inductor current ripple will be higher than in normal operation. Input voltage transients of up to 60V are also safely withstood, though the LT3667 stops switching while $V_{IN1} > V_{OVLO}$ (overvoltage lockout, 42V typical), allowing the output to fall out of regulation.

During start-up, short-circuit, or other overload conditions the inductor peak current might reach and even exceed the maximum current limit of the LT3667, especially in those cases where the switch already operates at minimum on-time. The catch diode current limit circuitry prevents the switch from turning on again if the inductor valley current is above 500mA nominal.

Inductor Selection and Maximum Output Current

For a given input and output voltage, the inductor value and switching frequency will determine the ripple current, which increases with higher V_{IN1} or V_{OUT1} and decreases with higher inductance and higher switching frequency.

A good first choice for the inductor value is:

$$L = \left(V_{OUT1} + V_D\right) \bullet \frac{2.4}{f_{SW}}$$

where f_{SW} is the switching frequency in MHz, V_{OUT1} is the output voltage, V_D is the catch diode drop (~0.5V) and L is the inductor value in µH. The inductor's RMS current rating must be greater than the maximum load current and its saturation current should be about 30% higher. For robust operation in fault conditions (start-up or short-circuit) and high input voltage (>30V), the saturation current should be above 900mA. To keep the efficiency high, the series resistance (DCR) should be less than 0.3Ω, and the core material should be intended for high frequency applications. Table 2 lists several vendors.

Table 2. Inductor Vendors

VENDOR	URL
Coilcraft	www.coilcraft.com
Sumida	www.sumida.com
Toko	www.tokoam.com
Würth Elektronik	www.we-online.com
Coiltronics	www.cooperet.com
Murata	www.murata.com

APPLICATIONS INFORMATION

This simple design guide will not always result in the optimum inductor selection for a given application. As a general rule, lower output voltages and higher switching frequency will require smaller inductor values. If the application requires less than 400mA load current, then a lesser inductor value may be acceptable. This allows the use of a physically smaller inductor, or one with a lower DCR resulting in higher efficiency. However, the inductance should in general not be smaller than 10µH.

Be aware that if the inductance differs from the simple rule above, then the maximum load current will depend on input voltage. In addition, low inductance may result in discontinuous mode operation, which further reduces maximum load current. For details of maximum output current and discontinuous mode operation, see Linear Technology's Application Note 44. Finally, for duty cycles greater than 50% ($V_{OUT1}/V_{IN1} > 0.5$), a minimum inductance is required to avoid sub-harmonic oscillations:

$$L_{MIN} = \left(V_{OUT1} + V_D\right) \bullet \frac{2}{f_{SW}}$$

where f_{SW} is the switching frequency in MHz, V_{OUT1} is the output voltage, V_D is the catch diode drop (~0.5V) and L_{MIN} is the inductor value in µH.

Catch Diode

The catch diode (D1 from block diagram) conducts current only during switch off-time. Use a 1A Schottky diode for best performance.

Peak reverse voltage is equal to V_{IN1} if it is below the overvoltage protection threshold. This feature keeps the switch off for V_{IN1} > OVLO (44V maximum). For inputs up to the maximum operating voltage of 40V, use a diode with a reverse voltage rating greater than the input voltage. If transients at the input of up to 60V are expected, use a diode with a reverse voltage rating only higher than the maximum OVLO of 44V. If operating at high ambient temperatures, consider using a Schottky with low reverse leakage. For example, Diodes Inc. SBR1U40LP or DFLS160, ON Semi MBRM140, and Central Semiconductor CMMSH1-60 are good choices for the catch diode.

Input Capacitor

Bypass the input of the LT3667 circuit with a ceramic capacitor of X7R or X5R type. Y5V types have poor performance over temperature and applied voltage, and should not be used. A 1µF to 4.7µF ceramic capacitor is adequate to bypass the LT3667 and will easily handle the ripple current. Note that a larger input capacitance is required when a lower switching frequency is used (due to longer on-times). If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor. Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT3667 and to force this very high frequency switching current into a tight local loop, minimizing EMI. A 1µF capacitor is capable of this task, but only if it is placed close to the LT3667 (see the PCB Layout section). A second precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT3667. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT3667 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT3667's voltage rating. This situation is easily avoided (see the Hot Plugging Safely section).

Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT3667 to produce the DC output. In this role it determines the output ripple, and low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the switching regulator's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. A good starting value is:

$$C_{OUT1} = \frac{50}{V_{OUT1} \bullet f_{SW}}$$

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where f_{SW} is in MHz, and C_{OUT1} is the recommended output capacitance in µF. Use X5R or X7R types. This choice will provide low output ripple and good transient response. Transient performance can be improved with a higher value capacitor if combined with a phase lead capacitor (typically 22pF) between the output and pin FB1. Note that a larger phase lead capacitor should be used with a large output capacitor. A lower value of output capacitor can be used to save space and cost but transient performance will suffer.

When choosing a capacitor, look carefully through the data sheet to find out what the actual capacitance is under operating conditions (applied voltage and temperature). A physically larger capacitor, or one with a higher voltage rating, may be required. Table 3 lists several capacitor vendors.

Table 3: Capacitor Vendors

VENDOR	URL
Panasonic	www.panasonic.com
Kemet	www.kemet.com
Sanyo	www.sanyovideo.com
Murata	www.murata.com
AVX	www.avxcorp.com
Taiyo Yuden	www.taiyo-yuden.com

Audible Noise

Ceramic capacitors are small, robust and have very low ESR. However, ceramic capacitors can sometimes cause problems when used with the LT3667 due to their piezoelectric nature. When in Burst Mode operation, the LT3667's switching frequency depends on the load current, and at very light loads the LT3667 can excite the ceramic capacitor at audio frequencies, generating audible noise. Since the LT3667 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet. If this is unacceptable, use a high performance tantalum or electrolytic capacitor at the output.

Low Ripple Burst Mode Operation

To enhance efficiency at light loads, the LT3667 operates in low ripple Burst Mode operation which keeps the output capacitor charged to the proper voltage while minimizing the input quiescent current. During Burst Mode operation, the LT3667 delivers single cycle bursts of current to the output capacitor followed by sleep periods where the output power is delivered to the load by the output capacitor. Because the LT3667 delivers power to the output with single, low current pulses, the output ripple is kept below 5mV for a typical application. As the load current decreases towards a no load condition, the percentage of time that the LT3667 operates in sleep mode increases and the average input current is greatly reduced resulting in high efficiency even at very low loads. Note that during Burst Mode operation, the switching frequency will be lower than the programmed switching frequency.

At higher output loads (above ~50mA for the front page application) the LT3667 will be running at the frequency programmed by the R_T resistor, and will be operating in standard PWM mode. The transition between PWM and low ripple Burst Mode operation is seamless, and will not disturb the output voltage.

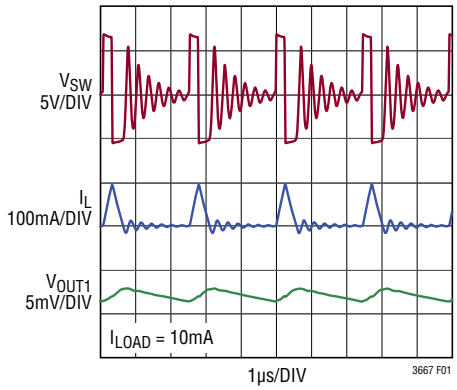


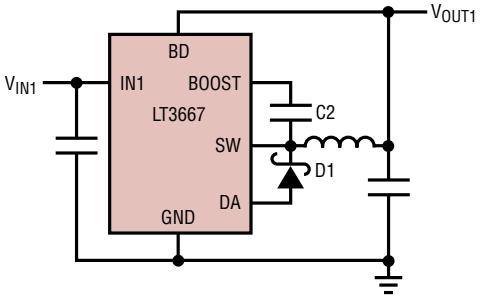
Figure 1. Burst Mode Operation

APPLICATIONS INFORMATION

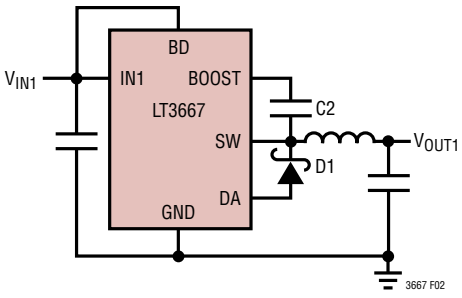
BOOST and BD, IN3/BD Pin Considerations

Capacitor C2 and the internal boost Schottky diode (see the Block Diagram) are used to generate a boost voltage that is higher than the input voltage. In most cases a 0.22µF capacitor will work well. Figure 2 shows two ways to arrange the boost circuit. The BOOST pin must be more than 1.9V above the SW pin for best efficiency. For outputs of 2.2V and above, the standard circuit (Figure 2a) is best. For outputs between 2.2V and 2.5V, use a 0.47µF boost capacitor. For output voltages below 2.2V, the boost diode can be tied to the input (Figure 2b), or to another external supply greater than 2.2V. However, the circuit in Figure 2a is more efficient because the BOOST pin current and BD pin quiescent current come from a lower voltage source. Also, be sure that the maximum voltage ratings of the BOOST and BD pins are not exceeded.

The minimum operating voltage of an LT3667 application is limited by the minimum input voltage (4.3V) and by the maximum duty cycle as outlined in a previous section. For proper start-up, the minimum input voltage is also limited by the boost circuit. If the input voltage is ramped slowly, the boost capacitor may not be fully charged. Because the boost capacitor is charged with the energy stored in the inductor, the circuit relies on some minimum load current to get the boost circuit running properly. This minimum load depends on input and output voltages, and on the arrangement of the boost circuit. The minimum load generally goes to zero once the circuit has started. Figure 3 shows a plot of minimum load to start and to run as a function of input voltage. In many cases the discharged output capacitor will present a load to the switcher, which will allow it to start. The plots show the worst-case situation where V_{IN1} is ramping very slowly. For lower start-up voltage, the boost diode can be tied to V_{IN1}; however, this restricts the input range to one-half of the absolute maximum rating of the BOOST pin.

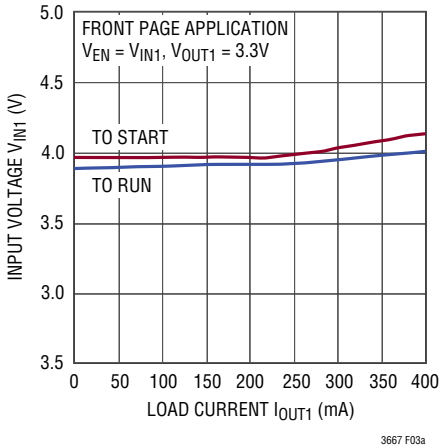


(2a) For $V_{OUT1} \geq 2.2V$



(2b) For $V_{OUT1} < 2.2V$; $V_{IN1} < 25V$

Figure 2. Two Circuits for Generating the Boost Voltage



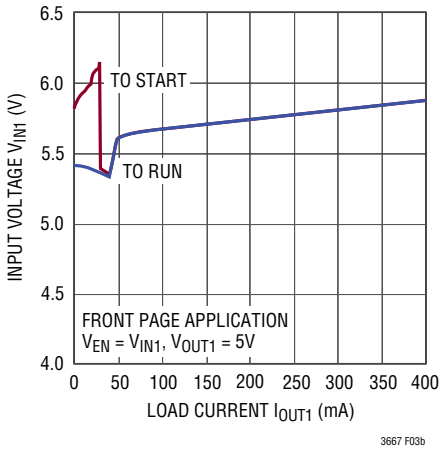


Figure 3. The Minimum Input Voltage Depends on Output Voltage, Load Current and Boost Circuit

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Synchronization (QFN Only)

Synchronizing the oscillator of the LT3667 to an external frequency can be done by connecting a digital clock signal to the SYNC pin. The LT3667 then synchronizes its SW node to the rising edge of this clock signal, as shown in Figure 4. The square wave amplitude should have valleys that are below 0.5V and peaks that are above 1.2V (up to 6V), and its on-time and off-time should not fall below 50ns. There is a time delay of typically 280ns between the rising edge of SYNC and the rising edge of SW which is in part caused by the minimum switch off-time. The falling edge of SW is sensitive to the falling edge of SYNC, it is therefore recommended to adjust the duty cycle of the SYNC clock signal accordingly to keep its on-time as short as possible. Alternatively, AC coupling as shown in Figure 5 can be used to shorten the clock signal's on-time.

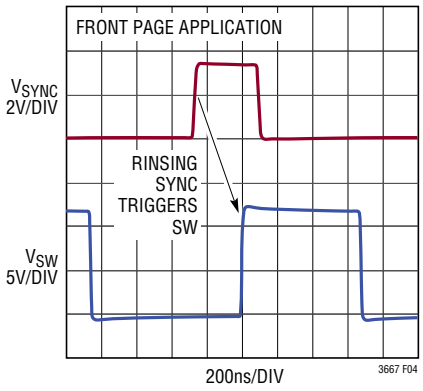


Figure 4. Synchronization Waveforms

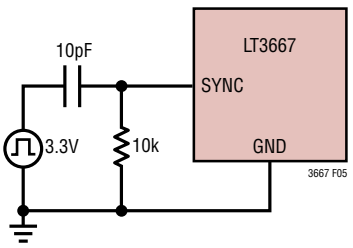


Figure 5. Example of AC Coupling of SYNC Clock Signal

The LT3667 still enters Burst Mode operation at low output loads while synchronized to an external clock, but the burst pulses are synchronized to that clock signal. If synchronization is not needed, the SYNC pin should be grounded. It may also be tied to a voltage above 1.2V (logic high), but note that there is an internal 4M resistor from SYNC to ground which will draw current.

The LT3667 may be synchronized over a 300kHz to 2.2MHz range. The R_T resistor should be chosen to set the switching frequency 20% below the lowest synchronization input. For example, if the synchronization signal is 360kHz, R_T should be chosen for 300kHz. Since R_T also sets the slope compensation which avoids subharmonic oscillations, the minimum inductor value must be calculated using the frequency determined by R_T.

UVLO1 Pin (QFN Only)

The switching regulator part of the LT3667 can be independently disabled via the UVLO1 pin. The falling threshold of the UVLO1 comparator is 1V, with a 75mV hysteresis. The UVLO1 pin has no effect if V_{IN1} and V_{IN2} are below 4.3V, because then the internal undervoltage lockout keeps the LT3667 shut down anyway.

Adding a resistive divider from IN1 to UVLO1 as shown in Figure 6 programs the LT3667 to enable the switching regulator only when V_{IN1} is above a certain threshold voltage $V_{IN(UVLO1)}$, given by:

$$V_{IN(UVLO1)} = \frac{R1+R2}{R2} \bullet 1V$$

Note that due to the comparator's hysteresis, the switching regulator will not be enabled until the input rises slightly above $V_{IN(UVLO1)}$.

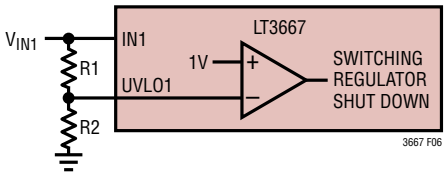


Figure 6. UVLO1 Pin Allows Programmable Undervoltage Lockout or Independent Disable of the Switching Regulator

Shorted and Reversed Input Protection

If the inductor is chosen so that it won't saturate excessively, the switching regulator will tolerate a shorted output. There is another situation to consider in systems where the output will be held high when the input to the LT3667 is absent. This may occur in battery charging applications or in battery backup systems where a battery

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or some other supply is diode ORed with the switching regulator's output. If the IN1 pin is allowed to float and the EN and UVLO1 pins are held high (either by a logic signal or because they are tied to IN1), then the LT3667's internal circuitry will pull its quiescent current through the SW pin. This is fine if the system can tolerate a few µA in this state. If the EN pin or the UVLO1 pin is grounded, the SW pin current will drop to 0.7µA. However, if the IN1 pin is grounded while the output is held high, regardless of EN and UVLO1, parasitic diodes inside the LT3667 can pull current from the output through the SW pin and the IN1 pin. Figure 7 shows a circuit that will run only when the input voltage is present and that protects against a shorted or reversed input. Alternatively, the switching regulator can be supplied by the LDO at OUT2 as shown in the Applications Information section of the LDOs.

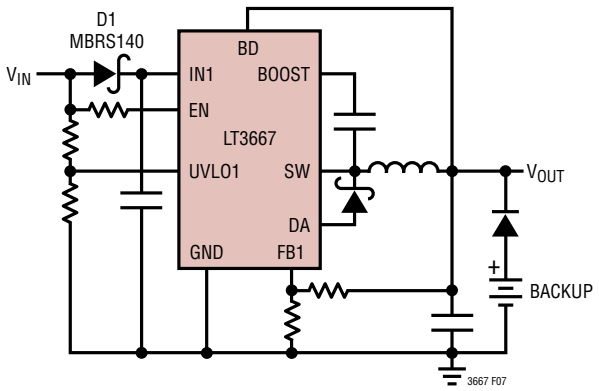


Figure 7. Diode D1 Prevents a Shorted Input from Discharging a Backup Battery Tied to the Output. It Also Protects the Circuit from a Reversed Input, in Which Case the Resistor at the EN Pin Limits the Current Drawn from That Pin. The LT3667 Runs Only When the Input Is Present

LDOs

FB2/FB3 Resistor Networks

Each LDO output voltage of the LT3667 is programmed with a resistor divider between the output of that LDO and its FB2/FB3 pin as shown in Figure 8. The pin current, I_{FB}, (3nA at 25°C, ±40nA at 150°C) of each FB2/FB3 pin flows out of that pin, which results in

$$V_{OUT} = 0.8V\left(\frac{R2}{R1}+1\right) - I_{FB} \bullet R2$$

The value of R1 should not exceed 160k to provide a minimum 5µA load current so that the output voltage error, caused by the FB2/FB3 pin current, is minimized. Rearranging for R2 gives:

$$R2 = \frac{0.8V - V_{OUT}}{I_{FB} - 0.8V/R1}$$

Note that choosing smaller resistors will increase the quiescent current of the application circuit.

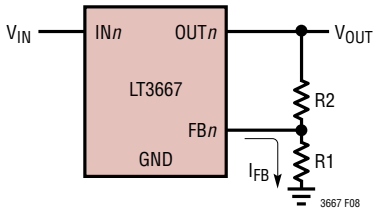


Figure 8. Setting the Output Voltage of Each LDO

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Input Supply

The internal biasing and reference circuitry of the LT3667 is supplied by the IN1 and IN2 pins. This allows connecting the switching regulator input IN1 to the LDO output OUT2. This can be used to shield the supply at IN2 from the high start-up currents of the switching regulator by utilizing the LDO's programmable current limit. The Typical Applications section shows an example of such an application, which also benefits from the reverse voltage protection of the LDO.

Input Capacitance and Stability

Each LDO is stable with an input capacitor typically between 1µF and 10µF. This input capacitor must be placed as close as possible to the corresponding input pin. Applications operating with smaller input to output differential voltages and that experience large load transients may require a higher input capacitor value to prevent input voltage droop and letting the regulator enter dropout.

Very low ESR ceramic capacitors may be used. However, in cases where long wires connect the power supply to the LDOs input and ground, use of low value input capacitors may result in instability. The resonant LC tank circuit formed by the wire inductance and the input capacitor is the cause and not a result of LDO instability.

The minimum input capacitance needed to stabilize the application also varies with power supply output impedance variations. Placing additional capacitance on an LDO's output also helps. However, this requires an order of magnitude more capacitance in comparison with additional input bypassing. Series resistance between the supply and an LDO's input also helps stabilize the application; as little as 0.1Ω to 0.5Ω suffices. This impedance dampens the LC tank circuit at the expense of dropout voltage. A better alternative is to use higher ESR tantalum or electrolytic capacitors at the input in place of ceramic capacitors.

Output Capacitance, Transient Response, Stability

Each LT3667's LDO is stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. Use a minimum output capacitor of 2.2µF to prevent oscillations. Applications with output voltages of less than 2.5V and applications where the difference between input and output voltage exceeds 20V require a minimum output capacitor of 10µF. In addition, the ESR of the output capacitor must not exceed 3Ω.

The LT3667 is a micropower device and output load transient response is a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes, especially for low output voltages. Bypass capacitors, used to decouple individual components powered by the LT3667, increase the effective output capacitor value. For applications with large load current transients, a low ESR ceramic capacitor in parallel with a bulk tantalum capacitor often provides an optimally damped response.

Note that some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress is induced by vibrations in the system or thermal transients. The resulting voltages produced cause appreciable amounts of noise. A ceramic capacitor produced the trace in Figure 9 in response to light tapping from a pencil. Similar vibration induced behavior can masquerade as increased output voltage noise.

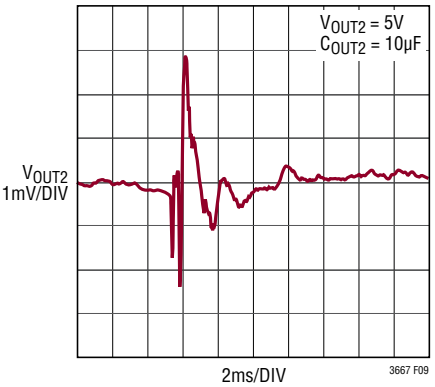


Figure 9. Noise Resulting from Tapping On a Ceramic Capacitor

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External Programmable Current Limit, Enable

Each EN/ILIM pin (EN2/ILIM2 and EN3/ILIM3) is the collector of a PNP which mirrors the corresponding LDO's output at a ratio of 1:799 (see Block Diagram). The EN2/ILIM2 and EN3/ILIM3 pins are also the inputs to precision current limit amplifiers. If an output load increases to the point where it causes the corresponding current limit amplifier input voltage to reach 0.4V, the current limit amplifier takes control of output regulation so that its input clamps at 0.4V, regardless of the output voltage. The current limit threshold (I_{LIMIT}) of an LDO is set by attaching a resistor (R_{IMAX}) from the corresponding EN/ILIM pin to ground:

$$R_{IMAX} = \frac{799 \bullet 0.4V}{I_{LIM}} - 80\Omega$$

In order to maintain stability, each EN/ILIM pin requires a 47nF capacitor from that pin to ground.

In cases where the input to output voltage differential exceeds 10V, foldback current limit will lower the internal current level limit, possibly causing it to preempt the external programmable current limit. See the Internal Current Limit vs Input/Output Differential graph in the Typical Performance Characteristics section.

If an external current limit is not needed, the corresponding EN/ILIM pin must be connected to ground, in which case no capacitor is required.

Each LDO can be individually shut down by pulling its EN/ILIM pin above 1.2V (1V typical). Note that in this case this pin will draw up to 500µA in certain operating conditions until the LDO is shut down, which the circuit driving this pin must be able to deliver. When an EN/ILIM pin is only used to enable/disable an LDO, no capacitor is required on this pin.

Overload Recovery

Each LDO of the LT3667 has a safe operating area protection, which decreases current limit as input-to-output voltage increases, and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. Each LDO provides some output current at all values of input-to-output voltage up to the device breakdown. When power is first applied to an LDO, the input voltage rises and the output follows the input; allowing the regulator to start-up into very heavy loads. During start-up, as the input voltage is rising, the input-to-output voltage differential is small, allowing the regulator to supply large output currents. With a high input voltage, a problem can occur wherein the removal of an output short will not allow the output to recover. The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations are: immediately after the removal of a short-circuit or if an LDO is enabled via its EN/ILIM pin after the input voltage is already turned on. In such cases, the regulator would have to operate its power device outside its safe operating are (high voltage and high current) in order to bring up the output voltage. Since this is prevented by the safe operating area protection, the output gets stuck at a low voltage. Essentially, the load line for such a load intersects the output current curve at two points, resulting in two stable output operating points for the regulator. With this double intersection, the input power supply needs to be cycled down to zero and brought up again to make the output recover.

Protection Features

The LT3667 LDO's protect against reverse-input voltages, reverse-output voltages and reverse output-to-input voltages. Current limit protection and thermal overload protection protect the LDOs against current overload conditions at their outputs. For normal operation, do not exceed the maximum operating junction temperature. The LT3667 IN2 and IN3 (QFN only) pins withstand reverse voltages of 45V. The device limits current flow to less than 300µA (typically less than 10µA) and no negative voltages appear at OUT2 or OUT3. The LDOs incur no damage if their outputs are pulled below ground. If an input is left open circuit or grounded, the corresponding output can be pulled below ground by 45V. No current flows through the pass transistor from the output. However, current flows in (but is limited by) the corresponding resistor divider that sets the output voltage. Current flows from the bottom resistor in the divider and from the FB2/FB3 pin's internal clamp through the top resistor in the divider to the external circuitry pulling OUT2/OUT3 below ground. If the input is powered by a voltage source, the output sources cur-

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rent equal to its current limit capability and the LT3667 protects itself by thermal limiting. Note that the externally programmable current limit is less accurate if the output is pulled below ground.

These protection features can be used to protect the switching regulator input as shown in the Typical Applications section.

COMMON

Ceramic Capacitor Characteristics

Give extra consideration to the use of ceramic capacitors. Manufacturers make ceramic capacitors with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics provide high C-V products in a small package at low cost, but exhibit strong voltage and temperature coefficients, as can be seen for Y5V in Figures 10 and 11. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied, and over the operating temperature range. The X5R and X7R dielectrics yield much more stable characteristics and are more suitable for use as input and output capacitors. The X7R type works over a wider temperature range and has better temperature stability, while the X5R is less expensive and is available in higher values. Still exercise care when using X5R and X7R capacitors; the X5R and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias with X5R and X7R capacitors is better than Y5V and Z5U capacitors, but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component case size increases, but expected capacitance at operating voltage should be verified.

PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figures 12 and 13 show the recommended component placement with trace, ground plane and via locations. Note that large, switched currents flow in the LT3667's IN1, SW, GND and DA pins, the catch diode and the input capacitor. The loop formed by these components should be as small as possible. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane below these components.

The SW and BOOST nodes should be as small as possible. Keep the FB1, FB2, and FB3 nodes small so that the ground traces will shield them from the SW and BOOST nodes. The exposed pad must be soldered such that it can act as a heat sink. (See High Temperature Considerations section.)

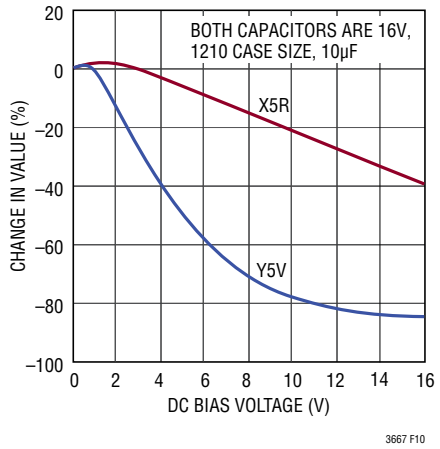


Figure 10. Ceramic Capacitor DC Bias Characteristics

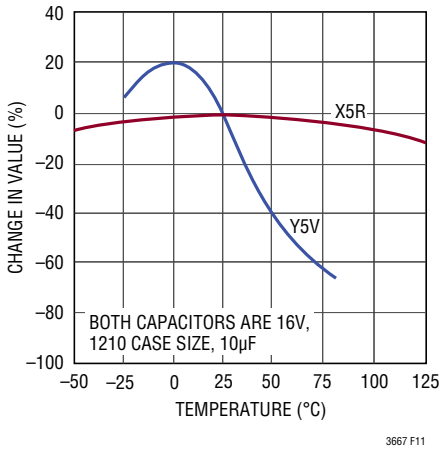


Figure 11. Ceramic Capacitor Temperature Characteristics

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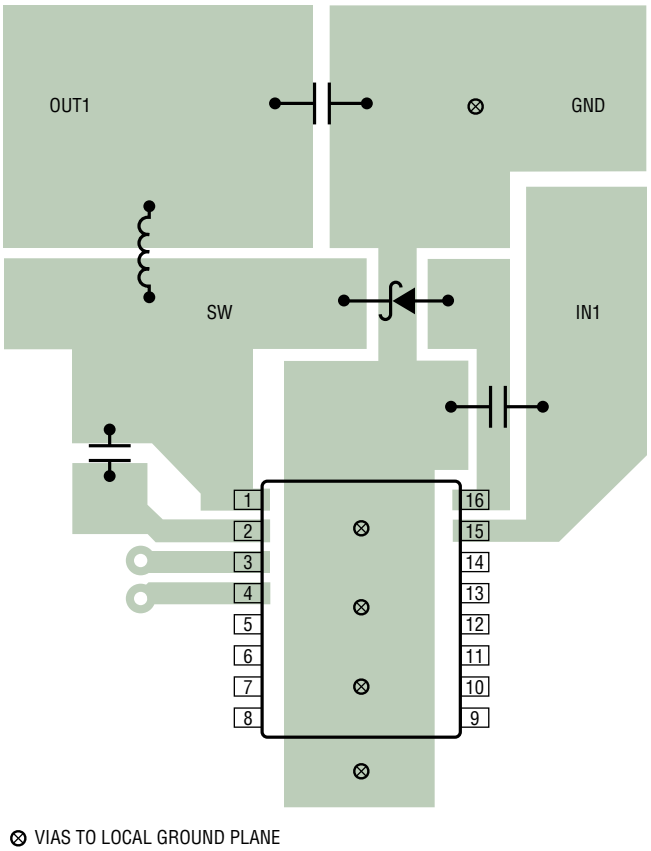


Figure 12. Good PCB Layout Ensures Proper, Low EMI Operation (MSOP)

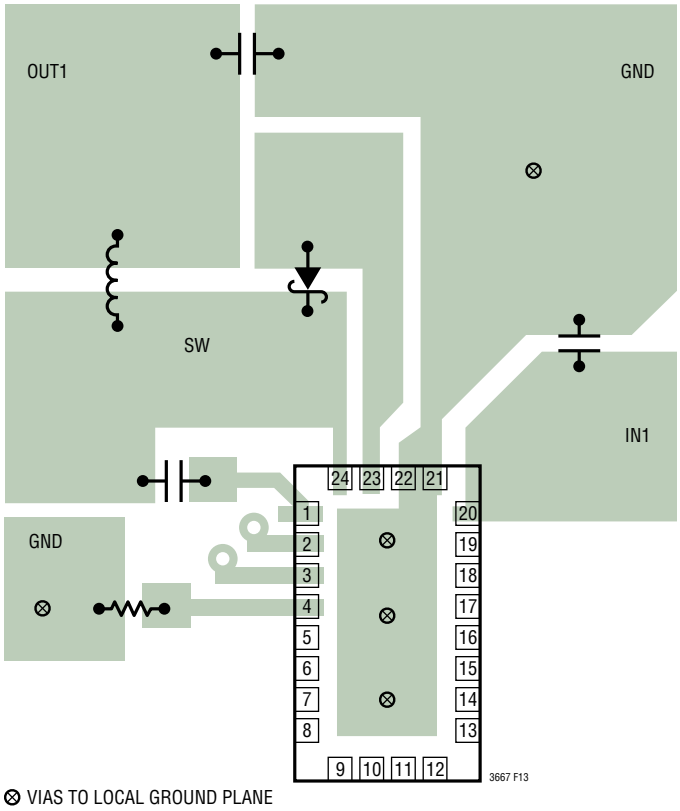


Figure 13. Good PCB Layout Ensures Proper, Low EMI Operation (QFN)

Hot Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitors of LT3667 circuits. However, these capacitors can cause problems if the LT3667 is plugged into a live supply. The low loss ceramic capacitor, combined with stray inductance in series with the power source, forms an under damped tank circuit, and the voltage at the input pins of the LT3667 can ring to twice their nominal input voltage, possibly exceeding the LT3667's rating and damaging the part. If the input supply is poorly controlled or the user will be plugging the LT3667 into an energized supply, the input network should be designed to prevent this overshoot. See Linear Technology Application Note 88 for a complete discussion.

High Temperature Considerations

The LT3667's maximum rated junction temperature of 125°C (E- and I-grades) and 150°C (H-grade) respectively limits its power handling capability.

Power dissipation within the switching regulator can be estimated by calculating the total power loss from an efficiency measurement and subtracting inductor loss. Be aware that at high ambient temperatures the external Schottky diode will have significant leakage current (see Typical Performance Characteristics), increasing the quiescent current of the switching regulator.

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The power dissipation of each LDO is comprised of two components. Each power device dissipates:

$$P_{PASS} = (V_{IN} - V_{OUT}) \bullet I_{OUT}$$

where P_{PASS} is the power, V_{IN} the input voltage, V_{OUT} the output voltage, and I_{OUT} the output current. The base currents of the LDO power PNP transistors flow to ground internally and are the major component of the ground current. For each LDO, this causes a power dissipation P_{GND} of:

$$P_{GND} = V_{IN} \bullet I_{GND}$$

where V_{IN} is the input voltage and I_{GND} the ground current generated by the corresponding power device. GND pin current is determined by the current gain of the power PNP, which has a typical value of 40 for the purpose of this calculation:

$$I_{GND} = \frac{I_{OUT}}{40}$$

The total power dissipation equals the sum of the power loss in the switching regulator and the two LDO components listed above.

The LT3667 has internal thermal limiting that protects the device during overload conditions. If the junction temperature reaches the thermal shutdown threshold, the LT3667 will shut down the LDOs and stop switching to prevent internal damage due to overheating. For continuous normal conditions, do not exceed the maximum operating junction temperature. Carefully consider all sources of thermal resistance from junction-to-ambient including other nearby heat sources. Both LT3667 packages have exposed pads that must be soldered to a ground plane to act as heat sink. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the LT3667 to additional ground planes within the circuit board and on the bottom side.

The die temperature rise is calculated by multiplying the power dissipation of the LT3667 by the thermal resistance from junction to ambient. Example: Given the front page application with maximum output current, an input voltage of 12V and a maximum ambient temperature of 85°C, what will the maximum junction temperature be?

As can be seen from the Typical Performance Characteristics, the switching regulator efficiency approaches 85% at 400mA output current. This leads to a power loss, P_{LOSS}, of:

$$P_{LOSS} = 5V \bullet 400mA \bullet \left(\frac{1}{0.85} - 1\right) = 353mW$$

(For the sake of simplicity and as a conservative estimate assume that all of this power is dissipated in the LT3667.) The power dissipations of the LDO power devices are:

$$P_{PASS2} = (5V - 2.5V) \bullet 100mA = 250mW$$

$$P_{PASS3} = (5V - 3.3V) \bullet 100mA = 170mW$$

For 100mA load current a maximum ground current of 2.5mA is to be expected. Thus, the corresponding power dissipations are:

$$P_{GND2} = P_{GND3} = 5V \bullet 2.5mA = 12.5mW$$

Finally, the total power dissipation is:

$$P_{TOT} = P_{LOSS} + P_{PASS2} + P_{PASS3} + P_{GND2} + P_{GND3} = 786mW$$

Using the MSOP package, which has a thermal resistance of approximately 40°C/W, this total power dissipation would raise the junction temperature above ambient by:

$$0.786W \bullet 40°C/W = 32°C$$

With the assumed maximum ambient temperature of 85°C, this puts the maximum junction temperature at:

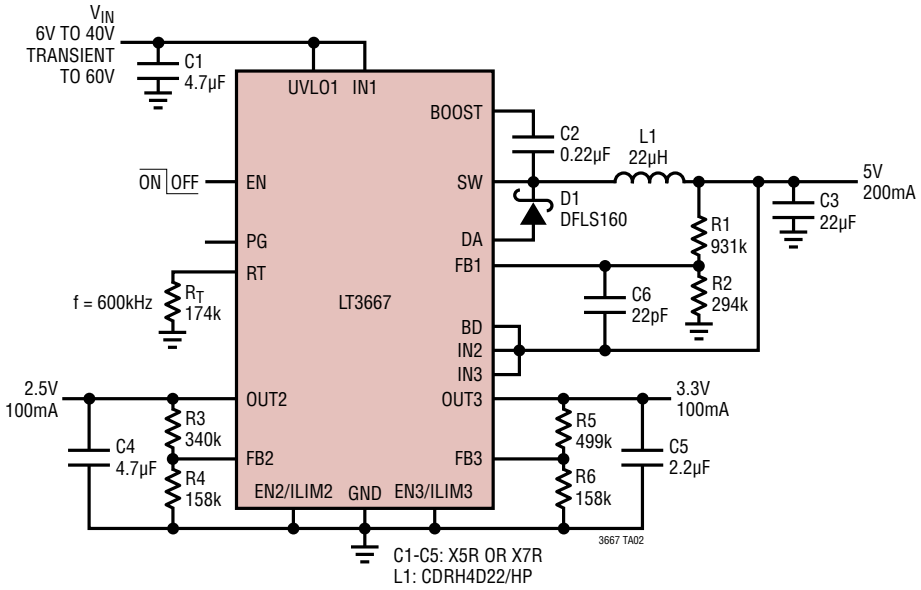
$$T_{JMAX} = 85°C + 32°C = 117°C$$

Other Linear Technology Publications

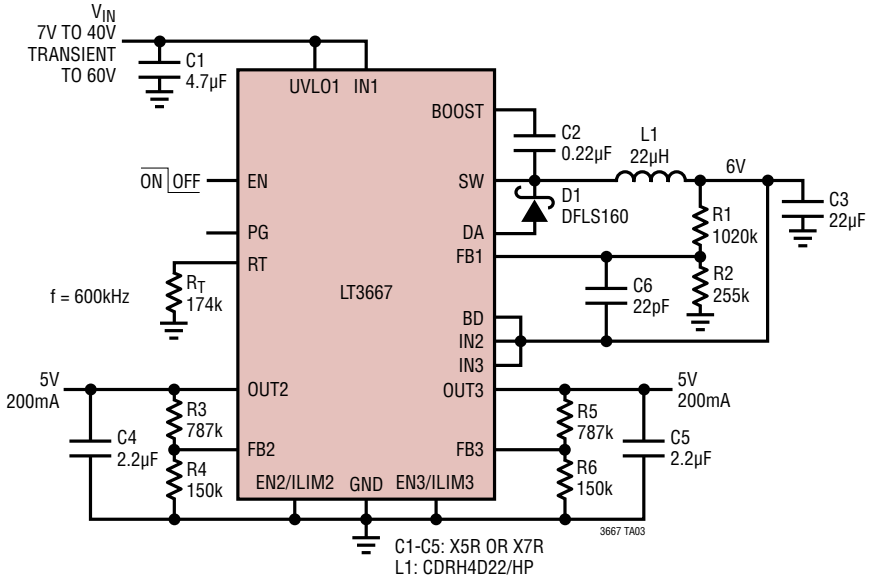
Application Notes 19, 35 and 44 contain more detailed descriptions and design information for buck regulators and other switching regulators. The LT1376 data sheet has a more extensive discussion of output ripple, loop compensation and stability testing. Design Note 318 shows how to generate a bipolar output supply using a buck regulator.

TYPICAL APPLICATIONS

5V, 3.3V and 2.5V Step-Down Converter

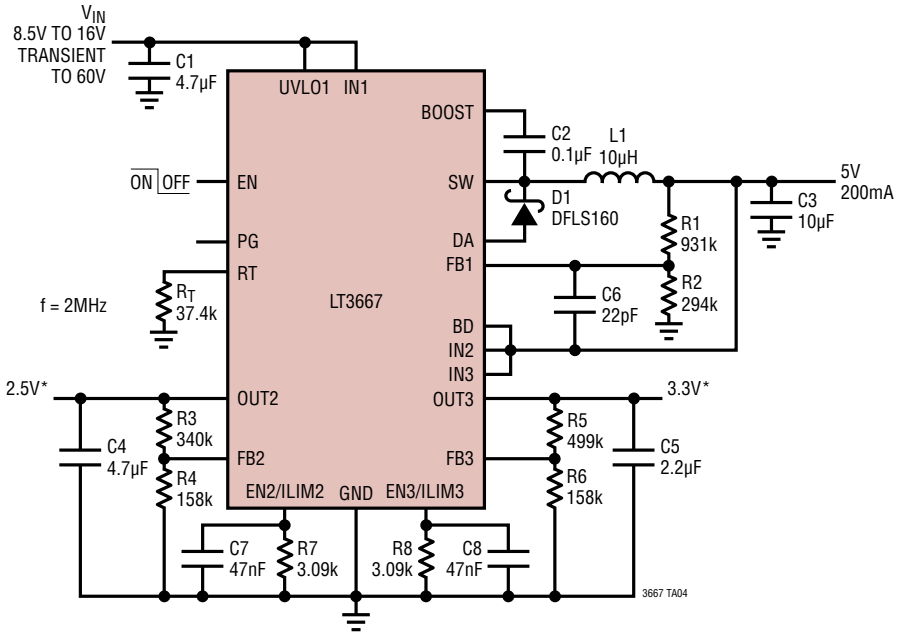


Dual 5V/200mA Step-Down Converter



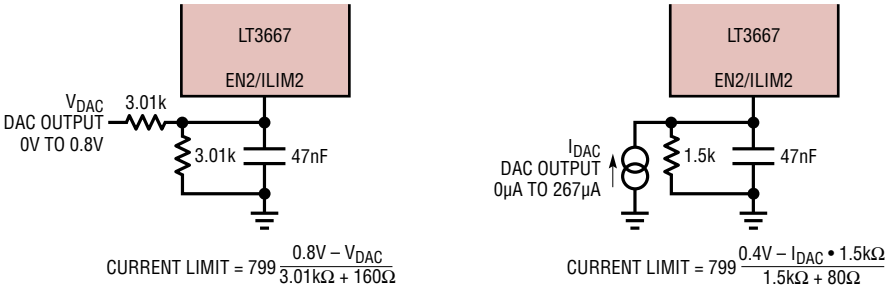
TYPICAL APPLICATIONS

5V, 3.3V and 2.5V Step-Down Converter with 100mA LDO Current Limits



*100mA CURRENT LIMIT
C1-C5: X5R OR X7R
L1: CDRH4D22/HP

Programming LDO Current Limits with a Digital/Analog Converter

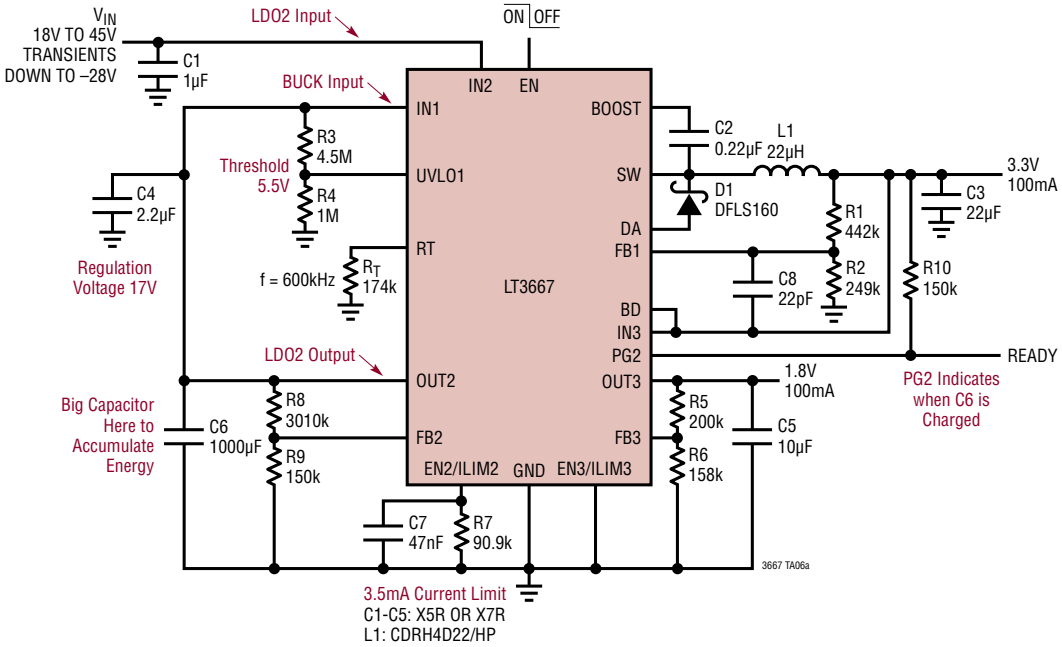


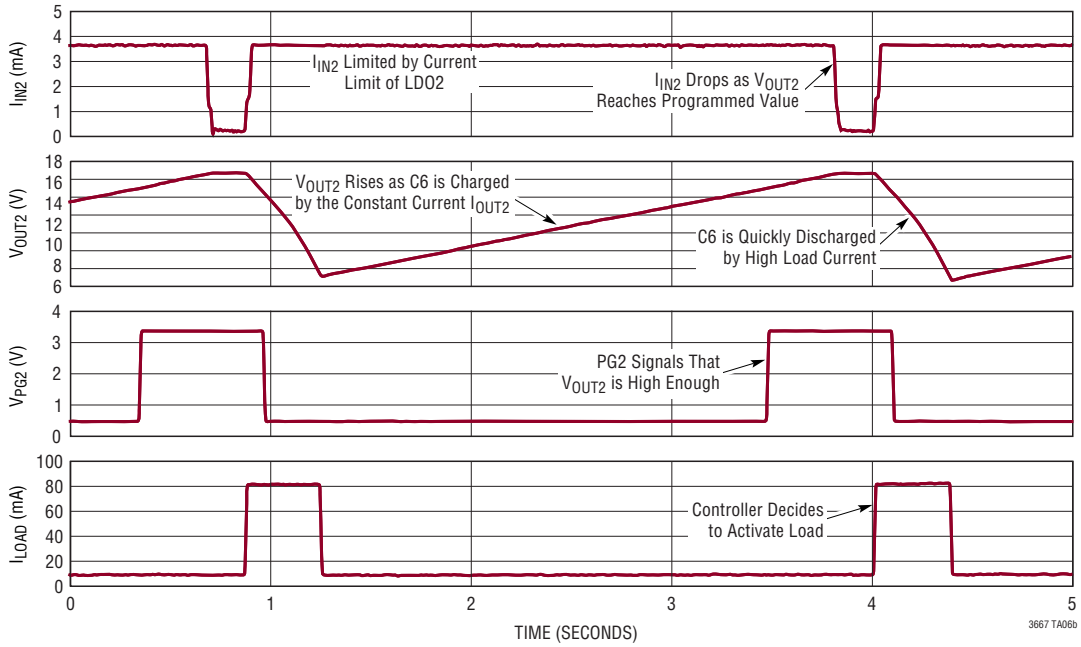
TYPICAL APPLICATIONS

This application allows a small input current to support a high current pulsed load. The switching regulator is supplied by the LDO2 at OUT2, which is programmed to limit its current to 3.5mA. PG2 serves as “READY” signal to tell a controller (not shown) that C6 is charged to 17V, the regulation voltage of LDO2. It can then turn on a load drawing high current out of the switching regulator.

Since LDO2 can only supply 3.5mA, this quickly discharges C6 and decreases V_{OUT2} (=V_{IN1}). The switching regulator will maintain its programmed output voltage until V_{IN1} drops below the undervoltage lockout threshold of 5.5V set by R3 and R4.

Pulsed Power Supply for 4mA to 20mA Current Loops.
OUT2 Supplies the Switching Regulator, Which Is Kept Off at Lower Voltages by UVLO1

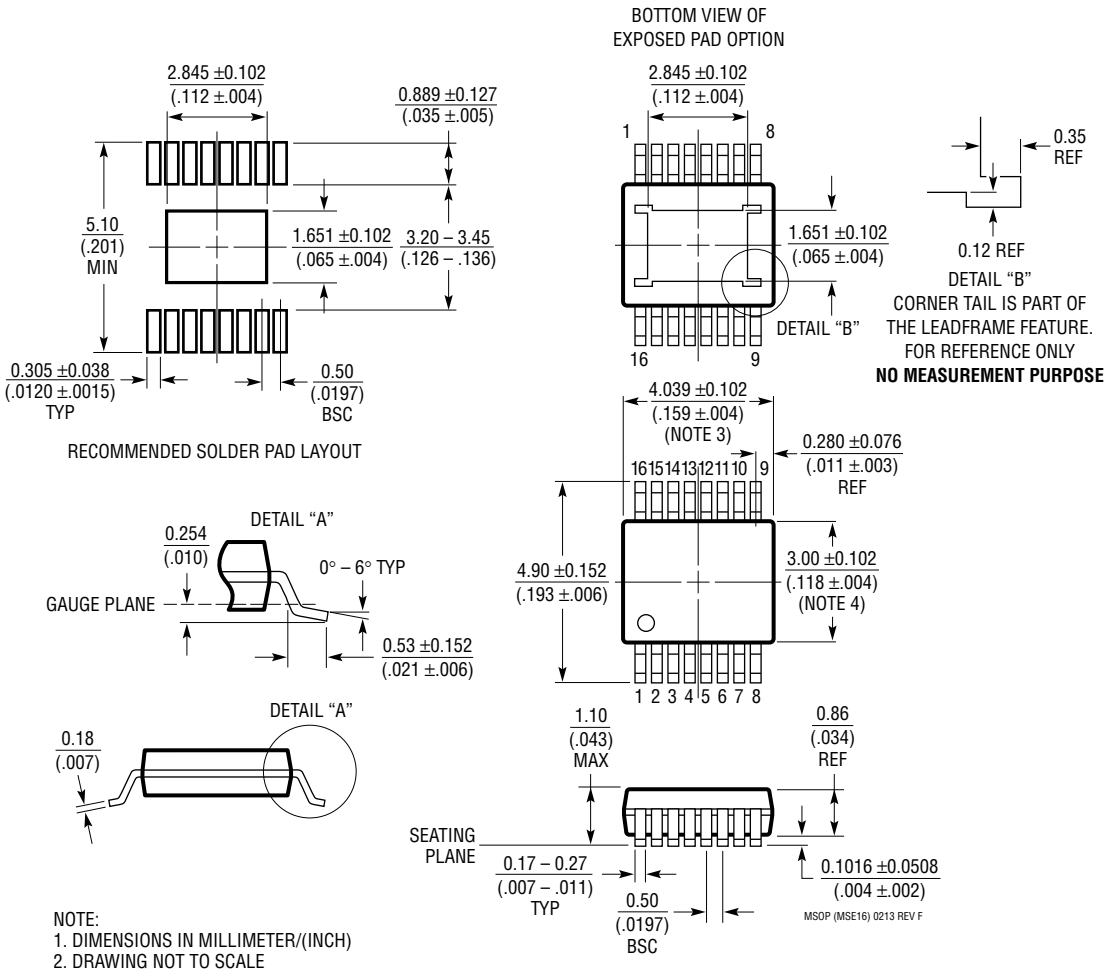




PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev F)

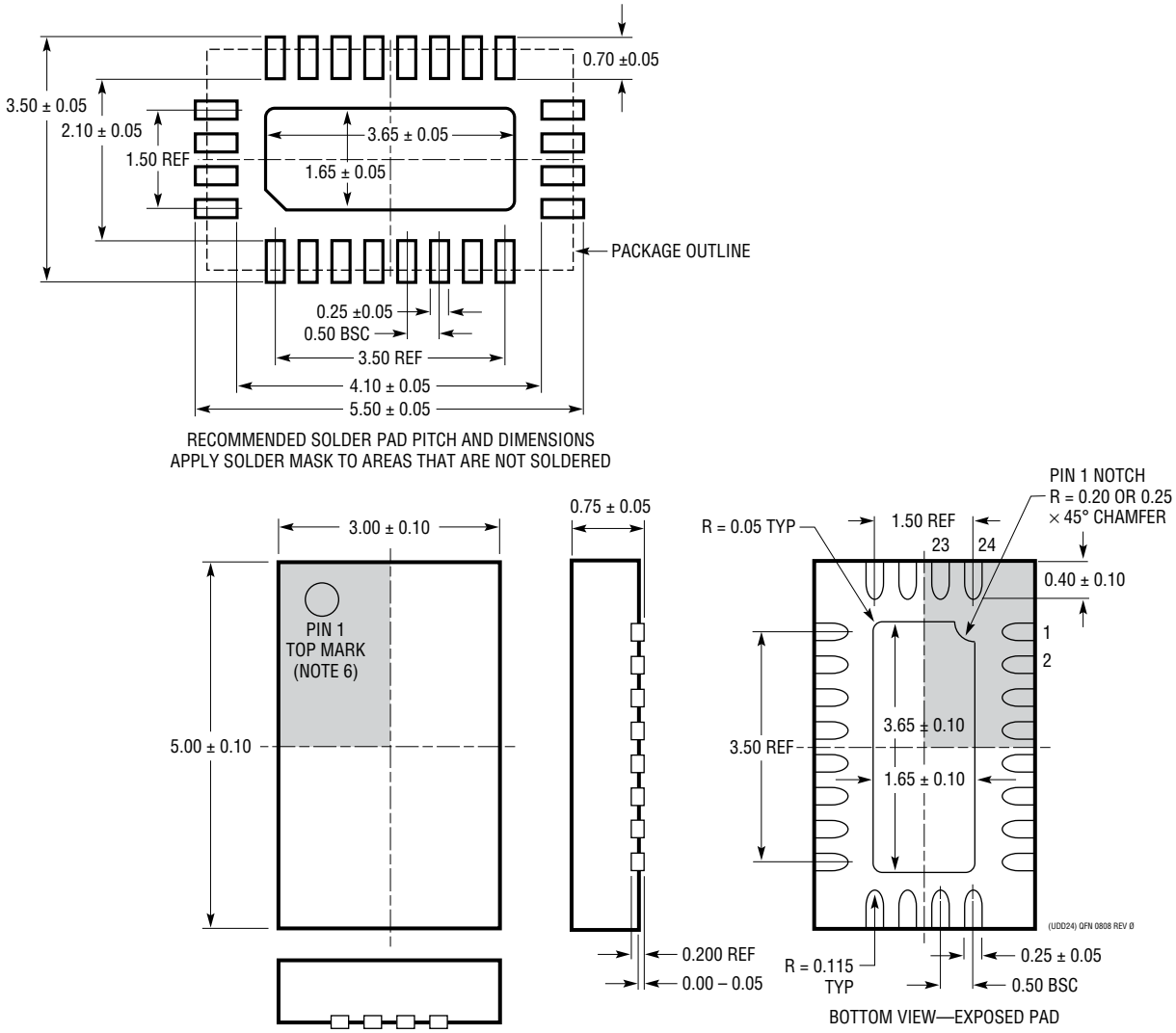


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UDD Package
24-Lead Plastic QFN (3mm × 5mm)
(Reference LTC DWG # 05-08-1833 Rev Ø)



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

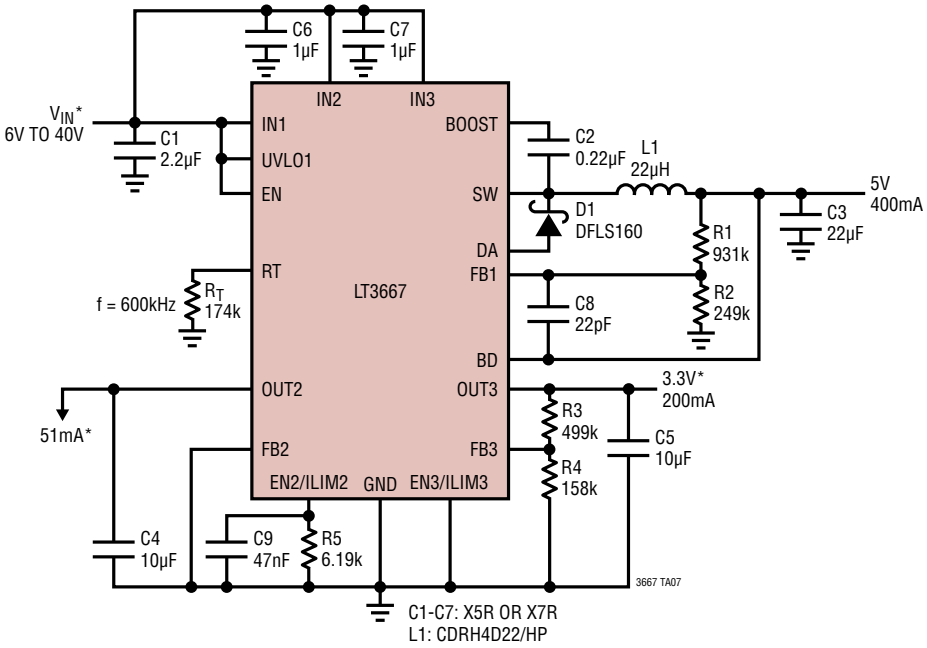
REV	DATE	DESCRIPTION	PAGE NUMBER
A	4/14	Added H-grade in MS16E package to Order Information	3
B	11/14	Clarified Externally Programmable Current Limit specifications	5
		Grammatical correction in Setting the Switching Frequency description	16
		Clarified Typical Application schematic	29

LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

5V, 3.3V and 51mA Regulator



*DERATE OUTPUT CURRENT AT HIGHER AMBIENT TEMPERATURES AND INPUT VOLTAGES TO MAINTAIN JUNCTION TEMPERATURE BELOW THE ABSOLUTE MAXIMUM

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3500	36V ($40V_{MAX}$), 2A (I_{OUT}), 2.2MHz Step-Down Switching Regulator with LDO Controller	V_{IN}: 3V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2.5mA, I_{SD} < 12µA, 3mm × 3mm DFN-10, MSOP-16E
LT1939	25V, 2A (I_{OUT}), 2.2MHz Step-Down Switching Regulator with LDO Controller	V_{IN}: 3V to 25V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2.5mA, I_{SD} < 12µA, 3mm × 3mm DFN-10, MSOP-16E
LT3694	36V ($70V_{MAX}$), 2.6A (I_{OUT}), 2.5MHz Step-Down Switching Regulator with Dual LDO Controller	V_{IN}: 4V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 1mA, I_{SD} < 1µA, 4mm × 5mm QFN-28, TSSOP-20E
LT3507/LT3507A	36V, 2.5MHz, Triple (2.4A + 1.5A + 1.5A (I_{OUT}) with LDO Controller High Efficiency Step-Down DC/DC Converter	V_{IN}: 4V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 7mA, I_{SD} = 1µA, 5mm × 7mm QFN-38
LT3970	40V, 350mA (I_{OUT}), 2.2MHz Step-Down Switching Regulator with I_Q = 2.5µA	V_{IN}: 4.2V to 40V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 2mm DFN, MSOP-10
LT3502/LT3502A	40V, 500mA (I_{OUT}), 1.1MHz/2.2MHz Step-Down Switching Regulator	V_{IN}: 3V to 40V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 1.5mA, I_{SD} < 1µA, 2mm × 2mm DFN-8, MSOP-10E

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