SNx5LBC176A 差分总线收发器

1 特性

- 专为信号传输速率而设计 [1] 高达 30Mbps
- 总线引脚 ESD 保护超过 12kV HBM
- 符合 ANSI 标准 TIA/EIA-485-A 和 ISO 8482:1987(E)
- 低偏斜
- 适用于嘈杂环境中的长距离总线线路上的多点传输
- 超低禁用电源电流要求：700 mA（最大值）
- -7V 至 12V 的共模电压范围
- 热关断保护
- 驱动器正负电流限制
- 开路失效防护接收器设计
- 接收器输入灵敏度：±200mV（最大值）
- 接收器输入迟滞：50mV（典型值）
- 无干扰上电和断电保护
- 可用于 Q 级温度汽车
  - 高可靠性汽车应用
  - 支持配置控制/打印
  - 通过汽车标准认证

2 说明

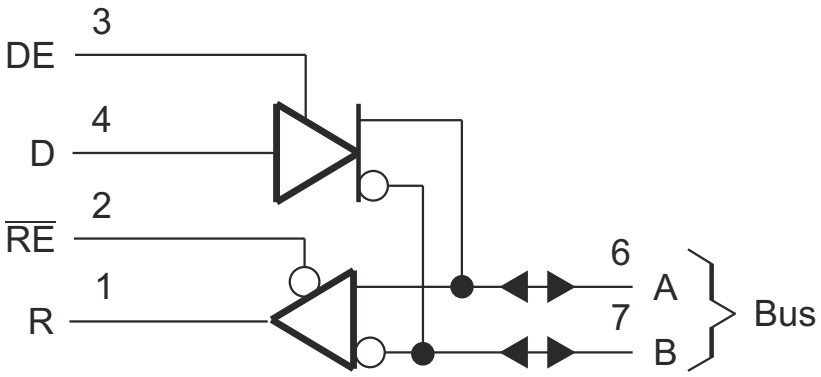
SN65LBC176A、SN65LBC176AQ 和 SN75LBC176A 差分总线收发器是单片集成电路，旨在用于多点总线传输线路上的双向数据通信。这些器件专为平衡传输线路而设计，符合 ANSI 标准 TIA/EIA-485-A 和 ISO 8482。与前代产品相比，A 版本可提供更高的开关性能，而不会显著降低功耗。

SN65LBC176A、SN65LBC176AQ 和 SN75LBC176A 整合了一个三态差分线路驱动器和一个差分输入线路接收器，两者均采用 5V 单电源供电。驱动器和接收器分别具有高电平有效和低电平有效使能端，它们可以在外部连接在一起以用作方向控制。驱动器差分输出端和接收器差分输入端在内部连接以形成差分输入/输出 (I/O) 总线端口，该端口用于在禁用驱动器或 V_{CC} = 0 时为总线提供最小负载。该端口具有较宽的正负共模电压范围，使得该器件适用于合用线应用。可以通过禁用驱动器和接收器来实现超低的器件待机电源电流。

封装信息

器件型号	封装(1)	封装尺寸（标称值）
SN65LBC176A SN75LBC176A	D (SOIC)	4.9 mm x 3.91 mm
	P (PDIP)	9.81mm x 6.35mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。



[1] TIA/EIA-485-A 定义规定的信号传输速率将转换时间限制在位持续时间的 30%，使用不同条件（请参阅“典型特性”部分）可以实现更高的信号传输速率。

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3 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision F (January 2023) to Revision G (February 2023) — **Page**

- Changed the *Thermal Information* table ... 5

Changes from Revision E (January 2023) to Revision F (January 2023) — **Page**

- Changed the SN65LBC176AQ values in the *Thermal Information* table ... 5

Changes from Revision D (August 200/8) to Revision E (January 2023) — **Page**

- 将文档更改为了最新 TI 格式 ... 1
- Added the *Thermal Information* table ... 5

4 Pin Configuration and Functions

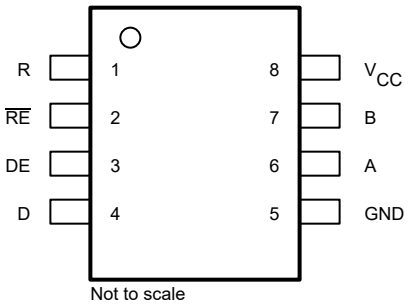


图 4-1. SN65LBC176AQD (Marked as B176AQ)
SN65LBC176AD (Marked as BL176A)
SN65LBC176AP (Marked as 65LBC176A)
SN75LBC176AD (Marked as LB176A)
SN75LBC176AP (Marked as 75LBC176A)
(Top View)

表 4-1. Pin Functions

NO	NAME	TYPE	DESCRIPTION
1	R	O	Receive data output
2	$\overline{RE}$	I	Receiver enable, active low
3	DE	I	Driver enable, active high
4	D	I	Driver data input
5	GND	GND	Device ground
6	A	I/O	Bus I/O port, A (complementary to B)
7	B	I/O	Bus I/O port, B(complementary to A)
8	V_{CC}	P	5 V Supply Pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
Supply voltage, V_{CC} (2)		–0.3 to 6	V
Voltage range at any bus terminal (A or B)		–10 to 15	V
Input voltage, V_I (D, DE, R, or $\overline{RE}$)		–0.3 to V_{CC} + 0.5	V
Electrostatic discharge:	Bus terminals and GND, Class 3, A: (3)	12	kV
	Bus terminals and GND, Class 3, B: (3)	400	V
	All terminals, Class 3, A	3	kV
	All terminals, Class 3, B	400	V
Continuous total power dissipation(4)		See Dissipation Rating Table	
Storage temperature range, T_{stg}		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.
(3) The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.
(4) Tested in accordance with MIL-STD-883C, Method 3015.7

5.2 Dissipation Ratings

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.5 mW/°C	464 mW	377 mW	145 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	—

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–7		12	V
V_{IH}	High-level input voltage	D, DE, and $\overline{RE}$	2		V_{CC}	V
V_{IL}	Low-level input voltage	D, DE, and $\overline{RE}$	0		0.8	V
V_{ID}	Differential input voltage(2)		–12(1)		12	V
I_{OH}	High-level output current	Driver	–60			mA
		Receiver	–8			
I_{OL}	Low-level output current	Driver			60	mA
		Reciever			8	
T_A	Operating free-air temperature	SN65LBC176AQ	–40		125	°C
		SN65LBC176A	–40		85	
		SN75LBC176A	0		70	

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.
(2) Differential input /output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

5.4 Thermal Information

THERMAL METRIC[1]		All Devices in 'P' Package	SN65LBC176ADR SN65LBC176AQDR	OPNs Not Listed in Previous Column	UNIT
		P (PDIP)	D (SOIC)	D (SOIC)	
		8-Pins	8-Pins	8-Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.7	116.7	110	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	54.7	56.3	44.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.1	63.4	53.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23	8.8	4.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	41.7	62.9	52.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Driver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA			–1.5	–0.8		V
$\lvert V_{OD} \rvert$	Differential output voltage	I_O = 0		SN65LBC176AQ	1.5	4	6	V
				SN65LBC176A, SN75LBC176A		4		
		R_L = 54 Ω,	See 图 6-1	SN65LBC176AQ	0.9	1.5	6	V
				SN65LBC176A	1	1.5	3	
				SN75LBC176A	1.1	1.5	3	
		V_{test} = –7 to 12 V,	See 图 6-2	SN65LBC176AQ	0.9	1.5	6	V
				SN65LBC176A	1	1.5	3	
				SN75LBC176A	1.1	1.5	3	
$\Delta \lvert V_{OD} \rvert$	Change in magnitude of differential output voltage	See 图 6-1 and 图 6-2			–0.2		0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See 图 6-1		SN65LBC176AQ	1.8	2.4	3	V
				SN65LBC176A, SN75LBC176A	1.8	2.4	2.8	
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage			SN65LBC176AQ	–0.2		0.2	V
				SN65LBC176A, SN75LBC176A	–0.1		0.1	
I_{OZ}	High-impedance output current	See receiver input currents						
I_{IH}	High-level enable input current	V_I = 2 V			–100			µA
I_{IL}	Low-level enable input current	V_I = 0.8 V			–100			µA
I_{OS}	Short-circuit output current	–7 V ≤ V_O ≤ 12 V			–250		250	mA
I_{CC}	Supply current	V_I = 0 or V_{CC}, No load	Receiver disabled and driver enabled			5	9	mA
			Receiver disabled and driver disabled			0.4	0.7	
			Receiver enabled and driver enabled			8.5	15	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

5.6 Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN65LBC176AQ			SN65LBC176A SN75LBC176A			UNIT
			MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 54 Ω, C_L = 50 pF, See 图 6-3	2		12	2	6	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output		2		12	2	6	12	ns
$t_{sk(p)}$	Pulse skew (| t_{PLH} – t_{PHL} |)				2		0.3	1	ns
t_r	Differential output signal rise time		1.2		11	4	7.5	11	ns
t_f	Differential output signal fall time		1.2		11	4	7.5	11	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	R_L = 110 Ω, See 图 6-4			22		12	22	ns
t_{PZL}	Propagation delay time, high-impedance-to-low- level output	R_L = 110 Ω, See 图 6-5			25		12	22	ns
t_{PHZ}	Propagation delay time, high-level-to-high- impedance output	R_L = 110 Ω, See 图 6-4			22		12	22	ns
t_{PLZ}	Propagation delay time, low-level-to-high- impedance output	R_L = 110 Ω, See 图 6-5			22		12	22	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

5.7 Receiver Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = – 8 mA					0.2	V
V_{IT-}	Negative-going input threshold voltage	I_O = 8 mA			– 0.2			V
V_{hys}	Hysteresis voltage (VIT + - VIT -)					50		mV
V_{IK}	Enable-input clamp voltage	II = - 18 mA			– 1.5	– 0.8		V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = – 8 mA,	See 图 6-6	4	4.9		V
V_{OL}	Low-level output voltage	V_{ID} = – 200 mV,	I_{OH} = 8 mA,	See 图 6-6		0.1	0.8	V
I_{OZ}	High-impedance-state output current	V_O = 0 to V_{CC}		SN65LBC176AQ	– 10		10	μA
				SN65LBC176A, SN75LBC176A	– 1		1	
I_I	Bus input current	V_{IH} = 12 V,	V_{CC} = 5 V	Other input at 0 V		0.4	1	mA
		V_{IH} = 12 V,	V_{CC} = 0			0.5	1	
		V_{IH} = – 7 V,	V_{CC} = 5 V		– 0.8	– 0.4		
		V_{IH} = – 7 V,	V_{CC} = 0		– 0.8	– 0.3		
I_{IH}	High-level enable-input current	V_{IH} = 2 V			– 100			μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.8 V			– 100			μA
I_{CC}	Supply current	V_I = 0 or V_{CC}, No load	Receiver enabled and driver disabled			4	7	mA
			Receiver disabled and driver disabled			0.4	0.7	
			Receiver enabled and driver enabled			8.5	15	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

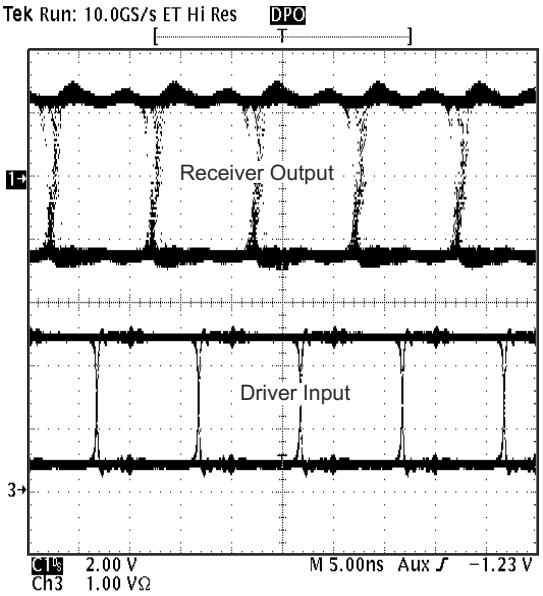
5.8 Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN65LBC176AQ			SN65LBC176A SN75LBC176A			UNIT
			MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
t_{PLH}	Propagation delay time output ↑	V_{ID} = –1.5 V to 1.5 V, See 图 6-7	7		30	7	13	20	ns
t_{PHL}	Propagation delay time output ↓		7		30	7	13	20	ns
$t_{sk(p)}$	Pulse skew (| t_{PLH} – t_{PHL} |)				6		0.5	1.5	ns
t_r	Rise time, output	See 图 6-7			5		2.1	3.3	ns
t_f	Fall time, output				5		2.1	3.3	ns
t_{PZH}	Output enable time to high level	C_L = 10 pF, See 图 6-8			50		30	45	ns
t_{PZL}	Output enable time to low level				50		30	45	ns
t_{PHZ}	Output disable time to high level				60		20	40	ns
t_{PLZ}	Output disable time to low level				60		20	40	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

Typical Characteristics



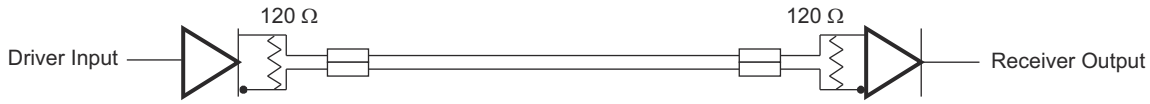


图 5-1. Typical Waveform of Non-Return-To-Zero (NRZ), Pseudorandom Binary Sequence (PRBS) Data at 100 Mbps Through 15m, of CAT 5 Unshielded Twisted Pair (UTP) Cable

TIA/EIA-485-A defines a maximum signaling rate as that in which the transition time of the voltage transition of a logic-state change remains less than or equal to 30% of the bit length. Transition times of greater length perform quite well even though they do not meet the standard definition.

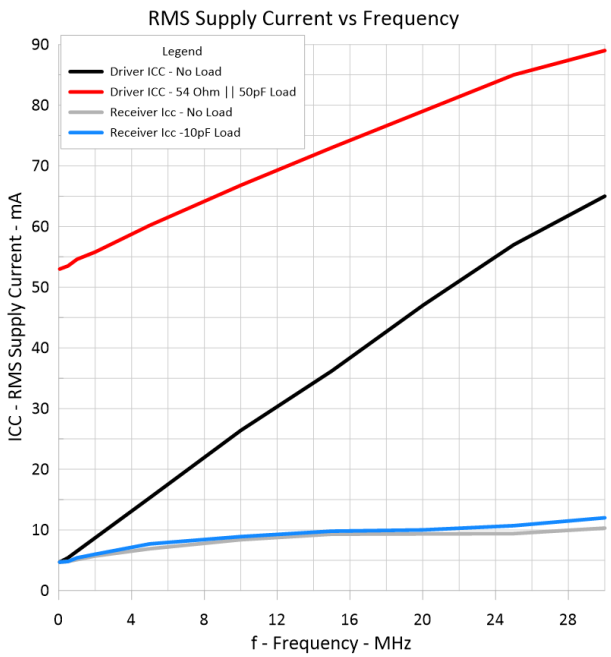


图 5-2. RMS Supply Current vs Frequency

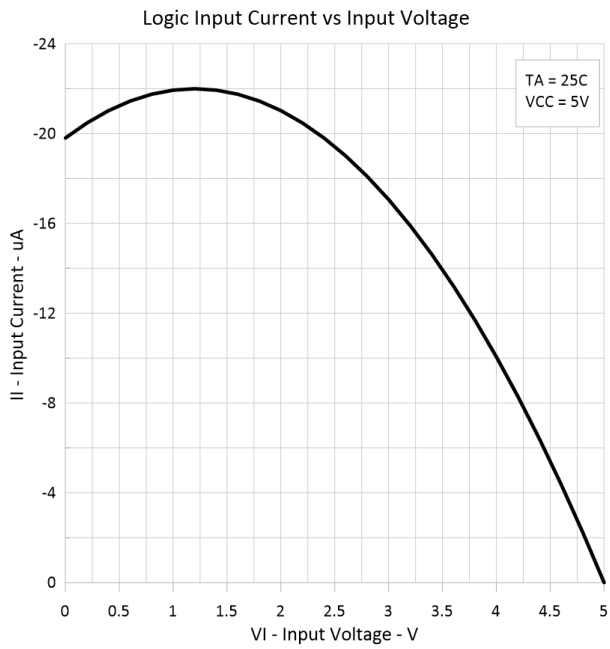


图 5-3. Logic Input Current vs Input Voltage

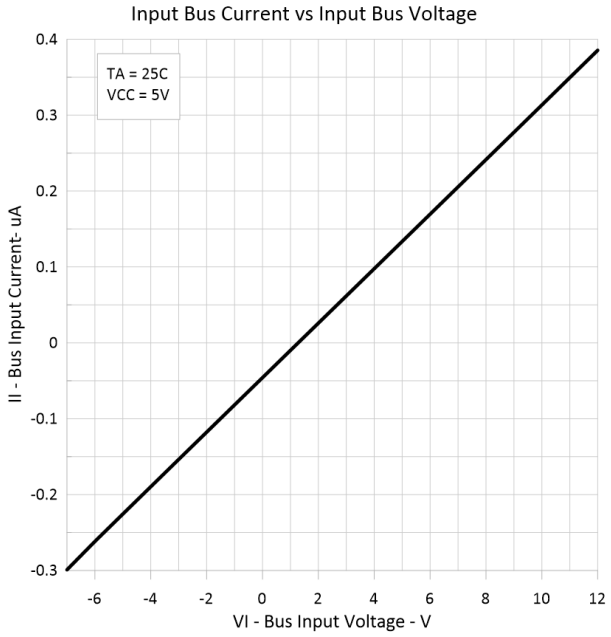


图 5-4. Input Current vs Input Voltage

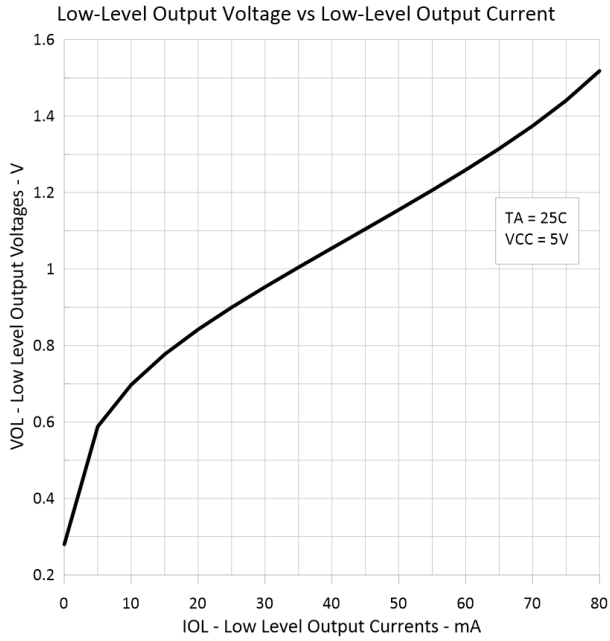


图 5-5. Low-Level Output Voltage vs Low-Level Output Current

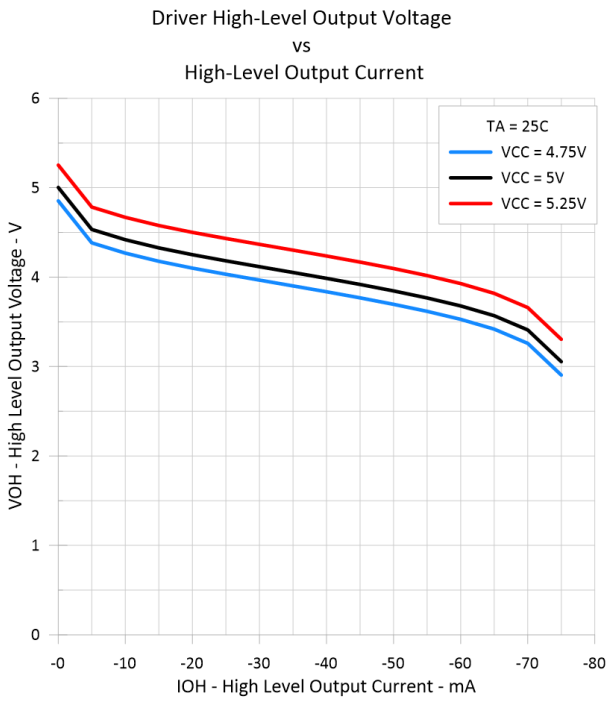


图 5-6. Driver High-Level Output Voltage vs High-Level Output Current

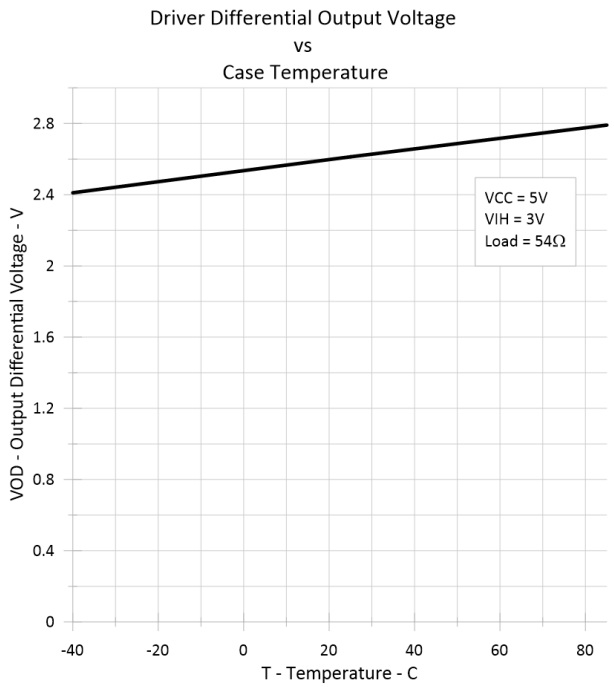


图 5-7. Driver Differential Output Voltage vs Case Temperature

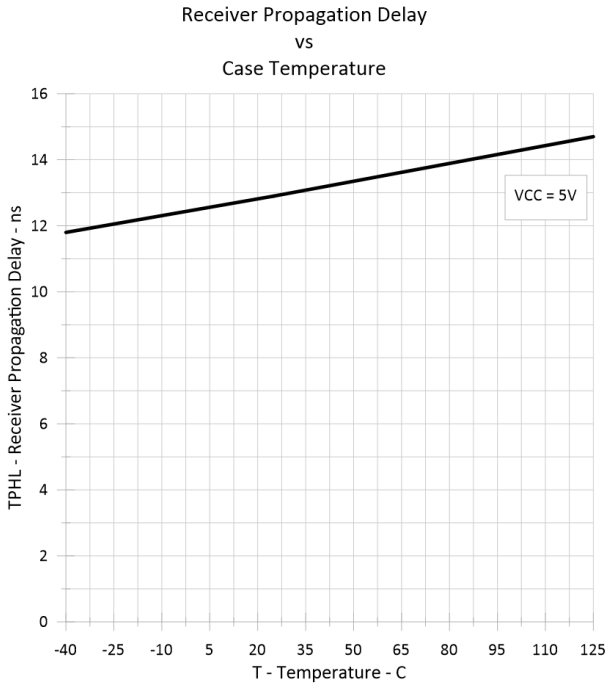


图 5-8. Receiver Propagation Time vs Case Temperature

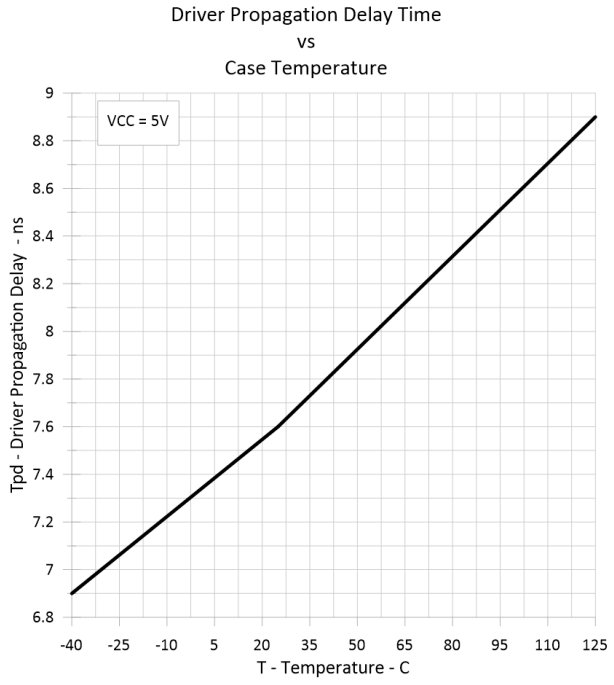


图 5-9. Driver Propagation Delay Time vs Case Temperature

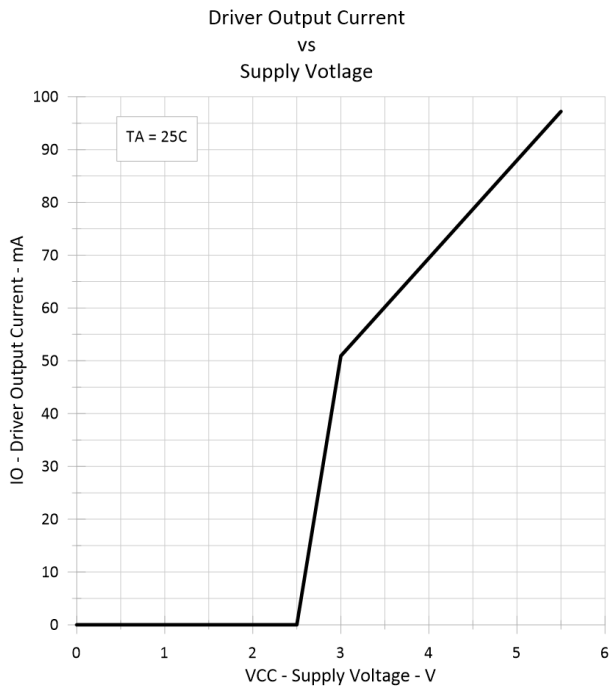


图 5-10. Driver Output Current vs Supply Voltage

参数测量信息

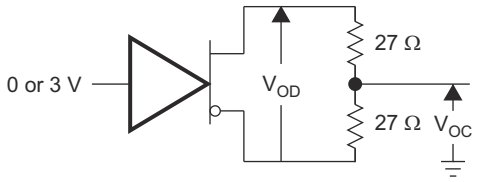


图 6-1. 驱动器 V_{OD} 和 V_{OC}

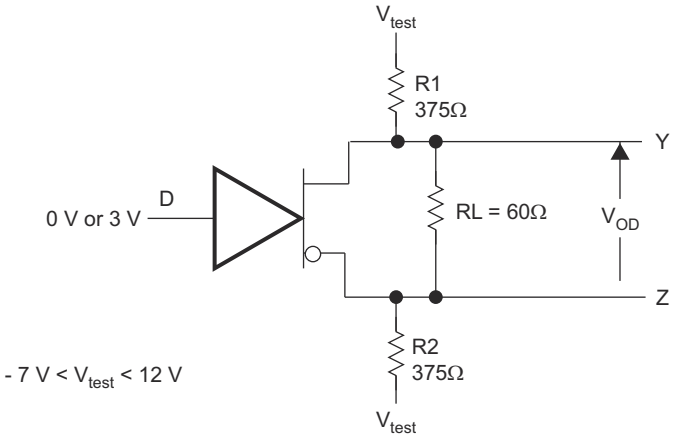
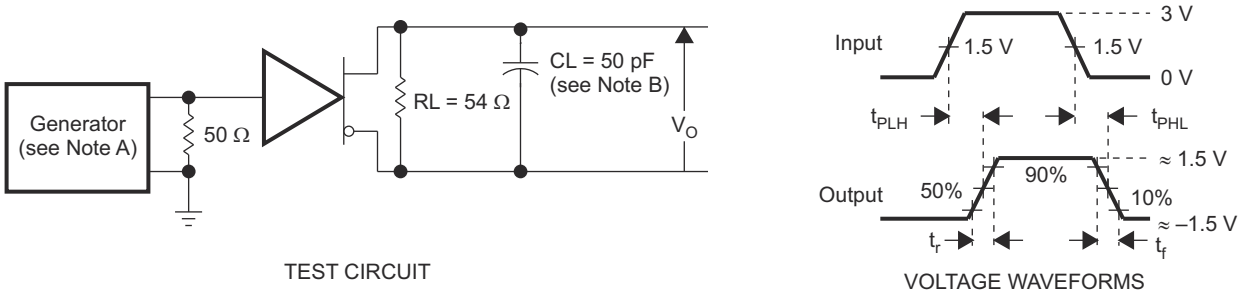


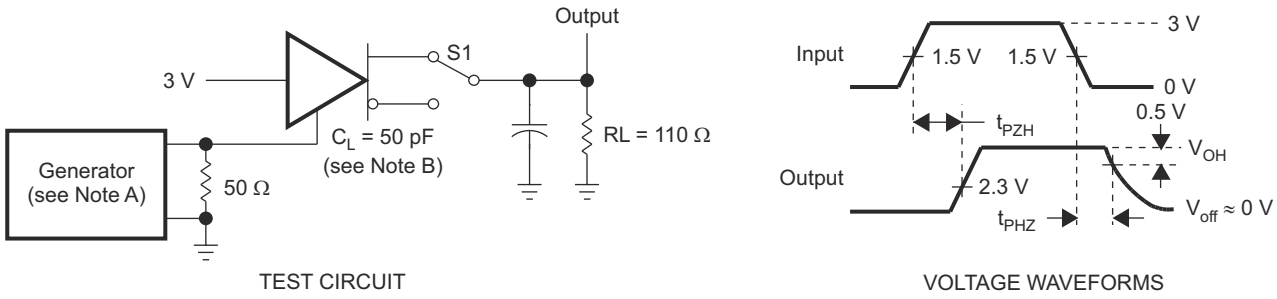
图 6-2. 驱动器 V_{OD3}



A. 输入脉冲由具有以下特性的发生器提供：PRR ≤ 1MHz，50% 占空比，t_r ≤ 6ns，t_f ≤ 6ns，Z_O = 50Ω。

B. C_L 包括探头和夹具电容。

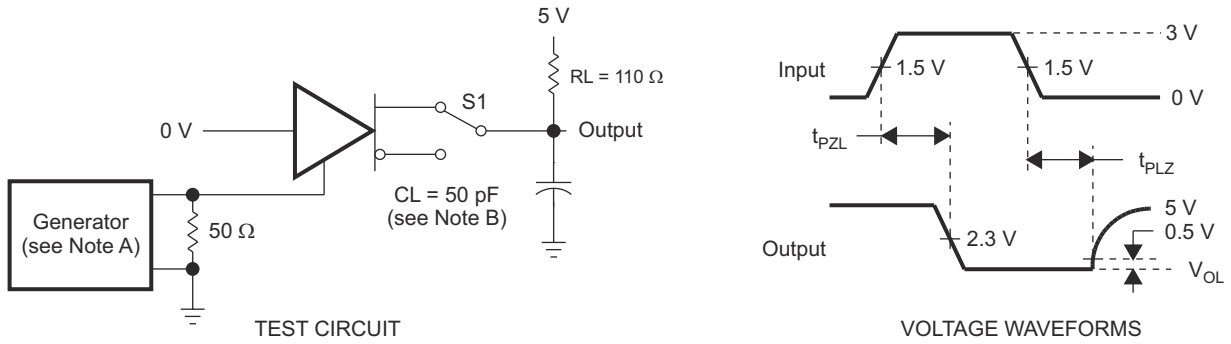
图 6-3. 驱动器测试电路和电压波形



A. 输入脉冲由具有以下特性的发生器提供：PRR ≤ 1MHz，50% 占空比，t_r ≤ 6ns，t_f ≤ 6ns，Z_O = 50Ω。

B. C_L 包括探头和夹具电容。

图 6-4. 驱动器测试电路和电压波形



A. 输入脉冲由具有以下特性的发生器提供：PRR ≤ 1MHz，50% 占空比，t_r ≤ 6ns，t_f ≤ 6ns，Z_O = 50Ω。

B. C_L 包括探头和夹具电容。

图 6-5. 驱动器测试电路和电压波形

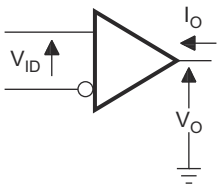
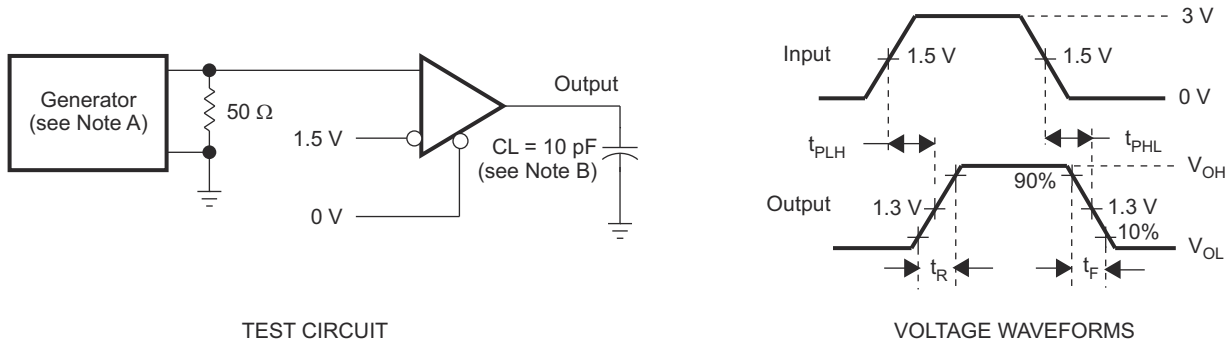


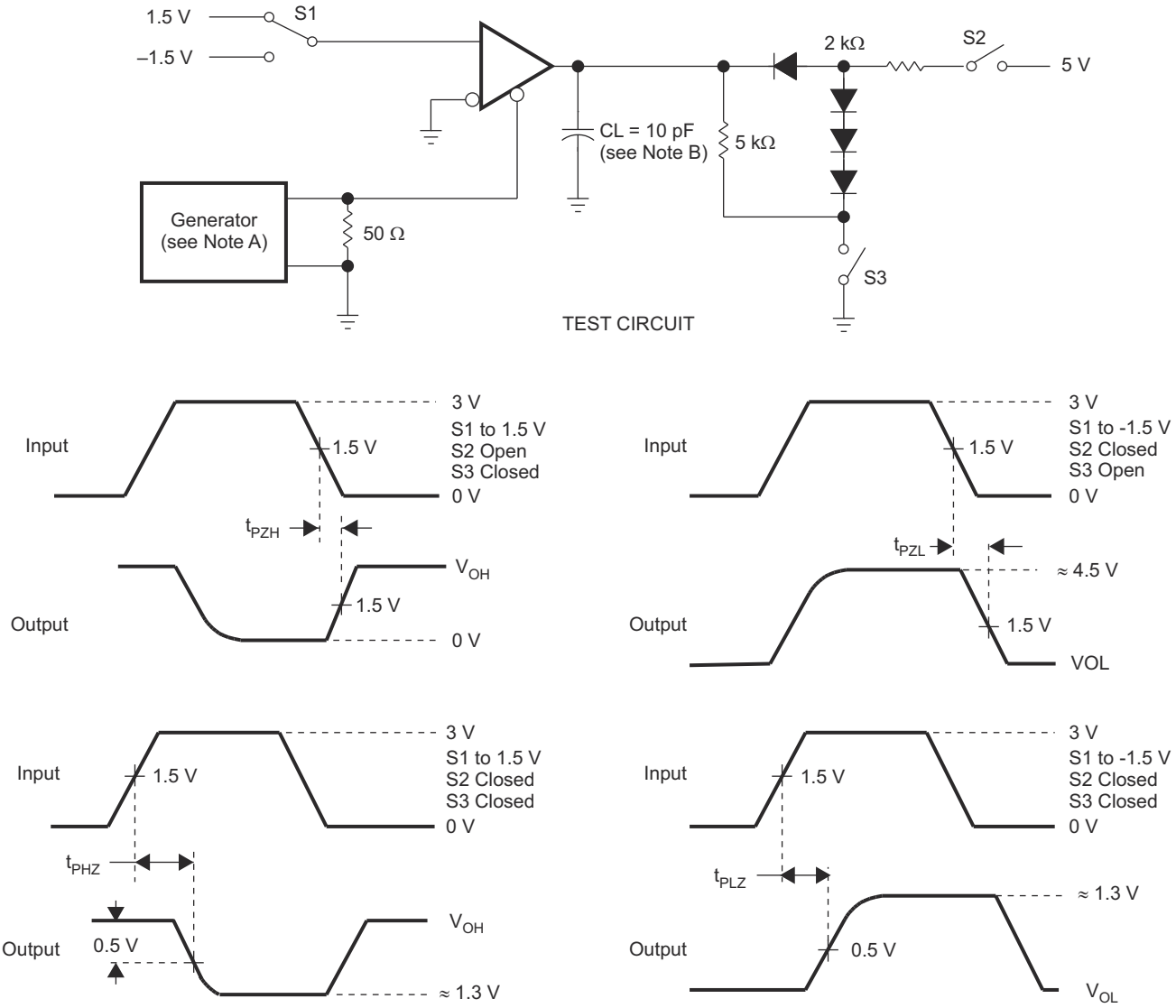
图 6-6. 接收器 V_{OH} 和 V_{OL}



A. 输入脉冲由具有以下特性的发生器提供：PRR ≤ 1MHz，50% 占空比，t_r ≤ 6ns，t_f ≤ 6ns，Z_O = 50Ω。

B. C_L 包括探头和夹具电容。

图 6-7. 接收器测试电路和电压波形



VOLTAGE WAVEFORMS

A. 输入脉冲由具有以下特性的发生器提供：PRR ≤ 1MHz，50% 占空比，t_r ≤ 6ns，t_f ≤ 6ns，Z_O = 50Ω。

B. C_L 包括探头和夹具电容。

图 6-8. 接收器测试电路和电压波形

6 Detailed Description

6.1 Device Functional Modes

6.1.1 Function Tables

DRIVER			
INPUT D	**ENABLE DE**	**OUTPUTS**	
		A	**B**
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L

RECEIVER			
DIFFERENTIAL INPUTS $V_A - V_B$		**ENABLE $\overline{RE}$**[1]	**OUTPUT R**[1]
$V_{ID} \geq 0.2$ V		L	H
-0.2 V < V_{ID} < 0.2 V		L	?
$V_{ID} \leq -0.2$ V		L	L
X		H	Z
Open		L	H

(1) H = high level, L - low level, ? = indeterminate, X = Irrelevant, Z = high impedance (off)

6.1.2 Schematics

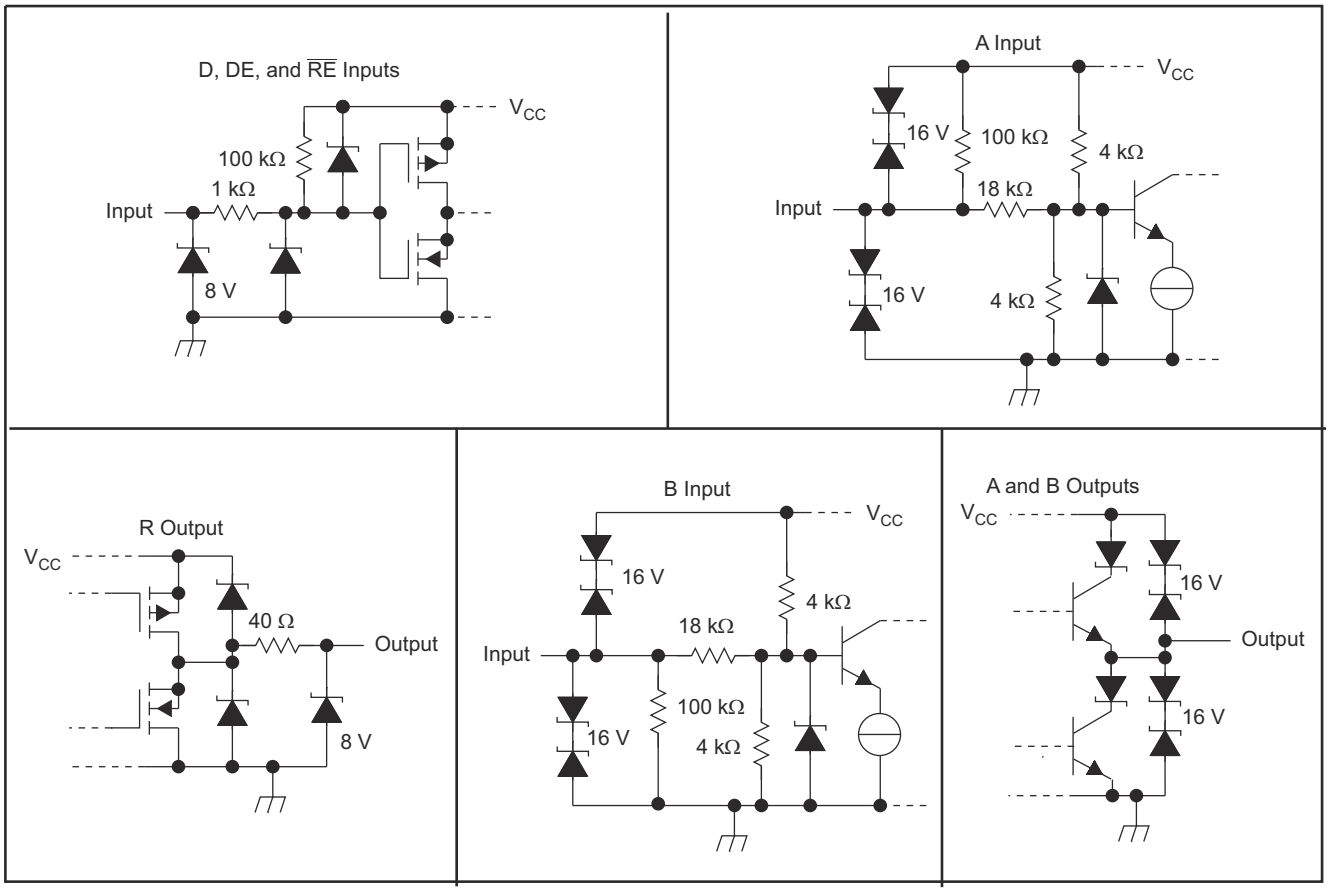


图 6-1. Schematics of Inputs and Outputs

7 Device and Documentation Support

7.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

7.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

7.3 商标

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7.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC176AD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL176A	
SN65LBC176ADR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL176A	Samples
SN65LBC176AP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	65LBC176A	Samples
SN65LBC176AQD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B176AQ	Samples
SN65LBC176AQDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		B176AQ	Samples
SN65LBC176AQDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B176AQ	Samples
SN65LBC176AQDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		B176AQ	Samples
SN75LBC176AD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LB176A	
SN75LBC176ADG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LB176A	
SN75LBC176ADR	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LB176A	
SN75LBC176ADRG4	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LB176A	
SN75LBC176AP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	75LBC176A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN65LBC176A :

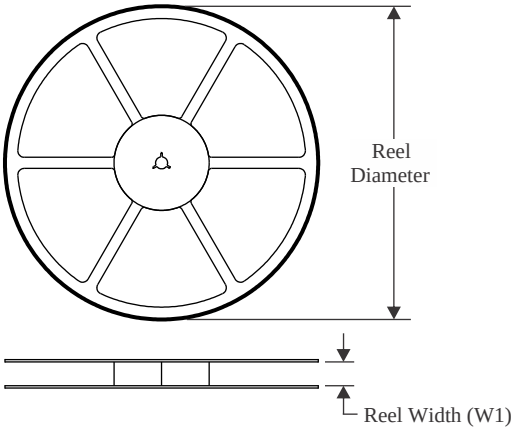
- Enhanced Product : SN65LBC176A-EP

NOTE: Qualified Version Definitions:

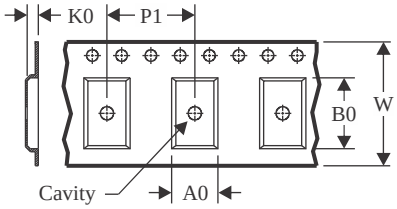
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

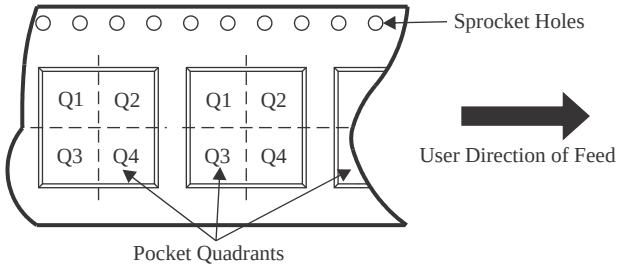


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

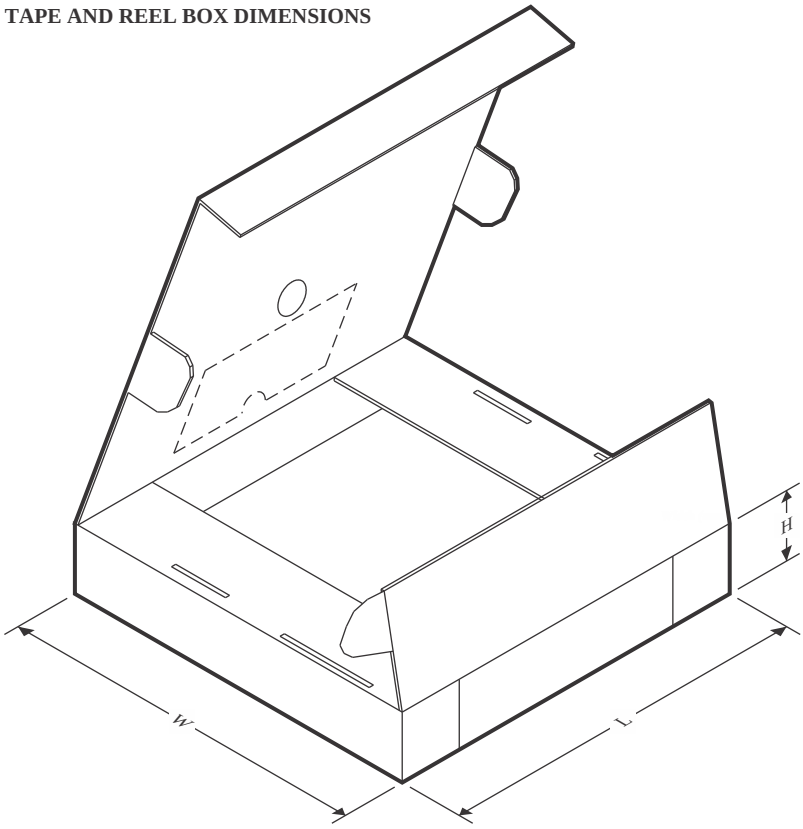
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC176ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LBC176AQDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75LBC176ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

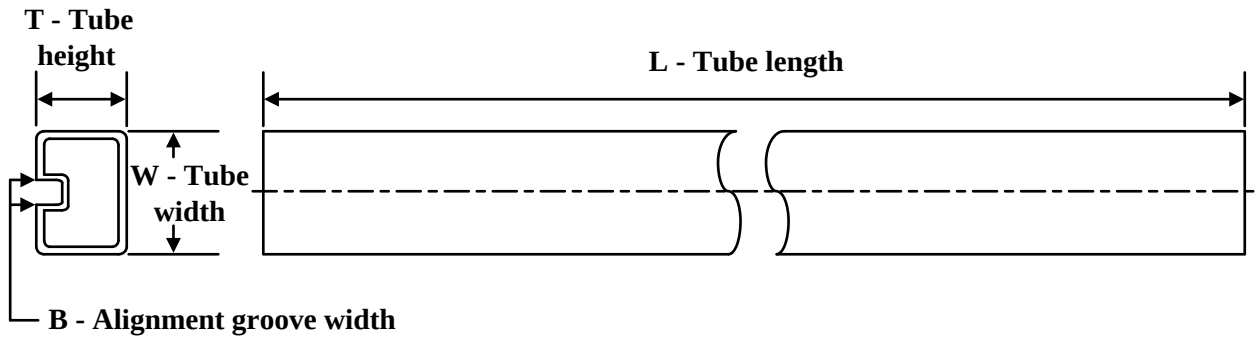
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

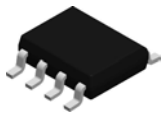
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC176ADR	SOIC	D	8	2500	340.5	336.1	25.0
SN65LBC176AQDR	SOIC	D	8	2500	340.5	336.1	25.0
SN75LBC176ADR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LBC176AD	D	SOIC	8	75	507	8	3940	4.32
SN65LBC176AP	P	PDIP	8	50	506	13.97	11230	4.32
SN65LBC176AQD	D	SOIC	8	75	505.46	6.76	3810	4
SN65LBC176AQDG4	D	SOIC	8	75	505.46	6.76	3810	4
SN75LBC176AD	D	SOIC	8	75	507	8	3940	4.32
SN75LBC176ADG4	D	SOIC	8	75	507	8	3940	4.32
SN75LBC176AP	P	PDIP	8	50	506	13.97	11230	4.32

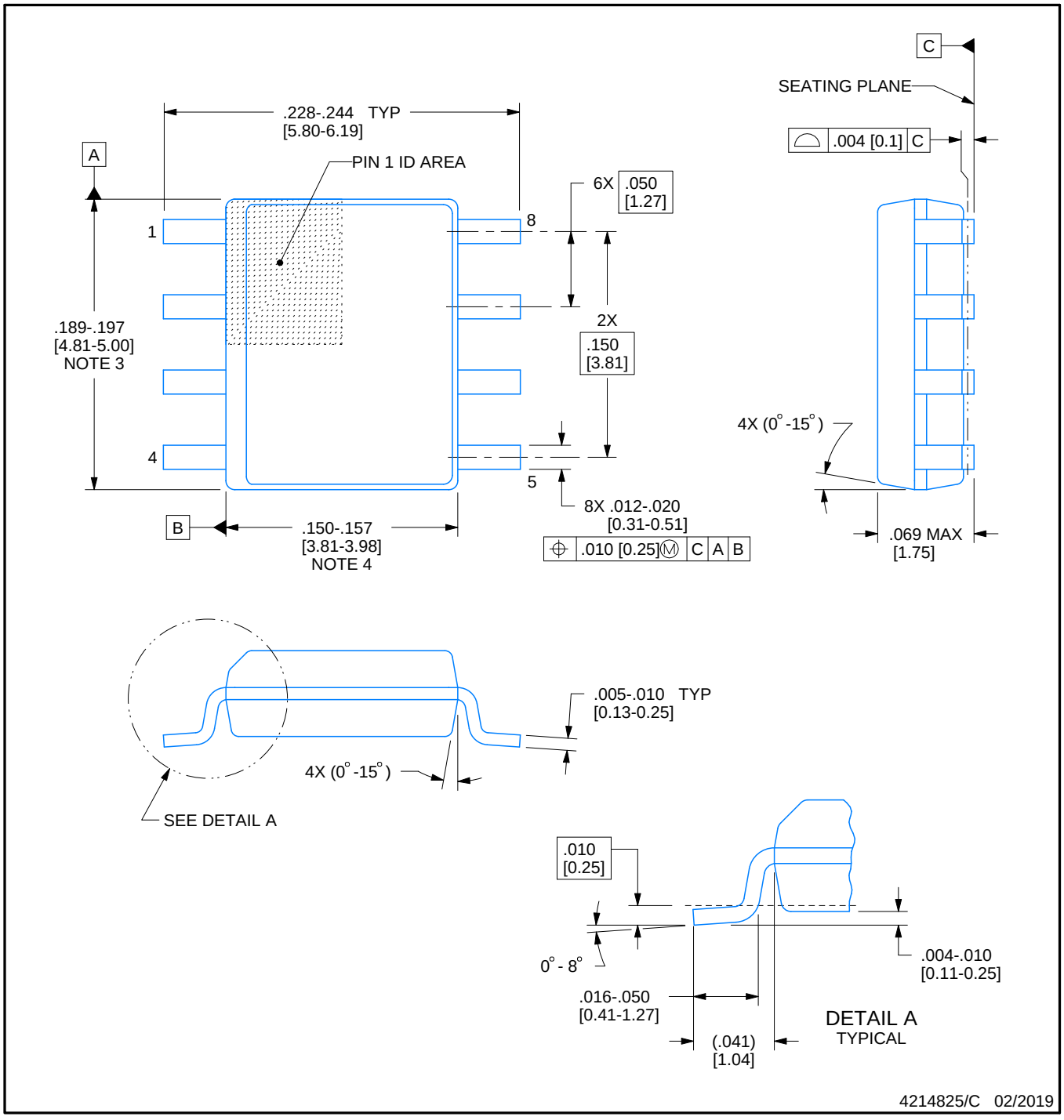


PACKAGE OUTLINE

D0008A

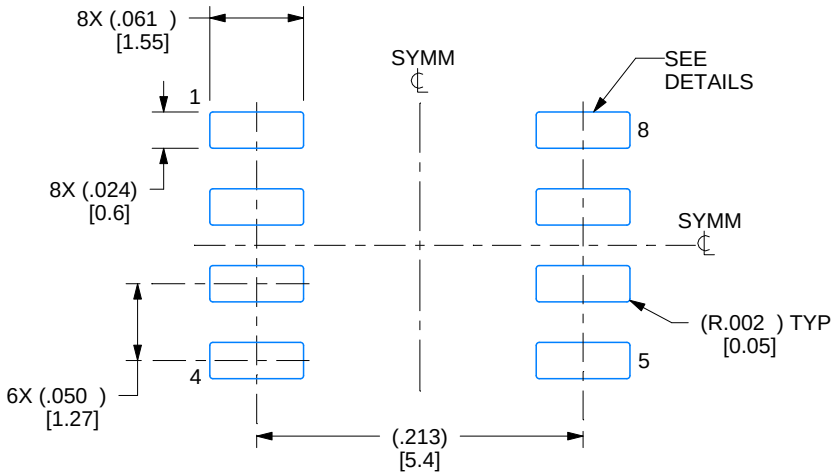
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

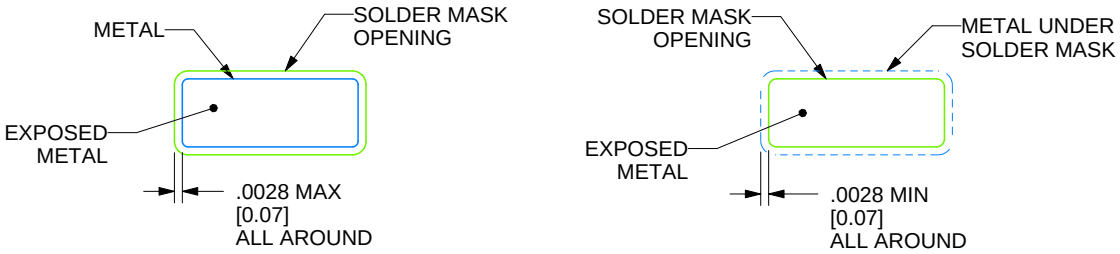


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

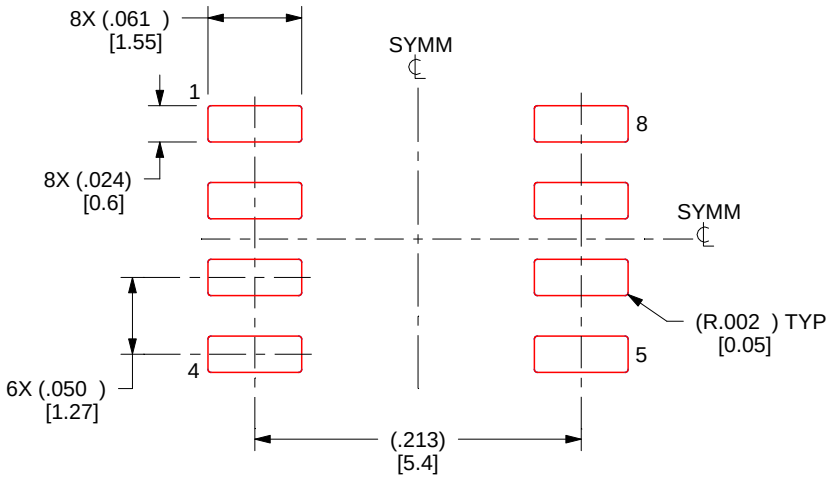
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



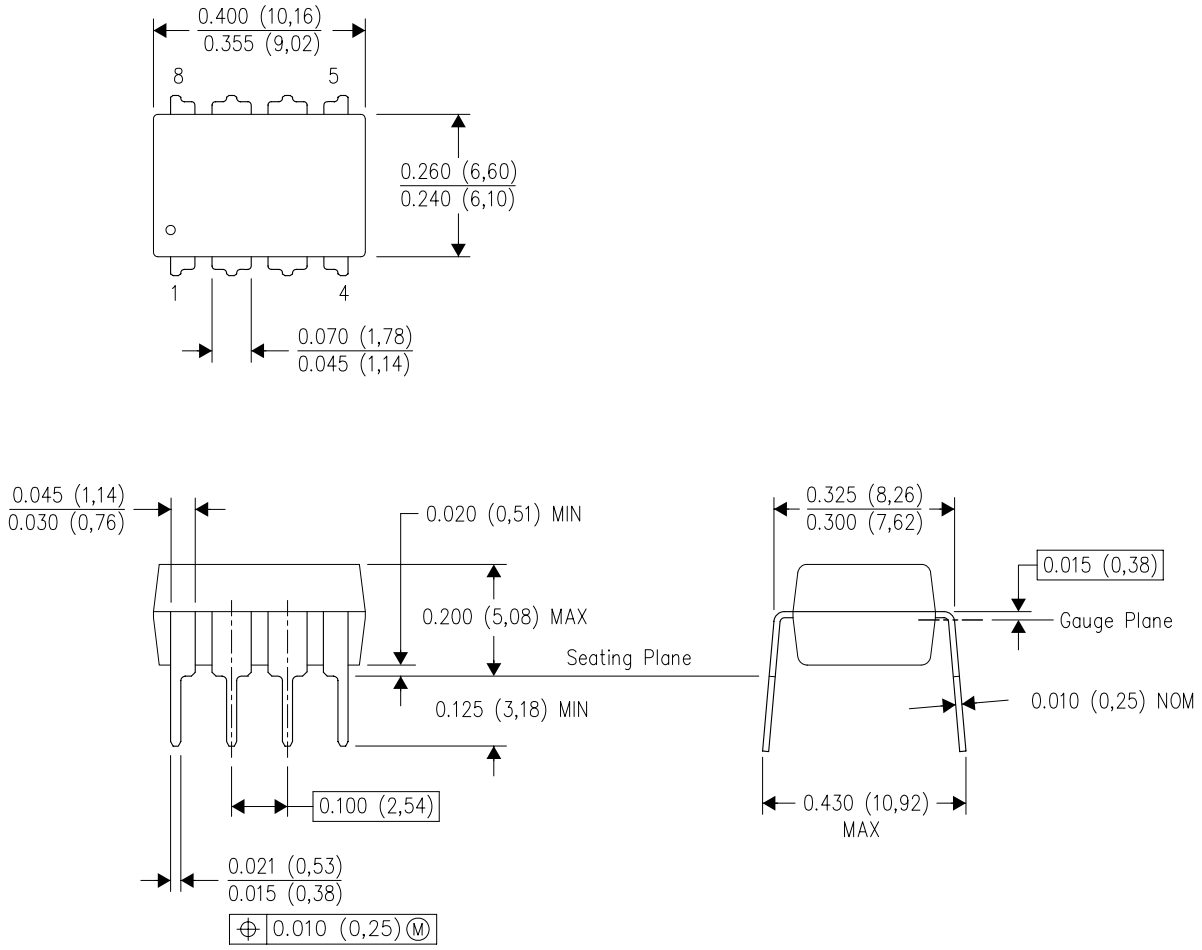
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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