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BCM8021 PRODUCT Brief



10-GbE XAUI™ TRANSCEIVER WITH HIGH-SPEED REDUNDANCY

FEATURES

- **10-GbE transceiver supporting various operating modes**
  - IEEE 802.3™ae-compliant XAUI™ to XGMII transceiver
  - XAUI-to-XAUI retiming
- **Low power dissipation**
  - Less than 300 mW per transceiver channel including I/O
- **SONET/SDH-quality jitter performance**
  - Less than three picoseconds rms jitter generation
  - Exceeds SONET jitter tolerance mask
- **High performance programmable receive equalization and transmit pre-emphasis**
  - Transmit pre-emphasis for interoperability with CML SerDes
  - Receive equalization for copper interconnects
- **Enhanced test capability**
  - Full loopback and on-chip PRBS generator/checker
  - IEEE (1149.1) JTAG
- **Compact 21-mm × 21-mm BGA package**
  - No requirement for heat sink or airflow

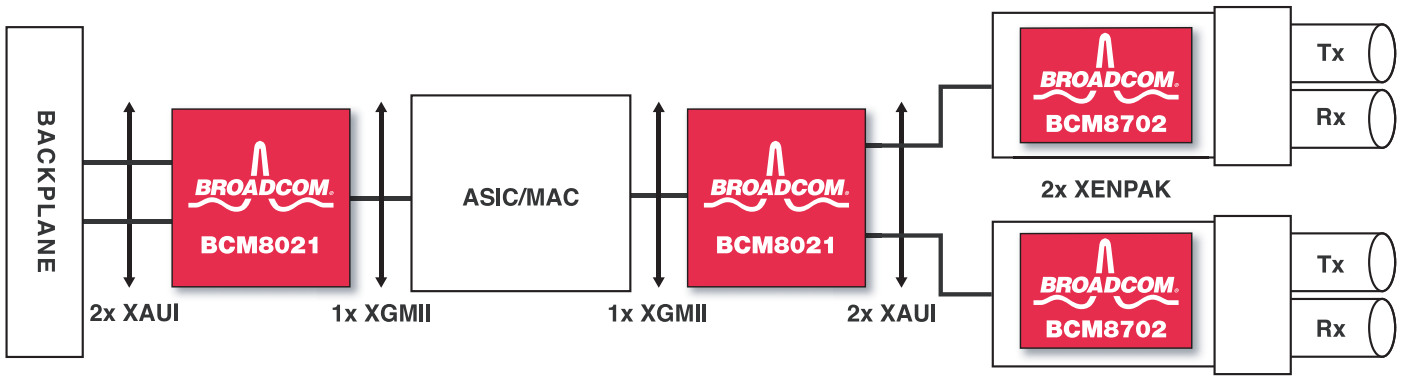
SUMMARY OF BENEFITS

- **Advanced 0.13µ CMOS process technology provides unparalleled performance while achieving the lowest possible power consumption**
- **IEEE 802.3ae 10-GbE physical coding sublayer (PCS) has a selectable 8B/10B encoding/decoding block on-chip that can be configured to support the 10-Gbps attachment unit interface (XAUI)**
- **Superior jitter characteristics enable the serializing/deserializing (SerDes) of data signals transmitted through front panel or backplane networking equipment supporting both primary and protection circuits**
- **Drive PMD devices or backplane directly with no external clean-up circuit required**
- **Simplifies manufacturability with integrated built-in self-test (BIST), high-speed and low-speed loopbacks, and programmable PRBS generator/checker**
- **Decreases complexity and reduces board space on multichannel linecard designs**

APPLICATIONS

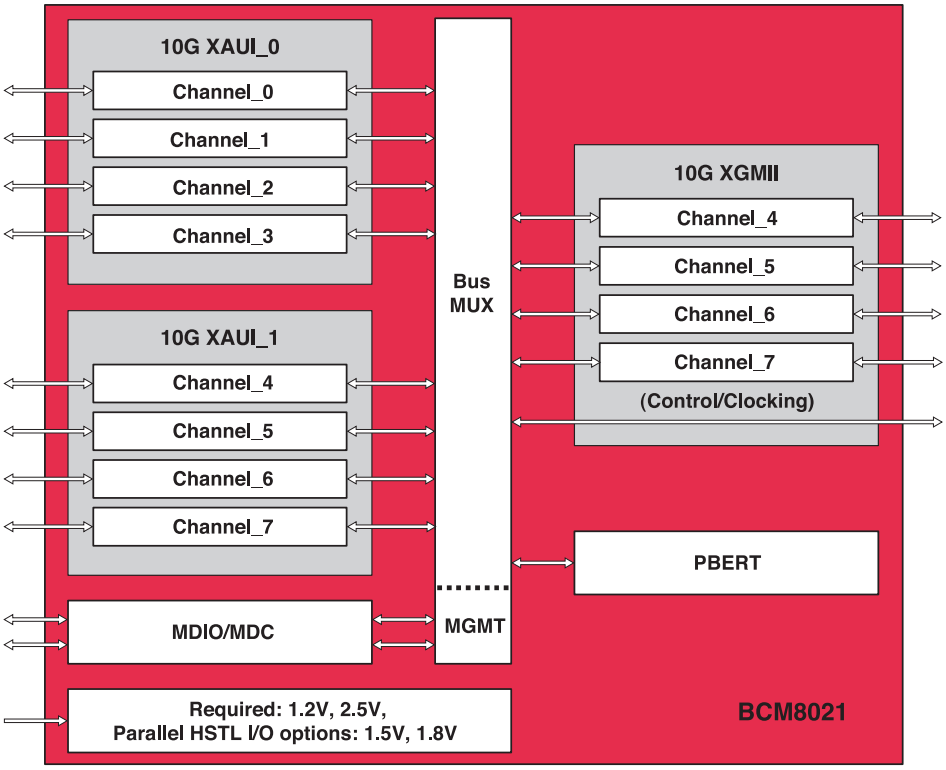
- **1-GbE and 10-GbE LAN, MAN, WAN switches and routers**
- **Advanced test equipment (ATE)**

XAUI SerDes Application Diagram



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OVERVIEW



BCM8021 Block Diagram

The BCM8021 device integrates XAUI serializer/deserializer (SerDes) channels leveraging Broadcom's high-performance mixed-signal design experience along with advanced 0.13µ CMOS process technology. This, combined this with a robust architecture offering the highest degree of flexibility, results is a highly programmable, lowest power SerDes solution for network line-card and backplane applications.

An internal MUX connects the parallel and serial ports to enable fully redundant operation. The MUX enables an active serial link to be switched to the parallel interface, while a protection serial link can be continuously monitored to insure its condition. If the active link fails, the protection link can be muxed over through external control to the parallel interface.

On the parallel side of the device, transmitters and receivers interface with a 32-bit wide data (XGMII) along with the clock and control signals. The low-speed I/O supports HSTL (1.5V or 1.8V) or SSTL_2 (2.5V) interfaces.

On the serial side of the device, transmitters and receivers support XAUI serial transmission rates. An on-chip phase lock loop (PLL) synthesizes the supplied reference clock to support the desired transmit rate, while vlock and data recovery (CDR) units recover the receive rate clock for timing.

For high-speed serial copper connections, the device incorporates both transmit pre-emphasis on the transmit channels and receive equalization on the receive channels. Transmit pre-emphasis is programmable to improve the overall cable reach and compensate for electrical imperfections associated with traces and connectors. Receive equalization provides optimal performance over a variety of receive interfaces.

Highly programmable test capabilities exist within the device to support high-speed and low-speed loopback using generators/checkers that support PRBS 27 to 231 patterns along with IEEE802.3ae-defined test patterns. A complete evaluation kit, including an evaluation board, related software, and documentation is available upon request.

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