PAM8006

10W Stereo Class-D Audio Power Amplifier

Key Features

- 10W@10%THD / Channel Output into a 8Ω Load at 13V
- Power Supply Range: 7.5V to 18V
- Low SNR: 95dB
- Over 90% Efficiency
- With Shutdown/Mute Function
- Over Current , Thermal, Short-Circuit Protection and UVLO
- Low THD+N
- Low Quiescent Current
- Pop noise suppression
- Small Package Outlines: Thin 32-pin QFN 5mm*5mm and TSSOP-28PP Package
- RoHS Pass and Green Package

General Description

The PAM8006 is a 10W (per channel) stereo class-D audio amplifier with fixed gain which offers low THD+N, low EMI, and good PSRR thus high-quality sound reproduction.

The PAM8006 runs off from a 7.5V to 18V supply at much higher efficiency than competitors' ICs.

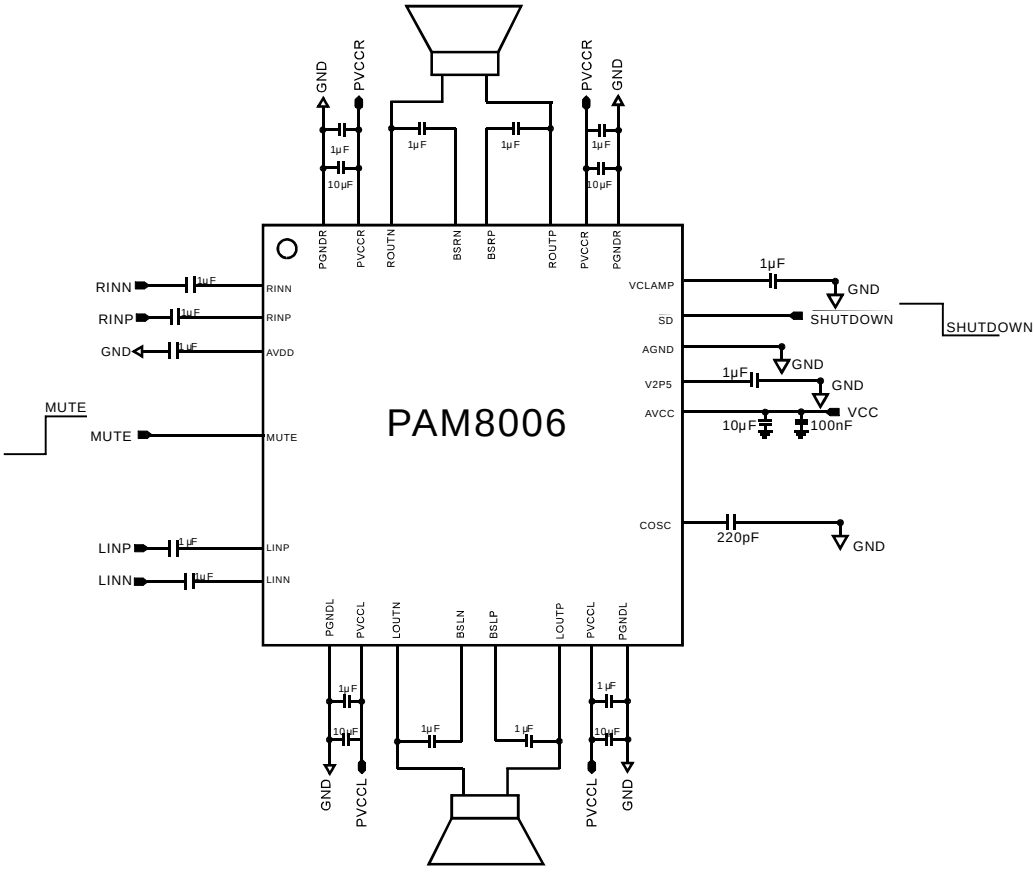
The PAM8006 only requires very few external components, significantly saving cost and board space.

The PAM8006 is available in a 32pin QFN 5mm*5mm and TSSOP-28PP package.

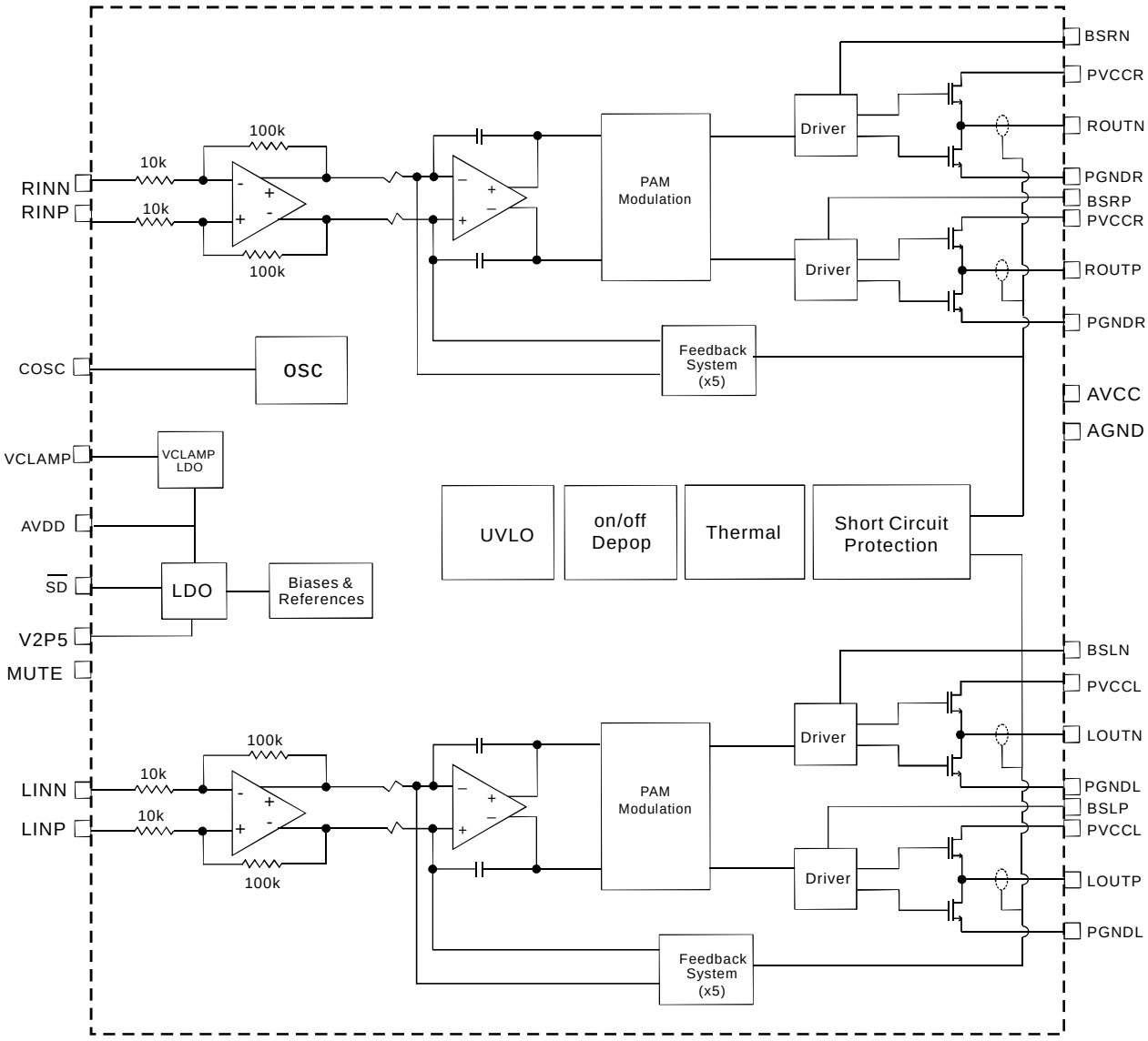
Applications

- Flat Monitor /LCD TVs
- Multi-media Speaker System
- DVD players, Game machines
- Boom Box
- Music instruments

Typical Application

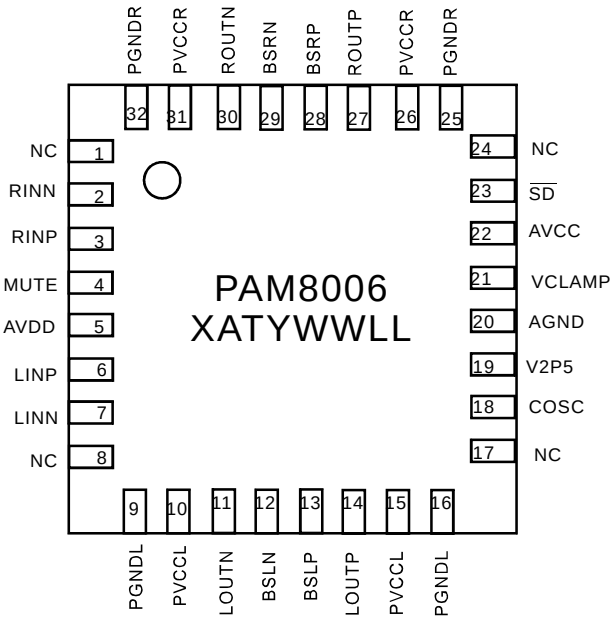


Block Diagram



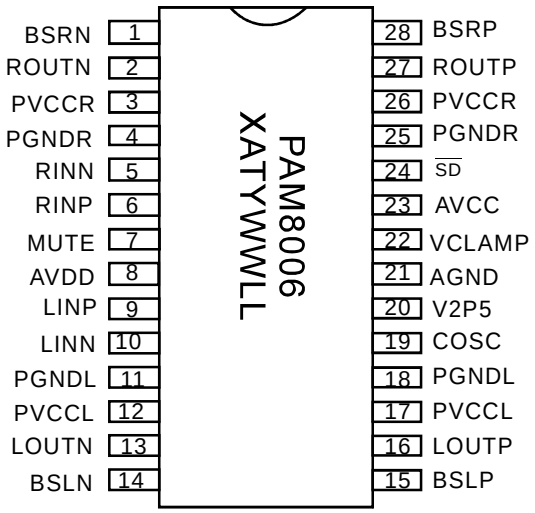
Pin Configuration & Marking Information

Top View
5mm*5mm QFN



X: Internal Code
A: Assembly Code
T: Testing Code
Y: Year
WW: Week
LL: Internal Code

Top View
TSSOP-28PP (Exposed Pad)



Pin Descriptions

QFN5X5	TSSOP-28	Name	Function
2	5	RINN	Negative differential audio input for right channel
3	6	RINP	Positive differential audio input for right channel
1,8,17,24	-	NC	No Connected
5	8	AVDD	5V Analog VDD
4	7	MUTE	A logic high on this pin disables the outputs and a logic low enables the outputs.
6	9	LINP	Positive differential audio input for left channel
7	10	LINN	Negative differential audio input for left channel
9,16	11,18	PGNDL	Power ground for left channel H-bridge
10,15	12,17	PVCCL	Power supply for left channel H-bridge, not connected to PVCCR or AVCC.
11	13	LOUTN	Class-D 1/2-H-bridge negative output for left channel
12	14	BSLN	Bootstrap I/O for left channel, negative high-side FET
13	15	BSLP	Bootstrap I/O for left channel, positive high-side FET
14	16	LOUTP	Class-D 1/2-H-bridge positive output for left channel
18	19	COSC	I/O for charge/discharging currents onto capacitor for ramp generator triangle wave biased at V2P5
22	23	AVCC	High-voltage analog power supply (7.5V to 18V)
19	20	V2P5	2.5V Reference for analog cells, as well as reference for unused audio input when using single-ended inputs.
20	21	AGND	Analog GND
23	24	$\overline{SD}$	Shutdown signal for IC (low= shutdown, high =operational). TTL logic levels with compliance to VCC.
21	22	VCLAMP	Internally generated voltage supply bootstrap capacitors.
25,32	4,25	PGNDR	Power ground for right channel H-bridge
26,31	3,26	PVCCR	Power supply for right channel H-bridge, not connected to PVCCL or AVCC.
27	27	ROUTP	Class-D 1/2-H-bridge positive output for right channel
28	28	BSRP	Bootstrap I/O for right channel, positive high-side FET
29	1	BSRN	Bootstrap I/O for right channel, negative high-side FET
30	2	ROUTN	Class-D 1/2-H-bridge negative output for right channel

Absolute Maximum Ratings

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

Supply Voltage V_{CC}.....-0.3V to 20V
Input Pin Voltage Range V_I:
$\overline{MUTE}$.....0V to 6.0V
$\overline{SD}$.....-0.3V to V_{CC}
RINN,RINP,LINN,LINP.....-0.3V to 6.0V
Junction Temperature Range,T_J.....-40°C to 150°C
Storage Temperature.....-65°C to150°C
Lead Temperature1,6mm(1/16 inch) from case for 5 seconds.....260°C

Recommended Operating Conditions

Supply Voltage (V_{CC}).....7.5V to 18V
Maximum Volume Control Pins, Input Pins Voltage.....0V to 5.0V
High Level Input Voltage: $\overline{SD}$.....2.0V to V_{CC}
MUTE, ...2.0V to 5V
Low Level Input Voltage: $\overline{SD}$.....0 to 0.3V
MUTE.....0 to 0.3V
Ambient Operating Temperature.....-20°C to 85°C
Junction Temperature Range,T_J.....-40°C to 125°C

Thermal Information

Parameter	Package	Symbol	Maximum	Unit
Thermal Resistance (Junction to Case)	QFN 5mm*5mm	θ_{JC}	7.6	°C/W
	TSSOP-28PP	θ_{JC}	14.4	
Thermal Resistance (Junction to Ambient)	QFN 5mm*5mm	θ_{JA}	18.1	
	TSSOP-28PP	θ_{JA}	27.8	
Internal Power Dissipation (T_A=25°C)	QFN 5mm*5mm	P_D	5.52	W
	TSSOP-28PP	P_D	3.60	

The Exposed PAD must be soldered to a thermal land on the PCB.

Electrical Characteristic

T_A=25°C, V_{CC}=12V,Gv=24dB,R_L=8Ω (unless otherwise noted)

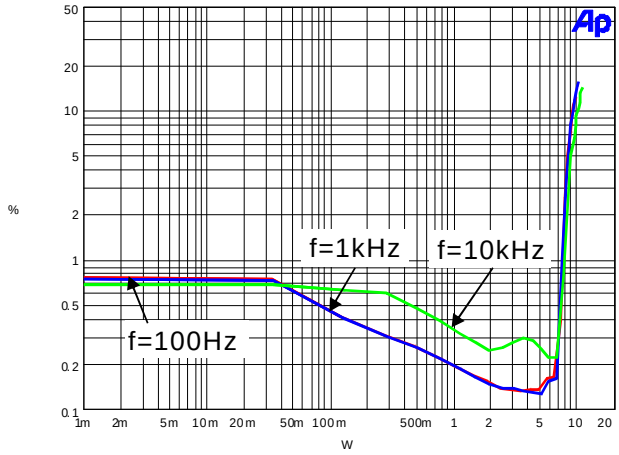
Parameter	Symbol	condition		MIN	TYP	MAX	Units
Supply Voltage	V_{CC}			7.5	12	18	V
Continuous Output Power	Po	THD+N=0.1%,f=1kHz,R_L=8Ω			5		W
		THD+N=1.0%,f=1kHz,R_L=8Ω			8		
		THD+N=10%,f=1kHz,R_L=8Ω, V_{CC}=13V			10		
		THD+N=10%,f=1kHz,R_L=4Ω (Note)			15		
Total Harmonic Distortion plus Noise	THD+N	P_O=5W, f=1kHz, R_L =8Ω			0.1		%
Quiescent Current	I_{CC}	(no load)			20	30	mA
Supply Quiescent Current in shutdown mode	I_{SD}	SHUTDOWN=0V			4	10	μA
Drain-source on-state resistance	$r_{ds(on)}$	V_{CC}=12V I_O=1A T_A=25℃	High side		300		mΩ
			Low side		300		
			Total		600		
Power Supply Ripple Rejection Ratio	PSRR	$1V_{PP}$ ripple, f=1kHz, Inputs ac-coupled to ground			-60		dB
Oscillator Frequency	f_{OSC}	C_{OSC}=220pF			250		kHz
Output Integrated Noise Floor	Vn	20Hz to 22 kHz, A-weighting			-90		dB
Crosstalk	CS	P_O=3W, R_L=8Ω, f=1kHz			-80		dB
Signal to Noise Ratio	SNR	Maximum output at THD+N< 0.5%, f=1kHz			95		dB
Output offset voltage (measured differentially)	$\|V_{OS}\|$	INN and INP connected together			30		mV
2.5V Bias voltage	V2P5	No Load			2.5		V
Internal Analog supply Voltage	AVDD	V_{CC}=7.5V to 18V			5	5.5	V
Over Temperature Shutdown	OTS				150		℃
Thermal Hysteresis	OTH				40		℃

Note: Heat sink is required for high power output.

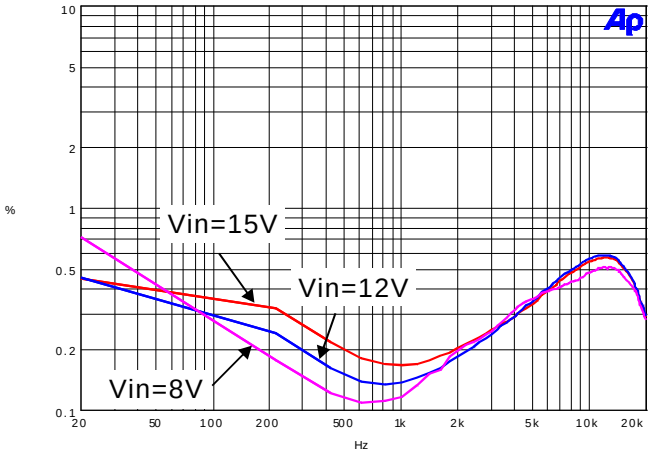
Typical Performance Characteristics

V_{CC}=12V,R_L=8Ω, Gv=24dB,T_A=25°C, unless otherwise noted.

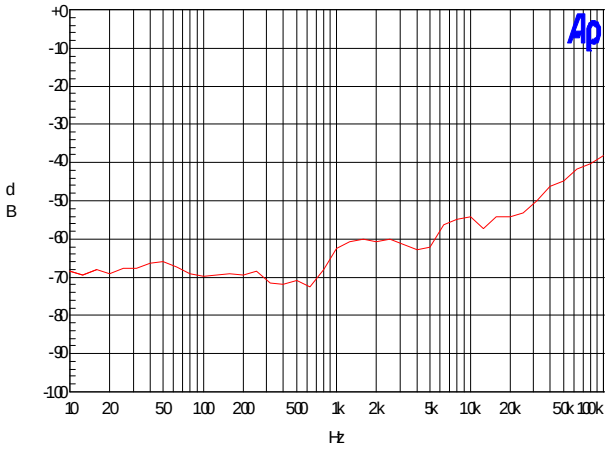
1. THD+N vs. Power



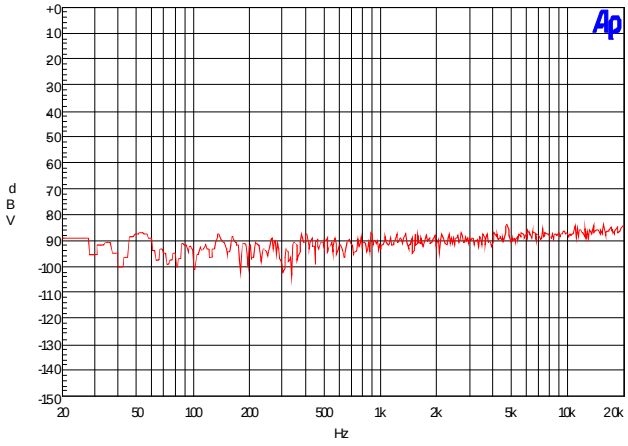
2. THD+N vs Frequency



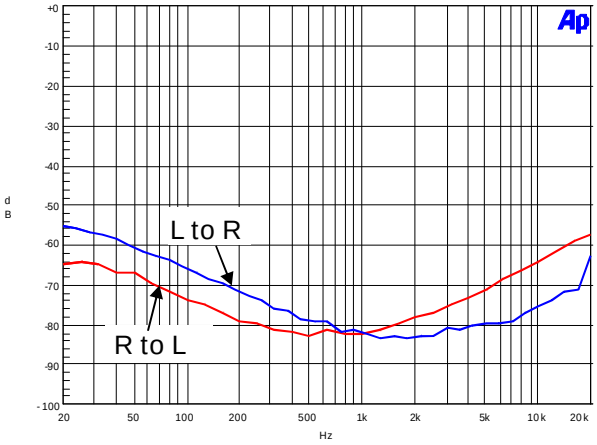
3. Power Supply Ripple Rejection



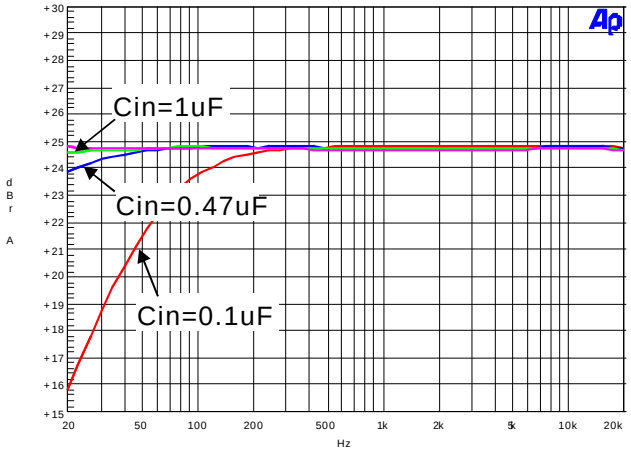
4. Noise Floor



5. Crosstalk



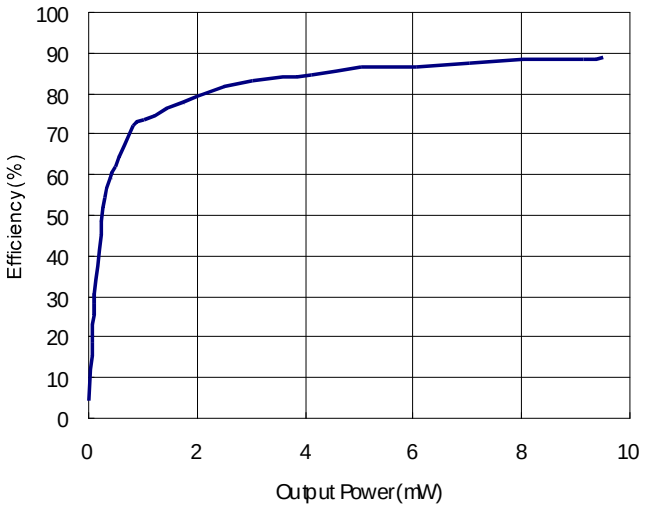
6. Frequency Response



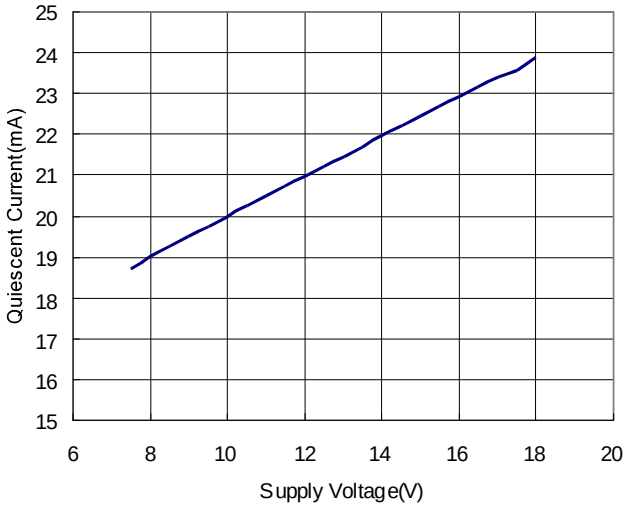
Typical Performance Characteristics

V_{CC}=12V,R_L=8Ω, Gv=24dB,T_A=25°C, unless otherwise noted.

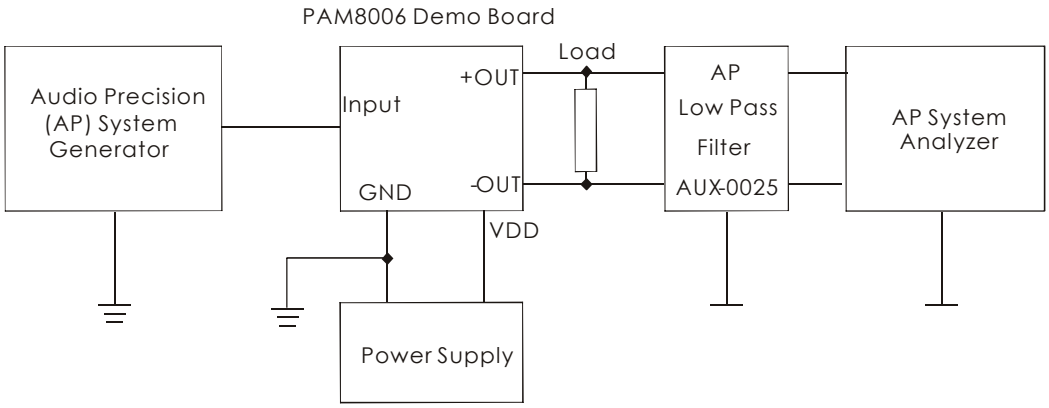
7. Efficiency vs Power



8. Quesicent Current vs Supply Voltage



Test Setup for Performance Testing



Notes

1. The Audio Precision(AP) AUX-0025 low pass filter is necessary for class-D amplifier measurement with AP analyzer.
2. Two 22µH inductors are used in series with load resistor to emulate the small speaker for efficiency measurement.

Application Information

Power and Heat Dissipation

Choose speakers that are able to stand large output power from the PAM8006. Otherwise, speaker may suffer damage.

Heat dissipation is very important when the device works in full power operation. Two factors affect the heat dissipation, the efficiency of the device that determines the dissipation power, and the thermal resistance of the package that determines the heat dissipation capability.

In operation, some of power is dissipated to the resistors.

Power Dissipation: $P_{loss}=(Po*(1-\eta)/\eta)*2$

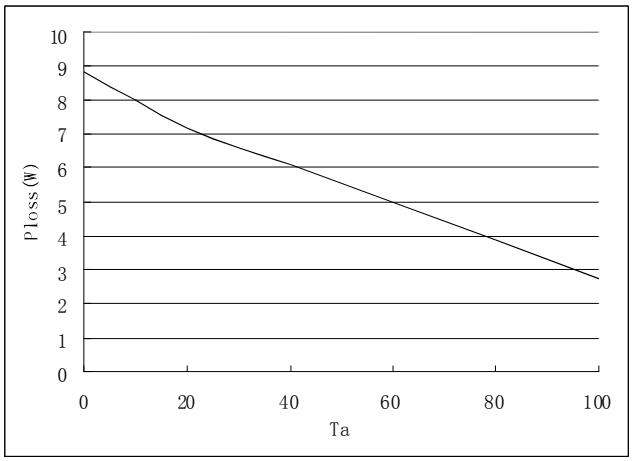
The PAM8006's efficiency is 90% with 10W ouput and 8Ω load. The dissipation power is 2.22W.

Thermal resistance of junction to ambient of the QFN package is 18.1°C/W and the junction temperature $Tj=P_{loss}*\theta jA+Ta$, where Ta is ambient temperature. If the ambient temperature is 85°C, the QFN's junction temperature

Tj=2.22*18.1+85=125°C

which is lower than 150°C rated junction temperature.

If the rated workable junction temperature is 150°C, the relationship between ambient temperature and permitted P_{loss} is shown in below diagram.



From the diagram, it can be found that when the device works at 10W/8Ω load the dissipation power is 1.1W per channel, 2.2W total, the permitted ambient temperature is over 100°C. This is proven by actual test. The PAM8006 can work in full output power under 85°C ambient temperature.

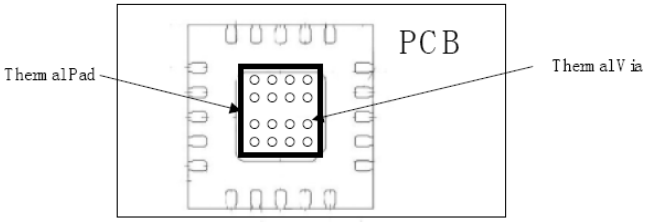
Heat Dissipation in PCB design

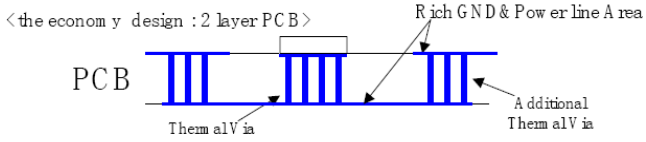
Generally, class-D amplifiers are high efficiency and need no heat sink. For high power ones that has high dissipation power, the heat sink may also not necessary if the PCB is carefully designed to achieve good heat dissipation by the PCB itself.

Dual-Side PCB

To achieve good heat dissipation, the PCB's copper plate should be thicker than 0.035mm and the copper plate on both sides of the PCB should be utilized for heat sink.

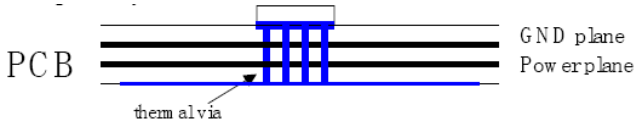
The thermal pad on the bottom of the device should be soldered to the plate of the PCB, and via holes, usually 9 to 16, should be drilled in the PCB area under the device and deposited copper on the vias should be thick enough so that the heat can be dissipated to the other side of the plate. There should be no insulation mask on the other side of the copper plate. It is better to drill more vias on the PCB around the device if possible.





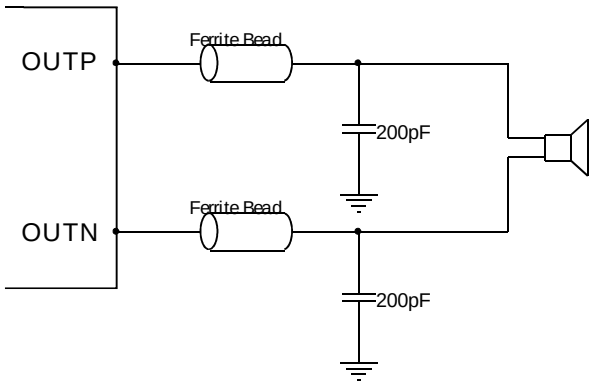
4-layer PCB

If it is 4-layer PCB, the two middle layers of grounding and power can be employed for heat dissipation, isolating them into serval islands to avoid short between ground and power.



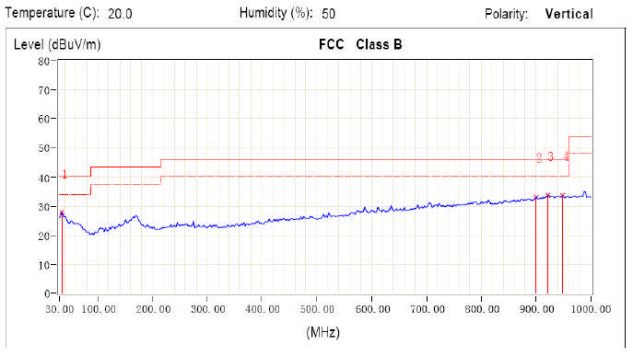
Consideration for EMI

Filters are not required if the traces from the amplifier to the speakers are short (<20cm). But most applications require a ferrite bead filter as shown in below figure. The ferrite bead filter reduces EMI of around 1MHz and higher to meet the FCC and CE's requirements. It is recommended to use a ferrite bead with very low impedances at low frequencies and high impedance at high frequencies (above 1MHz).

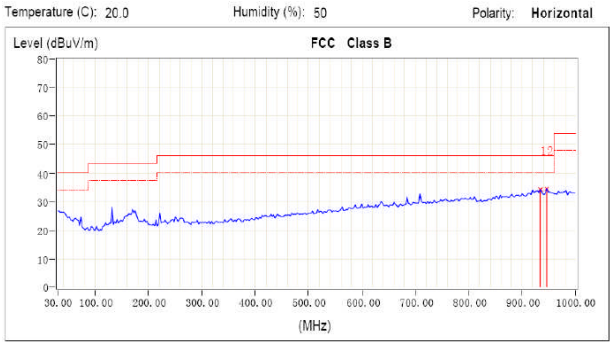


The EMI characteristics are as follows after employing the ferrite bead.

Vertical Polarization



Horizontal Polarization



MUTE Operation

The MUTE pin is an input for controlling the output state of the PAM8006. A logic high on this pin disables the outputs and low enables the outputs. This pin may be used as a quick disable or enable of the outputs.

For power saving, the $\overline{SD}$ pin should be used to reduce the quiescent current to the absolute minimum level.

Shutdown Operation

The PAM8006 employs a shutdown operation mode to reduce supply current to the absolute minimum level during periods of non-use to save power. The $\overline{SD}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{SD}$ low causes the outputs to mute and the amplifier to enter a low-current state. $\overline{SD}$ should never be left unconnected to prevent the amplifier from unpredictable operation.

For the best power-off pop performance, the amplifier should be set in shutdown mode prior to removing the power supply voltage.

Internal 2.5V Bias Generator Capacitor Selection

The internal 2.5V bias generator (V2P5) provides the internal bias for the preamplifier stage. The external input capacitors and this internal reference allow the inputs to be biased within the optimal common-mode range of the input preamplifiers.

The selection of the capacitor value on the V2P5 terminal is critical for achieving the best device performance. During startup or recovery from shutdown state, the V2P5 capacitor determines the rate at which the amplifier starts up. When the voltage on the V2P5 capacitor equals 0.75 x V2P5, or 75% of its final value, the device turns on and the class-D outputs start switching. The startup time is not critical for the best de-pop performance since any heard pop sound is the result of the class-D output switching-on other than that of the startup time. However, at least a 0.47µF capacitor is recommended for the V2P5 capacitor.
Another function of the V2P5 capacitor is to filter high frequency noise on the internal 2.5V bias generator.

Power Supply Decoupling, C_s

The PAM8006 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) as low as possible. Power supply decoupling also prevents oscillations caused by long lead between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1µF, is recommended, placing as close as possible to the device's VCC lead. To filter lower-frequency noises, a large aluminum electrolytic capacitor of 10µF or greater is recommended, placing near the audio power amplifier. The 10µF capacitor also serves as a local storage capacitor for supplying current during large signal transients on the amplifier outputs.

BSN and BSP Capacitors

The full H-bridge output stages use NMOS transistors only. They therefore require bootstrap capacitors for the high side of each output to turn on correctly. A at least 220nF ceramic capacitor, rated for at least 25V, must be connected from each output to its corresponding bootstrap input. Specifically, one 220nF capacitor must be connected from xOUTP to xBSP, and another 220nF capacitor from xOUTN to xBSN. It is recommended to use 1µF BST capacitor to replace 220nF (pin15, pin16, pin35 and pin36) for lower than 100Hz applications.

VCLAMP Capacitors

To ensure that the maximum gate-to-source voltage for the NMOS output transistors not exceeded, two internal regulators are used to clamp the gate voltage. Two 1µF capacitors must be connected from VCLAMP to ground and must be rated for at least 25V. The voltages at the VCLAMP terminals vary with V_{CC} and may not be used to power any other circuitry.

Internal Regulated 5-V Supply (AVDD)

The AVDD terminal is the output of an internally-generated 5V supply, used for the oscillator, preamplifier. It requires a 0.1µF to 1µF capacitor, placed very close to the pin to Ground to keep the regulator stable. The regulator may not be used to power any external circuitry.

Differential Input

The differential input stage of the amplifier eliminates noises that appear on the two input lines of the channel. To use the PAM8006 with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the PAM8006 with a single-ended source, ac-ground the INP input through a capacitor equal in value to the input capacitor on INN and apply the audio source to the INN input. In a single-ended input application, the INP input should be ac-grounded at the audio source other than at the device input for best noise performance.

Using low-ESR Capacitors

Low-ESR capacitors are recommended throughout this application section. A real (with respect to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves as an ideal capacitor.

Short-circuit Protection

The PAM8006 has short circuit protection circuitry on the outputs to prevent damage to the device when output-to-output shorts, output-to-GND shorts, or output-to-VCC shorts occur. Once a short-circuit is detected on the outputs, the output drive is immediately disabled. This is a latched fault and must be reset by cycling the voltage on the $\overline{SD}$ pin to a logic low and back to the logic high state for normal operation. This will clear the short-circuit flag and allow for normal operation if the short was removed. If the short was not removed, the protection circuitry will again activate.

Selection of COSC and Frequency Setting

The switching frequency is determined by the values of components connected to COSC and calculated as follows:

$f_{osc} = 22 / (Cosc*R)$

R is the internal resistor and the vaule is 400kΩ and with ± 20% tolerance.The frequency may varies from 200kHz to 300kHz by adjusting the values of C_{osc}. The recommended value is C_{osc} = 220pF for a switching frequency of 250kHz.

Selection of Gain and Input Signal Amplitude

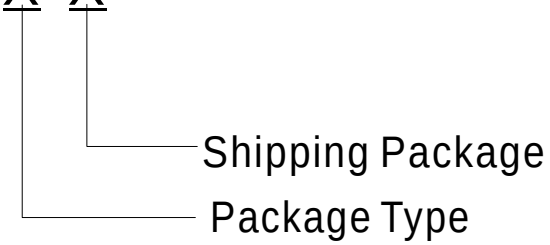
The PAM8006 has two internal amplifier stages with fixed gain. The pre-amp stage gain is 10X, while the second stage gain is 5X.
The pre-amp is powered internally by the 5V value of AVDD. At maximum pre-amp gain operation for avoiding the pre-amp saturation, it's worth noting that the peak value of input signal (Vp) shouldn't exceed 250mV when the THD+N of PAM8006 is lower than 1%; and the Vp value shouldn't exceed 300mV when the THD+N is lower than 10%.
Total gain is calculated as follows:
$Gain=20log[100k/(10k+R_{IN})*5]$
(R_{IN} is external input resistor.)

Thermal Protection

Thermal protection on the PAM8006 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15 degree tolerance on this trip point from device to device. Once the die temperature exceeds the set thermal point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 40°C. The device begins normal operation at this point without external system intervention.

Ordering Information

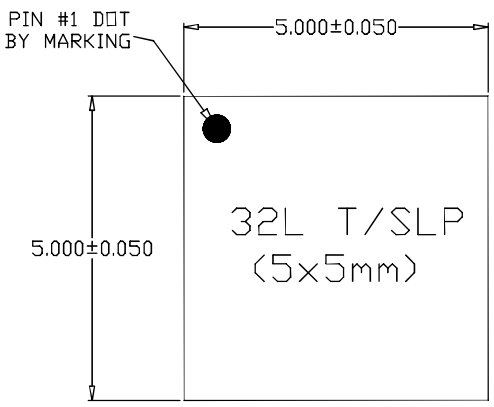
PAM8006 X X



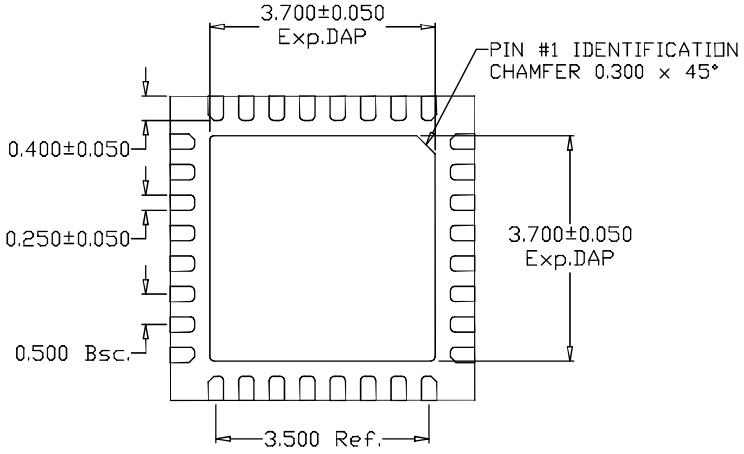
Part Number	Marking	Package Type	Standard Package
PAM8006TR	PAM8006 XATYWWLL	QFN 5mm*5mm	3,000 units/Tape & Reel
PAM8006HR	PAM8006 XATYWWLL	TSSOP-28PP	2,500 units/Tape & Reel

Outline Dimension

32pin QFN

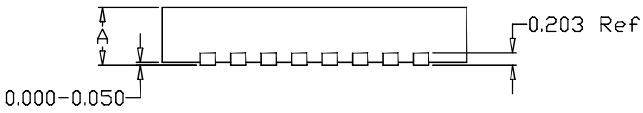


TOP VIEW



BOTTOM VIEW

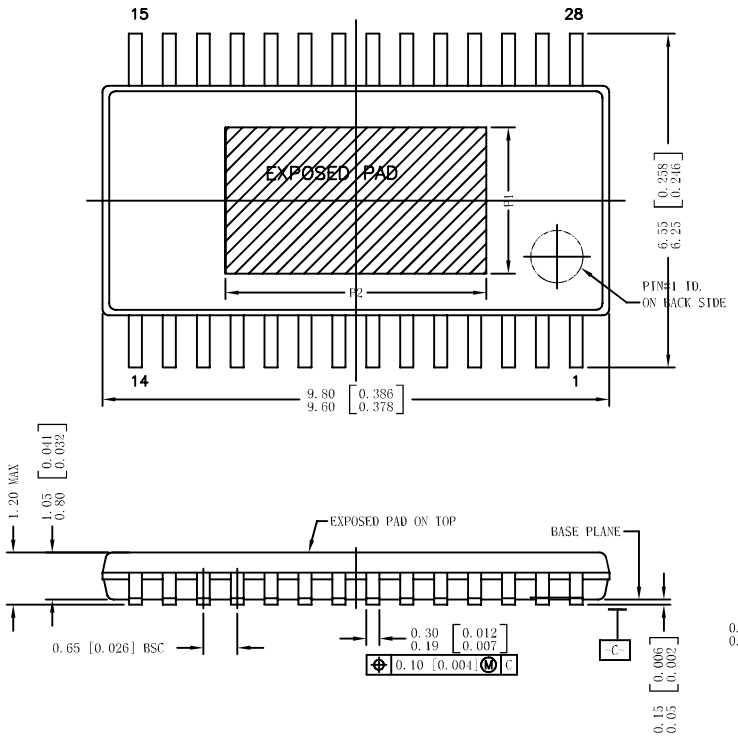
A	MAX.	0.800
	NOM.	0.750
	MIN.	0.700



SIDE VIEW

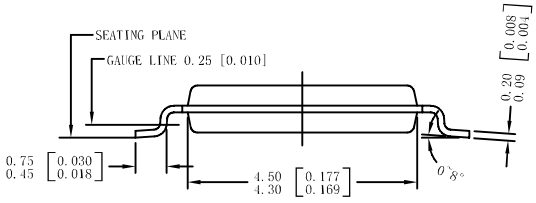
Outline Dimension

TSSOP-28PP



NOTES:

1) LEADFRAME MATERIAL : C7025 (THICKNESS: 0.127MM).
2) BOTH PACKAGE LENGTH & WIDTH DO NOT INCLUD MOLD FLASH.
3) FORMED LEAD SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.10MM.
4) UNREMOVED FLASH BETWEEN LEADS & PACKAGE END FLASH SHALL NOT EXCEED 0.15MM FROM BOTTOM BODY PER SIDE.
5) EXPOSED PAD SIZE P1 & P2 ARE VARIATIONS DEPENDING ON DEVICE FUNCTION (DIE PADDLE SIZE).
6) EXPOSED PAD ON TOP.
7) CONTROLLING DIMENSION : MM [INCH].



PAD SIZE	EXPOSED PAD SIZE		
		P1	P2
3.0 X 5.1 [.118 X .200]	MAX	3.05 [0.120]	5.15 [0.202]
	MIN	2.74 [0.108]	4.84 [0.190]