PRELIMINARY

Integrated Circuit Systems, Inc.

ICS858012

LOW SKEW, 1-TO-2, DIFFERENTIAL-TO-2.5V, 3.3V LVPECL FANOUT BUFFER

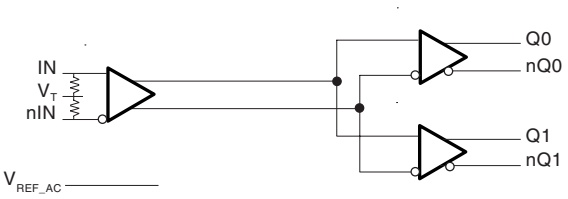
GENERAL DESCRIPTION

The ICS858012 is a high speed 1-to-2 Differential-to-2.5V, 3.3V LVPECL Fanout Buffer and is a member of the HiPerClockS™ family of high performance clock solutions from ICS. The ICS858012 is optimized for high speed and very low output skew, making it suitable for use in demanding applications such as SONET, 1 Gigabit and 10 Gigabit Ethernet, and Fibre Channel. The internally terminated differential input and V_{REF_AC} pin allow other differential signal families such as LVPECL, LVDS, LVHSTL and HCSL to be easily interfaced to the input with minimal use of external components. The ICS858012 is packaged in a small 3mm x 3mm 16-pin VFQFN package which makes it ideal for use in space-constrained applications.

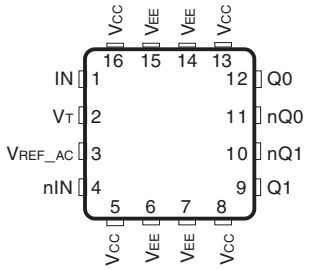
FEATURES

- Two differential LVPECL outputs
- One differential LVPECL clock input
- IN, nIN pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Output frequency: 2GHz (typical)
- Output skew: <15ps (typical)
- Part-to-part skew: TBD
- Additive phase jitter, RMS: TBD
- Propagation delay: 350ps (typical)
- Operating voltage supply range: V_{CC} = 2.375V to 3.63V, V_{EE} = 0V
- -40°C to 85°C ambient operating temperature
- Availabe in both standard and lead-free RoHS compliant packages

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS858012
16-Lead VFQFN
3mm x 3mm x 0.95 package body
K Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	IN	Input		Non-inverting LVPECL differential clock input.
2	V_T	Input		Termination input.
3	V_{REF_AC}	Output		Reference voltage for AC-coupled applications. V_{REF_AC} = to V_{CC} - 1.38V.
4	nIN	Input		Inverting differential LVPECL clock input.
5, 8, 13, 16	V_{CC}	Power		Positive supply pins.
6, 7, 14, 15	V_{EE}	Power		Negative supply pin.
9, 10	Q1, nQ1	Output		Differential output pair. LVPECL interface levels.
11, 12	nQ0, Q0	Output		Differential output pair. LVPECL interface levels.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V (LVPECL mode, V_{EE} = 0)
Inputs, V_I	-0.5V to V_{CC} + 0.5 V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Input Current, IN, nIN	±50mA
V_T Current, I_{VT}	±100mA
Input Sink/Source, I_{REF_AC}	± 0.5mA
Operating Temperature Range, TA	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	51.5°C/W (0 lfpm)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 2A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 2.375V TO 3.63V; V_{EE} = 0V

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	3.3	3.63	V
I_{EE}	Power Supply Current	Max., V_{CC}, No Load		30		mA

TABLE 2B. DC CHARACTERISTICS, V_{CC} = 2.375V TO 3.63V; V_{EE} = 0V

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
R_{IN}	Differential Input Resistance	(IN, nIN)		40	50	60	Ω
V_{IH}	Input High Voltage	(IN, nIN)		1.2		V_{CC}	V
V_{IL}	Input Low Voltage	(IN, nIN)		0		V_{IH} - 0.15	V
V_{IN}	Input Voltage Swing; NOTE 1			0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing			0.3			V
I_N to V_T						1.28	V
V_{REF_AC}	Output Reference Voltage			V_{CC} - 1.525	V_{CC} - 1.4	V_{CC} - 1.325	V

NOTE 1: Refer to Parameter Measurement Information, Input Voltage Swing Diagram

TABLE 2C. LVPECL DC CHARACTERISTICS, V_{CC} = 2.375V TO 3.63V; V_{EE} = 0V

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.145		V_{CC} - 0.895	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 1.945		V_{CC} - 1.695	V
V_{OUT}	Output Voltage Swing		550	800		mV
V_{DIFF_OUT}	Differential Output Voltage Swing		1100	1600		mV

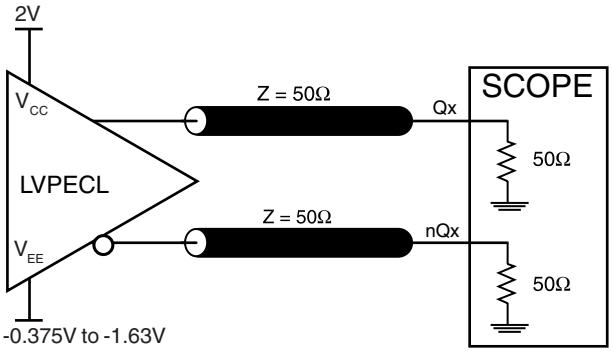
NOTE 1: Outputs terminated with 100Ω across differential output pair.

TABLE 3. AC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -3.63V TO -2.375V OR V_{CC} = 2.375 TO 3.63V; V_{EE} = 0V

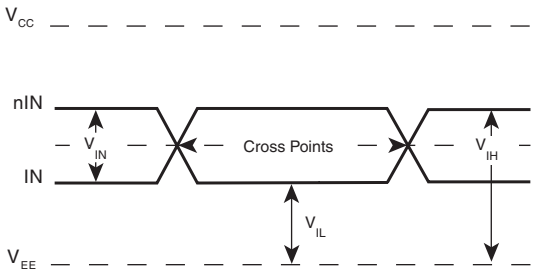
Symbol	Parameter	Condition	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			2		GHz
f_{IN}	Input Frequency			2.5		GHz
t_{PD}	Propagation Delay; (Differential); NOTE 1			350		ps
*t*sk(o)	Output Skew; NOTE 2, 4			<15		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			TBD		ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section			TBD		fs
t_R/t_F	Output Rise/Fall Time	20% to 80%		152		ps

All parameters characterized at ≤ 1GHz unless otherwise noted.
R_L = 100Ω after each output pair.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

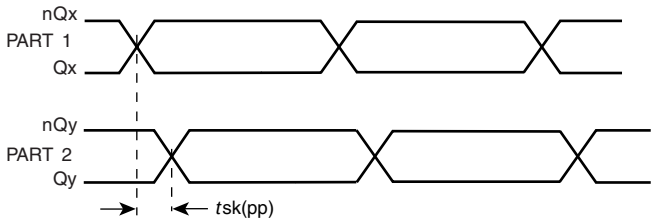
PARAMETER MEASUREMENT INFORMATION



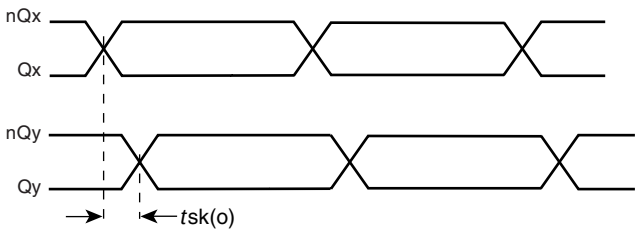
OUTPUT LOAD AC TEST CIRCUIT



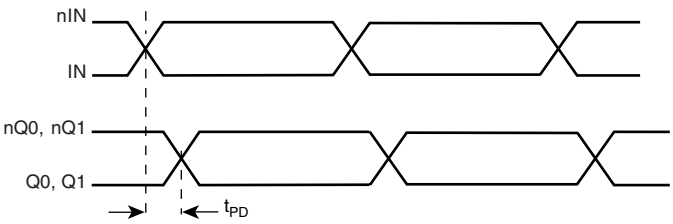
DIFFERENTIAL INPUT LEVEL



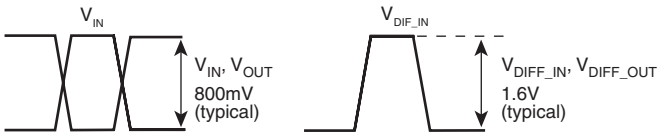
PART-TO-PART SKEW



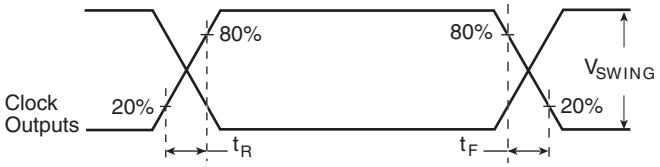
OUTPUT SKEW



PROPAGATION DELAY



SINGLE ENDED & DIFFERENTIAL INPUT VOLTAGE SWING



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

LVPECL INPUT WITH BUILT-IN 50Ω TERMINATION INTERFACE (2.5V)

The IN/nIN with built-in 50Ω terminations accepts LVDS, LVPECL, LVHSTL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 1A to 1E* show interface examples for the HiPerClockS IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

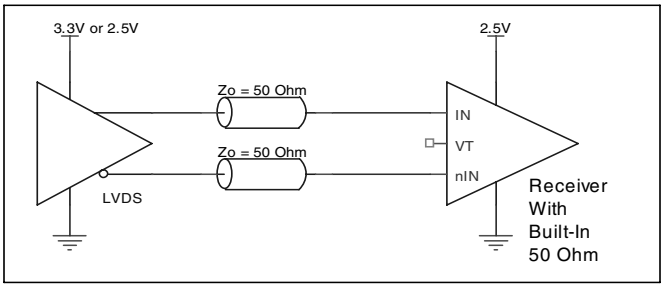


FIGURE 1A. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVDS DRIVER

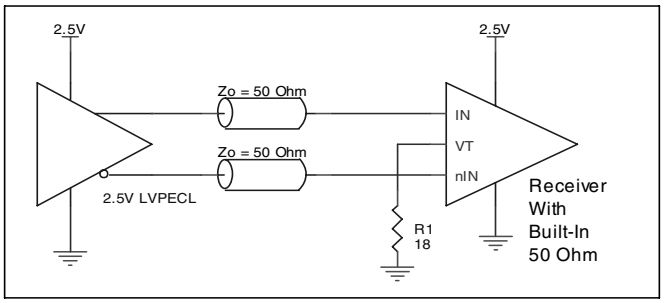


FIGURE 1B. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVPECL DRIVER

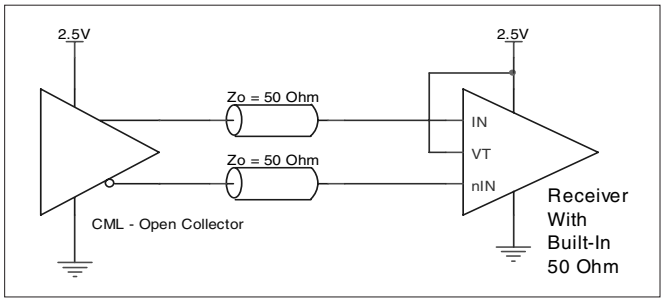


FIGURE 1C. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN OPEN COLLECTOR CML DRIVER

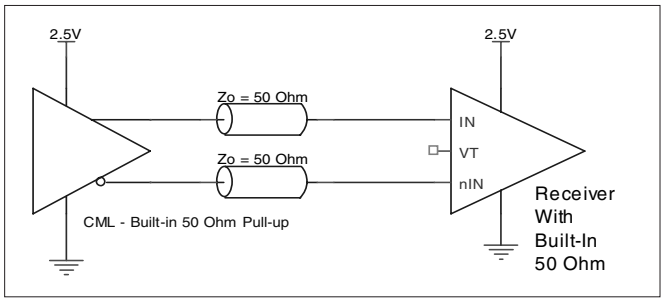


FIGURE 1D. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY A CML DRIVER WITH BUILT-IN 50Ω PULLUP

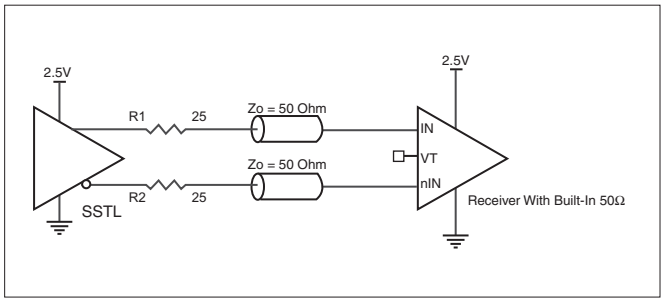


FIGURE 1E. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN SSTL DRIVER

LVPECL INPUT WITH BUILT-IN 50Ω TERMINATION INTERFACE (3.3V)

The IN /nIN with built-in 50Ω terminations accepts LVDS, LVPECL, LVHSTL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the HiPerClockS IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

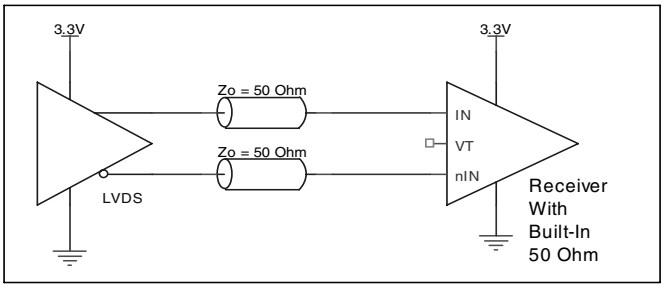


FIGURE 2A. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVDS DRIVER

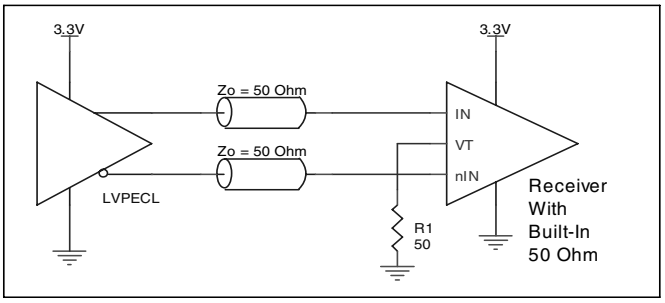


FIGURE 2B. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVPECL DRIVER

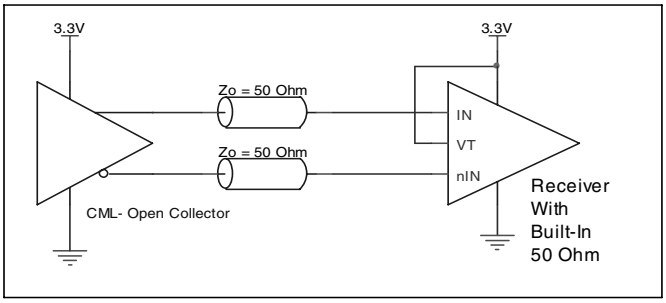


FIGURE 2C. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY A CML DRIVER WITH OPEN COLLECTOR

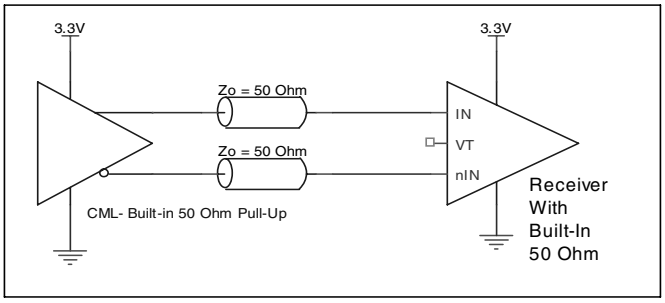


FIGURE 2D. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY A CML DRIVER WITH BUILT-IN 50Ω PULLUP

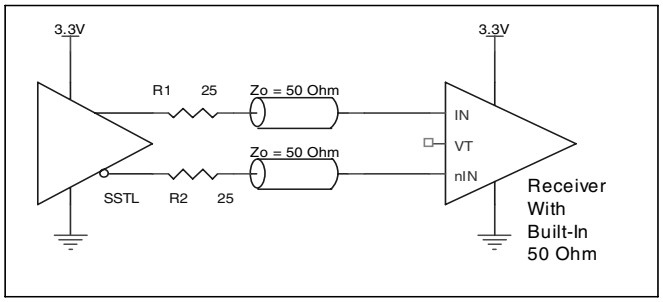


FIGURE 2E. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN SSTL DRIVER

2.5V DIFFERENTIAL INPUT WITH BUILT-IN 50Ω TERMINATION UNUSED INPUT HANDLING

To prevent oscillation and to reduce noise, it is recommended to have pullup and pulldown connect to true and compliment of the unused input as shown in *Figure 3.*

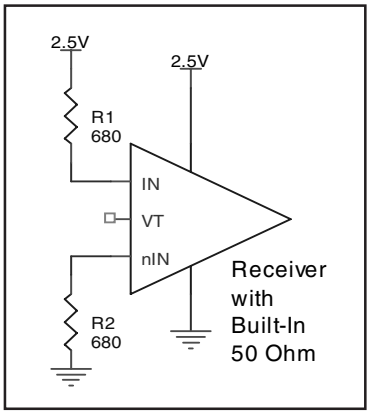


FIGURE 3. UNUSED INPUT HANDLING

3.3V DIFFERENTIAL INPUT WITH BUILT-IN 50Ω TERMINATION UNUSED INPUT HANDLING

To prevent oscillation and to reduce noise, it is recommended to have pullup and pulldown connect to true and compliment of the unused input as shown in *Figure 4.*

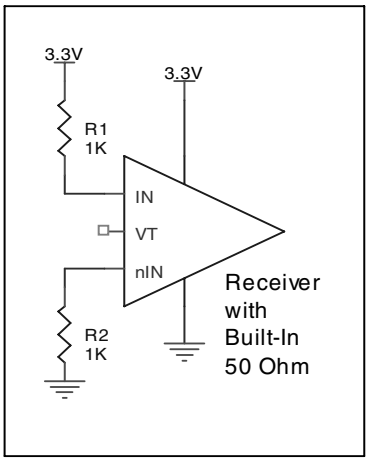


FIGURE 4. UNUSED INPUT HANDLING

RECOMMENDATIONS FOR UNUSED OUTPUT PINS

OUTPUTS:

LVPECL OUTPUT

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

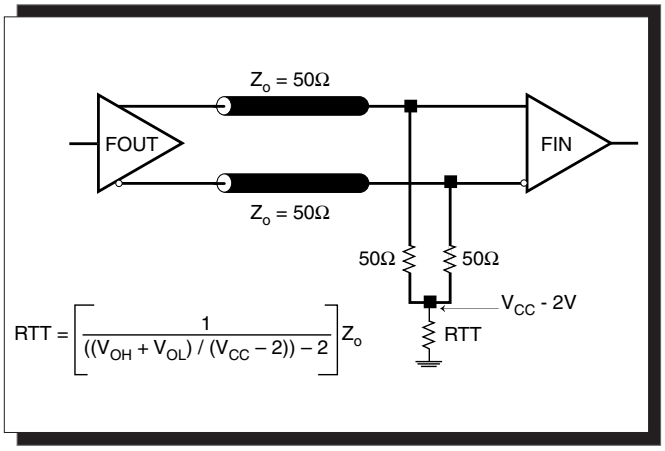


FIGURE 5A. LVPECL OUTPUT TERMINATION

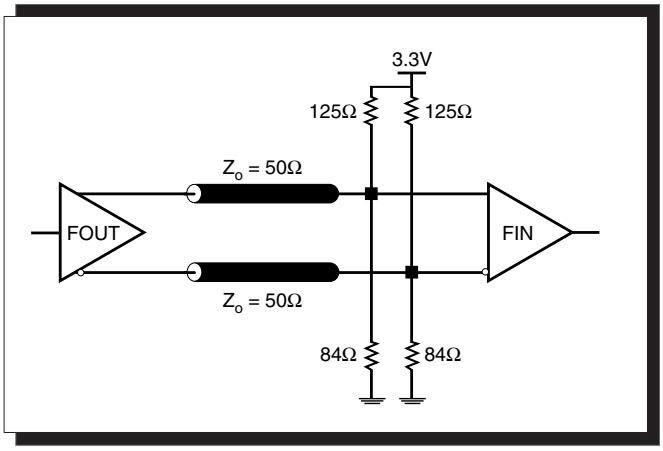


FIGURE 5B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 6A and *Figure 6B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 6B can be eliminated and the termination is shown in *Figure 6C.*

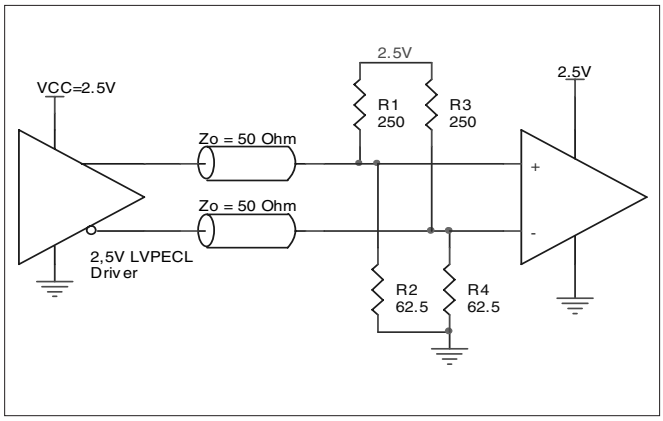


FIGURE 6A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

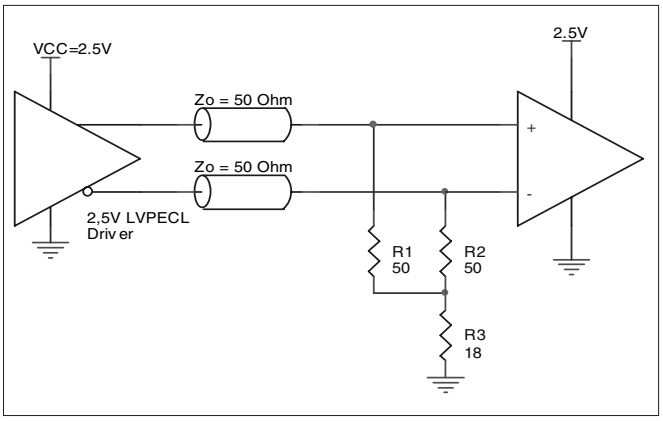


FIGURE 6B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

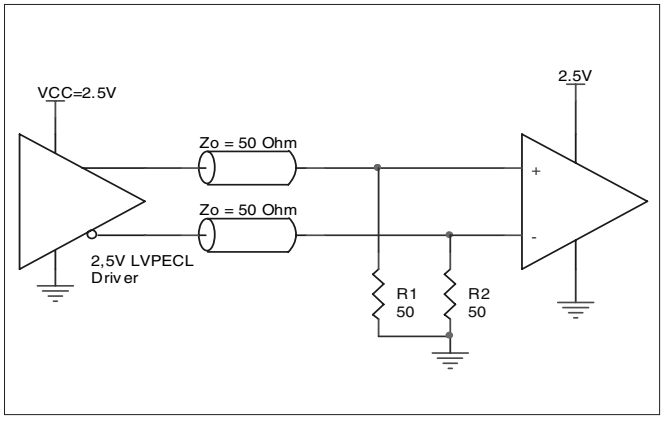


FIGURE 6C. 2.5V LVPECL TERMINATION EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS858012. Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS858012 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.63V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC_MAX} * I_{EE_MAX}$ = 3.63V * 30mA = **108.9mW**
- Power $(outputs)_{MAX}$ = **30.2mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 30.2mW = **60.4mW**

Total Power$_{_MAX}$ (3.63V, with all outputs switching) = 108.9mW + 60.4mW = **169.3mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 0 linear feet per minute and a multi-layer board, the appropriate value is 51.5°C/W per Table 4 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.169W * 51.5°C/W = 93.7°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 4. THERMAL RESISTANCE θ_{JA} FOR 16 LEAD VFQFN, FORCED CONVECTION

θ_{JA} at 0 Air Flow (Linear Feet per Minute)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W

3. Calculations and Equations.

LVPECL output driver circuit and termination are shown in *Figure 7.*

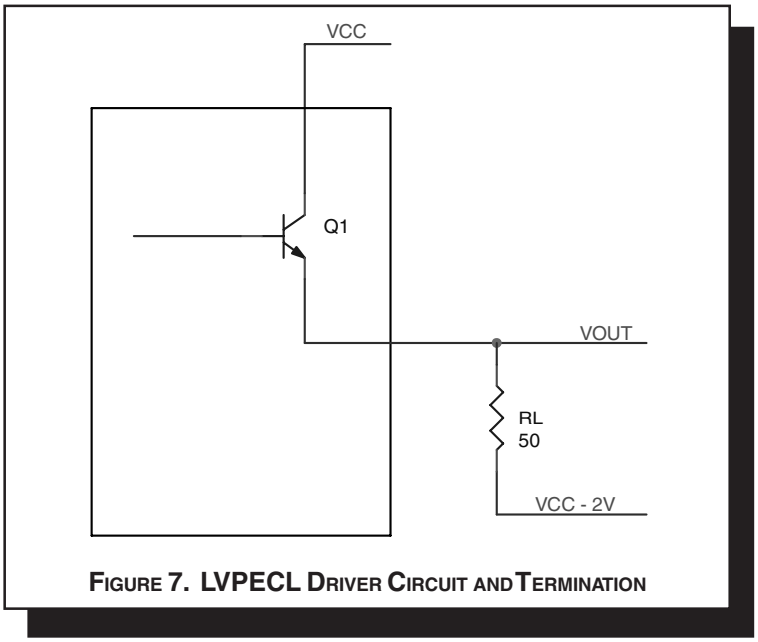


FIGURE 7. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH_MAX} = \mathbf{V_{CC_MAX} - 0.895V}$

  $(V_{CC_MAX} - V_{OH_MAX}) = \mathbf{0.895V}$

- For logic low, $V_{OUT} = V_{OL_MAX} = \mathbf{V_{CC_MAX} - 1.695V}$

  $(V_{CC_MAX} - V_{OL_MAX}) = \mathbf{1.695V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd_H = [(V_{OH_MAX} – (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - (V_{CC_MAX} - V_{OH_MAX}))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) =$
$[(2V - 0.895V)/50\Omega] * 0.895V =$ **19.78mW**

$Pd_L = [(V_{OL_MAX} – (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - (V_{CC_MAX} - V_{OL_MAX}))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) =$
$[(2V - 1.695V)/50\Omega] * 1.695V =$ **10.34mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.2mW**

RELIABILITY INFORMATION

TABLE 5. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD VFQFN

θ_{JA} at 0 Air Flow (Linear Feet per Minute)	
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W

TRANSISTOR COUNT

The transistor count for ICS858012 is: 113

Pin compatible with SY58012U

PACKAGE OUTLINE - K SUFFIX FOR 16 LEAD VFQFN

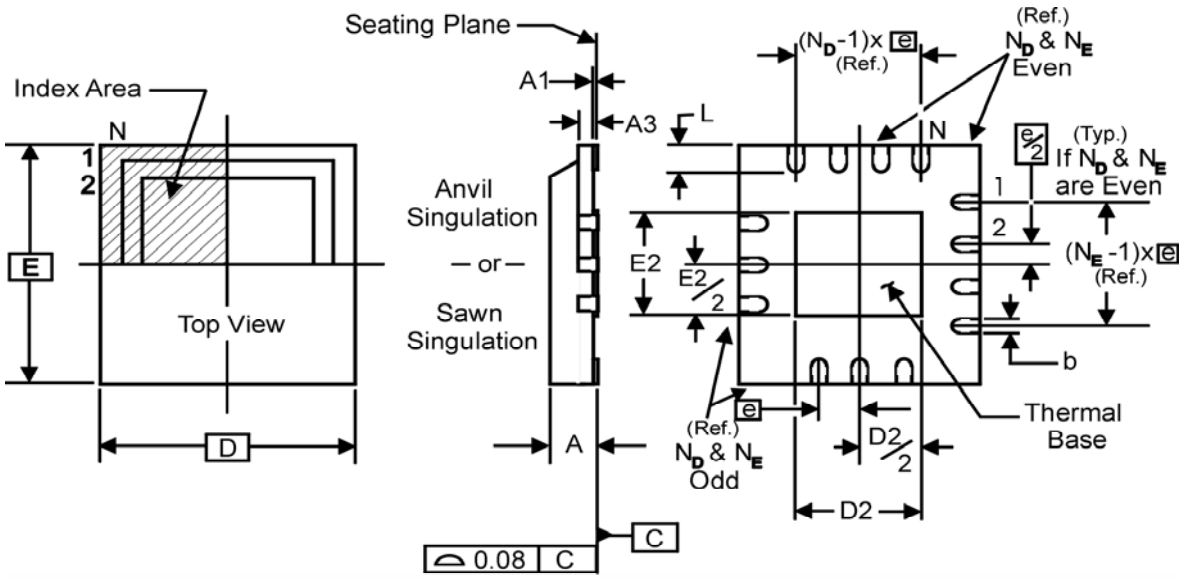


TABLE 6. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**MINIMUM**	**MAXIMUM**
N	16	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	4	
N_E	4	
D	3.0	
D2	0.25	1.25
E	3.0	
E2	0.25	1.25
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS858012AK	012A	16 Lead VFQFN	tube	-40°C to 85°C
ICS858012AKT	012A	16 Lead VFQFN	2500 tape & reel	-40°C to 85°C
ICS858012AKLF	TBD	16 Lead "Lead-Free" VFQFN	tube	-40°C to 85°C
ICS858012AKLFT	TBD	16 Lead "Lead-Free" VFQFN	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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