

Description

The RoHS 6/6 compliant STC5425 is a single chip clock synchronization solution for line card applications in SDH, SONET, and Synchronous Ethernet network elements.

The STC5425 accepts 5 clock reference inputs, 3 external frame sync inputs (EX_SYNC1, 2, 3) and generates 4 synchronized clock outputs. Synchronized outputs may be programmed for wide variety of frequencies from 1MHz up to 156.25MHz, in 1kHz steps. Reference inputs are individually monitored for activity and quality. Reference selection may be automatic, manual, or hard-wired manual.

The timing generator may operate in the **Freerun**, **Synchronized**, and **Holdover**. It includes a DSP-based PLL. Synchronized mode is external timing while freerun and holdover mode are self-timing. DSP-based PLL technology removes any external component except the oscillator. It provides excellent performance and reliability to STC5425.

The STC5425 is clocked by an external oscillator, either a stable TCXO or XO, as required by application.

Features

- Suitable for SONET, SDH, and Synchronous Ethernet applications
- Supports 4 different frequencies of external oscillator upon soft-reset: 10MHz, 12.8MHz, 19.2MHz, 20MHz
- Provides three 2kHz or 8kHz external frame sync input
- Accepts 5 clock reference inputs
- Supports automatically frequency detection or manually acceptable frequency. Each reference input is monitored for activity and quality
- Automatic, manual, and hard-wired manual reference selection
- Outputs 4 synchronized clock outputs, including 2 frame pulse clocks
- Frequency translation of input clock to a different local line card clock
- 3 clock synthesizers generate frequencies
- Phase-align locking or hit-less reference switching
- Programmable loop bandwidth, from 13Hz to 100Hz
- Programmable phase skew in synthesizer level
- SPI bus interface
- Single 3.3V operation
- IEEE 1149.1 JTAG boundary scan
- Available in TQFP64 package

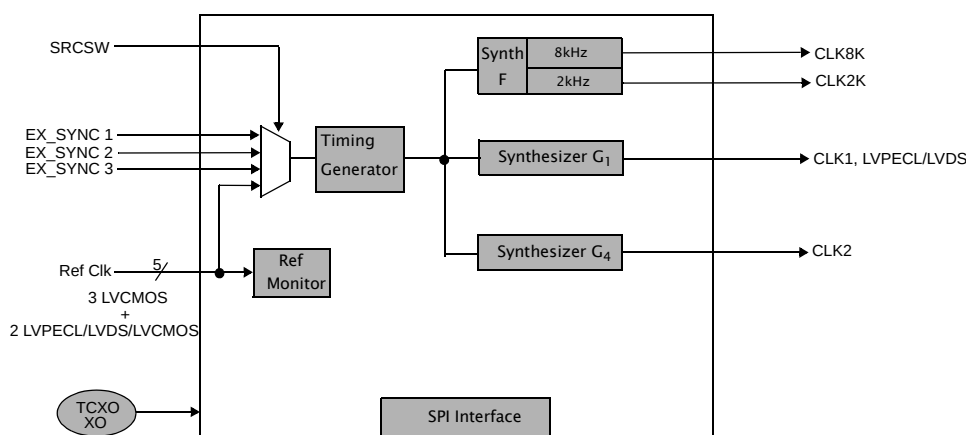


Figure 1:Functional Block Diagram

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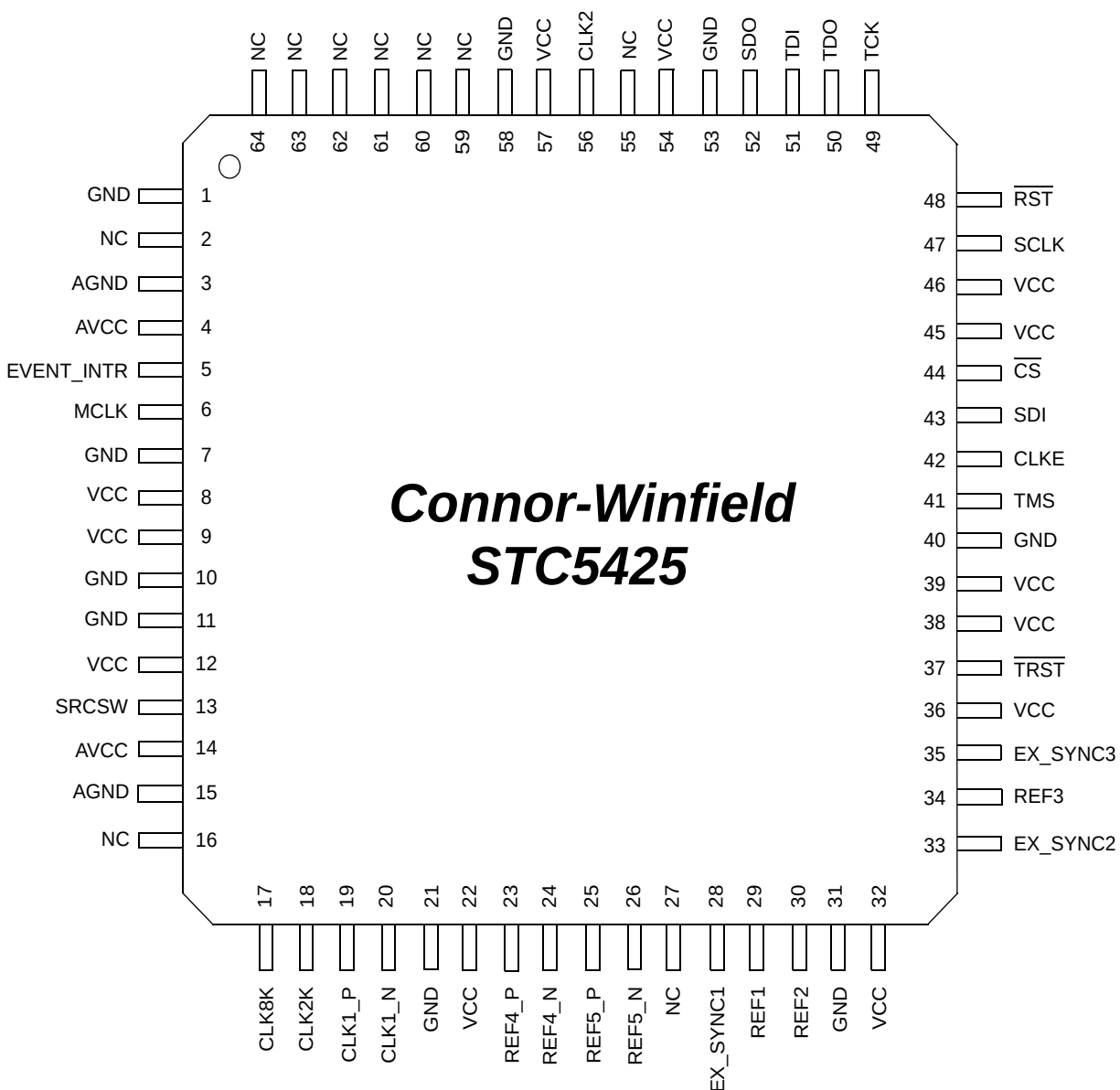
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STC5425 Pin Diagram (Top View)



STC5425 Pin Description

All I/O is LVCMOS, except for CLK1 is LVPECL/LVDS. REF4 and REF5 are LVCMOS/LVPECL/LVDS.

Table 1: Pin Description

Pin Name	Pin #	I/O	Description
AVCC	4,14		3.3V analog power input
AGND	3,15		Analog ground
VCC	8, 9, 12, 22, 32, 36, 38, 39, 45, 46, 54, 57		3.3V digital power input
GND	1, 7, 10, 11, 21, 31, 40, 53, 58		Digital ground
$\overline{\text{TRST}}$	37	I	JTAG boundary scan reset, active low
TCK	49	I	JTAG boundary scan clock
TMS	41	I	JTAG boundary scan mode selection
TDI	51	I	JTAG boundary scan data input
TDO	50	O	JTAG boundary scan data output
$\overline{\text{RST}}$	48	I	Active low to reset the chip
MCLK	6	I	Master clock input (TCXO or XO)
EVENT_INTR	5	O	Event interrupt
EX_SYNC1	28	I	Frame Sync signal 1
EX_SYNC2	33	I	Frame Sync signal 2
EX_SYNC3	35	I	Frame Sync signal 3
REF1	29	I	Reference input 1
REF2	30	I	Reference input 2
REF3	34	I	Reference input 3
REF4_P	23	I	Differential reference input 4 (LVPECL/LVDS)
REF4_N	24	I	Differential reference input 4 (LVPECL/LVDS)
REF5_P	25	I	Differential reference input 5 (LVPECL/LVDS)
REF5_N	26	I	Differential reference input 5 (LVPECL/LVDS)
CLK1_P	19	O	Clock output CLK1 positive. 1MHz to 156.25MHz, in 1kHz steps, from Synthesizer G ₁ LVPECL or LVDS
CLK1_N	20	O	Clock output CLK1 negative, 1MHz to 156.25MHz, in 1kHz steps, from Synthesizer G ₁ LVPECL or LVDS
CLK2	56	O	Clock output CLK2 1MHz to 156.25MHz, in 1kHz steps, from Synthesizer G ₃ , proprietary composite signal of Synthesizer F or Synthesizer G _{T4} (T4). LVCMOS.

Table 1: Pin Description

Pin Name	Pin #	I/O	Description
CLK8K	17	O	8kHz frame pulse signal, 50% duty cycle or programmable pulse width
CLK2K	18	O	2kHz frame pulse signal, 50% duty cycle or programmable pulse width
SRCSW	13	I	Hard-wired manual reference pre-selection
$\overline{\text{CS}}$	44	I	SPI bus chip select
SCLK	47	I	SPI bus clk
SDI	43	I	SPI bus data in
SDO	52	O	SPI bus data out
CLKE	42	I	SPI Clock edge selection
NC	2, 16, 27, 55, 59, 60, 61, 62, 63, 64		No connection. Pins are recommended to be tied to ground

Register Map

Table 2: Register Map

Addr	Reg Name	Bits	Type	Description
0x00	Chip_ID	15-0	R	Chip ID = 0x5425
0x01				
0x02	Chip_Rev	7-0	R	Chip revision number
0x03	Chip_Sub_Rev	7-0	R	Chip sub-revision number
0x07	Fill_Obs_Window	3-0	R/W	Activity monitor: Leaky bucket fill observation window
0x08	Leak_Obs_Window	3-0	R/W	Activity monitor: Leaky bucket leak observation window
0x09	Bucket_Size	5-0	R/W	Activity monitor: Leaky bucket size
0x0A	Assert_Threshold	5-0	R/W	Activity monitor: Leaky bucket alarm assert threshold
0x0B	De_Assert_Threshold	5-0	R/W	Activity monitor: Leaky bucket alarm de-assert threshold
0x0C	Freerun_Cali	10-0	R/W	Freerun calibration, 2's complement, -102.4 to +102.3ppm, step in 0.1ppm
0x0D				
0x0E	Disqualification_Range	9-0	R/W	Reference disqualification range, 0 ~102.3ppm. The value is also specified as pull-in range
0x0F				
0x10	Qualification_Range	9-0	R/W	Reference qualification range, 0 ~102.3ppm.
0x11				
0x12	Qualification_Soaking_Time	5-0	R/W	Reference qualification soaking time, 0 ~63s
0x13	Ref_Index_Selector	3-0	R/W	Determines which reference data is shown in register Ref_Info. Determines which of reference input is selected for manually acceptable reference input frequency
0x14	Ref_Info	15-0	R	Frequency offset and frequency info of the reference selected by register Ref_Index_Selector
0x15				
0x16	Ref_Activity	4-0	R	Reference activity for reference 1,2,3,4,5
0x18	Ref_Qual	4-0	R	Qualification status for reference 1,2,3,4,5
0x1A	Interrupt_Event_Status	7-0	R/W	Interrupt events
0x1B	Interrupt_Event_Enable	7-0	R/W	Selects which of interrupt events will assert pin EVENT_INTR
0x1C	Interrupt_Config	1-0	R/W	Pin EVENT_INTR configuration and idle mode
0x1D	Hard-wired_Switch_Pre_Selections	7-0	R/W	Pre-selected reference number 1 and reference number 2 for hard-wired manual switch mode
0x1E	SRCSW_States	0-0	R	Indicates the states of pin SRCSW
0x20	Control_Mode	7-2	R/W	Holdover history usage, Revertive, Manual/Auto, OOP, SRCSW
0x21	Loop_Bandwidth	7-0	R/W	Loop bandwidth selection
0x22	Auto_Elect_Ref	3-0	R	Indicates the reference elected by auto reference elector
0x23	Manual_Select_Ref	3-0	R	The reference specified by users for manual selection mode
0x24	Active_Ref	3-0	R	Indicates the PLL current selected reference
0x25	Device_Holdover_History	31-0	R	Device Holdover History
0x26				
0x27				
0x28				
0x2D	Short_Term_Accu_History	31-0	R	Short term Accumulated History
0x2E				
0x2F				
0x30				
0x35	Short_Term_History_Bandwidth	3-2	R/W	Control short term history accumulation bandwidth

Table 2: Register Map

Addr	Reg Name	Bits	Type	Description
0x36	REF_Priority_Table	19-0	R/W	REF1 ~ REF5 priority table
0x37				
0x38				
0x3C	PLL_Status	7-0	R/W	PLL status: SYNC, LOS, LOL, OOP, SAP, FEE, DHT, HHA
0x3E	PLL_Event_Out	7-0	R/W	PLL event out (TBD)
0x3F	PLL_Event_In	7-0	R/W	PLL event in: Relock
0x40	EX_SYNC_Edge_Config	2-0	R/W	Select framing edge (falling or rising edge) for EX_SYNC1/2/3
0x42	REF1/2_Frame_Phase_Align	7-0	R/W	Select framing reference input and sampling edge on selected REF1 and REF2 for frame alignment
0x43	REF3_Frame_Phase_Align	3-0	R/W	Select framing reference input and sampling edge on selected REF3 for frame alignment
0x44	REF4/5_Frame_Phase_Align	7-0	R/W	Select framing reference input and sampling edge on selected REF4 and REF5 for frame alignment
0x4A	Synth_Index_Select	3-0	R/W	Determine which synthesizer is selected for setting frequency value at register Synth_Freq_Value and adjusting phase skew at registers Synth_Skew_Adj
0x4B	Synth_Freq_Value	17-0	R/W	Selects synthesizer frequency value from 1MHz to 156.25MHz, in 1kHz steps, based on which synthesizer index is selected at the register Synth_Index_Select
0x4C				
0x4D				
0x4E	Synth_Skew_Adj	11-0	R/W	Adjust phase skew for the synthesizer with the index selected at register Synth_Index_Select
0x4F				
0x50	CLK1_Signal_Level	0-0	R/W	Select the signal level (LVDS or LVPECL) for clock outputs CLK1
0x51	CLK1_Sel	1-0	R/W	Select synthesizer or enable tri-state for CLK1
0x52	CLK2_Sel	1-0	R/W	Select synthesizer or enable tri-state for CLK2
0x59	CLK8K_Sel	6-0	R/W	8kHz frame pulse clock output duty cycle selection, signal inversion
0x5A	CLK2K_Sel	6-0	R/W	2kHz frame pulse clock output duty cycle selection, signal inversion
0x5B	Ref_Freq	14-0	R/W	Select integer N for manually acceptable frequency at Nx8kHz; Enable auto detection of reference input frequency
0x5C				
0x70	Field_Upgrade_Status	2-0	R	Indicates the status of field upgrade process
0x71	Field_Upgrade_Data	7-0	R/W	Load 7600 bytes of firmware configuration data
0x72	Field_Upgrade_Count	12-0	R	Count byte numbers that have been loaded
0x73				
0x74	Field_Upgrade_Start	7-0	W	Write three values consecutively to start the field upgrade process
0x7F	MCLK_Freq_Reset	7-0	R	Select the frequency of the external oscillator

Master Clock Frequency

The STC5425 supports four frequencies of master clock: 10MHz, 12.8MHz, 19.2MHz, and 20MHz. See Chip Master Clock for details. Initial default accepted frequency of MCLK is 12.8MHz.

Table 3: Master Clock Frequency

12.8MHz (Initial default frequency)
10MHz
19.2MHz
20MHz

Input and Output Frequencies

Input Frequencies

Auto-Detect Acceptable Input Frequencies

The STC5425 can automatically detect the frequency of the reference input when the user enable the auto-detection function at the register **Ref Freq**. The acceptable frequency for auto detection is shown in Table 4

Table 4: Auto-Detect Acceptable Ref Input Frequencies

Reference Input	Frequency
REF1 ~ REF5	8 kHz
	64 kHz
	19.44 MHz
	38.88 MHz
	77.76 MHz
	1.544 MHz
	2.048 MHz
	6.48 MHz
	8.192 MHz
	16.384 MHz
	25 MHz
	50 MHz
	125 MHz
EX_SYNC1 EX_SYNC2 EX_SYNC3	2kHz or 8kHz external frame sync inputs

Manually Acceptable Input Frequencies

When the frequency auto-detect function is disabled, STC5425 provides another option which allows the user to select the manually acceptable reference frequency for all the reference inputs, at the integer multiple of 8kHz ($N \times 8\text{kHz}$, N is integer from 1 to 32767). Hence the manually acceptable reference frequency range is 8kHz to 262.136MHz, in 8kHz steps. When a manually acceptable reference frequency is used, the user need to access the register **Ref Freq** to set the integer N .

$$\text{Input Frequency} = N \times 8\text{kHz}, \text{ where } N = 1 \sim 32767$$

Clock Output Frequencies

Table 5: Available Clock Output Frequencies

CLK	CLK Level	Synthesizer	Clock Output Frequency Range
CLK1	LVPECL/LVDS	G ₁	1MHz ~ 156.25MHz, in 1kHz steps
CLK2	LVC MOS	G ₄	1MHz ~ 156.25MHz, in 1kHz steps
CLK8K	LVC MOS	F	8kHz
CLK2K		F	2kHz

Clock Output Jitter

Table 6: Clock Output Jitter

Clock Output	Frequency	RMS jitter ¹ (Typical)	pk-pk jitter ¹ (10 ⁻¹²) (Typical)	
	(MHz)	(ps)	(ps)	(UI)
CLK1 (LVPECL)	156.25	13	210	0.03
	155.52	13	210	0.03
	125	13	210	0.03
	77.76	13	210	0.02
CLK2 (LVCMOS)	77.76	19	330	0.03
	38.88	16.5	280	0.01
	19.44	15	230	0.005
	25	13	180	0.005
	2.048	11	180	0.0004
	1.544	11	160	0.0003

Note 1: Filter bandwidth is from 12kHz to Frequency/2

General Description

Application

The STC5425 is a single chip line card solution for applications in SONET, SDH, and Synchronous Ethernet network elements. Its highly integrated design implements all necessary reference selection, monitoring, filtering, synthesis, and control functions. An external oscillator (e.g., stable TCXO or XO) completes a system level solution (see Functional Block Diagram, Figure 1). The STC5425 has four options for frequency of external oscillator.

Overview

The STC5425 accepts 5 reference inputs and generates 4 synchronized clock outputs, including 2 frame pulse clock outputs at 8kHz and 2kHz. One PLL-based timing generator provide the essential functions for frequency translation of reference input to a line card clock. It controls synthesizers G_1 , G_4 , and synthesizer F. Clock outputs CLK1 and CLK2 can be derived from synthesizer G_1 and G_4 , respectively. Frame pulse clock outputs are derived from synthesizer F. The STC5425 incorporates a SPI interface, providing access to status registers.

Chip Master Clock

The STC5425 operates with an external oscillator (e.g., TCXO or XO) as its master clock. The device supports four different frequencies of master clock: 10MHz, 12.8MHz, 19.2MHz, and 20MHz. Initial default accepted frequency is 12.8MHz.

Reference Inputs and External Sync Inputs

The STC5425 accepts 5 reference inputs. 3 LVCMOS and 2 LVPECL/LVDS/LVCMOS. The 5 reference inputs are continuously activity and quality monitored. The reference inputs may be selected to accept either the auto-detect acceptable reference frequency which can be automatically detected by STC5425 or manually acceptable reference frequency. The activity monitoring is implemented with a programmable leaky bucket algorithm. A reference is designated as "qualified" if it is active and its fractional frequency offset is within the programmed range for a programmed soaking time. An auto reference elector elects the

most appropriate one from the reference inputs according to the reversion status, and each reference's priority and qualification. Reversion determines whether a higher priority qualified reference should preempt a qualified current selected reference. If none of the references input is qualified, hold-over or freerun mode will be elected depending on the availability of the holdover history.

Reference selection may be automatic, manual, or hard-wired manual. In automatic reference selection mode, the most appropriate one elected from the auto reference elector will be the selected reference input. In manual reference selection mode, user may specify any of the reference inputs as the selected reference input for external timing or holdover/freerun for self-timing. In hard-wired manual mode, user can hard-wired switch using control pin SRCSW between two pre-programmed reference inputs. The reference input elected from the auto reference elector will not affect the selected reference input in manual or manual mode.

External Frame Sync Inputs

The STC5425 has three external frame sync inputs at 2kHz or 8kHz on the pin EX_SYNC1, EX_SYNC2, EX_SYNC3, respectively. The frequency of the external frame sync inputs are auto-detected.

To achieve frame phase alignment, any one of the three external sync inputs may be selected as frame reference for selected REF1 to REF5 individually.

Timing Generators and Operation Modes

The STC5425 includes one timing generator. It can individually operate in **Freerun**, **Synchronized**, and **Holdover** mode. The timing generator is in either external-timing mode or self-timing mode. In external timing mode, PLL of the timing generator phase locks to the selected external reference input. In self-timing mode, the PLL simply tunes the clock synthesizers to a given fractional frequency offset. Synchronization is in external timing mode. PLL's loop bandwidth may be programmed to vary the timing generator's filtering function. Conversely, freerun and holdover are all in self-timing mode. When selected reference input and previous holdover history are unavailable, such as in system's initialization stage, freerun mode may be entered or used. When selected reference input is

unavailable, STC5425 may enter holdover using device holdover history acquired from the short-term holdover history. In STC5425, the freerun clock is derived from the MCLK (external TCXO or XO) and digitally calibrated to compensate the external oscillator's accuracy offset. STC5425 also allow users to program and manipulate the holdover history accumulators.

Phase Synchronization

In synchronized mode, the phase relationship between the selected reference input and the clock output may be phase arbitrary or frame phase align. An arbitrary phase relationship incorporates phase rebuild on reference input switching. Zero frame phase relationship is produced for the timing generator by programming as frame phase align mode. The STC5425 may accept external frame reference to achieve frame phase alignment in frame phase align mode. The frame reference and the frame edge may be configured independently for each individual reference input.

Clock Outputs

The STC5425 outputs 4 synchronized clock outputs: CLK1 is differential output (LVPECL or LVDS), CLK2 is LVC MOS output, one 8kHz and one 2kHz frame pulse clock outputs (LVC MOS). CLK1 and CLK2 can be derived from synthesizer G_1 and G_4 . See Figure 1 for functional details. Frequency of clock outputs CLK1 and CLK2 is programmable by programming frequency of synthesizers from 1MHz up to 156.25MHz, in 1kHz steps. Each of the synthesizers has different default frequency value. The STC5425 allows the user to program the phase skew of each clock synthesizer, up and down 50ns in roughly 0.024ns step to adjust the phase of clock outputs.

Frame pulse clock synthesizer generates frame pulse clock outputs CLK8K/CLK2K at frequency of 8kHz/2kHz. The duty-cycle of CLK8K and CLK2K is programmable.

Control Interfaces

Control interface of the STC5425 is composed of hardware control pins and the SPI bus interface. They provide application access to the internal control and status registers.

Field Upgradability

The STC5425 supports Field Upgradability which allows the user to load size of 7600 byte firmware configuration data (provided as per request) via bus interface. It provides the user a flexible field solution for different applications.

Advantage and Performance

The kernel of the timing generator is a DSP-based PLL. In STC5425, all internal modules are either digital or numerical, including the phase detectors, filters, and clock synthesizers. The revolutionary pure-digital design makes the timing generator become an accurate and reliable deterministic system. This modern technology removes any external component except the external oscillator. It provides excellent performance and reliability to STC5425.

Detailed Description

The STC5425 is a single chip solution for line card application in SDH, SONET, and Synchronous Ethernet network elements. The revolutionary pure-digital internal modules, DSP-based PLL and clock synthesizer are used in the device so that the overall characteristics are more stable compared to ones in traditional method.

Chip Master Clock

The STC5425 operates with an external oscillator (e.g., TCXO or XO) as its master clock on the pin MCLK. Generally, user should select an oscillator has great stability and low phase noise as the master clock (MCLK).

The device supports four different accepted frequencies of master clock: 10MHz, 12.8MHz, 19.2MHz, and 20MHz. Initial default accepted frequency of MCLK for STC5425 is 12.8MHz. When 10MHz, 19.2MHz, or 20MHz is selected as the frequency of MCLK, the user must write register **MCLK Freq Reset** three times consecutively, with no intervening read/writes from/to other register. An internal soft-reset will occur after three writes completed. The accepted frequency of MCLK input returns to 12.8MHz following any regular reset. See register **MCLK Freq Reset** for details.

In the meantime, the STC5425 allows user to read three values at the register **MCLK Freq Reset**: FRQID, COUNT, and ID Written Value.

FRQID

Indicates the ID of the frequency of MCLK that the STC5425 currently accept.

COUNT

Indicates how many times the register **MCLK Freq Reset** has been written to.

ID Written Value

Indicates the ID of associated value that is being written to the register **MCLK Freq Reset**.

See the register **MCLK Freq Reset** for more details.

Operation Mode

The STC5425 includes a timing generator that has a PLL individually operate in either external-timing or self-timing mode. In external timing mode, PLL of a timing generator phase-locks to a reference input. In self-timing mode, PLL simply operates with the external oscillator (MCLK). The STC5425 supports three operation modes: *freerun* (self-timing), *synchronized* (external-timing), and *holdover* (self-timing).

Freerun Mode

Freerun mode is typically used during system's initialization stage when none of reference inputs is available and the clock synchronization has not been achieved. The clock output generated from the STC5425 in freerun mode is relative to the internal freerun clock which is synthesized from MCLK. Frequency of the internal freerun clock can be calibrated by writing to the register **Freerun Cali**.

Synchronized Mode

In synchronized mode, the built-in PLL of the timing generator locks to the selected reference input. Each timing generator's loop bandwidth is independently programmable from 13Hz to 100Hz by writing to the register **Loop Bandwidth**. The noise transfer function of the PLL is determined according to the loop bandwidth and has maximum gain under 0.2dB. In synchronized mode, the phase relationship between the reference input and the clock output can be configured as arbitrary or aligned at register **Frame Phase Align**.

Holdover Mode

When none of reference inputs is available, holdover mode is used to maintain the frequency offset of the clock output closely to previous value generated when the selected reference input was valid. In hold-over mode, the clock output is synthesized from the MCLK along with device holdover history which is acquired from the short-term holdover history. Short term holdover history is accumulated by a built in programmable short-term history accumulator consecutively, which indicate the latest updated fractional frequency offset of the synchronous clock output. The bandwidth of the accumulator may be configured at the register **Short Term History Bandwidth**. The user can read the short-term history from register **Short Term Accu History**.

PLL Event In

The STC5425 provides direct communication with the PLL's timing generator by writing to the register **PLL Event In**. Following events can be triggered:

- **Relock**. PLL starts a relock process if this event is triggered. In frame phase align mode, PLL relocks to the reference input and the frame edge is re-selected as well. In phase arbitrary mode, PLL relocks to the reference input and restart the phase rebuild process.

Frame Phase Relationship

In synchronized mode, the phase relationship between the reference input and the clock output can be programmed to frame phase arbitrary or frame phase align.

Frame Phase Arbitrary

If phase arbitrary is selected, phase relationship between clock output and reference input is non-zero fixed value. Frame phase arbitrary incorporates phase rebuild function on reference input switching or mode switching. Hit-less switching is achieved with phase rebuild function and the impact on downstream is minimized. Frame phase arbitrary is enabled at the register **Frame Phase Align**.

Frame Phase Align

If frame phase align is selected, the clock output has zero frame phase relationship with the selected reference input. The STC5425 may accept external frame reference and select frame edge to achieve frame phase alignment for REF1 ~ REF5 individually. Both external frame reference and frame edge are selected at the register **Frame Phase Align**.

History of Fractional Frequency Offset

The STC5425 monitors and tracks the fractional frequency offset between the clock output and MCLK. The history data of the frequency offset is used by clock synthesizers to generate desired outputs while the timing generator is pending for reference input availability. A weighted 3rd order low-pass filter is used internally as short term history accumulators. A mature short term history is stored and further updated as device holdover history. It is used when the STC5425 operates in holdover mode.

Short-Term History

Short-term history is an average frequency offset between the clock output and MCLK which is filtered internally using a weighted 3rd order low-pass filter with the small time constant. The -3dB filter response point can be programmed from 0.16Hz to 1.3Hz by writing to the register **Short Term History Bandwidth**. Short-term history can be read from the register **Short Term Accu History**. Typically, short-term history is used by clock synthesizer in two conditions: First, it is used in between the transition of two different operation modes; second, it is used if LOS occurs when the STC5425 operates in synchronized mode with manually reference selection. In addition, short-term history is provided to perform failure diagnostics and evaluations.

Device Holdover History

Device holdover history is the history data used when the STC5425 runs in holdover mode. It is acquired from the short term history previously described. In synchronized mode, when timing generators PLL has locked to the selected reference input, the short term history is stored and further updated as the device holdover history. If LOS or LOL occurs, the device holdover history will stay at the latest updated value until re-enter the synchronized mode and the PLL locks to the replaced selected reference input. Its value can be read from the register **Device Holdover History**.

Phase-Locked Loop Status Details

The register **PLL Status** contains the detailed status of the PLLs, including the signal activity of the selected reference, the synchronization status, and the availability of the holdover histories.

SYNC bit

In external-timing mode, this bit indicates the achievement of synchronization. This bit will not be asserted in self-timing mode.

LOS bit

In external-timing mode, this bit indicates the loss of signal on the selected reference. This bit will not be asserted in self-timing mode.

LOL bit

In external-timing mode, the bit will be set if the PLL fails to achieve or maintain lock to the selected reference. This bit will not be asserted in self-timing mode.

It is also not complementary to the SYNC bit. Both bits will not be asserted when the PLL is in the pull-in process. The pull-in process usually occur when switch to a new selected reference or recover from the LOS/LOL.

OOP bit

This bit indicates that the selected reference is out of the pull-in range. This is meaningful only if in external-timing mode. This bit will not be asserted in self-timing mode. The frequency offset is relative to the digitally calibrated freerun clock.

SAP bit

This bit when set indicates that the PLL's output clocks have stopped following the selected reference because the frequency offset of the selected reference is out of pull-in range (OOP). User can write to the **Control Mode** register to program whether the PLL shall follow the selected reference outside of the specified pull-in range or just stay within the pull-in range boundary.

FEE bit

This bit indicates whether an error occurs in the frame edge detection process in slave mode or master phase align mode.

DHT bit

This bit indicates whether the device holdover history is tracking on the current selected reference (updating by the short-term history).

HHA bit

This bit indicates the availability of the device hold-over history.

Reference Inputs and External SYNC Inputs Details

The STC5425 accepts 5 external reference inputs. The reference inputs may be selected to accept either the auto-detect acceptable reference frequency which can be automatically detected or manually acceptable reference frequency. Reference inputs REF4 and REF5 are LVPECL/LVDS/LVCMOS and the remaining three are LVCMOS. All 5 reference inputs are monitored continuously for frequency, activity and quality. The timing generator may select any of the reference inputs when the device is external timing mode.

External Frame Sync Inputs

The STC5425 has three external frame sync inputs at 2kHz or 8kHz on the pin EX_SYNC1, EX_SYNC2, and EX_SYNC3 respectively. The frequency of the external frame sync inputs are auto-detected.

To achieve frame alignment, any one of the three external sync inputs may be selected as frame reference for selected REF1 to REF5 individually at the register Frame Phase Align. Sampling edge of the external sync inputs can be configured as falling or rising at the register EX SYNC Edge Config.

Acceptable Frequency and Frequency Offset Detection

The STC5425 can automatically detect the frequency of the reference input when the user enable the auto-detection function at the register **Ref Freq**. The acceptable auto-detect frequencies are: 8kHz, 64kHz, 1.544MHz, 2.048MHz, 19.44MHz, 38.88MHz, 77.76MHz, 6.48MHz, 8.192MHz, 16.384MHz, 25MHz, 50MHz or 125MHz. These frequencies can be detected automatically in the detector. The detector operates continuously to detect the frequency of reference inputs. Any carrier frequency change will be detected within 1ms. Each input is also monitored for frequency offset between input and the internal freerun clock. The frequency offset is a key factor to determine qualification of the reference inputs. See register **Ref Index Selector** and **Ref Info**.

STC5425 provides another option which allows the user to select the manually acceptable reference frequency for all the reference inputs, at the integer multiple of 8kHz ($N \times 8\text{kHz}$, N is integer from 1 to 32767). Hence the manually acceptable reference frequency range is integer multiple of 8kHz from 8kHz to 262.136MHz. When a manually acceptable reference frequency is used, the user need to access the register **Ref Freq** to set the integer N . Each input is monitored for frequency offset between input and the internal freerun clock. The frequency offset is shown in the register **Ref Info** when associate reference index is selected at the register **Ref Index Selector**.

Activity Monitoring

Activity monitoring is also a continuous process which is used to identify if the reference input is in normal. It is accomplished with a leaky bucket accumulation algorithm, as shown in Figure 2. The "leaky bucket" accumulator has a fill observation window that may

be set from 1 to 16ms, where any hit of signal abnormality (or multiple hits) during the window increments the bucket count by one. The leak observation window is 1 to 16 times the fill observation window. The leaky bucket accumulator decrements by one for each leak observation window that passes with no signal abnormality. Both windows operate in a consecutive, non-overlapping manner. The bucket accumulator has alarm assert and alarm de-assert thresholds that can each be programmed from 1 to 64.

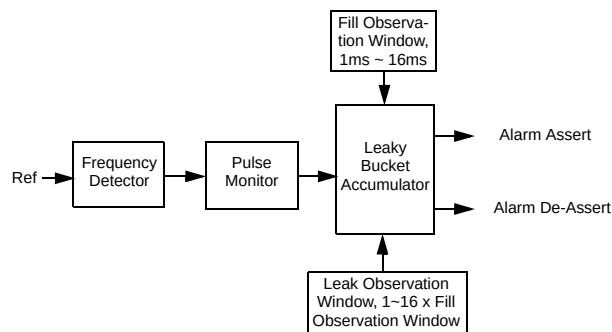


Figure 2: Activity Monitor

Applications can write to the following registers to configure the activity monitor: **Fill Obs Window**, **Leak Obs Window**, **Bucket Size**, **Assert Threshold**, and **De Assert Threshold**.

The activity monitor can be bypassed by setting the bucket size to 0. This operation de-asserts the activity alarms of all the references. A non-zero bucket size must be greater than or equal to the alarm assert threshold value. The alarm assert threshold value must be greater than the alarm de-assert threshold value and less than or equal to the bucket size value. Attempted writes of invalid values will be ignored. Therefore, user must carefully plan an appropriate sequence of writes when re-configure the activity monitor. See register **Bucket Size**, **Assert Threshold** and **De Assert Threshold** for details.

Alarms appear in the **Refs Activity** register. A "1" indicates activity, and a "0" indicates an alarm, no activity. Note that if a reference is detected as a different frequency, the leaky bucket accumulator is set to the bucket size value and the reference will become inactive immediately.

Input Qualification

A selected reference is "qualified" if it passes the activity evaluation and its frequency offset is within the programmed qualification range for over a pre-programmed soaking time.

A reference qualification range may be programmed up to 102.3 ppm by writing to register **Qualification Range**, and a disqualification range set up to 102.3 ppm, by writing to register **Disqualification Range**. The qualification range must be set less than the disqualification range. Additionally, qualification soaking time may be programmed from 0 to 63 seconds by writing to register **Qualification Soaking Time**. The pull-in range is the same as the disqualification range.

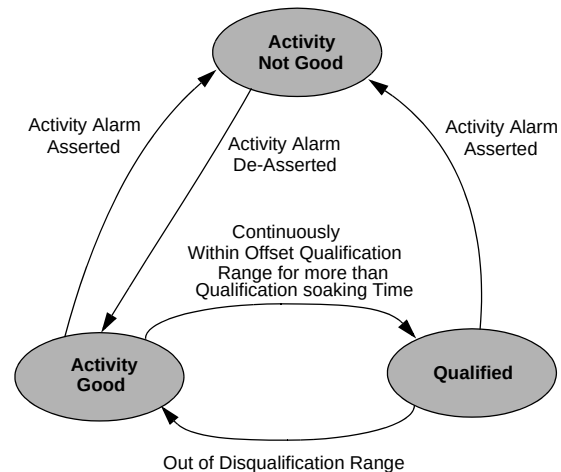


Figure 3: Reference Qualification Scheme

The frequency offset of each reference is relative to the internal freerun clock may be read by selecting the reference in the **Ref Info Selector** register and then reading the offset value from register **Ref Info**.

Figure 3 shows the reference qualification scheme. A reference is qualified if it has no activity alarm and is continuous within the qualification range for more than the qualification soaking time. An activity alarm or frequency offset beyond the disqualification range will disqualify the reference. It may then be re-qualified if the activity alarm is off and the reference is within the qualification range for more than the qualification time.

The reference qualification status of each reference

may be read from register **Ref Qual**.

Automatic Reference Election Mechanism

The STC5425 has an auto reference elector always elect the best candidate from the reference inputs according to the revertivity status, each reference's priority and qualification. This mechanism operates independent of reference selection mode. In other word, regardless what the current reference selection mode is, the auto reference elector always work in this mechanism. The detail description of the reference selection mode is in following sections.

The reference priority is indicated in the reference priority table which is shown in register **Ref Priority Table** individually for each timing generator. Each reference has one entry in the table, which may be set to value from 0 to 15. '0' revokes the reference from the election, while 1 to 15 set the priority, where '1' has the highest, and '15' has the lowest priority. The highest priority pre-qualified reference then is a candidate selected by the automatic reference elector. If multiple references share the same priority, the one that has been qualified for the longest time will be recommended to be the candidate. If the current highest priority reference input fails, the next-highest priority reference is selected as the candidate.

In order to avoid disturbance of the clock output, the candidate reference selected by automatic reference elector should be handled in two different mode. Revertive mode and non-revertive mode. The mode is determined by either enabling or disabling the "revertive" bit of the **Control Mode** to "1" for revertive or to "0" for non-revertive operation.

In revertive mode, the automatic reference elector will pre-empted the current candidate reference if the new recommended candidate reference has higher priority.

In non-revertive mode, the current candidate reference will not be pre-empted by any new candidate until it is disqualified.

If there is no candidate reference available, freerun or holdover will be recommended by the automatic reference elector depending on the holdover history availability.

Figure 4 shows the operation states for automatic reference elector.

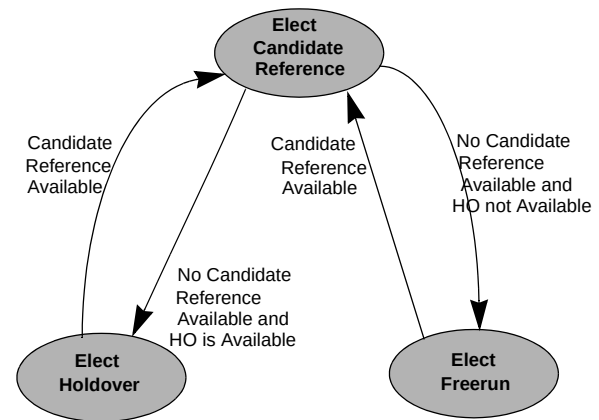


Figure 4: Automatic Reference Elector States

Automatic Reference Selection

The timing generators may be operated automatic reference input selection mode. The mode is selected via the **Control Mode** registers.

In automatic reference selection mode, the selected reference is the same reference elected by the automatic reference elector. The automatically selected reference for each PLL may be read from the Auto Select Ref registers.

Manual Reference Selection Mode

In manual reference selection mode, the user may select the reference manually. This mode is selected via the **Control Mode** registers. The reference is selected by writing to the **Manual Select Ref** registers. The user may also has the device enter freerun or holdover manually by writing to the **Manual Select Ref** registers.

Hard-wired Manual Reference Selection

Besides the manual reference selection mode, the STC5425 provides a special mode to switch between two pre-selected reference directly from a dedicated pin SRCSW. The two pre-selected references are configured at the register **Hard-wired Switch Pre Selection**. It can make the device enter the freerun or holdover by writing to the register **Hard-wired Switch Pre Selection**. In this mode, the pin SRCSW operates as a simple switch by setting high or low.

Clock Outputs Details

The STC5425 generates 1 synchronized differential (LVPECL or LVDS) clock output: CLK1; 3 LVCMOS clock outputs: CLK2, one 8kHz and one 2kHz frame pulse clock outputs. Figure 5, Figure 6, and Figure 7 respectively shows the clock output section for CLK1, CLK2, and CLK8K/CLK2K. Each output has individual clock output section consist of synthesizer and clock generator. Clock generator of CLK1 has LVPECL/LVDS driver to produce differential output. Clock generators of CLK2 include a mux and a LVCMOS signal driver. Clock generator of frame output CLK8K and CLK2K consist of a duty cycle controller and a LVCMOS driver.

Clock Synthesizers

The STC5425 has 3 clock synthesizers: synthesizer G₁, G₄ and one frame pulse clock synthesizer F; Clock synthesizers G₁ and G₄ produce frequencies from 1MHz to 156.25MHz, in 1kHz steps. Phase skew of these synthesizers are all programmable individually up and down 50ns. CLK1 is derived from synthesizer G₁. CLK2 can be derived from synthesizer G₄. Synthesizer F produces frame pulse at 8kHz and 2kHz with 50% duty cycle or programmable pulse width.

Clock Generators

Clock generator of CLK1 consist of a LVPECL/LVDS signal driver. The signal level of clock outputs CLK1 can be programmed to either LVPECL or LVDS. Clock generators of CLK2 consist of a LVCMOS driver. CLK2 is LVCMOS. Signal level is driven from LVCMOS driver in clock generator. The clock generator of frame pulse output CLK8K and CLK2K contains a duty cycle controller and a LVCMOS driver. The duty cycle is programmable at the register **CLK8K Sel** and **CLK2K Sel**.

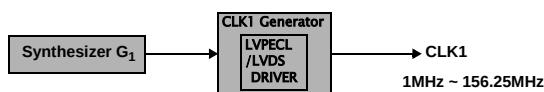


Figure 5: Output Clocks CLK1

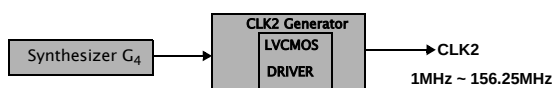


Figure 6: Output Clocks CLK2

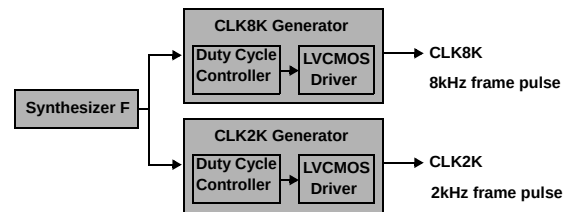


Figure 7: Output Clocks CLK8K and CLK2K

Clock Output Phase Alignment

Any of clock outputs which has frequency at the integer multiple of 8kHz is in phase alignment with the frame pulse output CLK8K if none of synthesizer skew is programmed.

Synthesizer Skew Programming

The STC5425 allows user to program the phase skew of each clock synthesizer, up and down 50ns in roughly 0.024ns steps. Since each of clock outputs is dedicate derived from its synthesizer respectively, adjust phase skew of the synthesizer will provide the associated clock output a phase skew adjustment. Phase skew of the synthesizers may be programmed at the register **Synth Skew Adj**.

Clock Outputs

Available frequencies of CLK1 and CLK2 are from 1MHz to 156.25MHz, in 1kHz steps. Phase skew is adjustable at the associate synthesizer level. Two clock outputs, CLK8K and CLK2K, generate two frame pulse clock at 8kHz and 2kHz.

Event Interrupts

The STC5425 events shown following below are interrupt events might occurred.

- Qualification status of the reference inputs change
- Activity status of the cross reference inputs change
- Selected reference of timing generator changes in automatic reference selection
- PLL status of timing generator changes
- Out-Event of timing generator asserts

The interrupt events can be read from the register **Interrupt Status**. Each bit indicates one events. The associate bit of the register **Interrupt Status** will not be changed automatically when the event is cleared. Therefore, the user need write '1' to the associate bit to erase the event.

The STC5425 has a pin EVENT_INTR (pin 8) for indicating the event interrupt occurrence. The pin may be wired to user's micro-controller. User can program the **Interrupt Mask** register to decide which of interrupt events will send an alarm to the micro-controller by asserting the EVENT_INTR pin. User can program at the **Interrupt Configuration** register to specify the logic level (active high or low) of the pin EVENT_INTR when it's triggered by the interrupt event. User may also program the **Interrupt Configuration** register to define pin states as tri-state or logic inactive when no interrupt event occurs.

Field Upgradability

The STC5425 supports field upgradability which allows the user to load size of 7600 byte firmware configuration data (provided as per request) via bus interface. Field upgrade can only be performed at least 3ms after reset.

1. User may read Bit READY of the register **Field Upgrade Status** to check if field upgrade is ready to start.
2. To begin the field upgrade, write to register **Field Upgrade Start** three times consecutively, with no intervening read/writes from/to other registers, see the register **Field Upgrade Start** for details.
3. Once the field upgrade process begins, the STC5425 is hold for data loading. Write 7600 bytes firmware configuration data to the register **Field Upgrade Data** one byte at a time to complete data loading. User can read the same register for the written byte. But no matter how many times the user read, only the last written byte will be read from the register.
4. Read the register **Field Upgrade Count** for how many bytes of configuration data has been loaded. Bit Load_Compelet of the register **Field Upgrade Status** will indicate whether the 7600 bytes loading is complete and meanwhile bit CHECKSUM will indicate the loading is failed or succeed. See register description of **Field Upgrade Status** for details.

Processor Interface Descriptions

The STC5425 supports SPI bus interface:

The SPI interface bus mode uses the $\overline{\text{CS}}$, SCLK, SDI, SDO pins, with timing as shown in Figure 8, Figure 9 and Figure 10. For read operation, serial data output can be read out from the STC5425 on either the rising or falling edge of the SCLK. The edge selection depends on pin CLKE logic level.

Serial Bus Timing

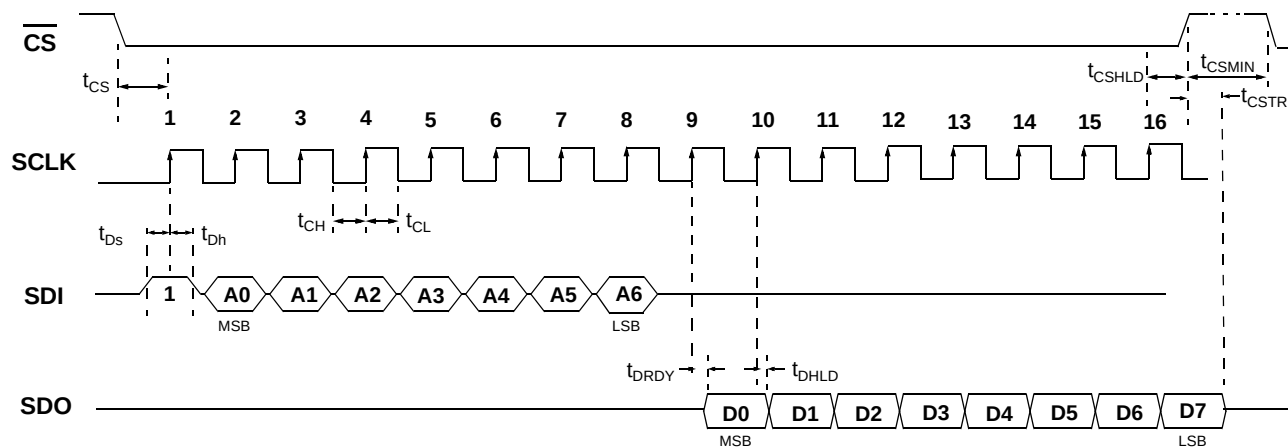


Figure 8: SPI Bus, Read access (Pin CLKE = Low)

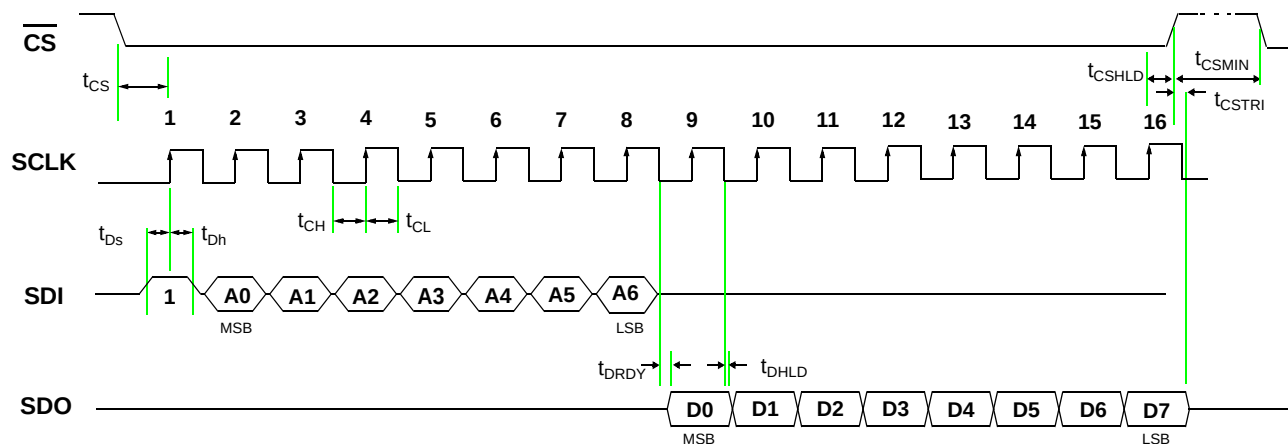


Figure 9: SPI Bus Timing, Read access (Pin CLKE = High)

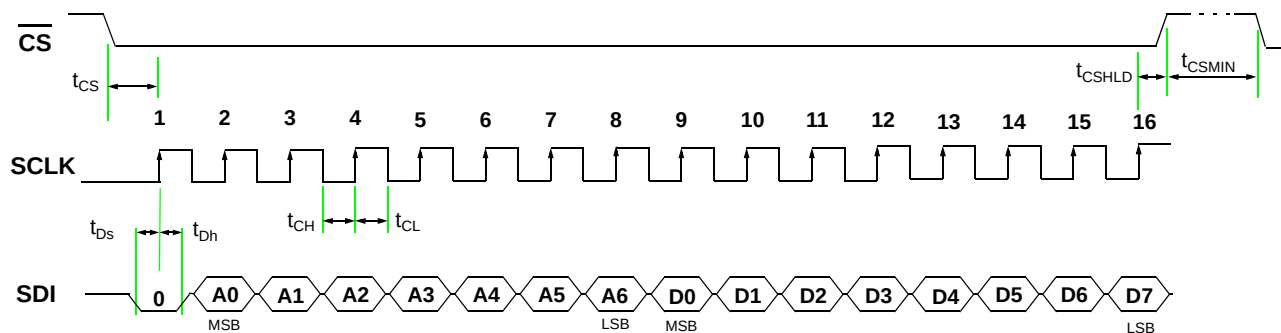


Figure 10:SPI Bus Timing, Write access

Table 7: SPI Bus Timing

Symbol	Description	Min	Max	Unit
t_{CS}	CS low to SCLK high	10		ns
t_{CH}	SCLK high time	25		ns
t_{CL}	SCLK low time	25		ns
t_{DS}	Data setup time	10		ns
t_{DH}	Data hold time	10		ns
t_{DRDY}	Data ready		7	ns
t_{DHLD}	Data hold	3		ns
t_{CSHLD}	Chip select hold	30		ns
t_{CSTRI}	Chip select to data tri-state		5	ns
t_{CSMIN}	Minimum delay between successive accesses	50		ns

Register Descriptions and Operation

General Register Operation

The STC5425 device has 1, 2, 3, and 4 byte registers. One-byte registers are read and written directly. Multiple -byte registers must be read and written in a specific manner and order, as follows:

Multibyte register reads

A multi byte register read must commence with a read of the least significant byte first. This triggers a transfer of the remaining byte(s) to a holding register, ensuring that the remaining data will not change with the continuing operation of the device. The remaining byte(s) must be read consecutively with no intervening read/writes from/to other registers.

Multibyte register writes

A multi byte register write must commence with a write to the least significant byte first. Subsequent writes to the remaining byte(s) must be performed in ascending byte order, consecutively, with no intervening read/writes from/to other registers, but with no timing restrictions. Multibyte register writes are temporarily stored in a holding register, and are transferred to the target register when the most significant byte is written.

Chip_ID, 0x00 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	0x25							
0x01	0x54							

Indicates chip's ID number

Chip_Rev, 0x02 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x02	Revision Number							

Indicates the revision number of STC5425

Chip_Sub_Rev, 0x03 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x03	Sub-Revision Number							

Indicates the firmware revision number of STC5425

Fill_Obs_Window, 0x07 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x07	Not used				Leaky bucket fill observation window, $m = 0 \sim 15$			

Sets the fill observation window size for the reference activity monitor to $(m+1)$ ms. The window size can be set from 1ms to 16ms.

Default value: $m = 0$, (1ms)

Leak_Obs_Window, 0x08 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x08	Not used				Leaky bucket fill observation window, $n = 0 \sim 15$			

Sets the leak observation window size for the reference activity monitor to $(n + 1)$ times the fill observation window size. The size can be set from 1 to 16ms times the fill observation window size.

Default value: $n = 3$, (4 times)

Bucket_Size, 0x09 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x09	Not used		Leaky bucket size, $0 \sim 63$					

Sets the leaky bucket size for the reference activity monitor. Bucket size equal to 0 will set the leaky bucket active monitor off, which will not assert activity alarm. The bucket size must be greater than or equal to the alarm assert value. Otherwise, the value will not be written to the register.

Default value: 20

Assert_Threshold, 0x0A (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0A	Not used		Leaky bucket alarm assert threshold, $1 \sim 63$					

Sets the leaky bucket alarm assert threshold for the reference activity monitor. The alarm assert threshold value must be greater than the de-assert threshold value and less than or equal to the bucket size value. Otherwise, the value will not be written to the register.

Default value: 15

De_Assert_Threshold, 0x0B (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0B	Not used		Leaky bucket alarm de-assert threshold, $0 \sim 62$					

Sets the leaky bucket alarm de-assert threshold for the reference activity monitor. The de-assert threshold value must be less than the assert threshold value. Otherwise, the value will not be written to the register.

Default value: 10

Freerun_Cali, 0x0C (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0C	Lower 8 bits of Freerun Calibration							
0x0D	Not used					Upper 3 bits of Freerun Calibration		

Freerun calibration, from -102.4 to +102.3 ppm, in 0.1ppm steps, 2's complement.

Default value: 0

Disqualification_Range, 0x0E (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0E	Lower 8 bits of Disqualification Range							
0x0F	Not used					Upper 2 bits Disqualification Range		

Reference disqualification range, from 0 to +102.3 ppm, in 0.1 ppm steps. This also sets the pull-in range. (See the **Reference Input Monitoring and Qualification** section). New disqualification range must be greater than qualification range in register Qualification_Range. Otherwise, the value will not be written to the register.

Default value: 360 (range = 36.0 ppm).

Qualification_Range, 0x10 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x10	Lower 8 bits of Qualification Range							
0x11	Not used					Upper 2 bits Qualification Range		

Reference qualification range, from 0 to +102.3 ppm, in 0.1 ppm steps. New qualification must be less than disqualification range. Otherwise, the value will not be written to the register.

Default value: 350 (range = 35.0 ppm).

Qualification_Soaking_Time, 0x12 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x12	Not used		0 ~ 63 s					

Sets the soaking time for reference qualification, from 0 to 63s, in 1s step.

Default value: 1 (1s)

Ref_Index_Selector, 0x13 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x13	Not used				REF1~REF5			

When frequency auto-detect function for reference inputs is enabled at the register **Ref_Info**:

- Determines which of reference inputs has the information (auto-detected frequency and frequency offset) shown in register **Ref_Info**.

When frequency auto-detect function is disabled and manually acceptable frequency is selected:

- Determines which of reference inputs is selected to accept the manually acceptable frequency. Refer to the register **Ref_Freq** for setting the integer N for associated manually acceptable frequency. The frequency offset of this selected reference input is shown in the register **Ref_Info**.

Field Value	Reference Inputs
1	Ref1
2	Ref2
5	Ref3
11	Ref4
12	Ref5

Invalid values will not be written to the register.

Default value: 1

Ref_Info, 0x14 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x14	Lower 8 bits of frequency offset							
0x15	Reference frequency				Upper 4 bits of frequency offset			

When frequency auto-detect function for reference inputs is enabled at the register **Ref_Info**:

- Indicates the frequency offset and frequency of the reference input selected by the register **Ref_Index_Selector**. Frequency offset is from -204.7 to +204.7 ppm relative to calibrated freerun, in 0.1 ppm steps, 2's complement. A value of -2048 indicates the reference is out of range.

When frequency auto-detect function is disabled and manually acceptable frequency is selected:

- Indicates only the frequency offset of the reference input selected by the register **Ref_Index_Selector**. Field value of Reference frequency (bit7~bit4) will be 15, which indicates manually acceptable frequency is selected for reference input. Refer to the register **Ref_Freq** for the manually acceptable frequency setting.

The auto-detect reference frequency is determined as follows ("Unknown" indicates a signal is present, but frequency is undetermined). If frequency auto-detect function is disabled at the register **Ref_Freq** and a manually acceptable reference input frequency is selected, field value of Reference Frequency is read as 15:

Field Value	Frequency
0	No signal
1	8 kHz
2	64 kHz
3	1.544 MHz

Field Value	Frequency
4	2.048 MHz
5	19.44 MHz
6	38.88 MHz
7	77.76 MHz
8	6.48MHz
9	8.192MHz
10	16.384MHz
11	25 MHz
12	50 MHz
13	125 MHz
14	Unknown
15	Manually acceptable frequency is being used

Refs_Activity, 0x16 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x16	Not used			Ref 5	Ref 4	Ref 3	Ref 2	Ref 1

Reference activity indicator.

0 = inactive, 1 = active

Refs_Qual, 0x18 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x18	Not used			Ref 5	Ref 4	Ref 3	Ref 2	Ref 1

Reference qualification indicator.

0 = not qualified, 1 = qualified.

Interrupt_Event_Sts, 0x1A (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1A	Not used			Event 4	Event 3	Event 2	Not used	Event 0

Event 0	Reference qualification status changed
Event 1	Reserved
Event 2	Selected reference changed in auto selection mode
Event 3	PLL status changed
Event 4	Timing generator's out-event occurred

Interrupt event status.

0 = no event, 1 = event occurred.

Interrupts are cleared by writing "1" to the bit positions to be cleared.

Default value: 0

Interrupt_Event_Enable, 0x1B (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1B	Not used			Event 4	Event 3	Event 2	Not used	Event 0

Event 0	Reference qualification status changed
Event 1	Reserved
Event 2	Selected reference changed in auto selection mode
Event 3	PLL status changed
Event 4	Timing generator's out-event occurred

Selects which of events will assert the pin EVENT_INTR to active mode (See register **Interrupt_Config**).
0 = mask out, 1 = enable

Default value: 0

Interrupt_Config, 0x1C (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1C	Not used						Idle mode	Signal active state

Signal active state

Specify the signal active state at pin EVENT_INTR
0 = active low. 1 = active high

Idle mode

Specify the state of pin EVENT_INTR when no interrupt event occurs.
0 = tri-state. 1 = logic inactive

Default value: 0

Hard-wired_Switch_Pre_Selection, 0x1D (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1D	Pre-selected reference number 2				Pre-selected reference number 1			

Pre select reference number 1 and reference number 2 in hard-wired manual reference selection mode. This mode is controlled by pin SRCSW. When pin SRCSW is LOW, reference number 1 is pre-selected. When pin SRCSW is HIGH, reference number 2 is pre-selected. It only can be configured when bit7 of Control_Mode register is set to 1 (See register **Control_Mode**).

Field Value	Selection
0	Freerun
1~5	Ref1~Ref5
13	Holdover
14,15	Reserved

Default value: 0

SRCSW_States, 0x1E (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1E	Not used							Pin states

Indicates states of pin SRCSW.
0 = Low; 1 = High

Default value: 0

Control_Mode, 0x20 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x20	Hard-wired_Switch	Not used	SAP	Ref_Sel_Mode	Revertive	Not used		

Mode control bits for individual timing generator.

Revertive

Selects the revertive mode or non-revertive mode of the auto selector.
0 = Non-revertive; 1 = Revertive

Ref_Sel_Mode

Determines reference selection mode.
0 = Manual; 1 = Auto

This bit may be overridden by bit7 of this register.

SAP

In manual mode, when the selected reference is out of the pull-in range, as specified in register **Disqualification_Range**. SAP determine whether clock output will follow the reference input
0 = Follow, 1 = Stop following at pull-in range boundary

Hard-wired_Switch

*0 = Not Hard-wired Switch, selects reference in manual selection mode or auto selection mode;
1 = Hard-wired Switch, selects reference in hard-wired manual selection mode by using control pin
SRCSW to hard-wired manual switch between two pre-selected reference inputs.
See register **Hard-wired_Switch_Pre_Selection**.*

Default value: 0

Loop_Bandwidth, 0x21 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x21	Bandwidth select							

Sets each timing generator's loop bandwidth:

Field Value	Bandwidth, Hz
0	103
1	52
2	27
3	13
255 ~ 4	Reserved

Default value: 2

Auto_Elect_Ref, 0x22 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x22	Not used				Auto selected reference			

Indicates the auto-elect reference. The auto-elect reference is elected according to revertivity status, and each reference's priority and qualification. Reference auto-elect also elect the reference in manual reference selection mode.

Bit 3 ~ Bit 0	Selection
0	Freerun
1 ~ 5	Sync with Ref 1 ~ Ref 5
6 ~ 12	Reserved
13	Holdover
14, 15	Reserved

Manual_Select_Ref, 0x23 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x23	Not used				Manually selected reference			

When manual reference selection mode is selected:

Selects the reference or set to freerun/holdover.

Bit 3 ~ Bit 0	Selection
0	Freerun
1 ~ 5	Sync with Ref 1 ~ Ref 5
6 ~ 12	Reserved
13	Holdover
14, 15	Reserved

When hard-wired manual reference selection mode is selected:

The register is read only and indicates the current reference defined by pin SRCSW and the register **Hard-wired_Switch_Pre_Selection**.

Default value: 0

Selected_Ref, 0x24 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x24	Not used				Current selected reference			

Indicates the current selected reference or operation mode.

Field Value	Current selected reference
0	Freerun
1~5	Sync with Ref 1 ~ Ref 5
6 ~ 12	Reserved
13	Holdover
14, 15	Reserved

Device_Holdover_History, 0x25 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x25	Bits 0 - 7 of 32 bit Device Holdover History							
0x26	Bits 8 - 15 of 32 bit Device Holdover History							
0x27	Bits 16 - 23 of 32 bit Device Holdover History							
0x28	Bits 24 - 31 of 32 bit Device Holdover History							

The accumulated device holdover history relative to MCLK. 2's complement. Resolution is 0.745×10^{-3} ppb.

Short_Term_Accu_History, 0x2D (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x2D	Bits 0 - 7 of 32 bit Short term History							
0x2E	Bits 8 - 15 of 32 bit Short term History							
0x2F	Bits 16 - 23 of 32 bit Short term History							
0x30	Bits 24 - 31 of 32 bit Short term History							

Short term accumulated history relative to MCLK. 2's complement. Resolution is 0.745×10^{-3} ppb.

Short_Term_History_Bandwidth, 0x35 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x35	Not used				Short Term History Accumulator Bandwidth		Not used	

Bandwidth of short term holdover history accumulator.

Bits 3 ~ 2	Short Term History -3dB Bandwidth
0	1.3 Hz
1	0.64 Hz
2	0.32 Hz
3	0.16 Hz

Default value: 4 (0.64Hz)

Ref_Priority_Table, 0x36 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x36	Ref 2 Priority				Ref 1 Priority			
0x37	Ref 4 Priority				Ref 3 Priority			
0x38	Not used				Ref 5 Priority			

Reference selection priority for REF1 to REF5. Lower values have higher priority:

Bits 7~4/Bits 3~0	Reference Priority
0	Revoke from auto reference elector
1 ~ 15	Value 1 ~ 15

Default value: 0

PLL_Status, 0x3C (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3C	HHA	DHT	FEE	SAP	OOP	LOL	LOS	SYNC

SYNC Indicates whether synchronization has been achieved

0 = Not synchronized

1 = Synchronized

LOS Loss of signal of the selected reference

0 = No Loss

1 = Loss (Indicate loss of signal, freerun, and holdover)

LOL Loss of lock (Failure to achieve or maintain lock)

0 = No loss of lock

1 = Loss of lock (Indicate loss of lock, freerun, and holdover)

OOP Out of pull-in range. Indicate the frequency offset of the selected reference input is out of pull-in range.

1 = Out of pull-in range

0 = In range

SAP Indicates whether the clock output have stopped following the selected reference, caused by out of

pull-in range

1 = Stop following at pull-in range boundary

0 = Following

FEE Frame edge error. Indicates whether an error occurs when select frame edge in frame phase align mode. Frame edge on the reference input is selected at the register **Frame_Phase_Align**
1 = Frame edge error occurs
0 = No frame edge error occurs

DHT Device Holdover History tracking
1 = Device holdover history is being tracked.
0 = Device holdover history is based on the last available history.

HHA Device Holdover History Availability.
1 = Available
0 = Not available

PLL_Event_Out, 0x3E (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3E	TBD							

PLL_Event_In, 0x3F (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3F	Not used							Relock

Writing 1 to trigger the event. If the event is acknowledged by the STC5425, event bit is cleared to be 0.

Event Relock:

PLL relocks the selected reference input. If the device operates in phase-align mode, PLL reselects the frame edge, relocks and frame phase align to the reference input. If the device operates in non phase-align mode, PLL relocks to the reference input and start over phase rebuild process.

Default value: 0

EX_SYNC_Edge_Config, 0x40 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x40	Not used					EX_SYNCN3 edge	EX_SYNCN2 edge	EX_SYNCN1 edge

Select sampling edge (falling or rising) of the external frame reference input EX_SYNC1, EX_SYNC2, or EX_SYNC3.

Bits 0/1/2	Edge Select
0	Falling edge
1	Rising edge

Default value: 7

Frame_Phase_Align, 0x42 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x42	Frame Phase Alignment and Edge Selection for Ref2		Frame Reference Selection for Ref2		Frame Phase Alignment and Edge Selection for Ref1		Frame Reference Selection for Ref1	
0x43	Not used				Frame Phase Alignment and Edge Selection for Ref3		Frame Reference Selection for Ref3	
0x44	Frame Phase Alignment and Edge Selection for Ref5		Frame Reference Selection for Ref5		Frame Phase Alignment and Edge Selection for Ref4		Frame Reference Selection for Ref4	

Selects frame reference input and the sampling of the selected reference for frame alignment.

Frame reference input selection:

Selects any one from the three external sync inputs as frame reference for Ref1~Ref5 individually. External sync inputs can take frequency of 2kHz or 8kHz and this frequency is auto-detectable. When none of frame reference inputs is used, set 0 to select its own frame pulse output of CLK8K as frame reference.

Bits 1 ~ 0 Bits 5 ~ 4	Frame Reference Select
0	Frame pulse output of CLK8K generated from the device
1	Frame reference input EX_SYNC1
2	Frame reference input EX_SYNC2
3	Frame reference input EX_SYNC3

Frame phase alignment and edge selection:

Selects either frame phase arbitrary mode or frame phase align mode. Selects the sampling edge on the selected reference input in phase align mode. If phase arbitrary mode is selected, any selection of frame reference will be dismissed.

Bits 3 ~ 2 Bits 7 ~ 6	Frame phase alignment	Frame Edge of Selected Reference Select
0	Frame phase arbitrary mode	Dismiss frame reference selection
1	Frame phase align mode	Rising edge nearest to the frame pulse on the external frame reference input
2		Rising edge previous to the frame pulse on the external frame reference input
3		Rising edge next to the frame pulse on the external frame reference input

Default value: 0

Synth_Index_Select, 0x4A (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x4A	Not Used				Synthesizer index selection for synthesizer frequency and phase skew adjustment			

Determines which synthesizer is selected for setting frequency value at the register **Synth_Freq_Value** and adjusting phase skew at the register **Synth_Skew_Adj**. When written value is 0, it can only adjust phase skew for synthesizer F. Since frequency of synthesizer F is fixed at 8kHz and 2kHz, the register **Synth_Freq_Value** is not writable to set frequency of synthesizer F.

Field Value	Synthesizer
0	Synthesizer F
1	Synthesizer G ₁ (for CLK1)
4	Synthesizer G ₄ (for CLK2)

Default value: 0

Synth_Freq_Value, 0x4B (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x4B	Bits 0-7 of 18 bits Synthesizer Frequency Selection							
0x4C	Bits 15-8 of 18 bits Synthesizer Frequency Selection							
0x4D	Not used						Bits 17-16 of 18 bits Synthesizer Frequency Selection	

Selects synthesizer frequency value from 1MHz to 156.25MHz, in 1kHz steps, based on which synthesizer index is selected at register **Synth_Index_Select**. See register description of the register **Synth_Index_Select**. If index of synthesizer F is selected, the register is read only.

Default value varies with synthesizer index selection at the register **Synth_Index_Select**, refer to table below:

Synthesizer Index Selection	Default Value
Synthesizer G ₁	155520 (155.52MHz)
Synthesizer G ₄	38880 (38.88MHz)

Written values less than 1000 or greater than 156250 are invalid.

Synth_Skew_Adj, 0x4E (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x4E	Lower 8 bits of Synthesizer Phase Skew Adjustment							
0x4F	Not used				Higher 4 bits of Synthesizer Phase Skew Adjustment			

Phase skew adjust for synthesizers based on which synthesizer index is selected at the register **Synth_Index_Select**. See description of the register **Synth_Index_Select**. The adjustment is from -6400/128 ns to 6396.875/128 ns, which is -50ns ~ 49.976 ns, in 3.125/128 ns steps, 2's complement.

Default value: 0 (For all the synthesizers)

CLK1_Signal_Level 0x50 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x50	Not used							CLK1 Signal Level

Selects the signal level for clock outputs CLK1
0 = LVPECL, 1 = LVDS

Default value: 0

CLK1_Sel, 0x51(R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x51	Not used						CLK1 Synthesizer Select	

Selects clock output CLK1 derived from synthesizer G₁ or put in tri-state.

Bits 1 ~ 0	CLK1 Synthesizer Select
0, 2, 3	Put CLK1 in tri-state mode
1	Synthesizer G ₁

Default value: 0

CLK2_Sel, 0x52 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x52	Not used						CLK2 Synthesizer Select	

Selects the clock output CLK2 derived from synthesizer G₄. Signal level of CLK2 is LVCMOS.

Bits 1 ~ 0	CLK3 Synthesizer Select
0, 2, 3	Put CLK2 in tri-state mode
1	Synthesizer G ₄

Default value: 0

CLK8K_Sel, 0x59 (R/W)
CLK2K_Sel, 0x5A (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x59	Not used	Invert	Duty Cycle Select					
0x5A	Not used	Invert	Duty Cycle Select					

Selects duty cycle of the 8kHz and 2kHz frame clock output generated from synthesizer F and determine whether the CLK8K or CLK2K is inverted. Default is not inverted and pulsed on the rising edge.

Bit 5 ~ 0	Duty Cycle Select
0	Disabled and tri-state
1~62	Pulse width 1 to 62 cycle of 155.52MHz
63	50% duty cycle

Bits 6	Invert
0	Not inverted (frame pulsed on rising edge)
1	Inverted (frame pulsed on falling edge)

Default value: 63 (50% duty cycle, not inverted)

Ref_Freq, 0x5B (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x5B	Lower 8 bits of integer N Select							
0x5C	Not used	Higher 7 bits of integer N Select						

Select the integer N for the manually acceptable reference frequency at Nx8kHz (N is integer from 1 to 32767) for REF1~REF5. Select which of reference input depends on the index selected at the register **Ref_Index_Selector**.

Setting this register to 0 is to enable the automatically detection for reference input frequency. The auto-detect acceptable reference input frequencies is shown in Table 4.

Setting integer N (from 1 to 32767) at this register allows user to manually select the acceptable reference input frequency at the integer multiple of 8kHz, range from 8kHz to 262.136MHz. For instance, user can select integer N = 32000 to manually accept frequency at 32000x8kHz = 256MHz.

Field Value	Integer N Select
0	Enable auto detection for reference input
1~32767	Integer N for the manual acceptable reference frequency

Default value: 0

Field_Upgrade_Status, 0x70 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x70	Not used					Load_Complete	READY	Checksum

Checksum

Checks whether the 7600 bytes firmware configuration data is loaded successfully.

0 = Fail, 1 = Success

READY

Indicates if field upgrade is ready to begin, normally is set to 1 at 3 milliseconds (3ms) after the reset.

0 = Not ready

1 = Ready

Load_Complete

Indicates whether the loading of 7600 bytes firmware configuration data is complete.

0 = Not complete

1 = Complete

Field_Upgrade_Data, 0x71 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x71	Field upgrade of firmware configuration data							

Writes the firmware configuration data (7600 bytes) to this register one byte at a time to complete data loading. Only the last written byte can be read from this register, regardless how many times of reads performed.

Default value: 0

Field_Upgrade_Count, 0x72 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x72	Lower 8 bits of byte count for firmware configuration data							
0x73	Not used				Higher 5 bits of byte count for firmware configuration data			

Reads this register for how many bytes of 7600 bytes firmware configuration data has been loaded through the register **Field_Upgrade_Data**.

Default value: 0

Field_Upgrade_Start, 0x74 (W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x74	Start field upgrade							

If bit READY of the register **Field Upgrade Status** is set to 1, user can write three values to this register consecutively, with no intervening read/writes from/to other registers to start the process of field upgrade. 7600 bytes firmware configuration data can only start loading after the three values are written successfully.

Write Sequence	Bit 7 ~ 0
First	0x51
Second	0x52
Third	0x53

MCLK_Freq_Reset, 0x7F (R/W)

Register Writes:

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x7F	External oscillator frequency selection							

Select accepted frequency of MCLK input by writing the associated value to this register three times consecutively, with no intervening read/writes from/to other register. The associated values for the four accepted frequency (10MHz, 12.8MHz, 19.2MHz, 20MHz) are as shown in table below. Three times of consecutive writes will trigger internal soft-reset. Initial default accepted frequency for STC5425 is 12.8MHz. The accepted frequency of MCLK input returns to 12.8MHz following any regular reset.

Perform writes at least 50us after the regular reset has done.

Written value is shown below:

Bit 7 ~ 0	External Oscillator Frequency Selection
0x11	10MHz
0x22	12.8MHz
0x44	19.2MHz
0x88	20MHz

Register Read:

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x7F	FRQID		COUNT		ID_Written_Value			

FRQID

Indicates the ID of the frequency of MCLK that the STC5425 currently accept. Constant 1 can be read from FRQID initially since the default accepted frequency for the STC5425 is 12.8MHz. The value of FRQID can only be updated when three consecutive valid writes are written to the register **MCLK_Freq_Reset** completely.

Bit 7 ~ 6 FRQID	MCLK Frequency
0	10MHz
1	12.8MHz
2	19.2MHz
3	20MHz

COUNT

Indicates how many times this register has been written to. COUNT is set to 1 when each time a different valid associated value is written to for the first time. COUNT is clear to 0 after three times valid writes are completed.

Bit 5 ~ 4 COUNT	Counter
0	Not written or complete one soft-reset cycle
1	Once
2	Twice
3	Three times

ID_Written_Value

Indicates the ID of the associated value that is being written to this register. The ID is updated when each time a different valid associated value is written to this register for the first time.

As described above in Register Writes, the associated value should be written to three times consecutively, with no intervening read/writes from/to other register. If the written value is invalid or the consecutive writes operation is interrupted by reading/writing from/to other register, ID_Written_Value is clear to 0.

Bit 3 ~ 0 ID_Written Value	Written value to this register (0x7F)
0	Not written
1	0x11
2	0x22
4	0x44
8	0x88

Default value: 0x40 (12.8MHz)

Noise Transfer Functions

User may write to register **Loop Bandwidth** to set the PLL loop bandwidth for each timing generator. The noise transfer function of the PLL filter is determined by the loop bandwidth. Figure 11 shows the noise transfer functions as the loop bandwidth vary from 100mHz to 103Hz.

TBD

Figure 11: Noise Transfer Functions

Order Information

All STC5425 parts are RoHS 6/6 compliant.

<u>Part Number</u>	<u>Description</u>
STC5425	Industrial Temperature Range Model (-40°C ~ +85 °C)

Application Notes

This section describes typical application use of the STC5425 device. The General section applies to all application variations.

General

Power and Ground

Well-planned noise-minimizing power and ground are essential to achieving the best performance of the device. The device requires 3.3V digital power and analog power input.

It is desirable to provide individual 0.1uF bypass capacitors, located close to the chip, for each of the power input leads, subject to board space and layout constraints.

Ground should be provided by as continuous a ground plane as possible. A separated analog ground plane is recommended.

Note: Un-used reference inputs must be grounded.

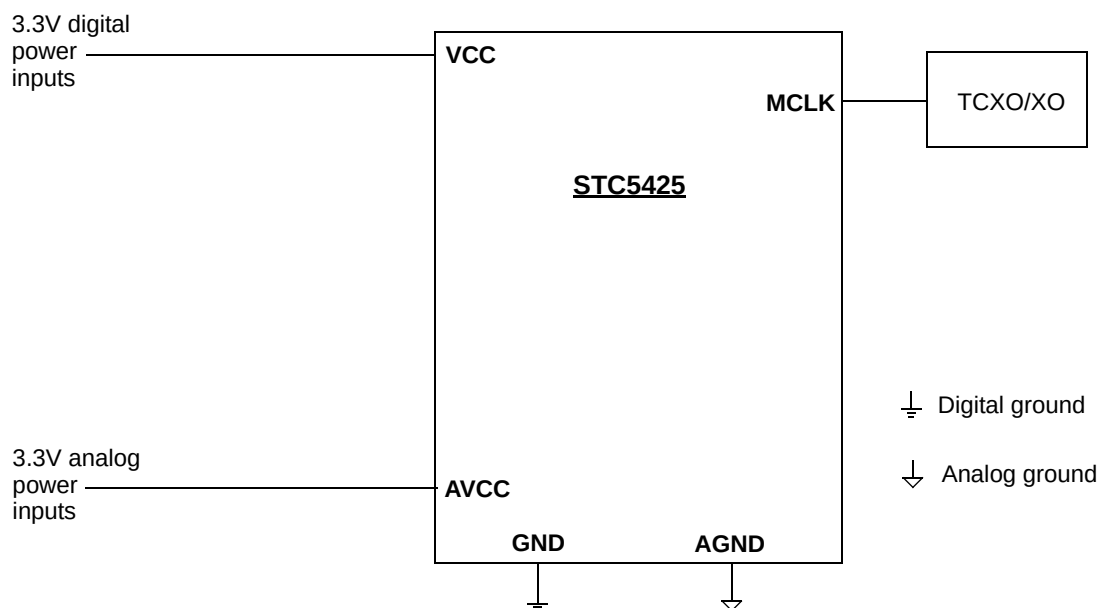
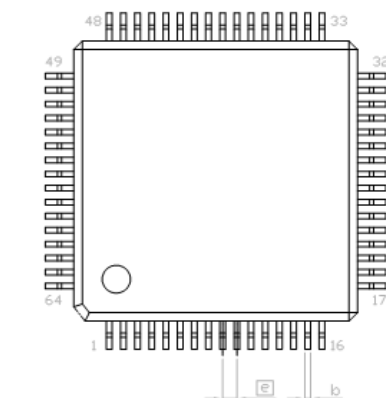


Figure 12: Power and Ground

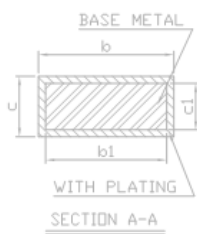
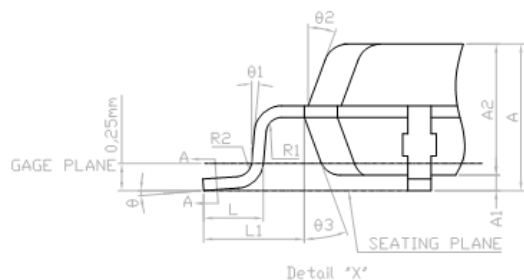
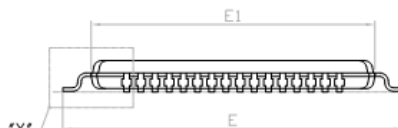
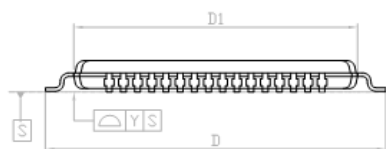
Master Oscillator

An external 3.3V LVCMOS level clock (generally driven from TCXO or XO) is supplied at pin MCLK as master clock. TCXO or XO should be carefully chosen as required by application. It is recommended that the oscillator is placed close to the STC5425. Frequency of the master oscillator has four options, see description of the register **MCLK Freq Rest** for details.

Mechanical Specifications



NOTES:
1.REFER TO JEDEC MS-026(ISSUE D) / ACD
2.DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
ALLOWABLE PROTRUSION IS 0.25mm PER SIDE D1 AND E1 ARE
MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE
DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED
THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
4.ALL DIMENSIONS IN MILLIMETERS.



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1,20			47
A1	0,05		0,15	2		6
A2	0,95	1,00	1,05	37	39	41
b	0,17	0,22	0,27	7	9	11
b1	0,17	0,20	0,23	7	8	12
c	0,09		0,20	4		8
c1	0,09		0,16	4		6
D	11,90	12,00	12,10	368	472	476
D1	9,90	10,00	10,10	390	394	398
E	11,90	12,00	12,10	368	472	476
E1	9,90	10,00	10,10	390	394	398
□	0,50 BSC			20 BSC		
L	0,45	0,60	0,75	18	24	30
L1	1,00 REF			39 REF		
R1	0,08			3		
R2	0,08		0,20	3		8
Y			0,08			3
θ	0°	3,5°	7°	0°	3,5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

Revision History

The following table summarizes significant changes made in each revision. Additions reference current pages.

Revision	Change Description	Pages
P1	Initial datasheet at Preliminary status	
P1.1	Change bits arrangement of register Ref_Priority_Table	9, 34
P1.2	Add mechanical specifications	46
P1.3	Correct SDI of of SPI Bus Timing, Write access	24

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