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ECL Products	

100158

Shift Matrix

FEATURES

- Typical propagation delay: 1.9ns
- Typical supply current ($-I_{EE}$): 118mA

DESCRIPTION

The 100158 contains a combinatorial network which performs the function of an

8-bit Shift Matrix. Three control lines (S_n) are internally decoded to define the number of places which an 8-bit word, present at the inputs (D_n), is shifted to the right. The shifted word appears on the outputs Q_n . A Mode Control is provided which, if Low, forces Low all outputs to the left of the one that contains D_7 . This operation is sometimes referred to as low backfill. If M

is High, a circular shift is performed, such that D_0 appears at the output just to the left of the one that contains D_7 . This operation is commonly referred to as barrel shifting.

All unused inputs can be left open due to integrated pull-down resistors.

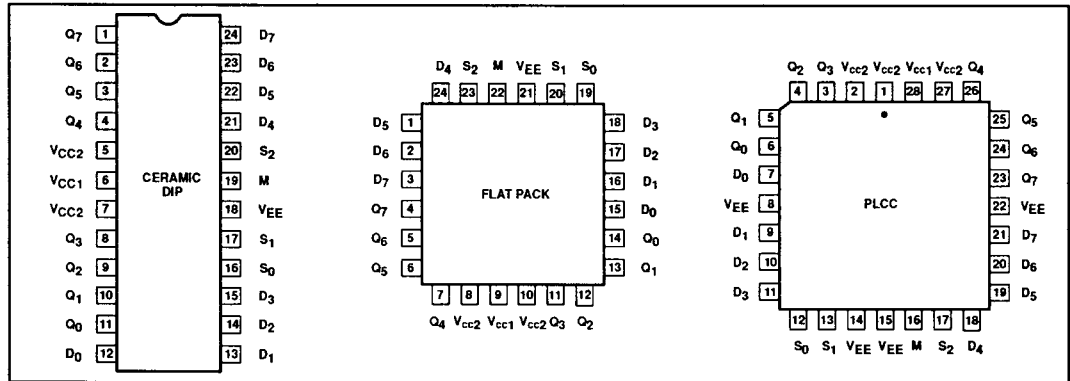
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_7$	Data Inputs
$S_0 - S_2$	Select Inputs
M	Mode Control Input
$Q_0 - Q_7$	Data Outputs

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Ceramic DIP (400 mils wide)	100158F
24-Pin Ceramic Flat Pack	100158Y
28-Pin PLCC	100158A

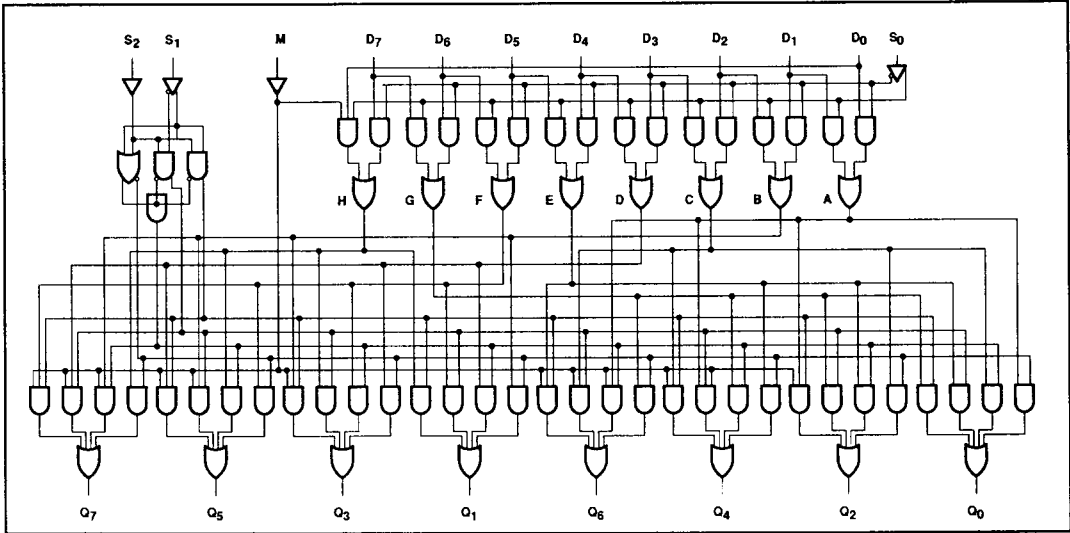
PIN CONFIGURATIONS



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LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS							
M	S ₂	S ₁	S ₀	Q ₇	Q ₆	Q ₅	Q ₄	Q ₃	Q ₂	Q ₁	Q ₀
X	L	L	L	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
L	L	L	H	L	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁
L	L	L	L	L	L	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂
L	L	L	H	L	L	L	D ₇	D ₆	D ₅	D ₄	D ₃
L	L	H	L	L	L	L	L	D ₇	D ₆	D ₅	D ₄
L	L	H	L	L	L	L	L	L	D ₇	D ₆	D ₅
L	L	H	H	L	L	L	L	L	L	D ₇	D ₆
L	L	H	H	L	L	L	L	L	L	L	D ₇
H	L	L	H	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁
H	L	L	L	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂
H	L	L	H	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃
H	L	L	L	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄
H	L	H	L	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅
H	L	H	L	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆
H	L	H	H	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2} = \text{ground}$, $T_A = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ unless otherwise specified:

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	-7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	-55	mA
T_S	Storage temperature range	-65 to +150	$^{\circ}\text{C}$
T_J	Maximum junction temperature	+150	$^{\circ}\text{C}$

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

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DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		-4.8	-4.5	-4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		-5.7			V
V_{IH}	High level input voltage	$V_{EE} = -4.2V$	-1150		-880	mV
		$V_{EE} = -4.5V$	-1165			
		$V_{EE} = -4.8V$	-1165			
V_{IL}	Low level input voltage	$V_{EE} = -4.2V$	-1810		-1475	mV
		$V_{EE} = -4.5V$			-1475	mV
		$V_{EE} = -4.8V$			-1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:

When operating at other than the specified V_{EE} voltages (-4.2V, -4.5V, -4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -4.8V \text{ to } -4.2V$, $T_A = 0^\circ\text{C to } +85^\circ\text{C}$ unless otherwise specified^{1,3,4}

SYMBOL	PARAMETER	TEST CONDITIONS ²			LIMITS			UNIT
					MIN.	TYP.	MAX.	
V _{OH}	High level output voltage	Outputs loaded with 50Ω to −2.0V ±0.010V	Inputs at V _{IHMAX} or V _{ILMIN}	V _{EE} = −4.2V	−1020		−870	mV
				V _{EE} = −4.5V	−1025	−955	−880	mV
				V _{EE} = −4.8V	−1035		−880	mV
V _{OHT}	High level output threshold voltage		Apply V _{IHMIN} or V _{ILMAX} to one input at a time. Other inputs at V _{IHMAX} or V _{ILMIN} .	V _{EE} = −4.2V	−1030			mV
			V _{EE} = −4.5V	−1035			mV	
			V _{EE} = −4.8V	−1045			mV	
V _{OLT}	Low level output threshold voltage		Apply V _{IHMIN} or V _{ILMAX} to one input at a time. Other inputs at V _{IHMAX} or V _{ILMIN} .	V _{EE} = −4.2V			−1595	mV
			V _{EE} = −4.5V			−1610	mV	
			V _{EE} = −4.8V			−1610	mV	
V _{OL}	Low level output voltage		Inputs at V _{IHMAX} or V _{ILMIN} .	V _{EE} = −4.2V	−1810		−1605	mV
			V _{EE} = −4.5V	−1810	−1705	−1620	mV	
			V _{EE} = −4.8V	−1830		−1620	mV	
I _{IH}	High level input current	One input under test at V _{IHMAX} . Other inputs at V _{ILMIN} .					220	μA
I _{IL}	Low level input current	One input under test at V _{ILMIN} . Other inputs at V _{IHMAX} .			0.5			μA
−I _{EE}	V _{EE} supply current	All inputs at V _{IHMAX}			84	118	205	mA

NOTES:

- The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
- Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
- The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
- The device can function down to $V_{EE} = -5.7V$, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

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AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -4.8\text{V}$ to -4.2V

Ceramic DIP $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -4.6\text{V to } -4.2\text{V}$									
SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0^{\circ}\text{C}$		$T_A = +25^{\circ}\text{C}$		$T_A = +85^{\circ}\text{C}$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.10 1.10	3.00 3.00	1.10 1.10	2.90 2.90	1.10 1.10	3.10 3.10	ns ns
t_{PLH} t_{PHL}	Propagation delay M to Q_n		1.15 1.15	4.40 4.40	1.25 1.25	4.40 4.40	1.15 1.15	4.70 4.70	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to Q_n		1.70 1.70	4.50 4.50	1.70 1.70	4.50 4.50	1.70 1.70	4.80 4.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n		0.50 0.50	2.20 2.20	0.50 0.50	2.20 2.20	0.50 0.50	2.20 2.20	ns ns

NOTE:

For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2\text{V} \pm 5\%$

Ceramic DIP $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 5\%$									
SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0^{\circ}\text{C}$		$T_A = +25^{\circ}\text{C}$		$T_A = +85^{\circ}\text{C}$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.10 1.10	3.00 3.00	1.10 1.10	2.90 2.90	1.10 1.10	3.10 3.10	ns ns
t_{PLH} t_{PHL}	Propagation delay M to Q_n		1.15 1.15	4.40 4.40	1.25 1.25	4.40 4.40	1.15 1.15	4.70 4.70	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to Q_n		1.70 1.70	4.50 4.50	1.70 1.70	4.50 4.50	1.70 1.70	4.80 4.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n		0.50 0.50	2.20 2.20	0.50 0.50	2.20 2.20	0.50 0.50	2.20 2.20	ns ns

NOTE:

For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -4.8\text{V}$ to -4.2V

Flat Pack and PLCC VCC1 = VCC2 = ground, VEE = -4.5V to -4.2V									
SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T _A = 0°C		T _A = +25°C		T _A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{PLH} t _{PHL}	Propagation delay D _n to Q _n	Waveform 1	1.10 1.10	2.80 2.80	1.10 1.10	2.70 2.70	1.10 1.10	2.90 2.90	ns ns
t _{PLH} t _{PHL}	Propagation delay M to Q _n		1.15 1.15	4.20 4.20	1.25 1.25	4.20 4.20	1.15 1.15	4.50 4.50	ns ns
t _{PLH} t _{PHL}	Propagation delay S _n to Q _n		1.70 1.70	4.30 4.30	1.70 1.70	4.30 4.30	1.70 1.70	4.60 4.60	ns ns
t _{TLH} t _{THL}	Transition time Q _n		0.50 0.50	2.20 2.20	0.50 0.50	2.20 2.20	0.50 0.50	2.20 2.20	ns ns

NOTE:

For AC test setup information, see AC Testing, Chapter 2, Section 3.

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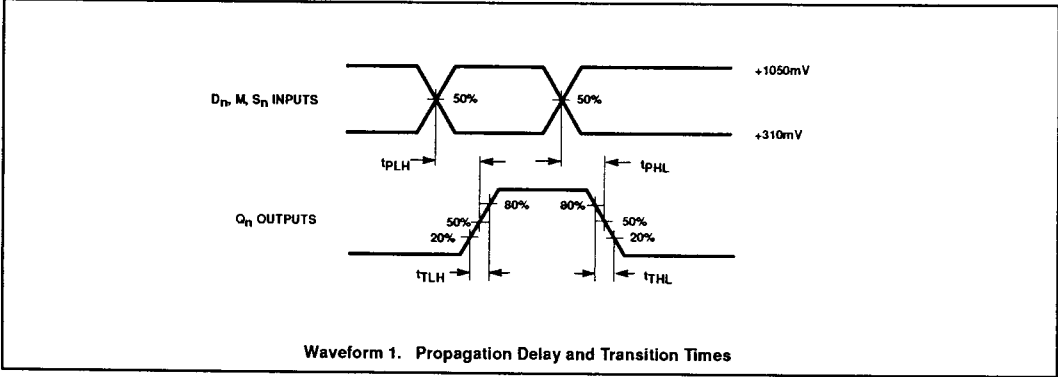
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T _A = 0°C		T _A = +25°C		T _A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{PLH} t _{PHL}	Propagation delay D _n to Q _n	Waveform 1	1.10 1.10	2.80 2.80	1.10 1.10	2.70 2.70	1.10 1.10	2.90 2.90	ns ns
t _{PLH} t _{PHL}	Propagation delay M to Q _n		1.15 1.15	4.20 4.20	1.25 1.25	4.20 4.20	1.15 1.15	4.50 4.50	ns ns
t _{PLH} t _{PHL}	Propagation delay S _n to Q _n		1.70 1.70	4.30 4.30	1.70 1.70	4.30 4.30	1.70 1.70	4.60 4.60	ns ns
t _{TLH} t _{THL}	Transition time Q _n		0.50 0.50	2.20 2.20	0.50 0.50	2.20 2.20	0.50 0.50	2.20 2.20	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.