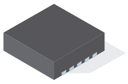


# 12-A Step-Down Regulator with Integrated Switcher

**Check for Samples: TPS53315**

## FEATURES

- **Conversion Input Voltage Range: 3 V to 15 V**
- **VDD Input Voltage Range: 4.5 V to 25 V**
- **Output Voltage Range: 0.6 V to 5.5 V**
- **5-V LDO Output**
- **Integrated Power MOSFETs with 12-A Continuous Output Current**
- **<10-µA Shut Down Current**
- **Auto-Skip Eco-mode™ for Light-Load Efficiency**
- **D-CAP™ Mode with Fast Transient Response**
- **Selectable Switching Frequency from 250 kHz to 1 MHz with an External Resistor**
- **Built-in 1%, 0.6-V Reference**
- **0.7-ms, 1.4-ms, 2.8-ms and 5.6-ms Selectable Internal Voltage Servo Soft-Start**
- **Pre-Charged Start-up Capability**
- **Integrated Boost Switch**
- **Adjustable Overcurrent Limit Via External Resistor**
- **Overvoltage/Undervoltage, UVLO and Over-Temperature Protection**
- **Support All Ceramic Output Capacitors**
- **Open Drain Power Good Indication**
- **40-pin QFN Package with PowerPAD™**

## APPLICATIONS

- **Server and Desktop Computers**
- **Notebook Computers**
- **Telecommunication Equipments**

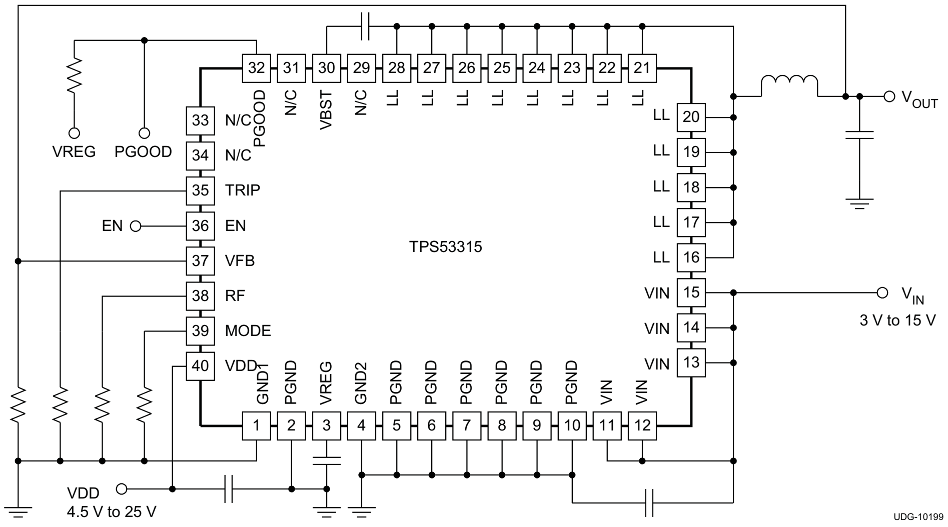
## DESCRIPTION

TPS53315 is a D-CAP™ mode, 12-A synchronous switcher with integrated MOSFETs. It is designed for ease of use, low external component count, and small package power systems.

This device features single-rail input support, one 19-mΩ and one 7-mΩ integrated MOSFET, accurate 1%, 0.6 V Reference, and integrated boost switch. A sample of competitive features include: greater than 96% maximum efficiency, 3 V to 15 V wide input voltage range, very low external component count, D-CAP™ mode control for super fast transient, selectable auto-skip and PWM operation, internal soft-start control, adjustable frequency, and no need for compensation.

The conversion input voltage ranges from 3 V to 15 V, the supply voltage range is from 4.5 V to 25 V, and the output voltage range is from 0.6 V to 5.5 V.

The TPS53315 is available in a 5 mm × 7 mm 40-pin, QFN package and is specified from –40°C to 85°C.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION[1]

| $T_A$ | PACKAGE | ORDERING NUMBER | PINS | TRANSPORT MEDIA | MINIMUM QUANTITY | ECO PLAN |
|---|---|---|---|---|---|---|
| –40°C to 85°C | Plastic QFN (RGF) | TPS53315RGFR | 40 | Tape and reel | 3000 | Green (RoHS and no Pb/Br) |
| | | TPS53315RGFT | 40 | Mini reel | 250 | |

(1) For the most current package and ordering information, see the *Package Option Addendum* at the end of this document, or see the TI web site at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS[1]

| | | | VALUE | UNIT |
|---|---|---|---|---|
| Input voltage range | VIN (main supply) | | –0.3 to 17 | V |
| | VDD | | –0.3 to 28 | |
| | VBST | | –0.3 to 24 | |
| | VBST(with respect to LL) | | –0.3 to 7 | |
| | EN, TRIP, VFB, RF, MODE | | –0.3 to 7 | |
| Output voltage range | LL | DC | –1 to 23 | V |
| | | Pulse < 20 ns, E = 5 μJ | –7 | |
| | PGOOD, VREG | | –0.3 to 7 | |
| | PGND | | –0.3 to 0.3 | |
| Source/Sink Current | VBST | | 50 | mA |
| Operating free-air temperature, $T_A$ | | | –40 to 85 | °C |
| Storage temperature range, $T_{stg}$ | | | –55 to 150 | °C |
| Junction temperature range, $T_J$ | | | –40 to 150 | °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | | | 300 | °C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## THERMAL INFORMATION

| THERMAL METRIC[1] | | TPS53315 | UNITS |
|---|---|---|---|
| | | RGF(40 PINS) | |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 35.8 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 23.8 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 10.1 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.4 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 10.0 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | 2.8 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## RECOMMENDED OPERATING CONDITIONS

| | | **VALUE** | **UNIT** |
|---|---|---|---|
| Input voltage range | VIN (main supply) | 3 to 15 | V |
| | VDD | 4.5 to 25 | |
| | VBST | 4.5 to 21 | |
| | VBST(with respect to LL) | 4.5 to 6.5 | |
| | EN, TRIP, VFB, RF, MODE | –0.1 to 6.5 | |
| Output voltage range | LL | –0.8 to 15 | V |
| | PGOOD, VREG | –0.1 to 6.5 | |
| Source/Sink Current | VBST | 50 | mA |
| Junction temperature range, $T_J$ | | –40 to 125 | °C |

## ELECTRICAL CHARACTERISTICS

Over recommended free-air temperature range, VDD = 12 V (Unless otherwise noted)

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE AND SUPPLY CURRENT** | | | | | | |
| $V_{VIN}$ | VIN pin power conversion input voltage | | 3 | | 15 | V |
| $V_{DD}$ | Supply input voltage | | 4.5 | | 25 | V |
| $I_{VIN(leak)}$ | VIN pin leakage current | $V_{EN}$ = 0 V | | | 1 | µA |
| $I_{VDD}$ | VDD supply current | VDD current, $T_A$ = 25°C, No Load, $V_{EN}$ = 5 V, $V_{VFB}$ = 0.630 V | | 420 | 590 | µA |
| $I_{VDDSDN}$ | VDD shutdown current | VDD current, $T_A$ = 25°C, No Load, $V_{EN}$ = 0 V | | | 10 | µA |
| **INTERNAL REFERENCE VOLTAGE** | | | | | | |
| $V_{VFB}$ | VFB regulation voltage | VFB voltage, CCM condition(1) | | 0.6000 | | V |
| | | $T_A$ = 25°C | 0.597 | 0.600 | 0.603 | V |
| | | $T_A$ = 0°C to 85°C | 0.5952 | 0.600 | 0.6048 | |
| | | $T_A$ = -40°C to 85°C | 0.594 | 0.600 | 0.606 | |
| $I_{VFB}$ | VFB input current | $V_{VFB}$ = 0.630 V, $T_A$ = 25°C | | 0.002 | 0.2 | µA |
| **LDO OUTPUT** | | | | | | |
| $V_{VREG}$ | LDO output voltage | 0 mA ≤ $I_{VREG}$ ≤ 30 mA | 4.77 | 5.0 | 5.35 | V |
| $I_{VREG}$ | LDO output current(1) | Maximum current allowed from LDO | | | 30 | mA |
| $V_{DO}$ | LDO drop out voltage | $V_{DD}$ = 4.5 V, $I_{VREG}$ = 30 mA | | | 295 | mV |
| **BOOT STRAP SWITCH** | | | | | | |
| $V_{FBST}$ | Forward voltage | $V_{VREG-VBST}$, $I_F$ = 10 mA, $T_A$ = 25°C | | 0.1 | 0.2 | V |
| $I_{VBSTLK}$ | VBST leakage current | $V_{VBST}$ = 23 V, $V_{LL}$ = 17 V, $T_A$ = 25°C | | 0.01 | 1.5 | µA |
| **DUTY AND FREQUENCY CONTROL** | | | | | | |
| $t_{OFF(min)}$ | Minimum off time | $T_A$ = 25°C | 150 | 260 | 400 | ns |
| $t_{ON(min)}$ | Minimum on time | $V_{VIN}$ = 17 V, $V_{OUT}$ = 0.6 V, $R_{RF}$ = 0 Ω to VREG, $T_A$ = 25°C(1) | | 35 | | |
| **SOFTSTART** | | | | | | |
| $t_{SS}$ | Internal SS time from $V_{OUT}$ = 0 to $V_{OUT}$ = 95% | $R_{MODE}$ = 39 kΩ | | 0.7 | | ms |
| | | $R_{MODE}$ = 100 kΩ | | 1.4 | | |
| | | $R_{MODE}$ = 200 kΩ | | 2.8 | | |
| | | $R_{MODE}$ = 470 kΩ | | 5.6 | | |
| **POWERGOOD** | | | | | | |
| $V_{THPG}$ | PG threshold | PG in from lower | 92.5% | 96% | 98.5% | |
| | | PG in from higher | 107.5% | 110% | 112.5% | |
| | | PG hysteresis | 2.5% | 5% | 7.8% | |
| $R_{PG}$ | PG transistor on-resistance | | 15 | 30 | 55 | Ω |
| $t_{PGDEL}$ | PG Delay after soft-start | | 0.8 | 1 | 1.2 | ms |

(1) Ensured by design. Not production tested.

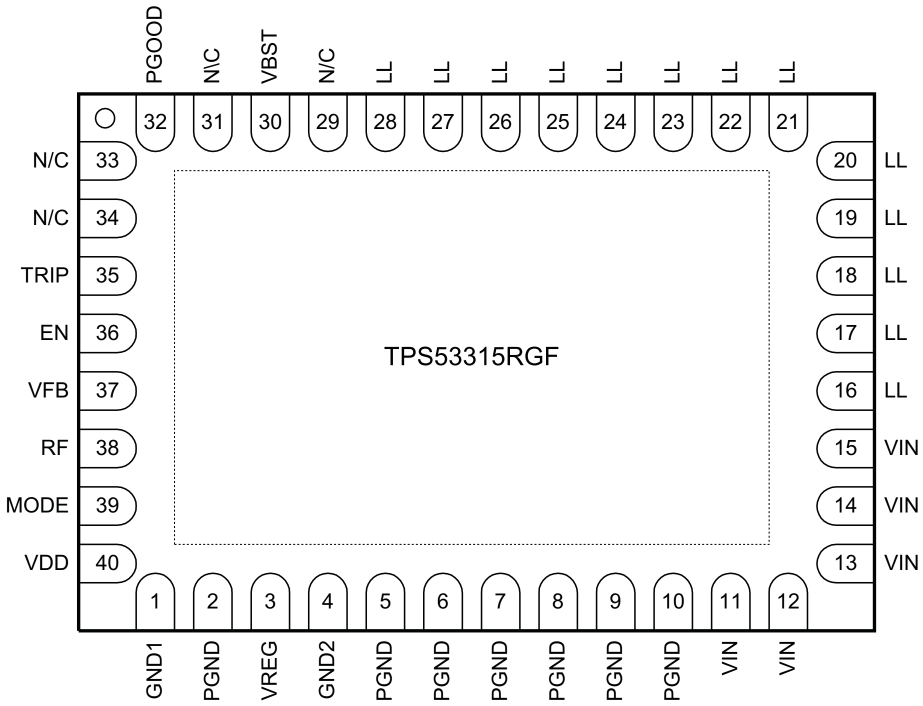
## ELECTRICAL CHARACTERISTICS

Over recommended free-air temperature range, VDD = 12 V (Unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **LOGIC THRESHOLD AND SETTING CONDITIONS** | | | | | | |
| $V_{EN}$ | EN voltage threshold | Enable | 1.8 | | | V |
| | | Disable | | | 0.6 | |
| $I_{EN}$ | EN input current | $V_{EN}$ = 5 V | | | 1.0 | µA |
| $f_{SW}$ | Switching frequency | $R_{RF}$ = 0 Ω to GND, $T_A$ = 25°C(1) | 200 | 250 | 300 | kHz |
| | | $R_{RF}$ = 187 kΩ to GND, $T_A$ = 25°C(1) | 250 | 300 | 350 | |
| | | $R_{RF}$ = 619 kΩ to GND, $T_A$ = 25°C(1) | 350 | 400 | 450 | |
| | | $R_{RF}$ = Open, $T_A$ = 25°C(1) | 450 | 500 | 550 | |
| | | $R_{RF}$ = 866 kΩ to VREG, $T_A$ = 25°C(1) | 580 | 650 | 720 | |
| | | $R_{RF}$ = 309 kΩ to VREG, $T_A$ = 25°C(1) | 670 | 750 | 820 | |
| | | $R_{RF}$ = 124 kΩ to VREG, $T_A$ = 25°C(1) | 770 | 850 | 930 | |
| | | $R_{RF}$ = 0 Ω to VREG, $T_A$ = 25°C(1) | 880 | 970 | 1070 | |
| **PROTECTION: CURRENT SENSE** | | | | | | |
| $I_{TRIP}$ | TRIP source current | $V_{TRIP}$ = 1 V, $T_A$ = 25°C | 9.4 | 10.0 | 10.6 | µA |
| $TC_{ITRIP}$ | TRIP current temperature coefficent | On the basis of 25°C(2) | | 4700 | | ppm/°C |
| $V_{TRIP}$ | Current limit threshold setting range | $V_{TRIP-GND}$ voltage | 0.2 | | 1.2 | V |
| $V_{OCL}$ | Current limit threshold | $V_{TRIP}$ = 1.2 V | 140 | 150 | 160 | mV |
| | | $V_{TRIP}$ = 0.2 | 19 | 26 | 33 | |
| $V_{OCLN}$ | Negative current limit threshold | $V_{TRIP}$ = 1.2 V | –160 | –150 | –140 | |
| | | $V_{TRIP}$ = 0.2 V | –33 | –26 | –19 | |
| $V_{AZCADJ}$ | Auto zero cross adjustable range | Positive | 3 | 15 | | mV |
| | | Negative | | –15 | –3 | |
| **PROTECTION: UVP and OVP** | | | | | | |
| $V_{OVP}$ | OVP trip threshold | OVP detect | 115% | 120% | 125% | |
| $t_{OVPDEL}$ | OVP propagation delay time | VFB delay with 50-mV overdrive | | 1 | | µs |
| $V_{UVP}$ | Output UVP trip threshold time | UVP detect | 65% | 70% | 75% | |
| $t_{UVPDEL}$ | Output UVP propagation delay time | | 0.8 | 1 | 1.2 | ms |
| $t_{UVPEN}$ | Output UVP enable delay time | from EN to UVP workable, $R_{MODE}$ = 39 kΩ | 2.0 | 2.6 | 3.2 | ms |
| **UVLO** | | | | | | |
| $V_{UVVREG}$ | VREG UVLO threshold | Wake up | 4.00 | 4.20 | 4.32 | V |
| | | Hysteresis | | 0.25 | | |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{SDN}$ | Thermal shutdown threshold | Shutdown temperature(2) | | 145 | | °C |
| | | Hysteresis(2) | | 10 | | |

(1) Not production tested. Test condition is $V_{IN}$ = 12 V, $V_{OUT}$= 1.1 V, $I_{OUT}$= 5 A using application circuit shown in Figure 33.
(2) Ensured by design. Not production tested.

## PIN DESCRIPTION



### PIN FUNCTIONS

| PIN | | I/O/P[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| EN | 36 | I | Enable pin. |
| GND1 | 1 | G | GND for controller |
| GND2 | 4 | G | GND for half-bridge |
| LL | 16<br>17<br>18<br>19<br>20<br>21<br>22<br>23<br>24<br>25<br>26<br>27<br>28 | B | Output of converted power. Connect this pin to the output Inductor. |
| MODE | 39 | I | Soft-start and skip/CCM selection. Connect a resistor to select soft-start time using Table 1. The soft-start time is detected and stored into internal register during start-up. |
| N/C | 29<br>31<br>33<br>34 | | No connection |

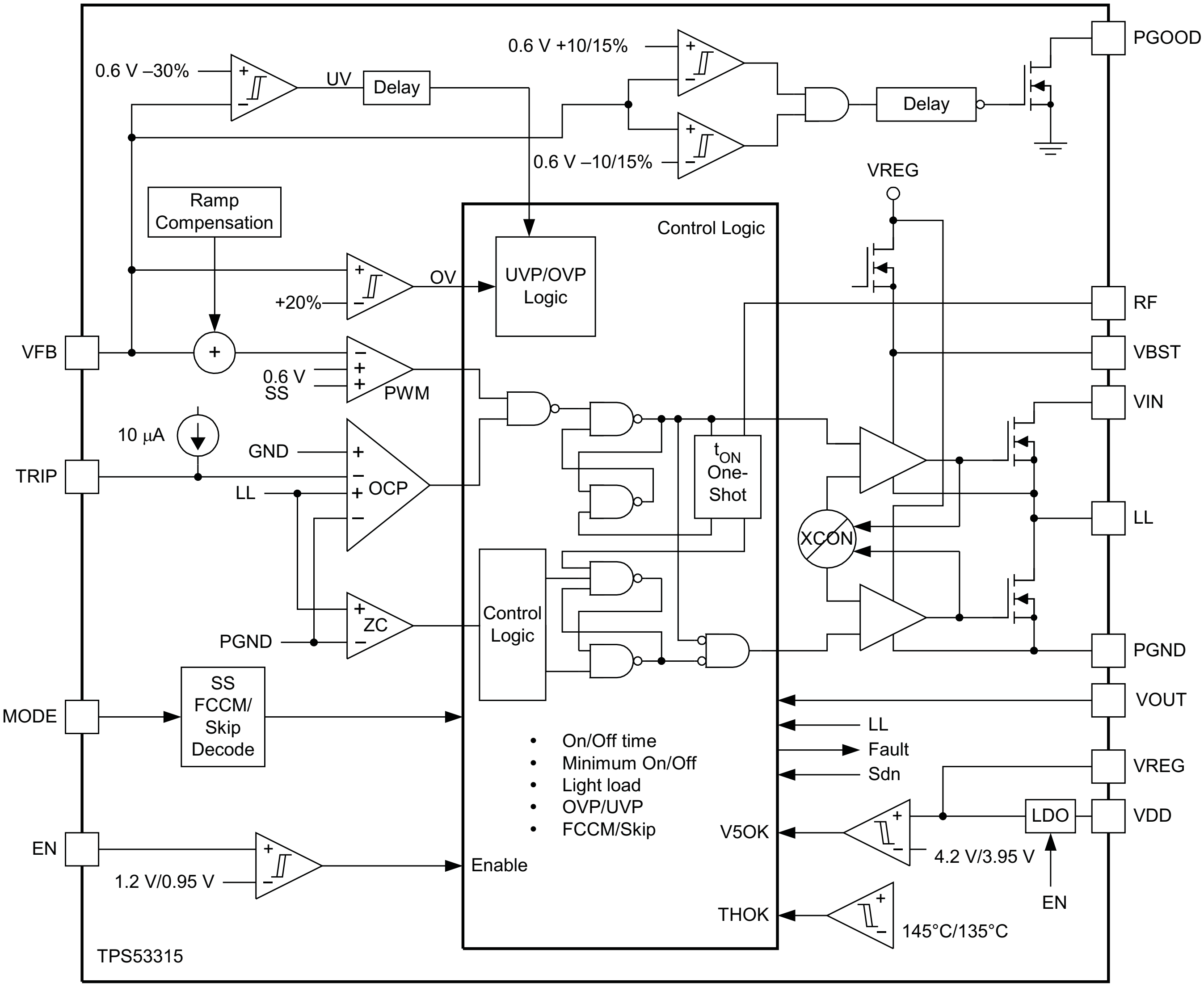
---

(1) I=Input, O=Output, B=Bidirectional, P=Supply, G=Ground

## PIN FUNCTIONS (continued)

| PIN | | I/O/P[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| PGOOD | 32 | O | Open drain power good flag. Provides a 1-ms start up delay after the VFB pin voltage falls within specified limits. When the VFB pin voltage goes outside the specified limits, the PGOOD pin goes low within 10 µs. |
| PGND | 2<br>5<br>6<br>7<br>8<br>9<br>10 | G | Power GND |
| RF | 38 | I | Switching frequency selection. Connect a resistance to GND or VREG to select switching frequency using Table 2. The switching frequency is detected and stored during the startup. |
| TRIP | 35 | I | OCL detection threshold setting pin. 10 µA at room temperature, 4700 ppm/°C current is sourced and set the OCL trip voltage as follows.<br>$V_{OCL} = V_{TRIP}/8$ ( $V_{TRIP} \le 1.2$ V, $V_{OCL} \le 150$ mV) |
| VBST | 30 | P | Supply input for high-side FET gate driver (boost terminal). Connect capacitor from this pin to LL-node. Internally connected to the VREG pin via bootstrap MOSFET switch. |
| VDD | 40 | P | Controller power supply input. |
| VFB | 37 | I | Output feedback input. Connect this pin to $V_{OUT}$ through a resistor divider. |
| VIN | 11<br>12<br>13<br>14<br>15 | P | Conversion power input. |
| VREG | 3 | P | 5-V LDO output. |

## FUNCTIONAL BLOCK DIAGRAM



UDG-10200

## TYPICAL CHARACTERISTICS

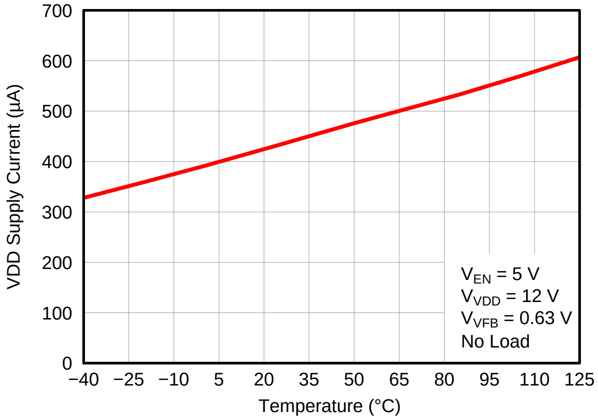


Figure 1. VDD Supply Current vs. Temperature

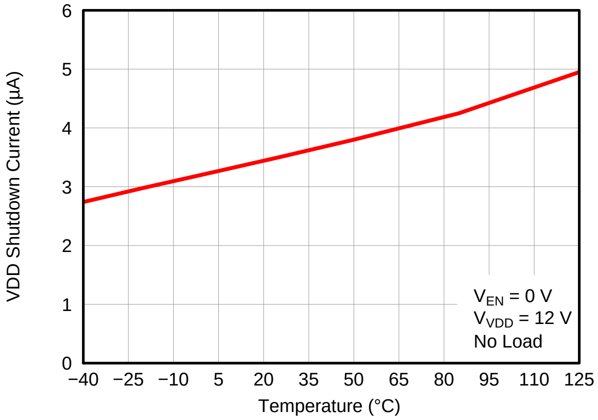


Figure 2. VDD Shutdown Current vs. Temperature

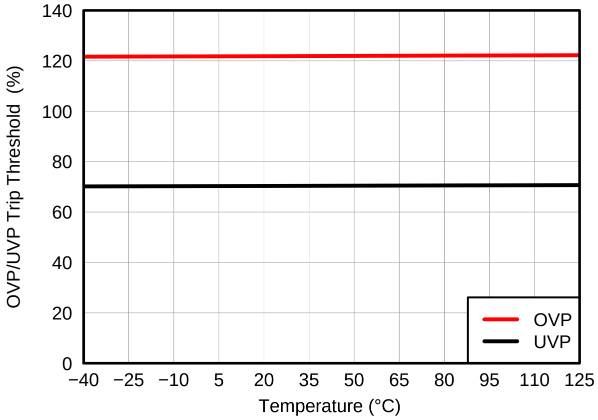


Figure 3. OVP/UVP Trip Threshold vs. Temperature

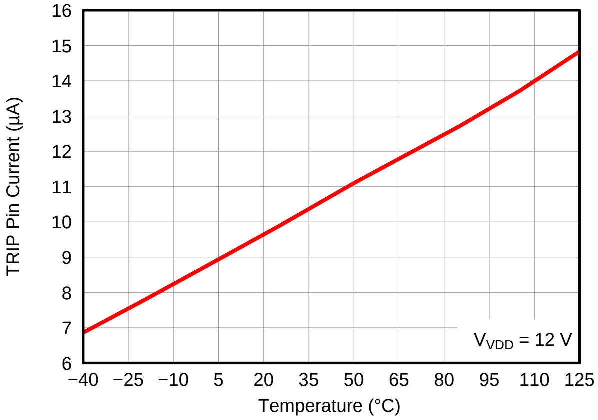


Figure 4. Trip Pin Current vs. Temperature

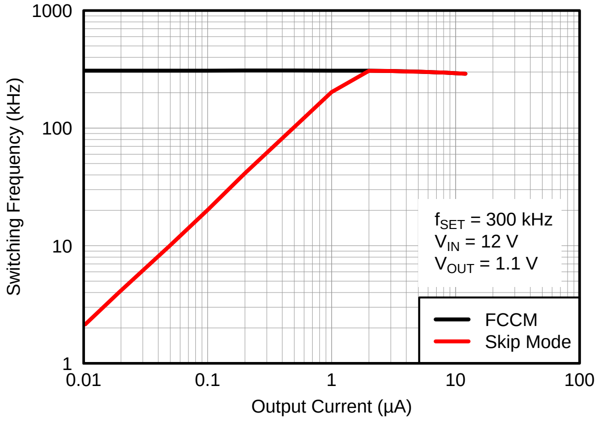


Figure 5. Frequency vs. Temperature ($f_{SET}$ = 300 kHz)

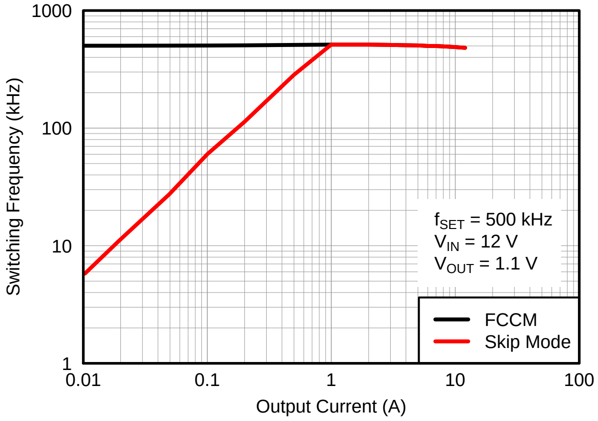


Figure 6. Frequency vs. Temperature ($f_{SET}$ = 500 kHz)

## TYPICAL CHARACTERISTICS

Inductor Values

IN06155: 1 µH, 2.3 mΩ, HCB1175-501: 0.5 µH, 0.29 mΩ

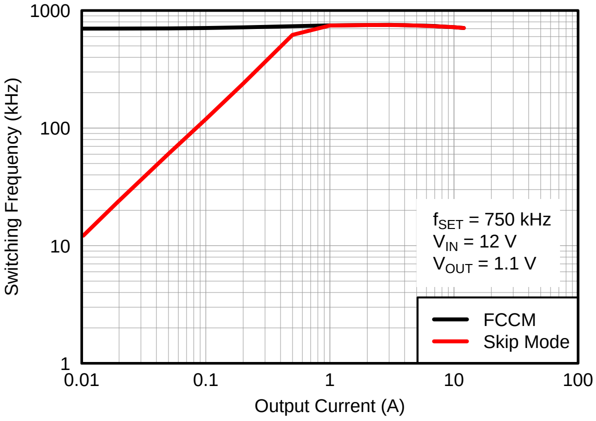


**Figure 7. Frequency vs. Temperature ($f_{SET}$ = 750 kHz)**

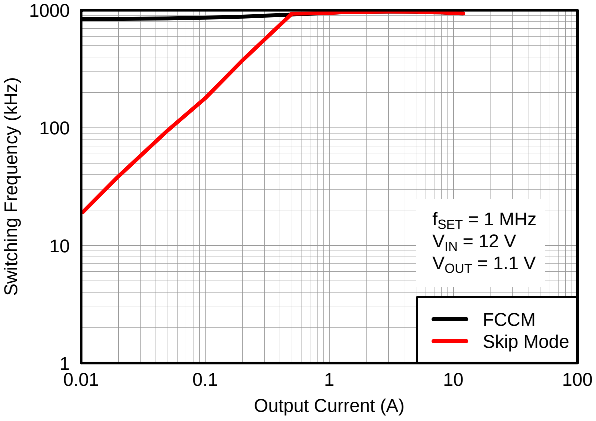


**Figure 8. Frequency vs. Temperature ($f_{SET}$ = 1 MHz)**

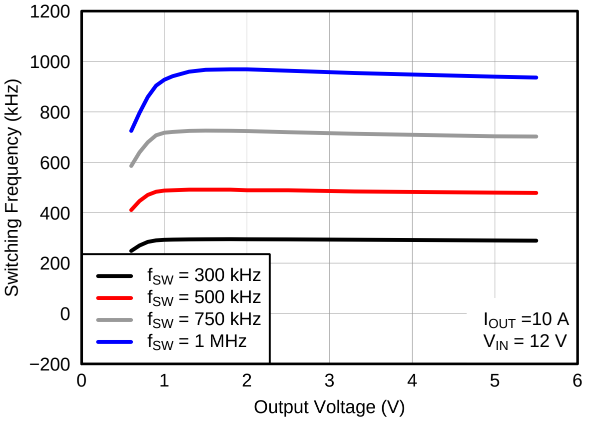


**Figure 9. Switching Frequency vs. Output Voltage**

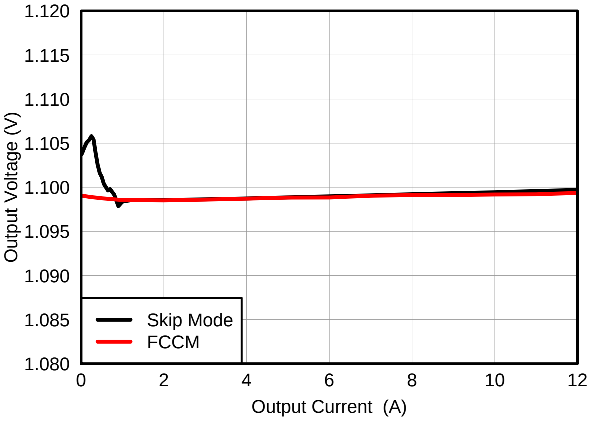


**Figure 10. Output Voltage vs. Output Current**

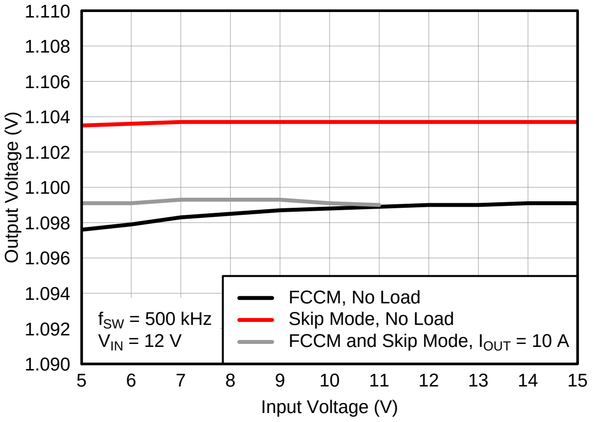


**Figure 11. Output Voltage vs. Input Voltage**

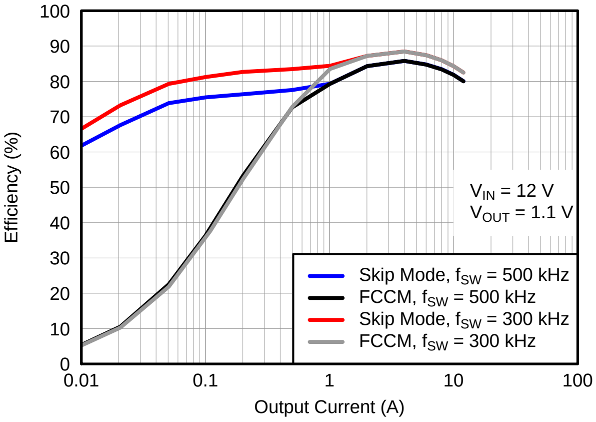


**Figure 12. Efficiency vs. Output Current, Inductor: IN06155**

# TYPICAL CHARACTERISTICS

Inductor Values

IN06155: 1 µH, 2.3 mΩ, HCB1175-501: 0.5 µH, 0.29 mΩ

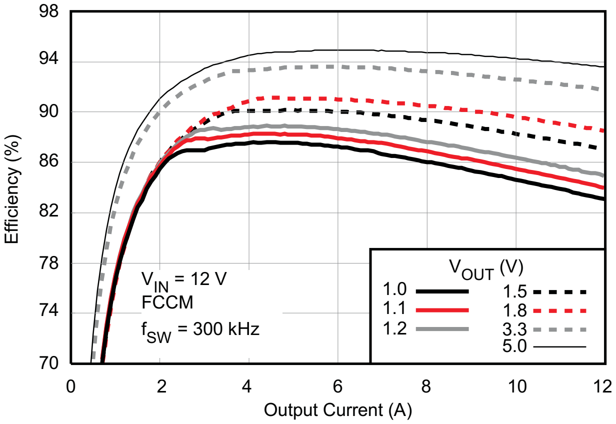


Figure 13. Efficiency vs Output Current, Inductors: $V_{OUT}$ ≤ 1.8 V: HCB1175-501, $V_{OUT}$ ≥ 3.3 V: IN06155

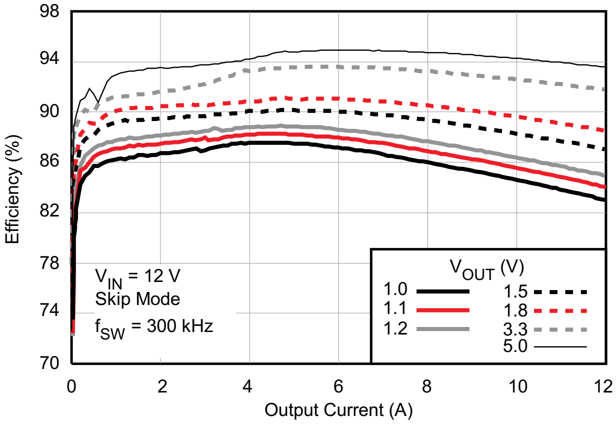


Figure 14. Efficiency vs Output Current, Inductors: $V_{OUT}$ ≤ 1.8 V: HCB1175-501, $V_{OUT}$ ≥ 3.3 V: IN06155

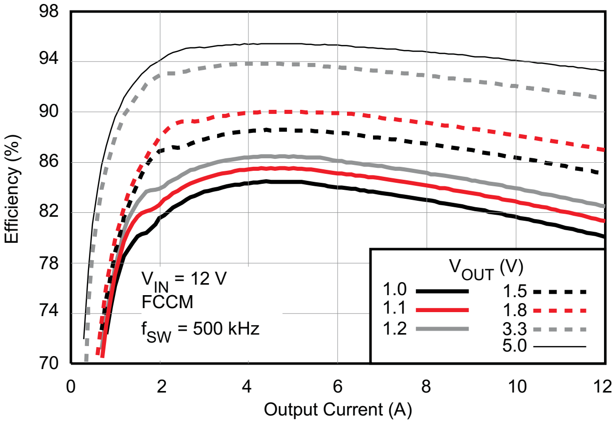


Figure 15. Efficiency vs Output Current, Inductors: $V_{OUT}$ ≤ 1.8 V: HCB1175-501, $V_{OUT}$ ≥ 3.3 V: IN06155

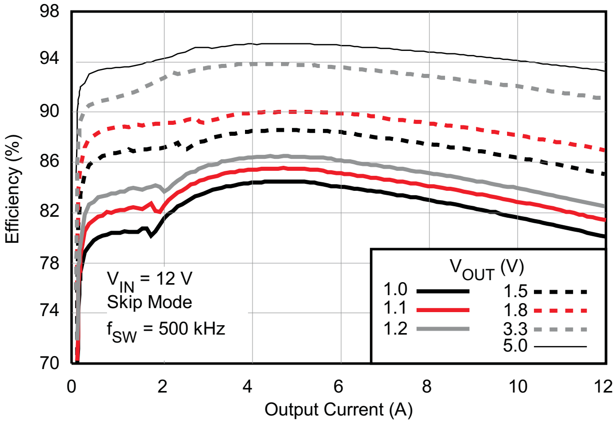


Figure 16. Efficiency vs Output Current, Inductors: $V_{OUT}$ ≤ 1.8 V: HCB1175-501, $V_{OUT}$ ≥ 3.3 V: IN06155

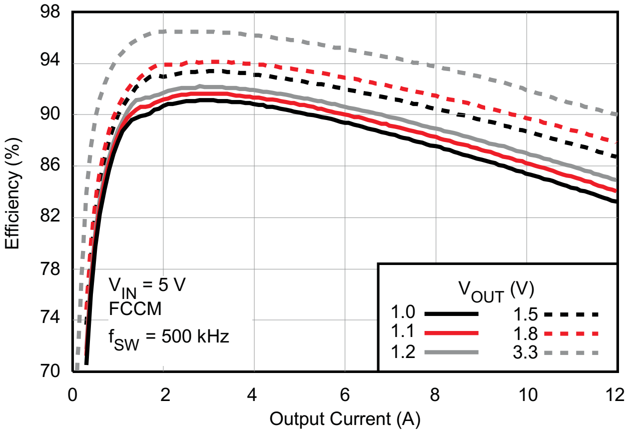


Figure 17. Efficiency vs Output Current, Inductor: HCB1175-501

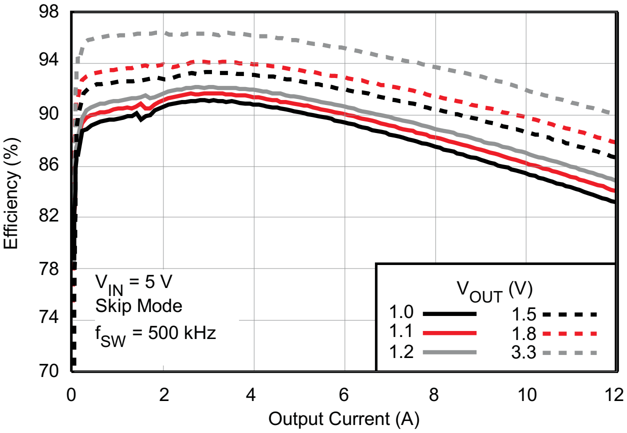


Figure 18. Efficiency vs Output Current, Inductor: HCB1175-501

## TYPICAL CHARACTERISTICS

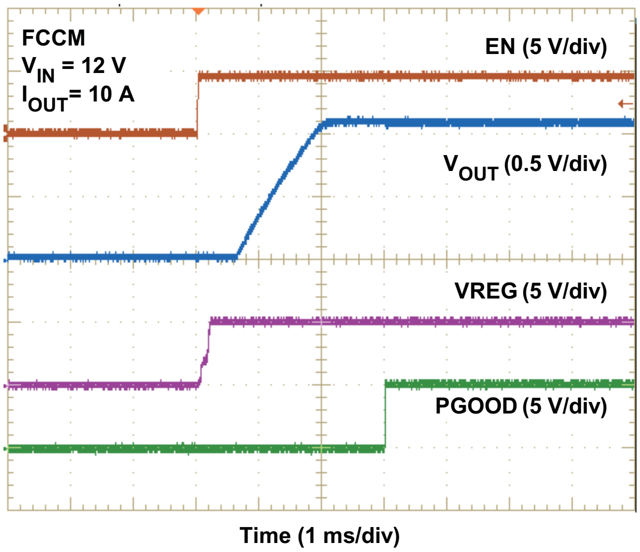


Figure 19. Start-Up

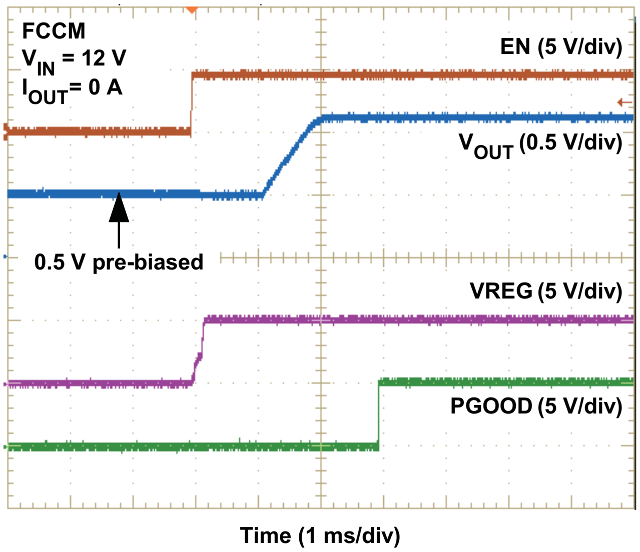


Figure 20. Pre-Bias Start-Up

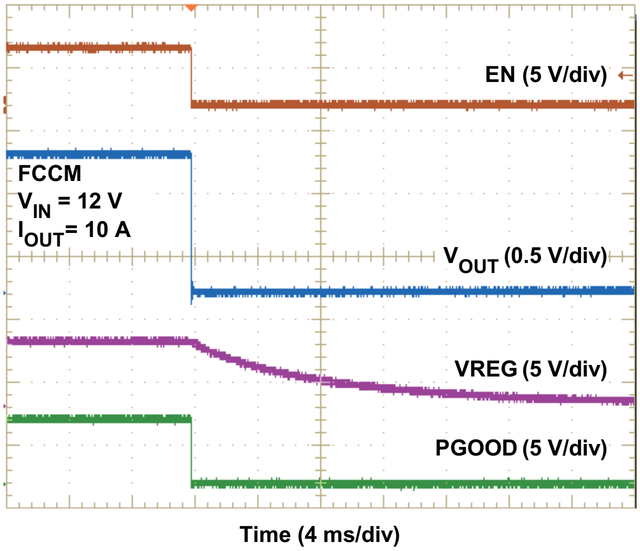


Figure 21. Turn-Off

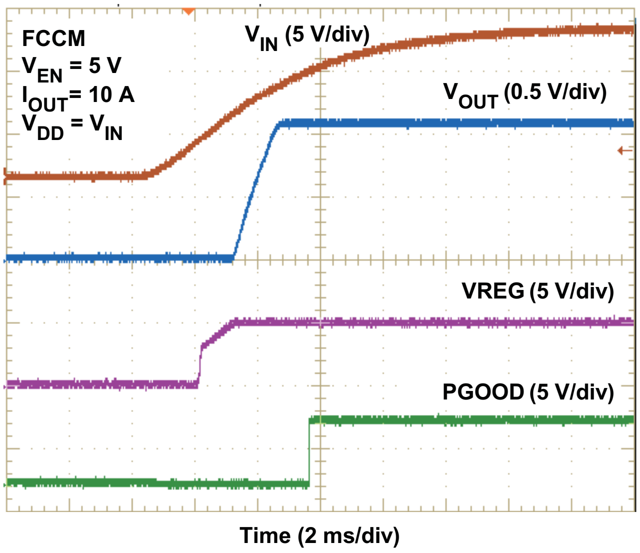


Figure 22. UVLO Start-Up

## TYPICAL CHARACTERISTICS

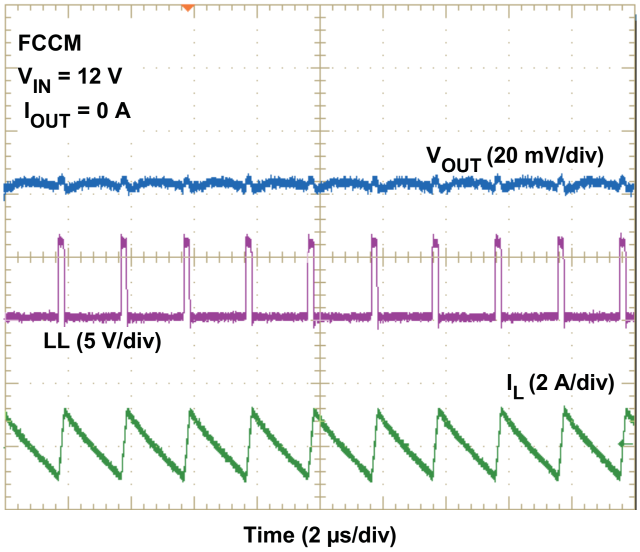


Figure 23. 1.1-V Output FCCM Steady-State Operation

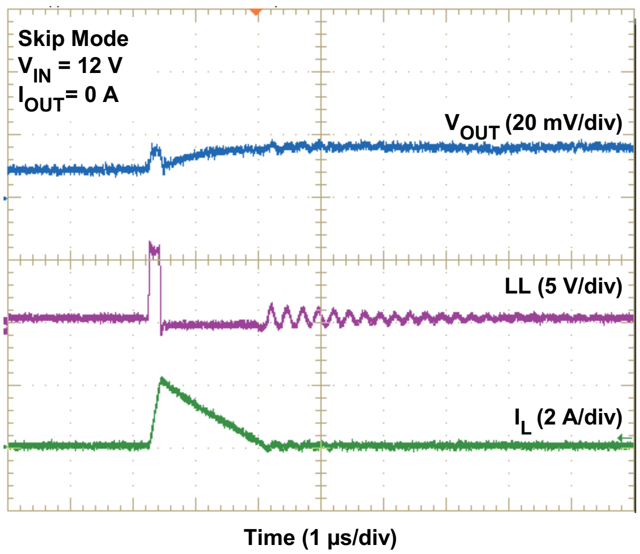


Figure 24. 1.1-V Output Skip Mode Steady-State Operation

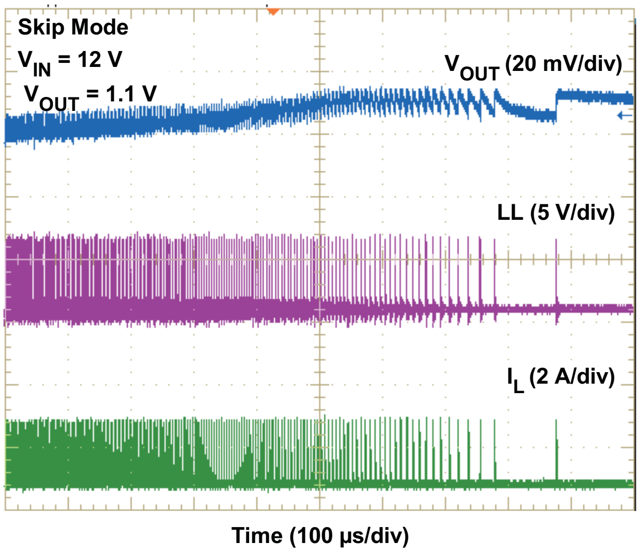


Figure 25. CCM to DCM Transition

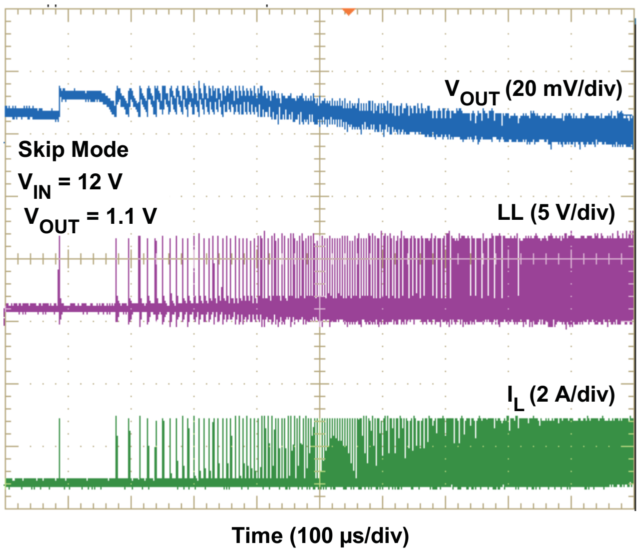


Figure 26. DCM to CCM Transition

## TYPICAL CHARACTERISTICS

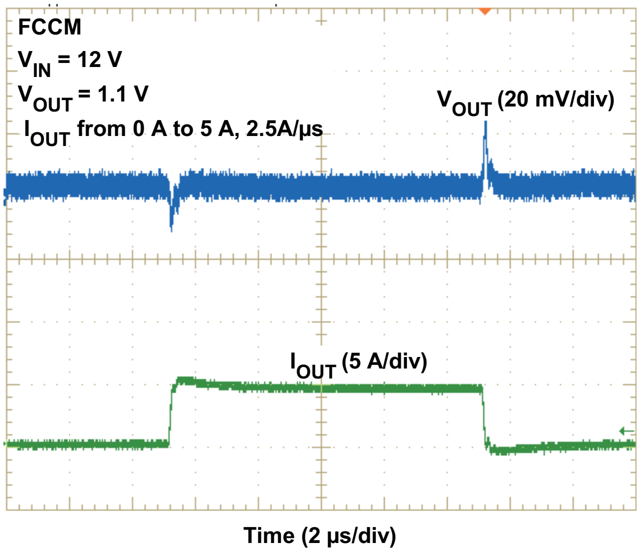


Figure 27. FCCM Load Transient

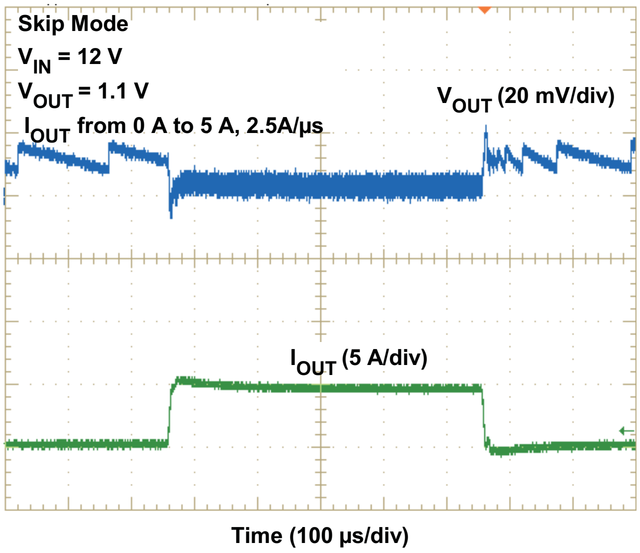


Figure 28. Skip Mode Load Transient

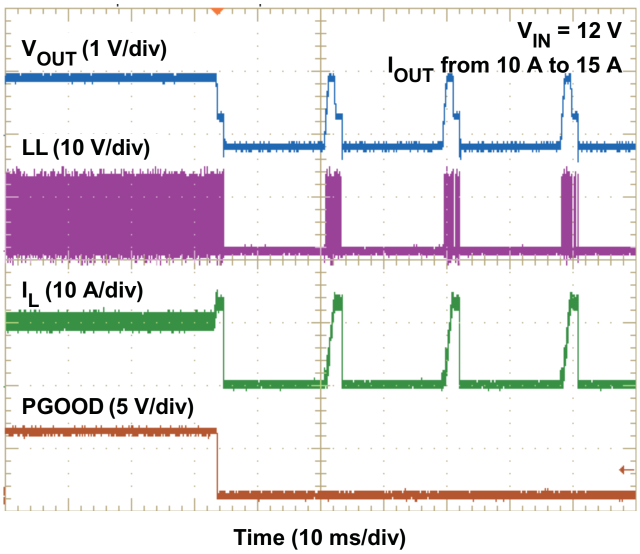


Figure 29. Overcurrent Protection

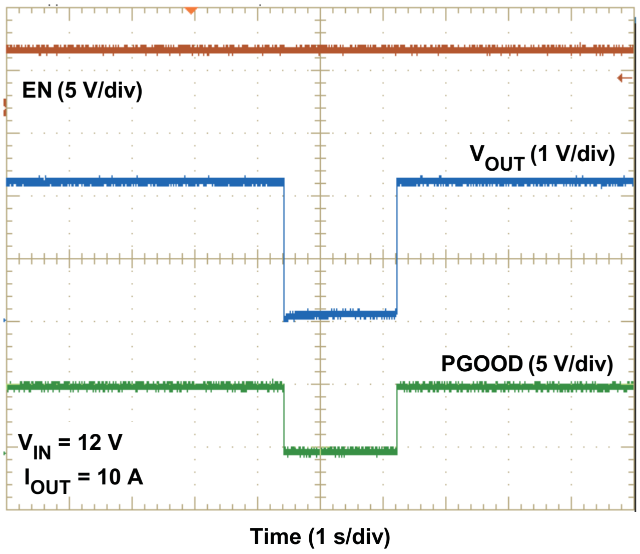


Figure 30. Over-temperature Protection

## TYPICAL CHARACTERISTICS

Figure 31, shows the thermal signature of the TPS53315 EVM, $V_{IN}$ = 12 V, $V_{OUT}$ = 1.1 V, $I_{OUT}$= 12 A, $f_{SW}$ = 500 kHz at room temperature with no airflow.

Figure 32 shows the thermal signature of the TPS53315 EVM, $V_{IN}$ = 12 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$= 12 A, $f_{SW}$ = 650 kHz at room temperature with no airflow.

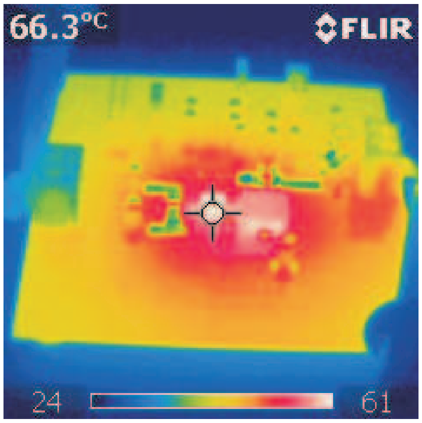


**Figure 31. Thermal Signature of TPS53315 EVM, $f_{SW}$ = 500 kHz**

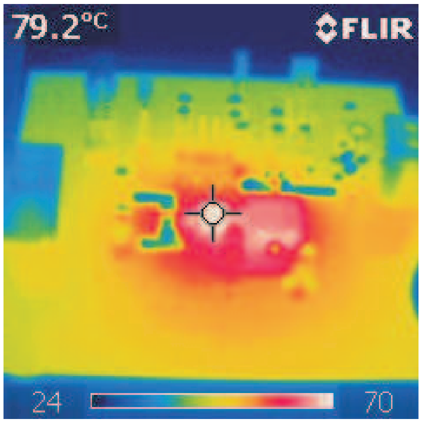


**Figure 32. Thermal Signature of TPS53315 EVM, $f_{SW}$ = 650 kHz**

## APPLICATION INFORMATION

## APPLICATION CIRCUIT DIAGRAM

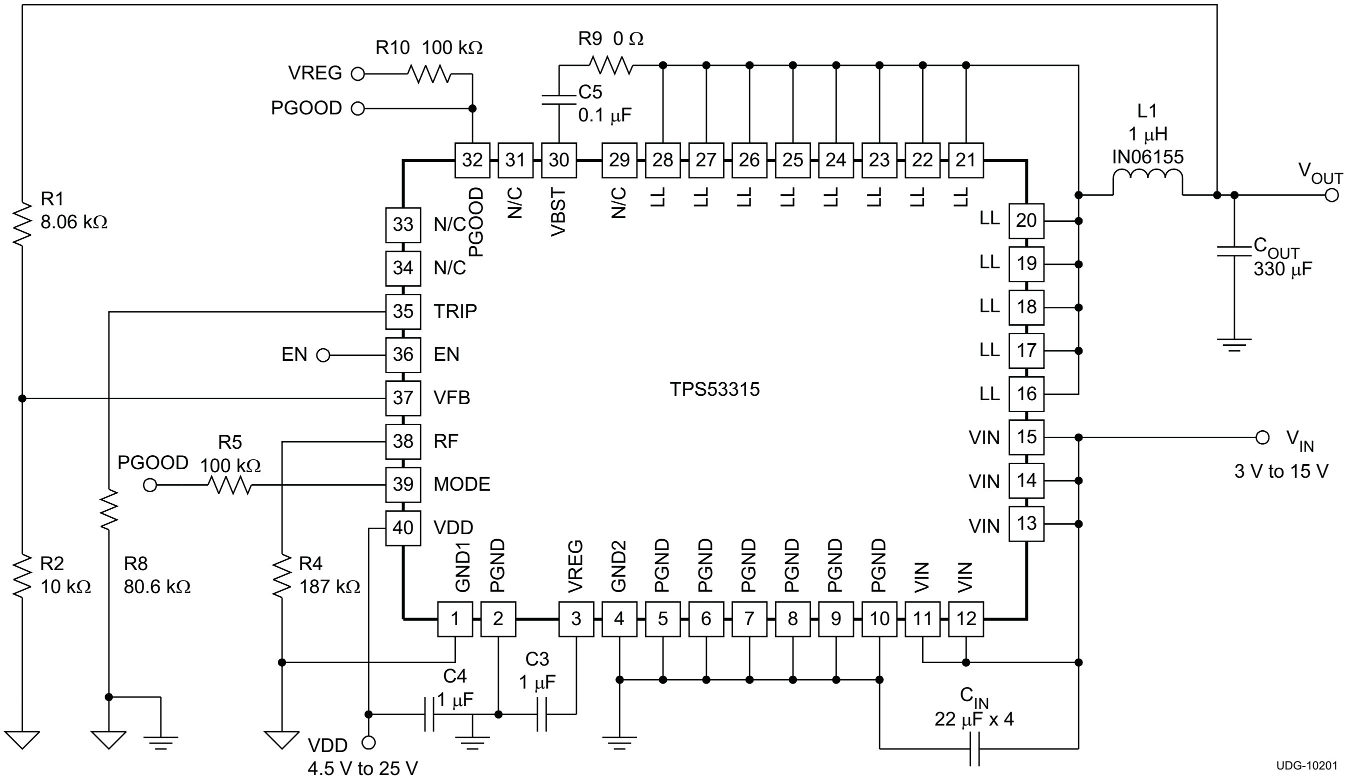


Figure 33. Typical Application Circuit Diagram

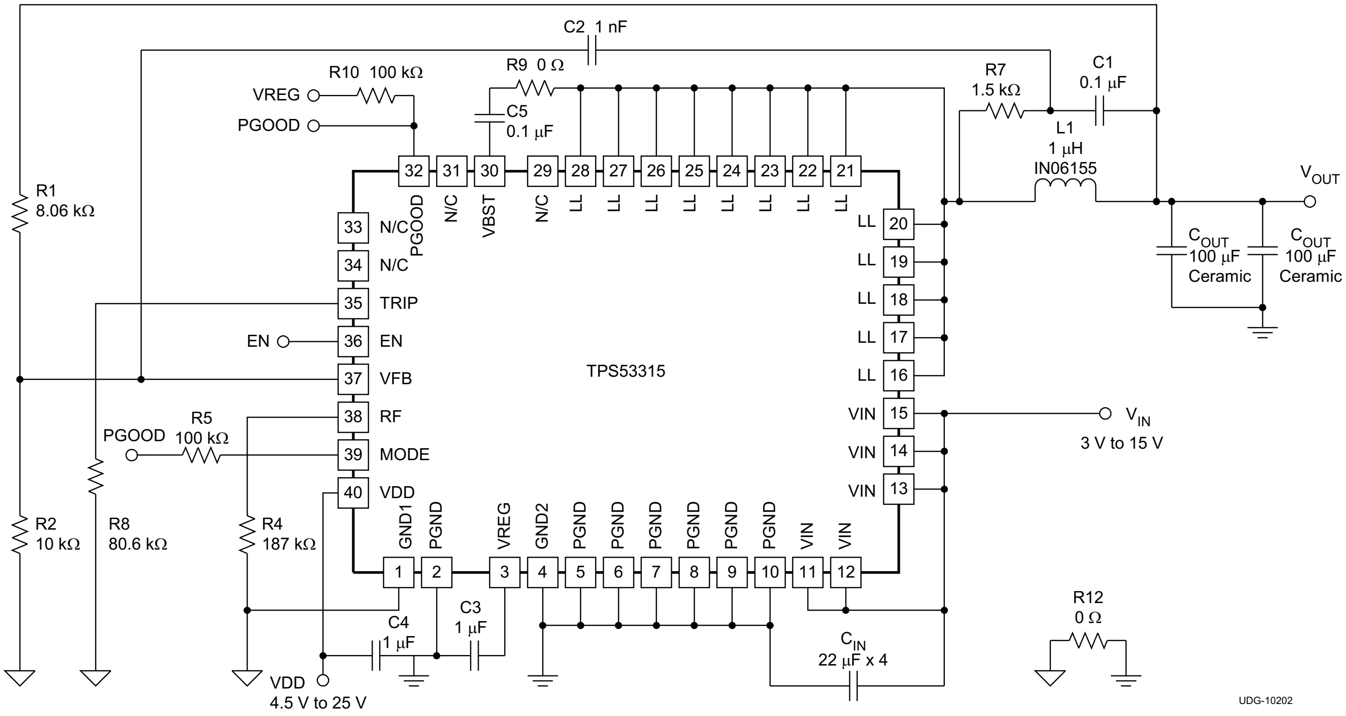


Figure 34. Typical Application Circuit Diagram with Ceramic Output Capacitors

## General Description

The TPS53315 is a high-efficiency, single channel, synchronous buck converter suitable for low output voltage point-of-load applications in computing and similar digital consumer applications. The device features proprietary D-CAP™ mode control combined with an adaptive on-time architecture. This combination is ideal for building modern low duty ratio, ultra-fast load step response DC-DC converters. The output voltage ranges from 0.6 V to 5.5 V. The conversion input voltage range is from 3 V up to 15 V. The D-CAP™ mode uses the ESR of the output capacitor(s) to sense the device current. One advantage of this control scheme is that it does not require an external phase compensation network. This allows a simple design with a low external component count. Eight preset switching frequency values can be chosen using a resistor connected from the RF pin to ground or the VREG pin. Adaptive on-time control tracks the preset switching frequency over a wide input and output voltage range while allowing the switching frequency to increase at the step-up of the load.

The TPS53315 has a MODE pin to select between auto-skip mode and forced continuous conduction mode (FCCM) for light load conditions. The MODE pin also sets the selectable soft-start time ranging from 0.7 ms to 5.6 ms.

## Enable and Soft Start

When the EN pin voltage rises above the enable threshold voltage (typically 1.2 V), the controller enters its start-up sequence. The internal LDO regulator starts immediately and regulates to 5 V at the VREG pin. The controller then uses the first 250 μs to calibrate the switching frequency setting resistance attached to the RF pin and stores the switching frequency code in internal registers. However, switching is inhibited during this phase. In the second phase, an internal DAC starts ramping up the reference voltage from 0 V to 0.6 V. Depending on the MODE pin setting, the ramping up time varies from 0.7 ms to 5.6 ms. Smooth and constant ramp-up of the output voltage is maintained during start-up regardless of load current.

**Table 1. Soft-Start and MODE**

| MODE SELECTION | ACTION | SOFT-START TIME (ms) | $R_{MODE}$ (kΩ) |
|---|---|---|---|
| Auto Skip | Pull down to GND | 0.7 | 39 |
| | | 1.4 | 100 |
| | | 2.8 | 200 |
| | | 5.6 | 475 |
| Forced CCM (1) | Connect to PGOOD | 0.7 | 39 |
| | | 1.4 | 100 |
| | | 2.8 | 200 |
| | | 5.6 | 475 |

(1) The device transitions into FCCM after the PGOOD pin goes high.

## Adaptive On-Time D-CAP™ Control

The TPS53315 does not have a dedicated oscillator to determine switching frequency. However, the device operates with pseudo-constant frequency by feed-forwarding the input and output voltages into the on-time one-shot timer. The adaptive on-time control adjusts the on-time to be inversely proportional to the input voltage and proportional to the output voltage $\left( t_{ON} \propto \frac{V_{IN}}{V_{OUT}} \right)$.

This makes the switching frequency fairly constant in steady state conditions over a wide input voltage range. The switching frequency is selectable from eight preset values by a resistor connected between the RF pin and GND or between the RF pin and the VREG pin as shown in Table 2. (Leaving the resistance open sets the switching frequency to 500 kHz.)

**Table 2. Resistor and Switching Frequency**

| RESISTOR ($R_{RF}$) CONNECTIONS | SWITCHING FREQUENCY (kHz) |
|---|---|
| 0 Ω to GND | 250 |
| 187 kΩ to GND | 300 |
| 619 kΩ to GND | 400 |
| Open | 500 |
| 866 kΩ to VREG | 600 |
| 309 kΩ to VREG | 750 |
| 124 kΩ to VREG | 850 |
| 0 Ω to VREG | 970 |

The off-time is modulated by a PWM comparator. The VFB node voltage (the mid-point of resistor divider) is compared to the internal 0.6-V reference voltage added with a ramp signal. When the signal values match, the PWM comparator asserts a set signal to terminate the off-time (turn off the low-side MOSFET and turn on high-side MOSFET). The *set* signal is valid if the inductor current level is below the OCP threshold, otherwise the off-time is extended until the current level falls below the threshold.

Figure 35 and Figure 36 show two on-time control schemes.

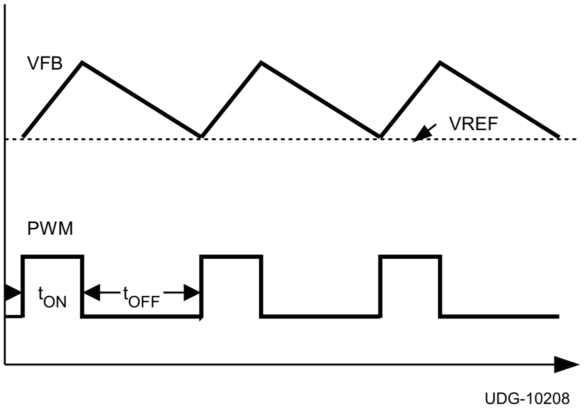


**Figure 35. On-Time Control Without Ramp Compensation**

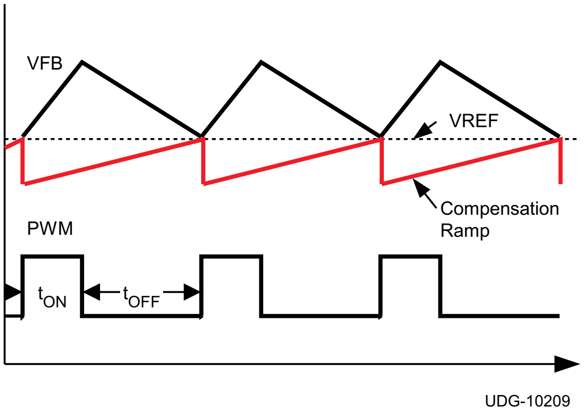


**Figure 36. On-Time Control With Ramp Compensation**

## Small Signal Model

From small-signal loop analysis, a buck converter using D-CAP™ mode can be simplified as shown in Figure 37.

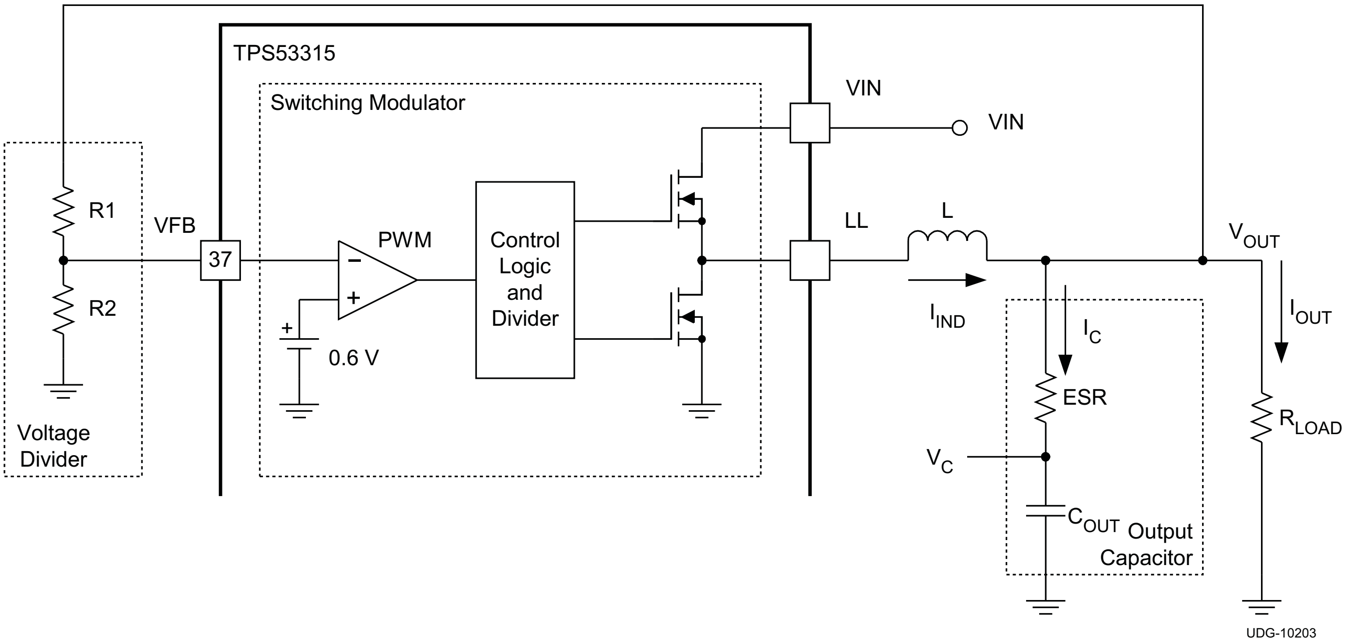


**Figure 37. Simplified Modulator Model**

The output voltage is compared with the internal reference voltage (ramp signal is ignored here for simplicity). The PWM comparator determines the timing to turn on the high-side MOSFET. The gain and speed of the comparator can be assumed high enough to keep the voltage at the beginning of each on-cycle substantially constant.

$$H(s) = \frac{1}{s \times ESR \times C_{OUT}} \quad (1)$$

For the loop stability, the 0 dB frequency, $f_0$, defined in Equation 2 must be lower than ¼ of the switching frequency.

$$f_0 = \frac{1}{2\pi \times ESR \times C_{OUT}} \leq \frac{f_{SW}}{4} \quad (2)$$

According to Equation 2, the loop stability of D-CAP™ mode modulator is mainly determined by the capacitor chemistry. For example, specialty polymer capacitors (SP-CAP) have $C_{OUT}$ on the order of several 100 µF and ESR in range of 10 mΩ. These makes $f_0$ on the order of 100 kHz or less and the loop is stable. However, ceramic capacitors have an $f_0$ at more than 700 kHz, and need special care when used with this modulator. An application circuit using ceramic capacitors is described in External Parts Selection section under *All Ceramic Output Capacitors*.

## Ramp Signal

The TPS53315 adds a ramp signal to the 0.6-V reference in order to improve jitter performance. The feedback voltage is compared with the reference information to keep the output voltage in regulation. By adding a small ramp signal to the reference, the signal-to-noise ratio at the onset of a new switching cycle is improved. Therefore the operation becomes less jittery and more stable. The ramp signal is controlled to start with –7 mV at the beginning of an on-cycle and becomes 0 mV at the end of an off-cycle in steady state.

## Auto-Skip Eco-mode™ Light Load Operation

While the MODE pin is pulled low via $R_{MODE}$, the TPS53315 automatically reduces the switching frequency at light-load conditions to maintain high efficiency. Detailed operation is described as follows. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to the point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The synchronous MOSFET is turned off when this zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode (DCM). The on-time is maintained as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light-load operation $I_{OUT(LL)}$ (i.e., the threshold between continuous and discontinuous conduction mode) can be calculated as shown in Equation 3.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN}}$$

where

- $f_{SW}$ is the PWM switching frequency (3)

Switching frequency versus output current in the light load condition is a function of L, $V_{IN}$ and $V_{OUT}$, but it decreases almost proportionally to the output current from the $I_{OUT(LL)}$ given in Equation 3. For example, it is 60 kHz at $I_{OUT(LL)}/5$ if the frequency setting is 300 kHz.

## Adaptive Zero Crossing

The TPS53315 has an adaptive zero crossing circuit which performs optimization of the zero inductor current detection at skip mode operation. This function pursues ideal low-side MOSFET turning off timing and compensates inherent offset voltage of the Z-C comparator and delay time of the Z-C detection circuit. It prevents SW-node swing-up caused by postponed detection and minimizes diode conduction period caused by premature detection. As a result, better light-load efficiency is delivered.

## Forced Continuous Conduction Mode

When the MODE pin is tied to PGOOD through a resistor, the controller keeps continuous conduction mode (CCM) during light-load conditions. In this mode, the switching frequency is maintained over the entire load range which is suitable for applications needing tight control of the switching frequency at a cost of lower efficiency.

## Power Good

The TPS53315 has powergood output that indicates high when switcher output is within the target. The powergood function is activated after soft-start has finished. If the output voltage becomes within +10% or –5% of the target value, internal comparators detect the powergood state and the powergood signal becomes high after a 1-ms internal delay. If the output voltage goes outside of +15% or –10% of the target value, the power-good signal becomes low after two microsecond (2-µs) internal delay. The powergood output is an open drain output and must be pulled up externally.

In order for the PGOOD logic to be valid, the VDD input must be higher than 1 V. To avoid invalid PGOOD logic before the TPS53315 is powered up, it is recommended the PGOOD be pull to VREG (either directly or through a resistor divider) because VREG remains low when the device is off.

## Current Sense and Overcurrent Protection

TPS53315 has cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the *OFF* state and the controller maintains the *OFF* state during the period in that the inductor current is larger than the overcurrent trip level. In order to provide both good accuracy and cost effective solution, TPS53315 supports temperature compensated MOSFET $R_{DS(on)}$ sensing. The TRIP pin should be connected to GND through the trip voltage setting resistor, $RT_{RIP}$. The TRIP pin sources $I_{TRIP}$ current, which is 10 µA typically at room temperature, and the trip level is set to the OCL trip voltage $V_{TRIP}$ as shown in Equation 4.

$$V_{TRIP}\left(mV\right) = R_{TRIP}\left(k\Omega\right) \times I_{TRIP}\left(\mu A\right) \quad (4)$$

The inductor current is monitored by the voltage between the GND pin and the SW pin so that the SW pin should be connected to the drain terminal of the low-side MOSFET properly. $I_{TRIP}$ has 4700 ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(on)}$. The GND pin is used as the positive current sensing node. The GND pin should be connected to the proper current sensing device, (for example, the source terminal of the low-side MOSFET.)

As the comparison is done during the *OFF* state, $V_{TRIP}$ sets the valley level of the inductor current. Thus, the load current at the overcurrent threshold, $I_{OCP}$, can be calculated as shown in Equation 5.

$$I_{OCP} = \frac{V_{TRIP}}{\left(8 \times R_{DS(on)}\right)} + \frac{I_{IND(ripple)}}{2} = \frac{V_{TRIP}}{\left(8 \times R_{DS(on)}\right)} + \frac{1}{2 \times L \times f_{SW}} \times \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN}} \tag{5}$$

In an overcurrent condition, the current to the load exceeds the current to the output capacitor, therefore the output voltage tends to decrease. Eventually, it crosses the undervoltage protection threshold and shuts down. After a hiccup delay (16 ms with 0.7-ms sort-start), the controller restarts. If the overcurrent condition remains, the procedure is repeated and the device enters hiccup mode.

During CCM, the negative current limit (NCL) protects the internal FET from carrying too much current. The NCL detect threshold is set as the same absolute value as positive OCL but negative polarity. Note that the threshold continues to represent the valley value of the inductor current.

## Overvoltage and Undervoltage Protection

The TPS53315 monitors a resistor divided feedback voltage to detect overvoltage and undervoltage. When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1 ms, TPS53315 latches OFF both high-side and low-side MOSFETs drivers. The controller restarts after a hiccup delay (16 ms with 0.7-ms soft-start). This function is enabled 1.5 ms after the soft-start is completed.

When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches OFF the high-side MOSFET driver and latches ON the low-side MOSFET driver. The output voltage decreases. If the output voltage reaches the UV threshold, then both high-side MOSFET and low-side MOSFET driver is OFF and the device restarts after a hiccup delay. If the OV condition remains, both high-side MOSFET and low-side MOSFET driver remains OFF until the OV condition is removed.

## UVLO Protection

The TPS53315 uses VREG undervoltage lockout protection (UVLO). When the VREG voltage is lower than the UVLO threshold voltage, the switch mode power supply shuts off. This is a non-latch protection.

## Thermal Shutdown

TPS53315 includes a temperature monitoring feature. If the temperature exceeds the threshold value (typically 145°C), TPS53315 shuts off. When the temperature falls approximately 10°C below the threshold value, the device turns on again. This is a non-latch protection.

## External Parts Selection

The external components selection is a simple process using D-CAP™ Mode.

1. CHOOSE THE INDUCTOR

   The inductance value should be determined to give the ripple current of approximately 1/4 to ½ of maximum output current. Larger ripple current increases output ripple voltage and improves signal-to-noise ratio and helps stable operation.

$$L = \frac{1}{I_{IND(ripple)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{3}{I_{OUT(max)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \qquad (6)$$

   The inductor requires a low DCR to achieve good efficiency. It also requires enough room above peak inductor current before saturation. The peak inductor current can be estimated in Equation 7.

$$I_{IND(peak)} = \frac{V_{TRIP}}{8 \times R_{DS(on)}} + \frac{1}{L \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \qquad (7)$$

2. CHOOSE THE OUTPUT CAPACITOR(S)

   When organic semiconductor capacitor(s) or specialty polymer capacitor(s) are used, for loop stability, capacitance and ESR should satisfy Equation 2. For jitter performance, Equation 8 is a good starting point to determine ESR.

$$ESR = \frac{V_{OUT} \times 10(mV) \times (1 - D)}{0.6(V) \times I_{IND(ripple)}} = \frac{10(mV) \times L \times f_{SW}}{0.6(V)} = \frac{L \times f_{SW}}{60} (\Omega)$$

   where

   - D is the duty factor
   - $t_{SW}$ is the switching period
   - the required output ripple slope is approximately 20 mV per $t_{SW}$ in terms of $V_{VFB}$ (8)

3. DETERMINE THE VALUE OF R1 AND R2

   The output voltage is programmed by the voltage-divider resistor, R1 and R2 shown in Figure 37. R1 is connected between VFB pin and the output, and R2 is connected between the VFB pin and GND. Recommended R2 value is from 10kΩ to 20kΩ. Determine R1 using Equation 9.

$$R1 = \frac{V_{OUT} - \frac{I_{IND(ripple)} \times ESR}{2} - 0.6}{0.6} \times R2 \qquad (9)$$

## External Parts Selection with All Ceramic Output Capacitors

When ceramic output capacitors are used, the stability criteria in Equation 2 cannot be satisfied. The ripple injection approach as shown in Equation 10 is implemented to increase the ripple on the VFB pin and make the system stable. C2 can be fixed at 1 nF. The value of C1 can be selected between 10 nF to 200 nF.

The increased ripple on the VFB pin causes the increase of the VFB DC value. The AC ripple coupled to the VFB pin has two components, one coupled from SW node and the other coupled from $V_{OUT}$ and they can be calculated using Equation 10 and Equation 11.

$$V_{INJ\_SW} = \frac{V_{IN} - V_{OUT}}{R7 \times C1} \times \frac{D}{f_{SW}} \tag{10}$$

$$V_{INJ\_OUT} = ESR \times I_{IND(ripple)} + \frac{I_{IND(ripple)}}{8 \times C_{OUT} \times f_{SW}} \tag{11}$$

The DC value of VFB can be calculated by Equation 12:

$$V_{VFB} = 0.6 + \frac{V_{INJ\_SW} + V_{INJ\_OUT}}{2} \tag{12}$$

And the resistor divider value can be determined by Equation 13:

$$R1 = \frac{V_{OUT} - V_{FB}}{V_{FB}} \times R2 \tag{13}$$

## LAYOUT CONSIDERATIONS

Certain points must be considered before starting a layout work using the TPS53315.

- The power components (including input/output capacitors, inductor and TPS53315) should be placed on one side of the PCB (solder side). Other small signal components should be placed on another side (component side). At least one inner plane should be inserted, connected to ground, in order to shield and isolate the small signal traces from noisy power lines.
- All sensitive analog traces and components such as VFB, PGOOD, TRIP, MODE and RF should be placed away from high-voltage switching nodes such as LL, VBST to avoid coupling. Use internal layer(s) as ground plane(s) and shield feedback trace from power traces and components.
- Place the VIN decoupling capacitors as close to the VIN and PGND pins as possible to minimize the input AC current loop.
- Since the TPS53315 controls output voltage referring to voltage across the $V_{OUT}$ capacitor, the top-side resistor of the voltage divider should be connected to the positive node of VOUT capacitor. In a same manner both bottom side resistor and GND pad of the device should be connected to the negative node of $V_{OUT}$ capacitor. The trace from these resistors to the VFB pin should be short and thin. Place on the component side and avoid via(s) between these resistors and the device.
- Connect the overcurrent setting resistors from TRIP pin to ground and make the connections as close as possible to the device. The trace from TRIP pin to resistor and from resistor to ground should avoid coupling to a high-voltage switching node.
- Connect the frequency setting resistor from RF pin to ground, or to the VREG pin, and make the connections as close as possible to the device. The trace from the RF pin to the resistor and from the resistor to ground should avoid coupling to a high-voltage switching node.
- Connect the MODE setting resistor from MODE pin to ground, or to the PGOOD pin, and make the connections as close as possible to the device. The trace from the MODE pin to the resistor and from the resistor to ground should avoid coupling to a high-voltage switching node.
- The PCB trace defined as switch node, which connects the LL pins and high-voltage side of the inductor, should be as short and wide as possible.

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/ Ball Finish | MSL Peak Temp [3] | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| TPS53315RGFR | ACTIVE | VQFN | RGF | 40 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | Purchase Samples |
| TPS53315RGFT | ACTIVE | VQFN | RGF | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | Request Free Samples |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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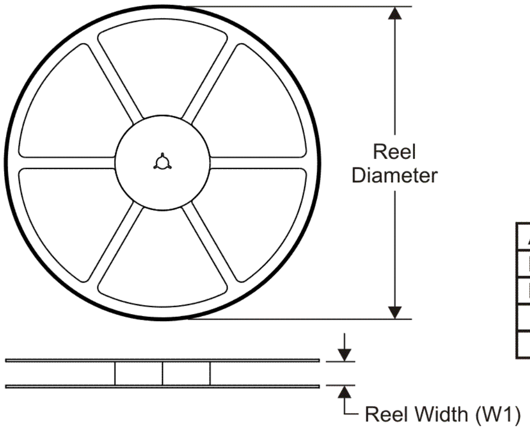
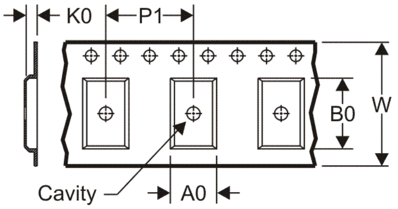
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

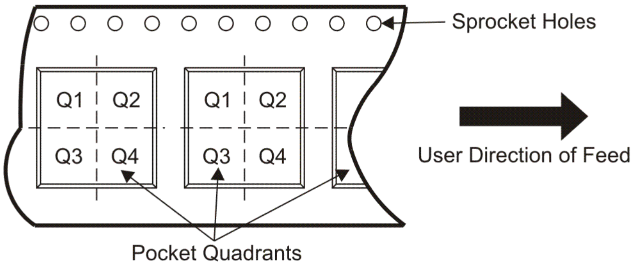


**TAPE DIMENSIONS**



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

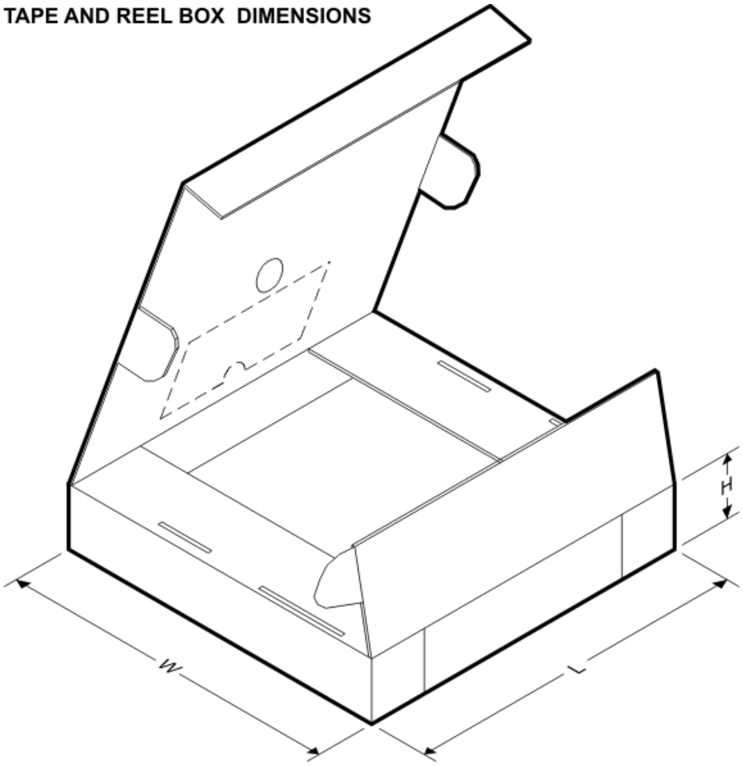
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS53315RGFR | VQFN | RGF | 40 | 3000 | 330.0 | 16.4 | 5.25 | 7.25 | 1.45 | 8.0 | 16.0 | Q1 |
| TPS53315RGFT | VQFN | RGF | 40 | 250 | 180.0 | 16.4 | 5.25 | 7.25 | 1.45 | 8.0 | 16.0 | Q1 |

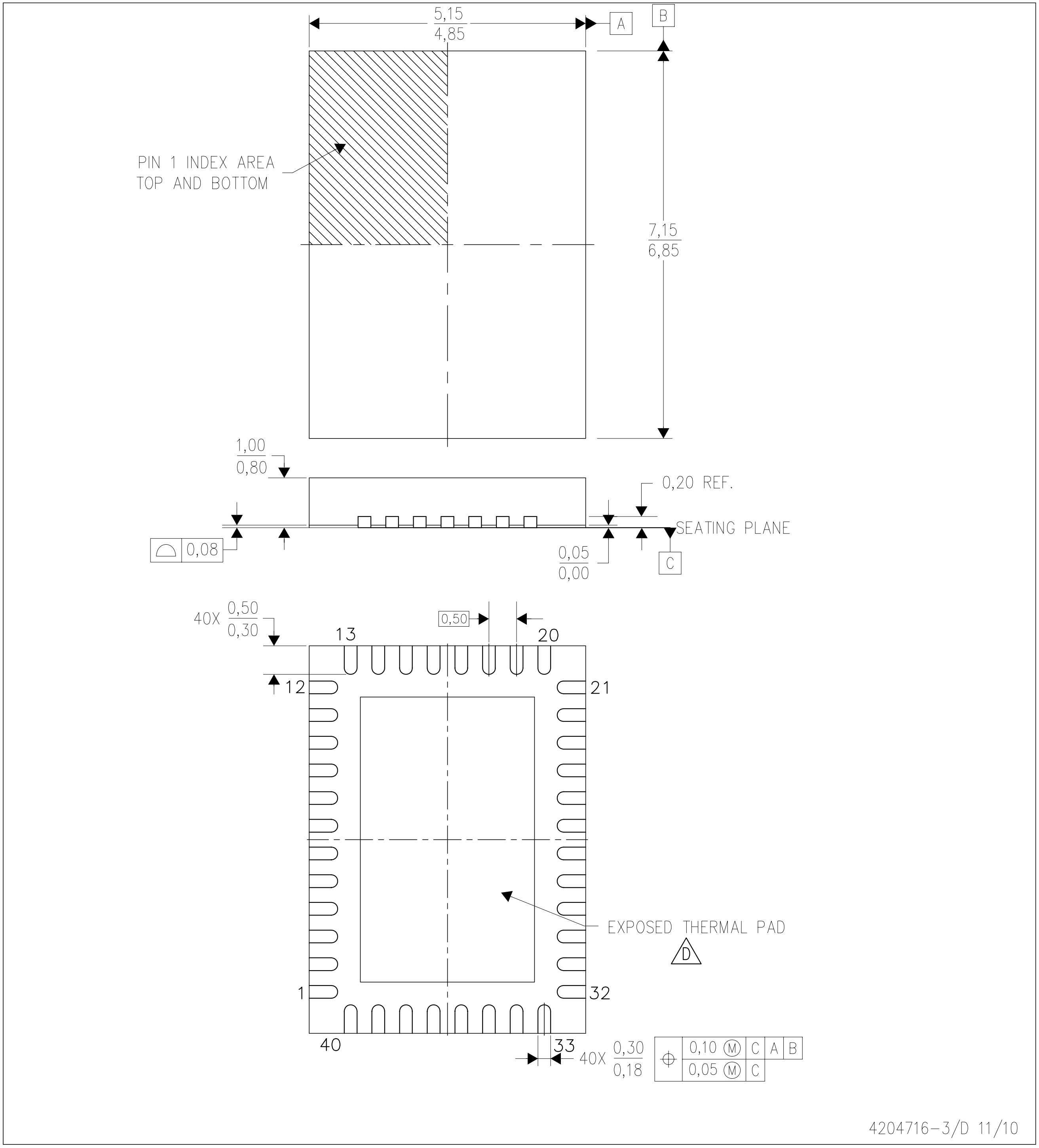
## TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS53315RGFR | VQFN | RGF | 40 | 3000 | 346.0 | 346.0 | 33.0 |
| TPS53315RGFT | VQFN | RGF | 40 | 250 | 190.5 | 212.7 | 31.8 |

## RGF (R–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

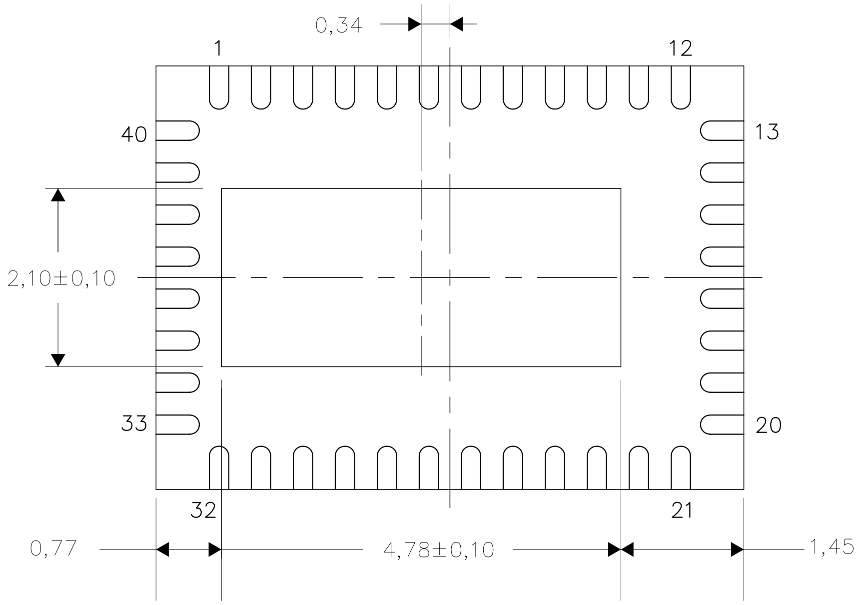
RGF (R-PVQFN-N40) PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



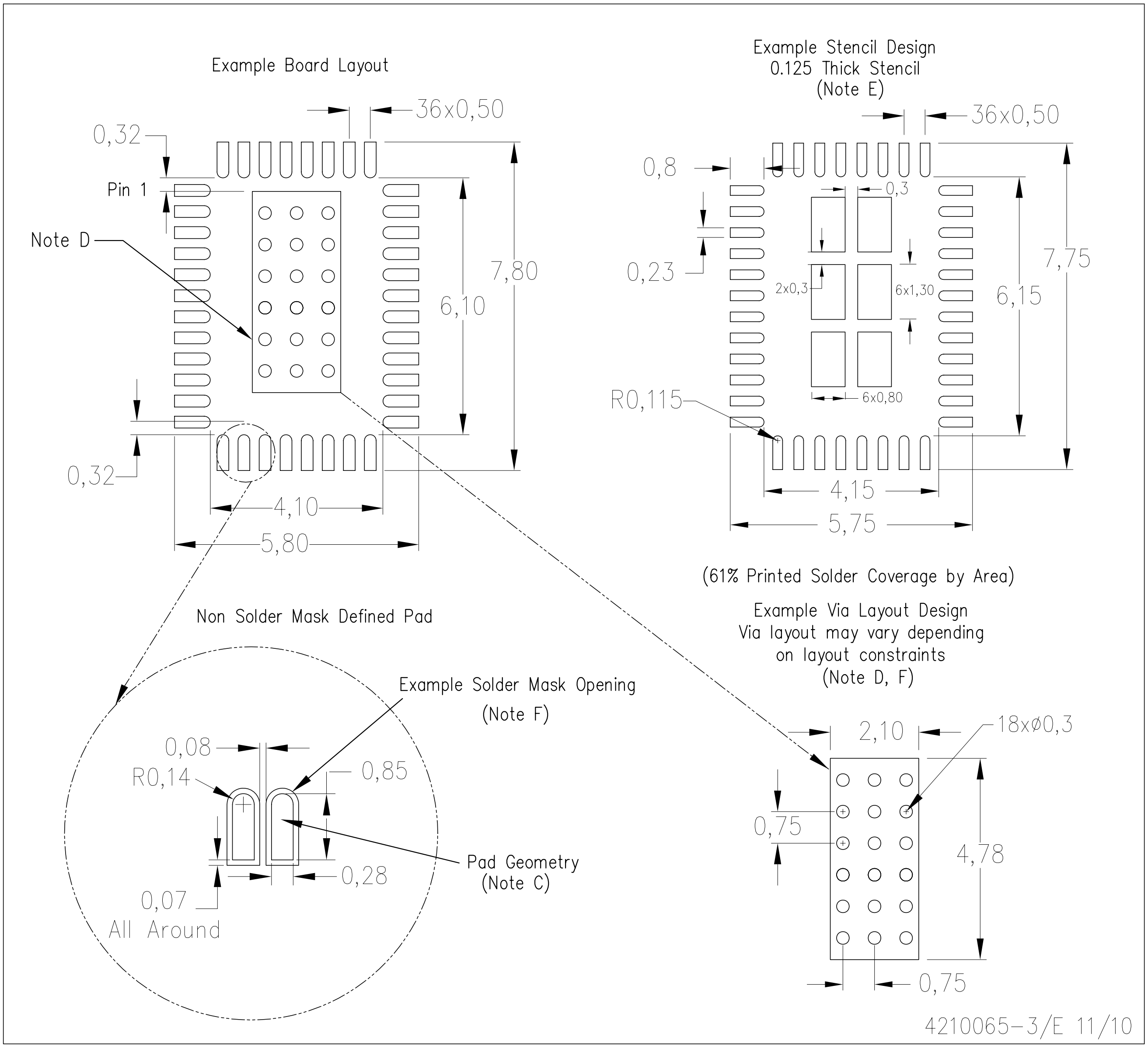
Bottom View

Exposed Thermal Pad Dimensions

4206345-7/I 11/10

NOTE: A. All linear dimensions are in millimeters

## RGF (R–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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