January 2011

FAN3213 / FAN3214
Dual-4A, High-Speed, Low-Side Gate Drivers

Features

- Industry-Standard Pinouts
- 4.5 to 18V Operating Range
- 5A Peak Sink/Source at V_{DD} = 12V
- 4.3A Sink / 2.8A Source at V_{OUT} = 6V
- TTL Input Thresholds
- Two Versions of Dual Independent Drivers:
  - Dual Inverting (FAN3213)
  - Dual Non-Inverting (FAN3214)
- Internal Resistors Turn Driver Off If No Inputs
- MillerDrive™ Technology
- 12ns / 9ns Typical Rise/Fall Times with 2.2nF Load
- Typical Propagation Delay Under 20ns Matched within 1ns to the Other Channel
- Double Current Capability by Paralleling Channels
- Standard SOIC-8 Package
- Rated from –40°C to +125°C Ambient

Applications

- Switch-Mode Power Supplies
- High-Efficiency MOSFET Switching
- Synchronous Rectifier Circuits
- DC-to-DC Converters
- Motor Control

Description

The FAN3213 and FAN3214 dual 4A gate drivers are designed to drive N-channel enhancement-mode MOSFETs in low-side switching applications by providing high peak current pulses during the short switching intervals. They are both available with TTL input thresholds. Internal circuitry provides an under-voltage lockout function by holding the output LOW until the supply voltage is within the operating range. In addition, the drivers feature matched internal propagation delays between A and B channels for applications requiring dual gate drives with critical timing, such as synchronous rectifiers. This also enables connecting two drivers in parallel to effectively double the current capability driving a single MOSFET.

The FAN3213/14 drivers incorporate MillerDrive™ architecture for the final output stage. This bipolar-MOSFET combination provides high current during the Miller plateau stage of the MOSFET turn-on / turn-off process to minimize switching loss, while providing rail-to-rail voltage swing and reverse current capability.

The FAN3213 offers two inverting drivers and the FAN3214 offers two non-inverting drivers. Both are offered in a standard 8-pin SOIC package.

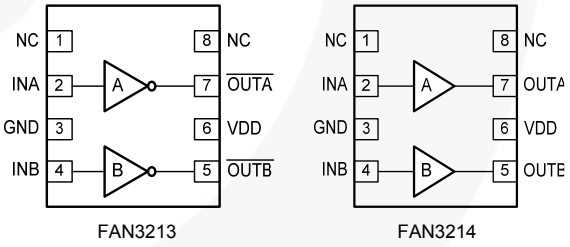


Figure 1. Pin Configurations

Ordering Information

Part Number	Logic	Input Threshold	Package	Packing Method	Quantity per Reel
FAN3213TMX	Dual Inverting Channels	TTL	SOIC-8	Tape & Reel	2,500
FAN3214TMX	Dual Non-Inverting Channels	TTL	SOIC-8	Tape & Reel	2,500

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Package Outlines

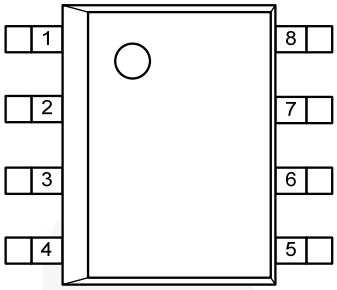


Figure 2. SOIC-8 (Top View)

Thermal Characteristics[1]

Package	Θ_{JL}[2]	Θ_{JT}[3]	Θ_{JA}[4]	Ψ_{JB}[5]	Ψ_{JT}[6]	Units
8-Pin Small Outline Integrated Circuit (SOIC)	38	29	87	41	2.3	°C/W

Notes:

1. Estimates derived from thermal simulation; actual values depend on the application.
2. Theta_JL (Θ_{JL}): Thermal resistance between the semiconductor junction and the bottom surface of all the leads (including any thermal pad) that are typically soldered to a PCB.
3. Theta_JT (Θ_{JT}): Thermal resistance between the semiconductor junction and the top surface of the package, assuming it is held at a uniform temperature by a top-side heatsink.
4. Theta_JA (Θ_{JA}): Thermal resistance between junction and ambient, dependent on the PCB design, heat sinking, and airflow. The value given is for natural convection with no heatsink, using a 2S2P board, as specified in JEDEC standards JESD51-2, JESD51-5, and JESD51-7, as appropriate.
5. Psi_JB (Ψ_{JB}): Thermal characterization parameter providing correlation between semiconductor junction temperature and an application circuit board reference point for the thermal environment defined in Note 4. For the SOIC-8 package, the board reference is defined as the PCB copper adjacent to pin 6.
6. Psi_JT (Ψ_{JT}): Thermal characterization parameter providing correlation between the semiconductor junction temperature and the center of the top of the package for the thermal environment defined in Note 4.

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Pin Configurations

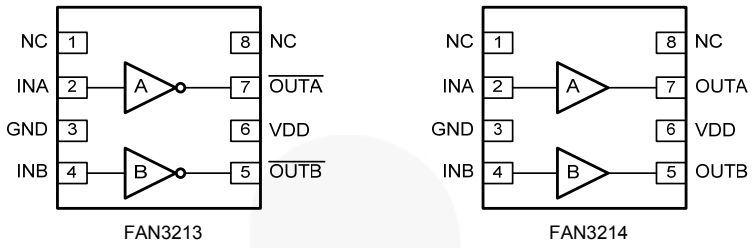


Figure 3. Pin Configurations (Repeated)

Pin Definitions

Pin	Name	Pin Description
1	NC	**No Connect.** This pin can be grounded or left floating.
2	INA	**Input to Channel A**.
3	GND	**Ground**. Common ground reference for input and output circuits.
2	INA	**Input to Channel A**.
4	INB	**Input to Channel B**.
7	OUTA	**Gate Drive Output A**: Held LOW unless required input(s) are present and V_{DD} is above UVLO threshold.
5 (FAN3213)	$\overline{\text{OUTB}}$	**Gate Drive Output B** (inverted from the input): Held LOW unless required input is present and V_{DD} is above UVLO threshold.
5 (FAN3214)	OUTB	**Gate Drive Output B**: Held LOW unless required input(s) are present and V_{DD} is above UVLO threshold.
6	VDD	**Supply Voltage**. Provides power to the IC.
7 (FAN3213)	$\overline{\text{OUTA}}$	**Gate Drive Output A** (inverted from the input): Held LOW unless required input is present and V_{DD} is above UVLO threshold.
7 (FAN3214)	OUTA	**Gate Drive Output A**: Held LOW unless required input(s) are present and V_{DD} is above UVLO threshold.
8	NC	**No Connect.** This pin can be grounded or left floating.

Output Logic

FAN3213 (x=A or B)	
INx	**$\overline{\text{OUTx}}$**
0	0
1[7]	0
0	1
1[7]	0

FAN3214 (x=A or B)	
INx	**OUTx**
0[7]	0
1	0
0[7]	0
1	1

Note:
7. Default input signal if no external connection is made.

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Block Diagrams

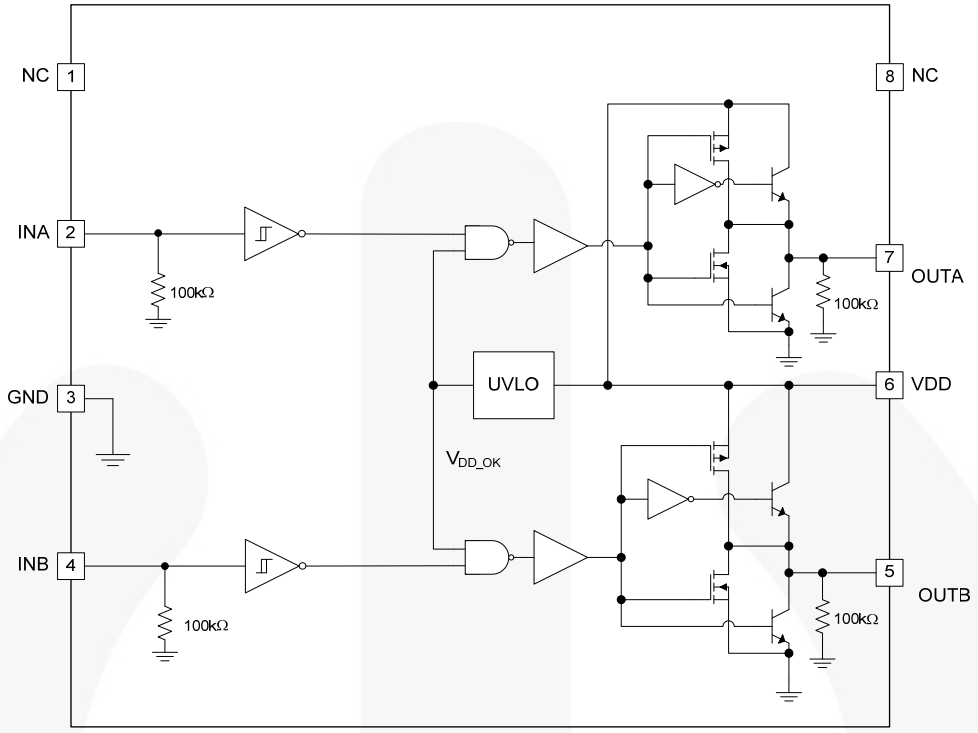


Figure 4. FAN3213 Block Diagram

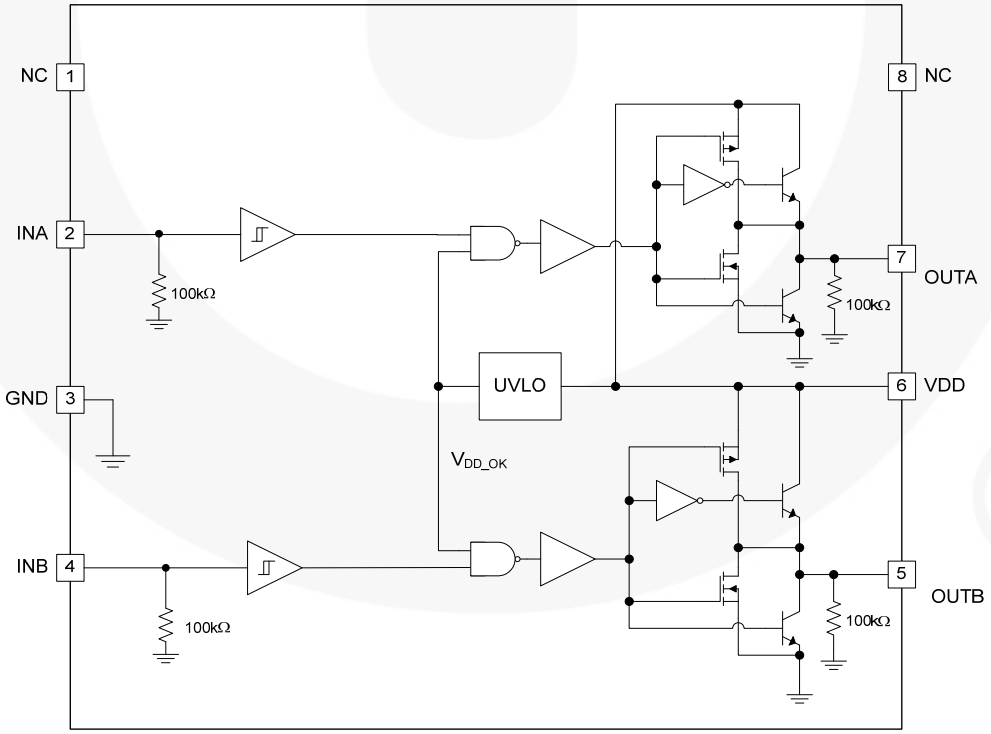


Figure 5. FAN3214 Block Diagram

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	VDD to PGND		-0.3	20.0	V
V_{IN}	INA, INA+, INA–, INB, INB+ and INB– to GND		GND - 0.3	V_{DD} + 0.3	V
V_{OUT}	OUTA and OUTB to GND		GND - 0.3	V_{DD} + 0.3	V
T_L	Lead Soldering Temperature (10 Seconds)			+260	ºC
T_J	Junction Temperature		-55	+150	ºC
T_{STG}	Storage Temperature		-65	+150	ºC
ESD	Electrostatic Discharge Protection Level	Human Body Model, JEDEC JESD22-A114	4		kV
		Charged Device Model, JEDEC JESD22-C101	1		

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage Range	4.5	18.0	V
V_{IN}	Input Voltage INA, INA+, INA–, INB, INB+ and INB–	0	V_{DD}	V
T_A	Operating Ambient Temperature	-40	+125	ºC

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Electrical Characteristics

Unless otherwise noted, V_{DD}=12V, T_J=-40°C to +125°C. Currents are defined as positive into the device and negative out of the device.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply						
V_{DD}	Operating Range		4.5		18.0	V
I_{DD}	Supply Current, Inputs Not Connected			0.70	0.95	mA
V_{ON}	Turn-On Voltage	INA = V_{DD}, INB = 0V	3.5	3.9	4.3	V
V_{OFF}	Turn-Off Voltage	INA = V_{DD}, INB = 0V	3.3	3.7	4.1	V
Inputs						
V_{IL_T}	INx Logic Low Threshold		0.8	1.2		V
V_{IH_T}	INx Logic High Threshold			1.6	2.0	V
I_{IN+}	Non-Inverting Input	IN from 0 to V_{DD}	-1.5		175.0	µA
I_{IN-}	Inverting Input	IN from 0 to V_{DD}	-175.0		1.5	µA
V_{HYS_T}	TTL Logic Hysteresis Voltage		0.2	0.4	0.8	V
Output						
I_{SINK}	OUT Current, Mid-Voltage, Sinking[8]	OUTx at V_{DD}/2, C_{LOAD}=0.22µF, f=1kHz		4.3		A
I_{SOURCE}	OUT Current, Mid-Voltage, Sourcing[8]	OUTx at V_{DD}/2, C_{LOAD}=0.22µF, f=1kHz		-2.8		A
I_{PK_SINK}	OUT Current, Peak, Sinking[8]	C_{LOAD}=0.22µF, f=1kHz		5		A
I_{PK_SOURCE}	OUT Current, Peak, Sourcing[8]	C_{LOAD}=0.22µF, f=1kHz		-5		A
t_{RISE}	Output Rise Time[9]	C_{LOAD}=2200pF		12	20	ns
t_{FALL}	Output Fall Time[9]	C_{LOAD}=2200pF		9	17	ns
t_{D1}, t_{D2}	Output Propagation Delay, TTL Inputs[9]	0 - 5V_{IN}, 1V/ns Slew Rate	9	17	29	ns
	Propagation Matching Between Channels	INA=INB, OUTA and OUTB at 50% Point		2	4	ns
I_{RVS}	Output Reverse Current Withstand[8]			500		mA

Notes:

8. Not tested in production.
9. *See Timing Diagrams of Figure 6 and Figure 7.*

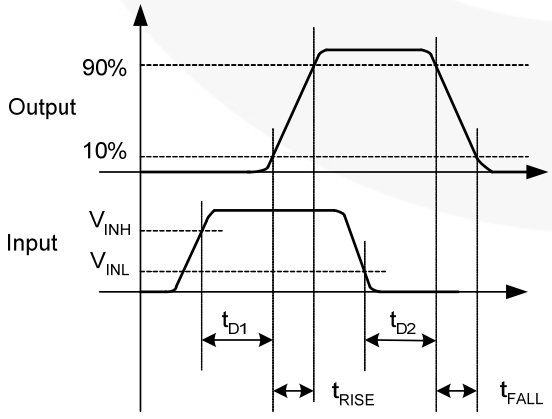


Figure 6. Non-Inverting Timing Diagram

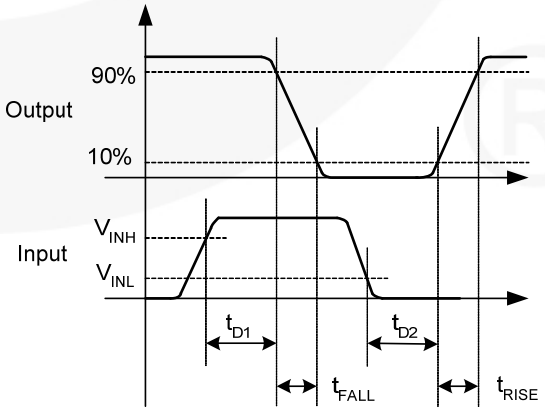


Figure 7. Inverting Timing Diagram

Typical Performance Characteristics

Typical characteristics are provided at T_A=25°C and V_{DD}=12V unless otherwise noted.

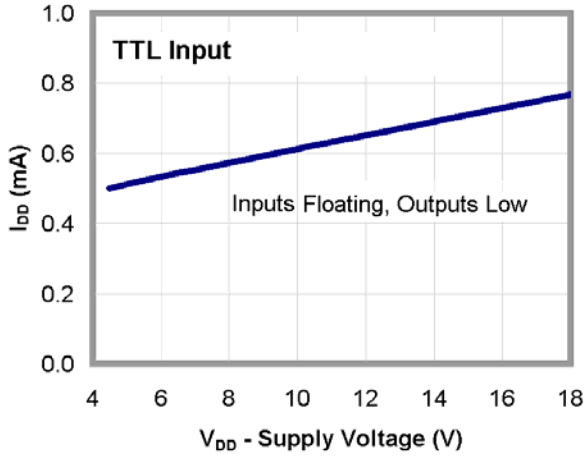


Figure 8. I_{DD} (Static) vs. Supply Voltage(10)

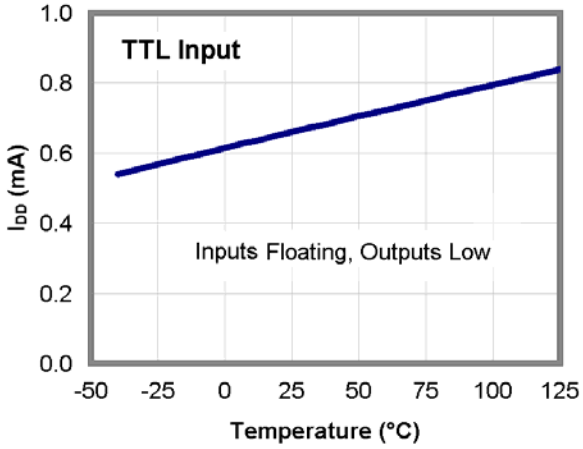


Figure 9. I_{DD} (Static) vs. Temperature(10)

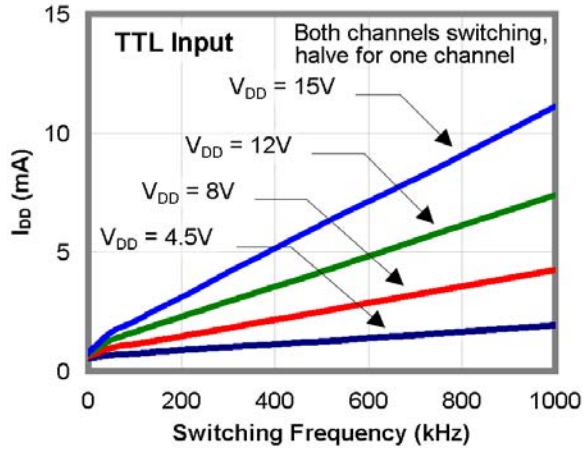


Figure 10. I_{DD} (No Load) vs. Frequency

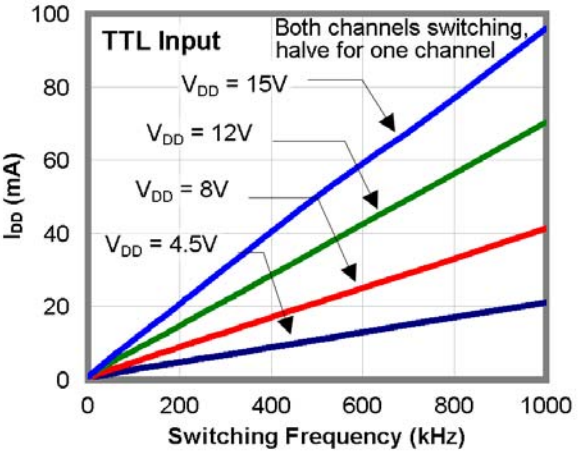


Figure 11. I_{DD} (2.2nF Load) vs. Frequency

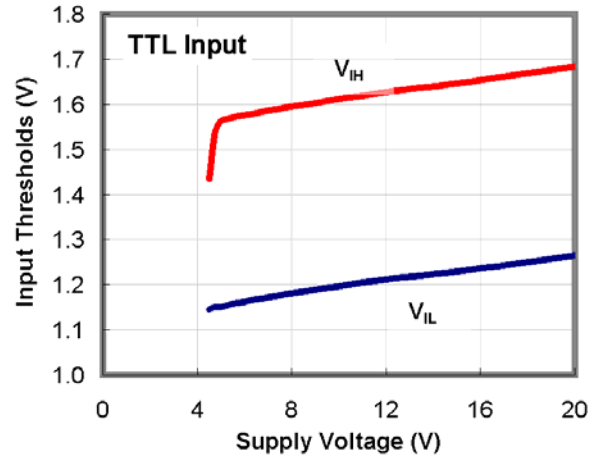


Figure 12. Input Thresholds vs. Supply Voltage

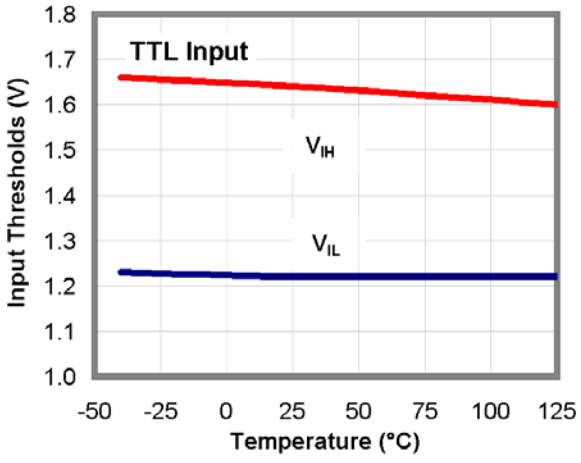
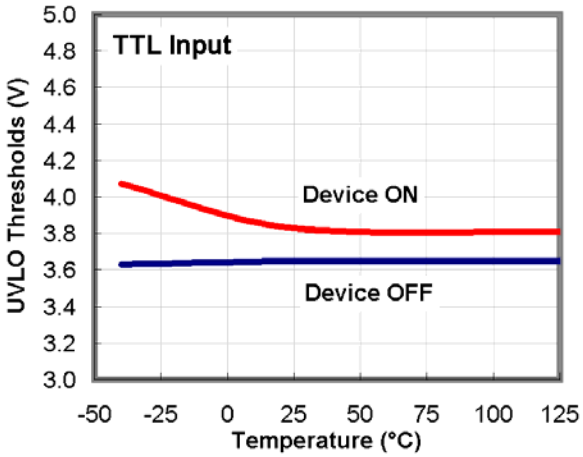


Figure 13. Input Thresholds vs. Temperature

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Typical Performance Characteristics

Typical characteristics are provided at T_A=25°C and V_{DD}=12V unless otherwise noted.



UVLO Threshold vs. Temperature

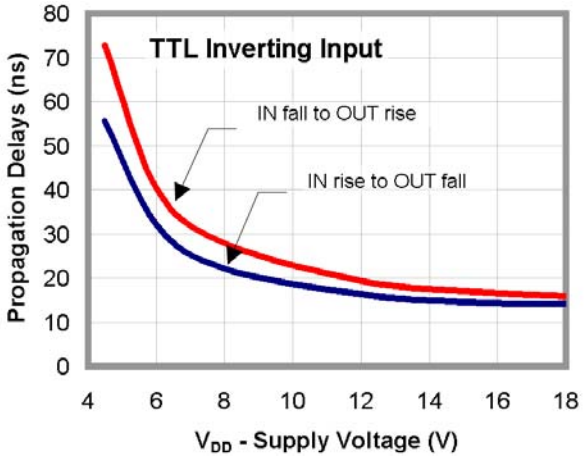


Figure 14. Propagation Delay vs. Supply Voltage

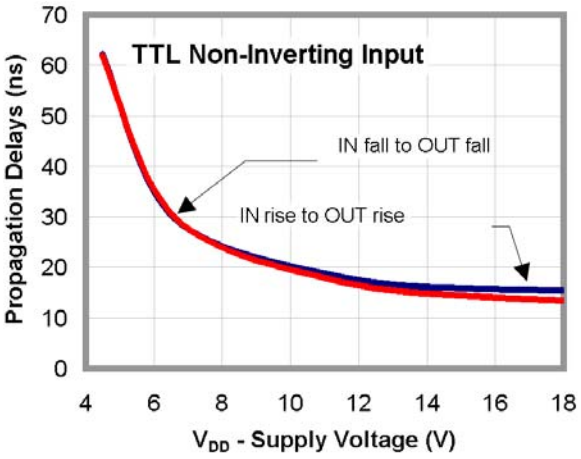


Figure 15. Propagation Delay vs. Supply Voltage

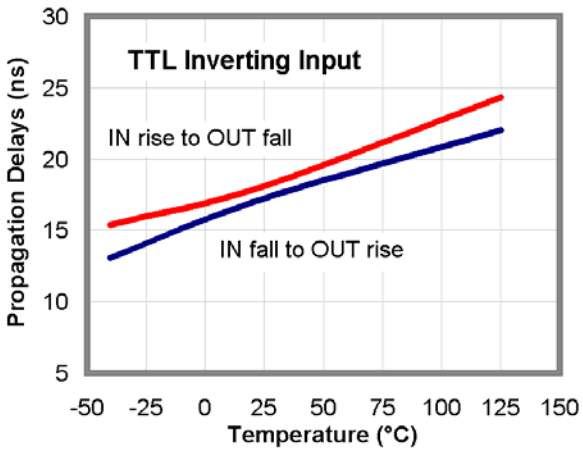


Figure 16. Propagation Delays vs. Temperature

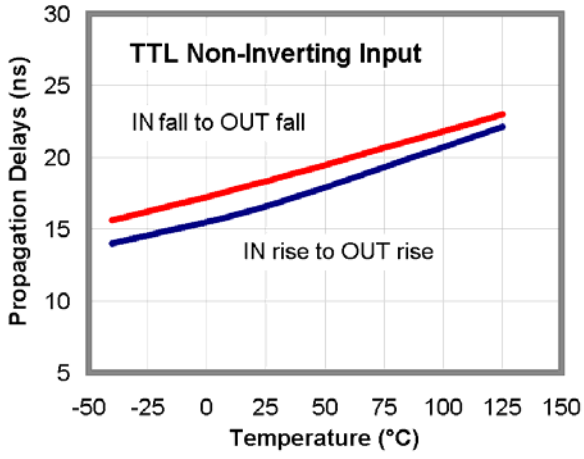


Figure 17. Propagation Delays vs. Temperature

Typical Performance Characteristics

Typical characteristics are provided at T_A=25°C and V_{DD}=12V unless otherwise noted.

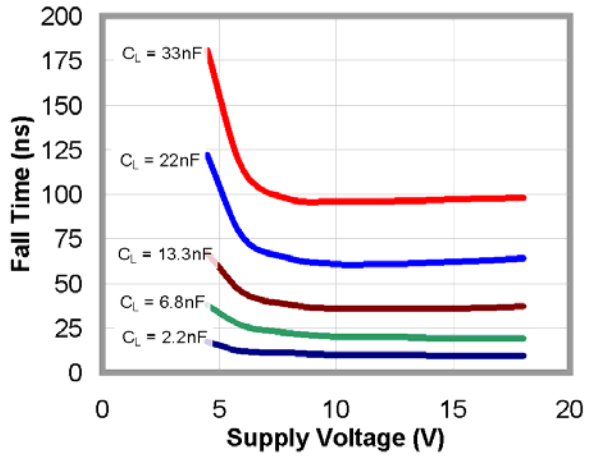


Figure 18. Fall Time vs. Supply Voltage

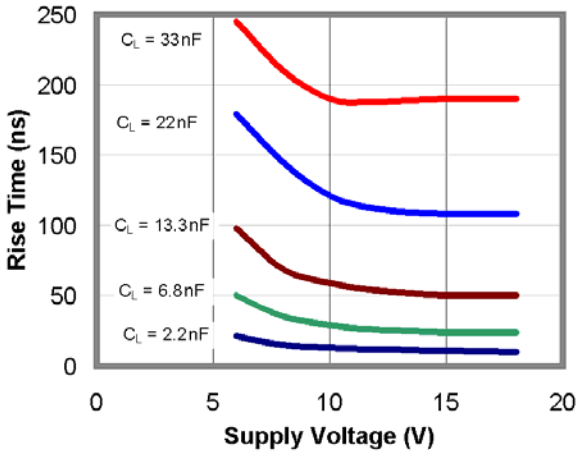


Figure 19. Rise Time vs. Supply Voltage

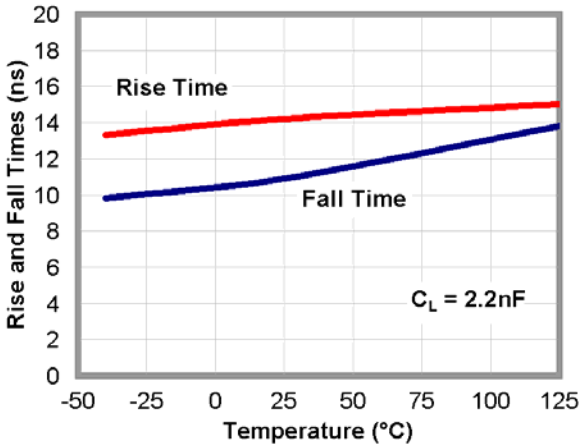


Figure 20. Rise and Fall Times vs. Temperature

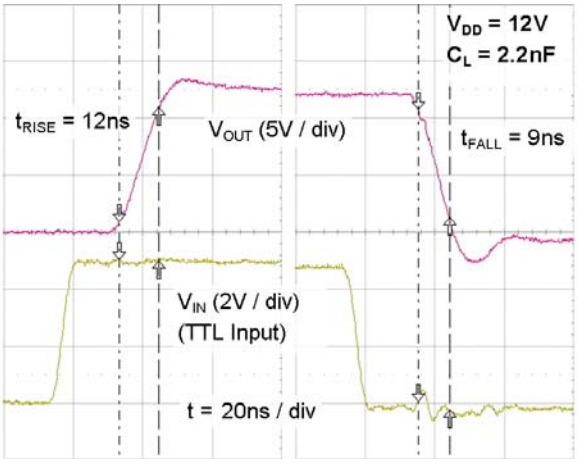


Figure 21. Rise/Fall Waveforms with 2.2nF Load

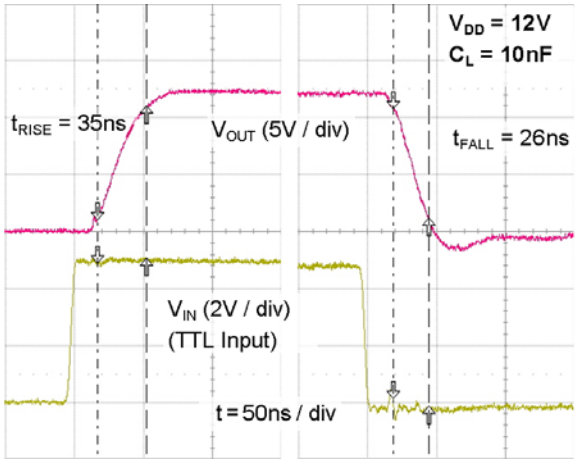


Figure 22. Rise/Fall Waveforms with 10nF Load

Typical Performance Characteristics

Typical characteristics are provided at T_A=25°C and V_{DD}=12V unless otherwise noted.

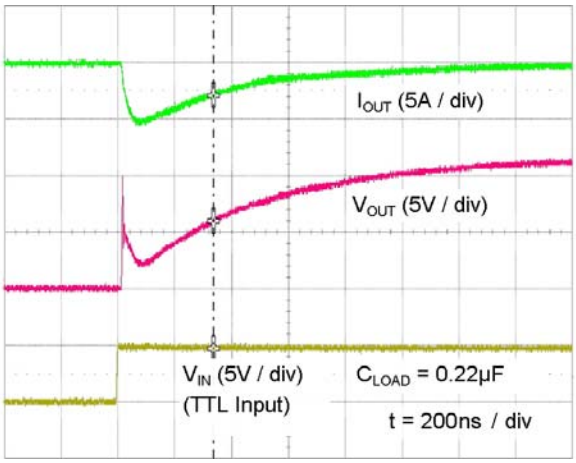


Figure 23. Quasi-Static Source Current with V_{DD}=12V(11)

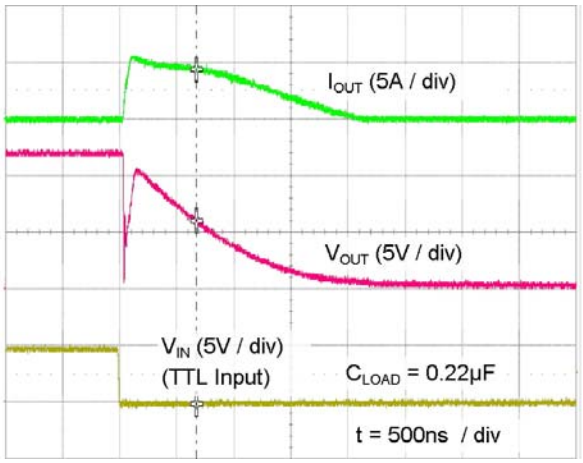


Figure 24. Quasi-Static Sink Current with V_{DD}=12V(11)

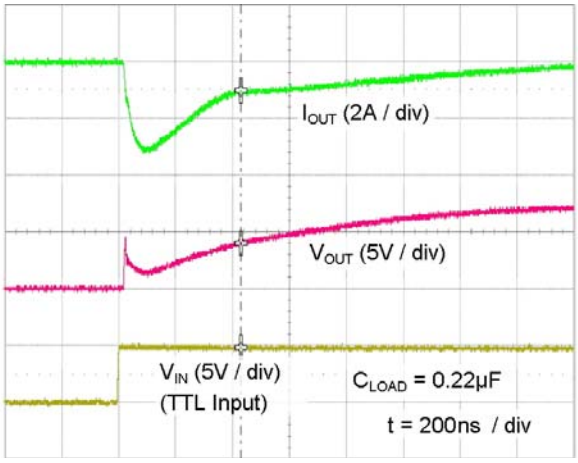


Figure 25. Quasi-Static Source Current with V_{DD}=8V(11)

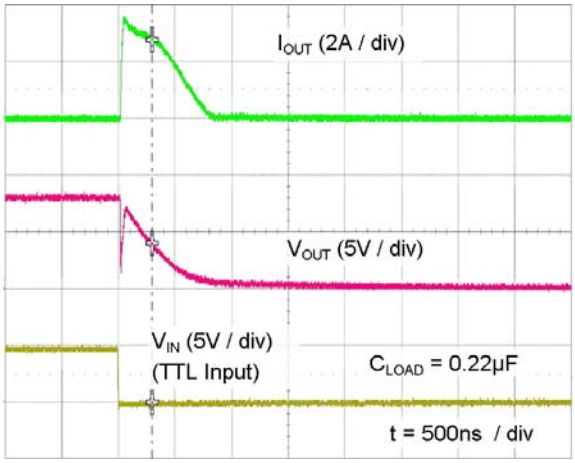


Figure 26. Quasi-Static Sink Current with V_{DD}=8V(11)

Notes:

10. For any inverting inputs pulled LOW, non-inverting inputs pulled HIGH, or outputs driven HIGH; static I_{DD} increases by the current flowing through the corresponding pull-up/down resistor shown in Figure 4 and Figure 5.
11. The initial spike in each current waveform is a measurement artifact caused by the stray inductance of the current-measurement loop.

Test Circuit

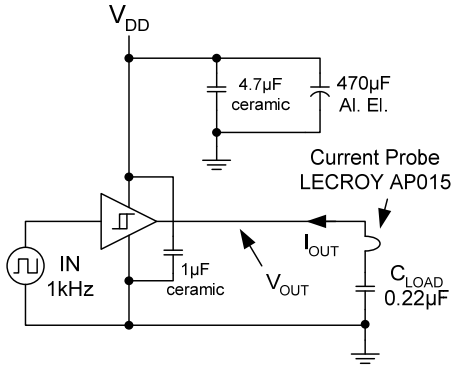


Figure 27. Quasi-Static I_{OUT} / V_{OUT} Test Circuit

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Applications Information

Input Thresholds

The FAN3213 and the FAN3214 drivers consist of two identical channels that may be used independently at rated current or connected in parallel to double the individual current capacity.

The input thresholds meet industry-standard TTL-logic thresholds independent of the V_{DD} voltage, and there is a hysteresis voltage of approximately 0.4V. These levels permit the inputs to be driven from a range of input logic signal levels for which a voltage over 2V is considered logic HIGH. The driving signal for the TTL inputs should have fast rising and falling edges with a slew rate of 6V/µs or faster, so a rise time from 0 to 3.3V should be 550ns or less. With reduced slew rate, circuit noise could cause the driver input voltage to exceed the hysteresis voltage and retrigger the driver input, causing erratic operation.

Static Supply Current

In the I_{DD} (static) typical performance characteristics shown in Figure 8 and Figure 9, each curve is produced with both inputs floating and both outputs LOW to indicate the lowest static I_{DD} current. For other states, additional current flows through the 100kΩ resistors on the inputs and outputs shown in the block diagram of each part *(see Figure 4 and Figure 5)*. In these cases, the actual static I_{DD} current is the value obtained from the curves plus this additional current.

MillerDrive™ Gate Drive Technology

FAN3213 and FAN3214 gate drivers incorporate the MillerDrive™ architecture shown in Figure 28. For the output stage, a combination of bipolar and MOS devices provide large currents over a wide range of supply voltage and temperature variations. The bipolar devices carry the bulk of the current as OUT swings between 1/3 to 2/3 V_{DD} and the MOS devices pull the output to the HIGH or LOW rail.

The purpose of the MillerDrive™ architecture is to speed up switching by providing high current during the Miller plateau region when the gate-drain capacitance of the MOSFET is being charged or discharged as part of the turn-on / turn-off process.

For applications with zero voltage switching during the MOSFET turn-on or turn-off interval, the driver supplies high peak current for fast switching even though the Miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before the MOSFET is switched ON.

The output pin slew rate is determined by V_{DD} voltage and the load on the output. It is not user adjustable, but a series resistor can be added if a slower rise or fall time at the MOSFET gate is needed.

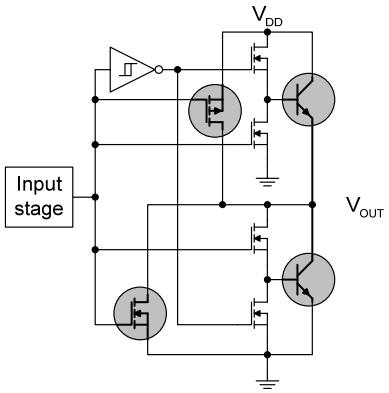


Figure 28. MillerDrive™ Output Architecture

Under-Voltage Lockout

The FAN321x startup logic is optimized to drive ground-referenced N-channel MOSFETs with an under-voltage lockout (UVLO) function to ensure that the IC starts up in an orderly fashion. When V_{DD} is rising, yet below the 3.9V operational level, this circuit holds the output LOW, regardless of the status of the input pins. After the part is active, the supply voltage must drop 0.2V before the part shuts down. This hysteresis helps prevent chatter when low V_{DD} supply voltages have noise from the power switching. This configuration is not suitable for driving high-side P-channel MOSFETs because the low output voltage of the driver would turn the P-channel MOSFET on with V_{DD} below 3.9V.

V_{DD} Bypass Capacitor Guidelines

To enable this IC to turn a device ON quickly, a local high-frequency bypass capacitor, C_{BYP}, with low ESR and ESL should be connected between the VDD and GND pins with minimal trace length. This capacitor is in addition to bulk electrolytic capacitance of 10µF to 47µF commonly found on driver and controller bias circuits.

A typical criterion for choosing the value of C_{BYP} is to keep the ripple voltage on the V_{DD} supply to ≤ 5%. This is often achieved with a value ≥ 20 times the equivalent load capacitance C_{EQV}, defined here as Q_{GATE}/V_{DD}. Ceramic capacitors of 0.1µF to 1µF or larger are common choices, as are dielectrics, such as X5R and X7R, with good temperature characteristics and high pulse current capability.

If circuit noise affects normal operation, the value of C_{BYP} may be increased, to 50-100 times the C_{EQV}, or C_{BYP} may be split into two capacitors. One should be a larger value, based on equivalent load capacitance, and the other a smaller value, such as 1-10nF mounted closest to the VDD and GND pins to carry the higher-frequency components of the current pulses. The bypass capacitor must provide the pulsed current from both of the driver channels and, if the drivers are switching simultaneously, the combined peak current sourced from the C_{BYP} would be twice as large as when a single channel is switching.

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Layout and Connection Guidelines

The FAN3213 and FAN3214 gate drivers incorporate fast-reacting input circuits, short propagation delays, and powerful output stages capable of delivering current peaks over 4A to facilitate voltage transition times from under 10ns to over 150ns. The following layout and connection guidelines are strongly recommended:

- Keep high-current output and power ground paths separate from logic input signals and signal ground paths. This is especially critical for TTL-level logic thresholds at driver input pins.
- Keep the driver as close to the load as possible to minimize the length of high-current traces. This reduces the series inductance to improve high-speed switching, while reducing the loop area that can radiate EMI to the driver inputs and surrounding circuitry.
- If the inputs to a channel are not externally connected, the internal 100kΩ resistors indicated on block diagrams command a low output. In noisy environments, it may be necessary to tie inputs of an unused channel to VDD or GND using short traces to prevent noise from causing spurious output switching.
- Many high-speed power circuits can be susceptible to noise injected from their own output or other external sources, possibly causing output re-triggering. These effects can be obvious if the circuit is tested in breadboard or non-optimal circuit layouts with long input or output leads. For best results, make connections to all pins as short and direct as possible.
- FAN3213 and FAN3214 are pin-compatible with many other industry-standard drivers.
- The turn-on and turn-off current paths should be minimized, as discussed in the following section.

Figure 29 shows the pulsed gate drive current path when the gate driver is supplying gate charge to turn the MOSFET on. The current is supplied from the local bypass capacitor, C_{BYP}, and flows through the driver to the MOSFET gate and to ground. To reach the high peak currents possible, the resistance and inductance in the path should be minimized. The localized C_{BYP} acts to contain the high peak current pulses within this driver-MOSFET circuit, preventing them from disturbing the sensitive analog circuitry in the PWM controller.

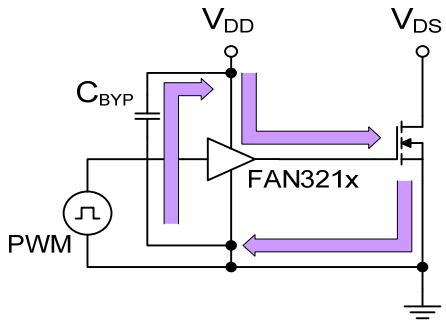


Figure 29. Current Path for MOSFET Turn-On

Figure 30 shows the current path when the gate driver turns the MOSFET OFF. Ideally, the driver shunts the current directly to the source of the MOSFET in a small circuit loop. For fast turn-off times, the resistance and inductance in this path should be minimized.

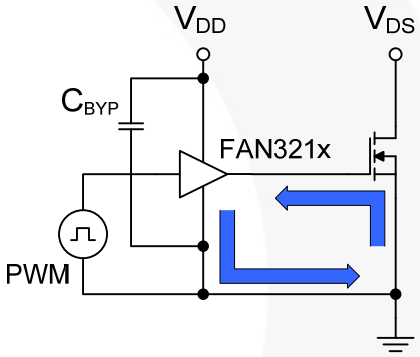


Figure 30. Current Path for MOSFET Turn-Off

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Operational Waveforms

At power-up, the driver output remains LOW until the V_{DD} voltage reaches the turn-on threshold. The magnitude of the OUT pulses rises with V_{DD} until steady-state V_{DD} is reached. The non-inverting operation illustrated in Figure 31 shows that the output remains LOW until the UVLO threshold is reached, then the output is in-phase with the input.

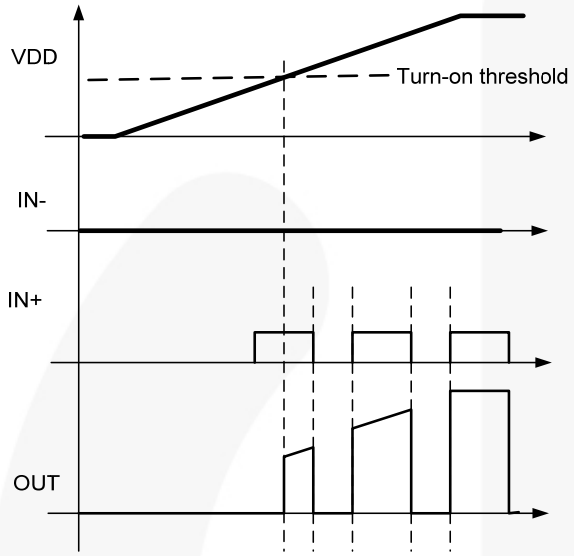


Figure 31. Non-Inverting Startup Waveforms

The inverting configuration of startup waveforms are shown in Figure 32. With IN+ tied to VDD and the input signal applied to IN–, the OUT pulses are inverted with respect to the input. At power-up, the inverted output remains LOW until the V_{DD} voltage reaches the turn-on threshold, then it follows the input with inverted phase.

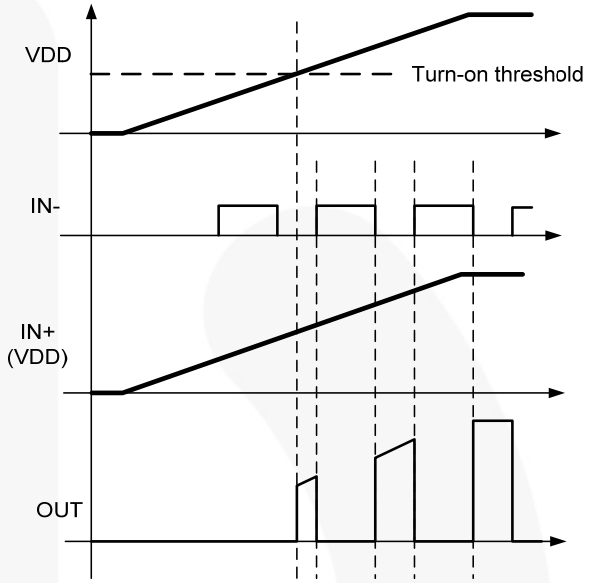


Figure 32. Inverting Startup Waveforms

Thermal Guidelines

Gate drivers used to switch MOSFETs and IGBTs at high frequencies can dissipate significant amounts of power. It is important to determine the driver power dissipation and the resulting junction temperature in the application to ensure that the part is operating within acceptable temperature limits.

The total power dissipation in a gate driver is the sum of two components, P_{GATE} and $P_{DYNAMIC}$:

$$P_{TOTAL} = P_{GATE} + P_{DYNAMIC} \quad (1)$$

Gate Driving Loss: The most significant power loss results from supplying gate current (charge per unit time) to switch the load MOSFET on and off at the switching frequency. The power dissipation that results from driving a MOSFET at a specified gate-source voltage, V_{GS}, with gate charge, Q_G, at switching frequency, f_{SW}, is determined by:

$$P_{GATE} = Q_G \bullet V_{GS} \bullet f_{SW} \bullet n \quad (2)$$

where n is the number of driver channels in use (1 or 2).

Dynamic Pre-Drive / Shoot-through Current: A power loss resulting from internal current consumption under dynamic operating conditions, including pin pull-up / pull-down resistors, can be obtained using the graphs in Typical Performance Characteristics to determine the current $I_{DYNAMIC}$ drawn from V_{DD} under actual operating conditions:

$$P_{DYNAMIC} = I_{DYNAMIC} \bullet V_{DD} \bullet n \quad (3)$$

Once the power dissipated in the driver is determined, the driver junction rise with respect to circuit board can be evaluated using the following thermal equation, assuming Ψ_{JB} was determined for a similar thermal design (heat sinking and air flow):

$$T_J = P_{TOTAL} \bullet \Psi_{JB} + T_B \quad (4)$$

where:

T_J = driver junction temperature;

Ψ_{JB} = (psi) thermal characterization parameter relating temperature rise to total power dissipation; and

T_B = board temperature in location as defined in the Thermal Characteristics table.

To give a numerical example, if the synchronous rectifier switches in the forward converter of Figure 33 are FDMS8660S, the datasheet gives a total gate charge of 60nC at V_{GS} = 7V, so two devices in parallel would have 120nC gate charge. At a switching frequency of 300kHz, the total power dissipation is:

$$P_{GATE} = 120nC \bullet 7V \bullet 300kHz \bullet 2 = 0.504W \quad (5)$$

$$P_{DYNAMIC} = 7.5mA \bullet 7V \bullet 2 = 0.011W \quad (6)$$

$$P_{TOTAL} = 0.515W \approx 0.52W \quad (7)$$

The SOIC-8 has a junction-to-board thermal characterization parameter of Ψ_{JB} = 42°C/W. In a system application, the localized temperature around the device is a function of the layout and construction of the PCB along with airflow across the surfaces. To ensure reliable operation, the maximum junction temperature of the device must be prevented from exceeding the maximum rating of 150°C; with 80% derating, T_J would be limited to 120°C. Rearranging Equation 4 determines the board temperature required to maintain the junction temperature below 120°C:

$$T_{B,MAX} = T_J - P_{TOTAL} \bullet \Psi_{JB} \quad (8)$$

$$T_{B,MAX} = 120°C – 0.52W \bullet 42°C/W = 98°C \quad (9)$$

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Typical Application Diagrams

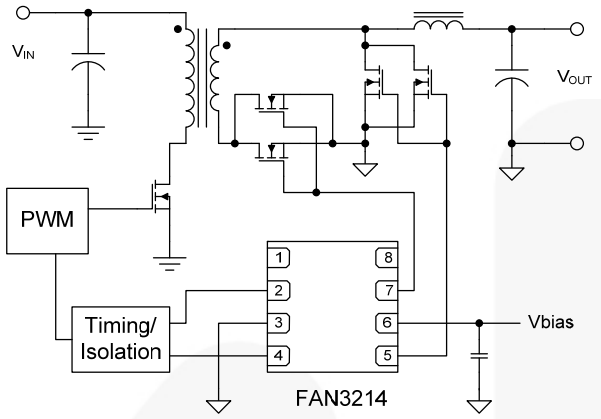


Figure 33. High-Current Forward Converter with Synchronous Rectification

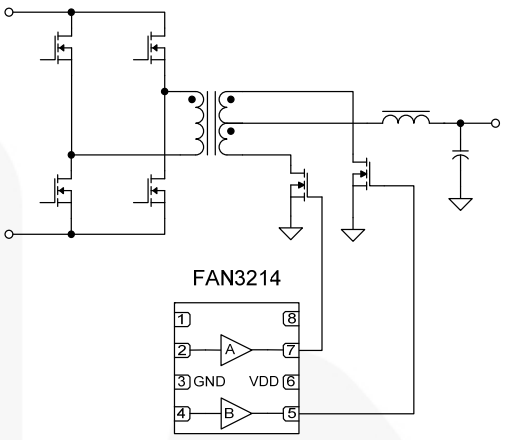


Figure 34. Center-Tapped Bridge Output with Synchronous Rectifiers

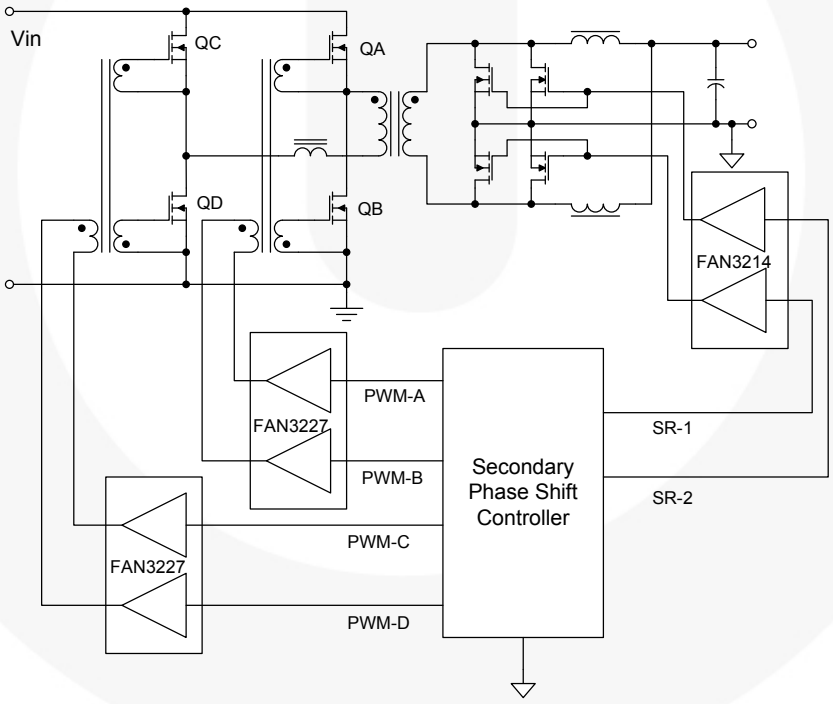


Figure 35. Secondary Controlled Full Bridge with Current Doubler Output, Synchronous Rectifiers (Simplified)

Table 1. Related Products

Type	Part Number	Gate Drive[12] (Sink/Src)	Input Threshold	Logic	Package
Single 1A	FAN3111C	+1.1A / -0.9A	CMOS	Single Channel of Dual-Input/Single-Output	SOT23-5, MLP6
Single 1A	FAN3111E	+1.1A / -0.9A	External[13]	Single Non-Inverting Channel with External Reference	SOT23-5, MLP6
Single 2A	FAN3100C	+2.5A / -1.8A	CMOS	Single Channel of Two-Input/One-Output	SOT23-5, MLP6
Single 2A	FAN3100T	+2.5A / -1.8A	TTL	Single Channel of Two-Input/One-Output	SOT23-5, MLP6
Dual 2A	FAN3216T	+2.5A / -1.8A	TTL	Dual Inverting Channels	SOIC8
Dual 2A	FAN3217T	+2.5A / -1.8A	TTL	Dual Non-Inverting Channels	SOIC8
Dual 2A	FAN3226C	+2.4A / -1.6A	CMOS	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
Dual 2A	FAN3226T	+2.4A / -1.6A	TTL	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
Dual 2A	FAN3227C	+2.4A / -1.6A	CMOS	Dual Non-Inverting Channels + Dual Enable	SOIC8, MLP8
Dual 2A	FAN3227T	+2.4A / -1.6A	TTL	Dual Non-Inverting Channels + Dual Enable	SOIC8, MLP8
Dual 2A	FAN3228C	+2.4A / -1.6A	CMOS	Dual Channels of Two-Input/One-Output, Pin Config.1	SOIC8, MLP8
Dual 2A	FAN3228T	+2.4A / -1.6A	TTL	Dual Channels of Two-Input/One-Output, Pin Config.1	SOIC8, MLP8
Dual 2A	FAN3229C	+2.4A / -1.6A	CMOS	Dual Channels of Two-Input/One-Output, Pin Config.2	SOIC8, MLP8
Dual 2A	FAN3229T	+2.4A / -1.6A	TTL	Dual Channels of Two-Input/One-Output, Pin Config.2	SOIC8, MLP8
Dual 2A	FAN3268T	+2.4A / -1.6A	TTL	20V Non-Inverting Channel (NMOS) and Inverting Channel (PMOS) + Dual Enables	SOIC8
Dual 2A	FAN3278T	+2.4A / -1.6A	TTL	30V Non-Inverting Channel (NMOS) and Inverting Channel (PMOS) + Dual Enables	SOIC8
Dual 4A	FAN3213T	+2.5A / -1.8A	TTL	Dual Inverting Channels	SOIC8
Dual 4A	FAN3214T	+2.5A / -1.8A	TTL	Dual Non-Inverting Channels	SOIC8
Dual 4A	FAN3223C	+4.3A / -2.8A	CMOS	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
Dual 4A	FAN3223T	+4.3A / -2.8A	TTL	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
Dual 4A	FAN3224C	+4.3A / -2.8A	CMOS	Dual Non-Inverting Channels + Dual Enable	SOIC8, MLP8
Dual 4A	FAN3224T	+4.3A / -2.8A	TTL	Dual Non-Inverting Channels + Dual Enable	SOIC8, MLP8
Dual 4A	FAN3225C	+4.3A / -2.8A	CMOS	Dual Channels of Two-Input/One-Output	SOIC8, MLP8
Dual 4A	FAN3225T	+4.3A / -2.8A	TTL	Dual Channels of Two-Input/One-Output	SOIC8, MLP8
Single 9A	FAN3121C	+9.7A / -7.1A	CMOS	Single Inverting Channel + Enable	SOIC8, MLP8
Single 9A	FAN3121T	+9.7A / -7.1A	TTL	Single Inverting Channel + Enable	SOIC8, MLP8
Single 9A	FAN3122T	+9.7A / -7.1A	CMOS	Single Non-Inverting Channel + Enable	SOIC8, MLP8
Single 9A	FAN3122C	+9.7A / -7.1A	TTL	Single Non-Inverting Channel + Enable	SOIC8, MLP8

Notes:

12. Typical currents with OUTx at 6V and V_{DD}=12V.
13. Thresholds proportional to an externally supplied reference voltage.

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Physical Dimensions

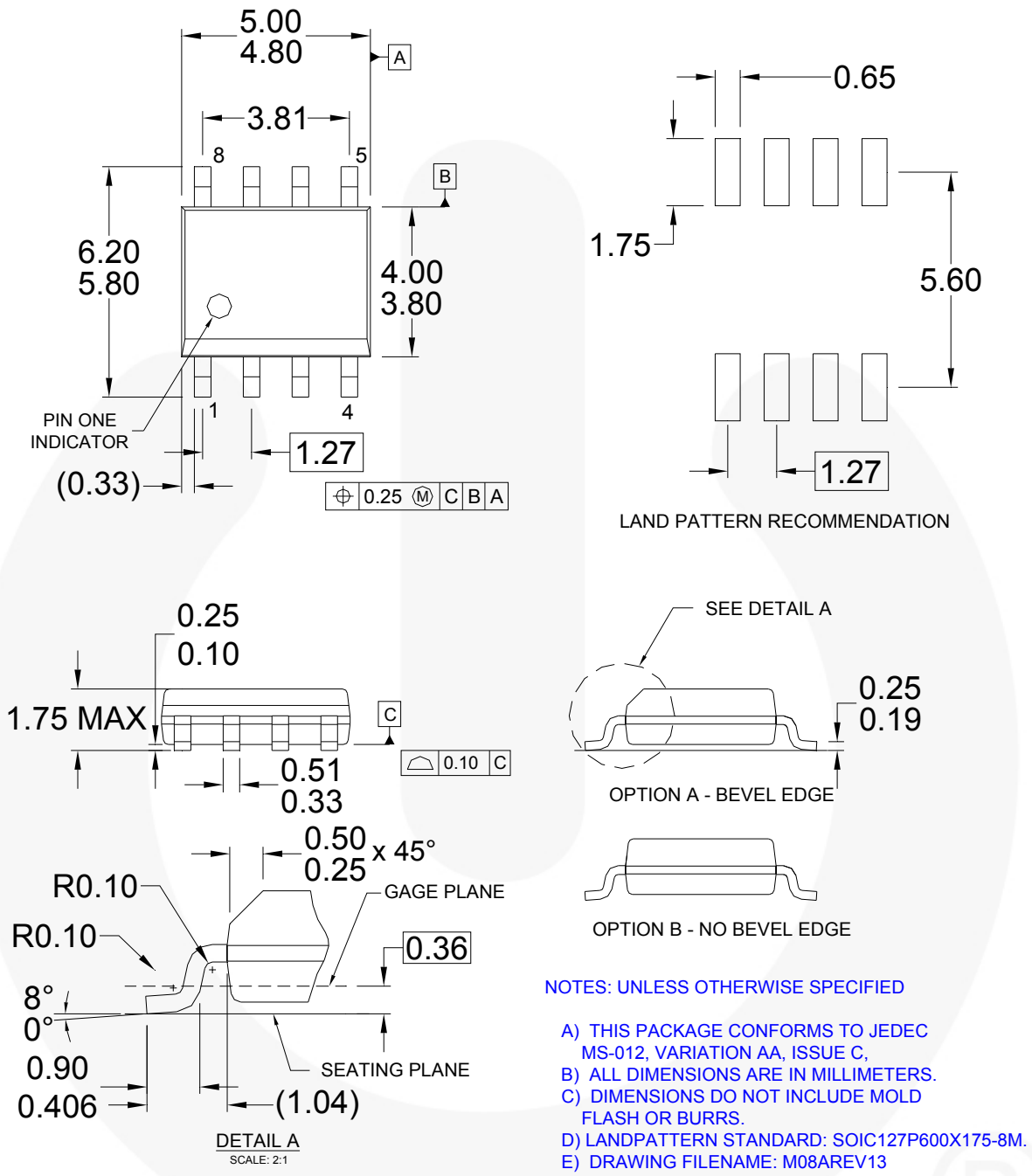


Figure 36. 8-Lead Small Outline Integrated Circuit (SOIC)

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