PROGRAMMABLE PORT CONTROLLER (PORT EXPANDER WITH BUILT-IN E^2PROM CIRCUIT)

S-7750C

The S-7750C is a programmable port controller IC comprised of an E^2PROM, a control circuit for data output, a circuit to prevent malfunction caused by low power supply voltage and others.
This IC operates at 400 kHz and interfaces with exteriors via I^2C-bus. Using a serial signal, users can control both of the 8ch digital output "H" or "L" and delay time which can be set at each channel.
For the digital output pins at the 8 channels, the default value and inverted delay time are settable at each port. This IC is effective to control ON / OFF the chips surrounding MPU. And this IC maintains the default value for control despite power-off due to the included E^2PROM.

■ Features

- Operating voltage range: 2.3 to 4.5 V
- 8ch digital output
- Operating frequency of I^2C-bus interface: 400 kHz
- Function to prevent malfunction during low power supply voltage operation
- Low current consumption at standby: 3.0 μA Max. (V_{CCH} = 4.5 V)
- Built-in E^2PROM circuit
- E^2PROM endurance: 10^5 cycles / word*1 (at –40 to +85 °C)
- E^2PROM data retention: 10 years (after rewriting 10^5 cycles / word)
- Function to protect Write in E^2PROM
- Lead-free product
- Small package: WLP-16A

***1.** For each address (Word: 8-bit)

■ Application

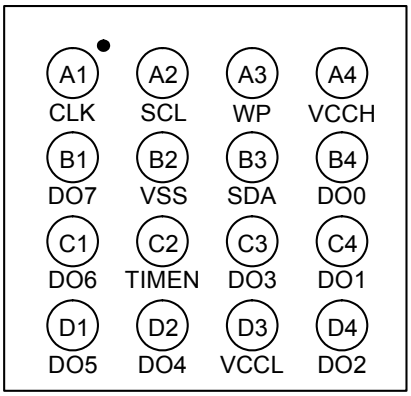
- Mobile phone
- Portable communication device
- Digital still camera
- Digital video camera

■ Package

Package Name	Drawing Code		
	Package	Tape	Reel
WLP-16A	HA016-A	HA016-A	HA016-A

■ Pin Configuration

WLP-16
Bottom View



(1.93×2.07×0.6 max.)

Figure 1

■ List of Pin

Table 1 WLP-16A List of Pin

Pin No.	Pin name	Description
A1	CLK	Input for external clock
A2	SCL	Input for serial clock
A3	WP	Input for Write protect
A4	VCCH	Power supply
B1	DO7	Output port 7
B2	VSS	GND
B3	SDA	Serial data I/O
B4	DO0	Digital output port 0
C1	DO6	Digital output port 6
C2	TIMEN	Input for timer enable
C3	DO3	Digital output port 3
C4	DO1	Digital output port 1
D1	DO5	Digital output port 5
D2	DO4	Digital output port 4
D3	VCCL	Power supply for output port
D4	DO2	Digital output port 2

■ Block Diagram

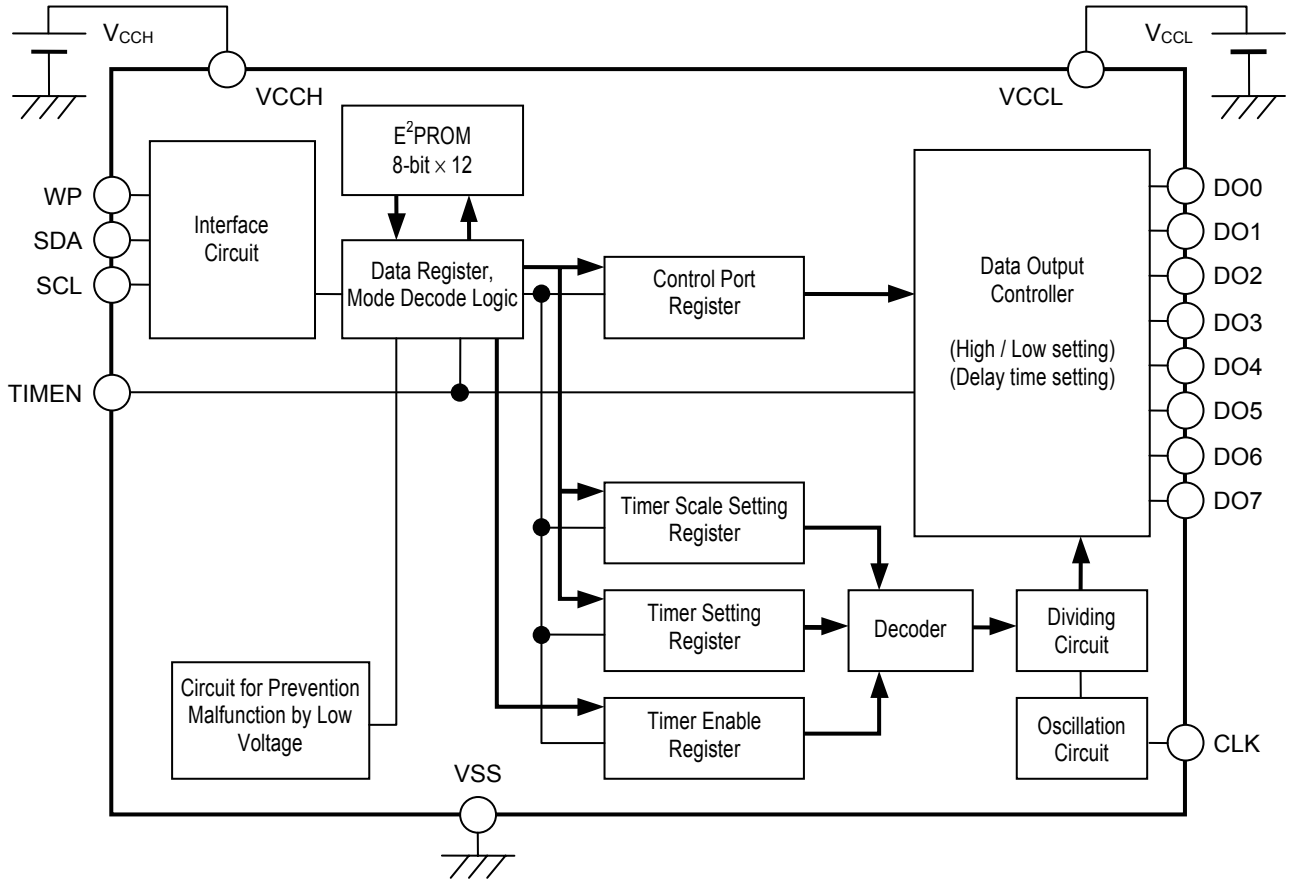


Figure 2

■ General Description of Pin Function

1. SDA (Serial data I/O) pin

The SDA pin transmits serial data bi-directionally, is comprised of a signal input pin and a pin with Nch transistor open drain output. In use, generally, connect the SDA line to any other device which has the open-drain or open-collector output with Wired-OR connection by pulling up to V_{CCH} by a resistor.

2. SCL (Input for serial clock) pin

The SCL pin is an input pin for serial clock, processes a signal at a rising / falling edge of SCL clock. Pay attention fully to the rising / falling time and comply with specifications.

3. WP (Input for Write protect) pin

This pin performs Write Protect to E^2PROM (This pin does not have a function for Write protect to the register).
Set the WP pin in V_{CCH} when using the Write Protect function. If not, set the WP pin to GND.

4. TIMEN (Input for timer enable) pin

This pin controls enable (“H”) /disable (“L”) / start (“L”→”H”) in the timer action (inversion of digital output due to elapsed period). Regarding the timer action, refer to “■ **Command**” and “■ **Condition to start timer, Port Output and Register**”. When raising VCCH and TIMEN simultaneously, set $V_{CCH} \geq 2.5$ V.

5. CLK (Input for external clock) pin

As primary clock in the circuit action, users are able to use clock either from the internal oscillation circuit or input it externally by option. Users can input clock from this pin in case of using external clock. If not, connect this pin to VCCH or GND.

6. DO7 to DO0 (Digital output) pin

These pins are for the digital output port. Their values are equal to the ones of a control port register during output. Its output inverts after; the timer starts and delay time has elapsed. Regarding the timer action, refer to “■ **Command**” and “■ **Condition to start timer, Port Output and Register**”.

7. VSS pin

Connect to GND.

8. VCCH pin

Except for the output ports, the power supply is applied to the entire circuit via this pin. Regarding the voltage’s value to be applied to this pin, refer to “■ **Recommended Operating Conditions**”.

9. VCCL pin

This pin is to apply the power supply for the output ports. Regarding the voltage’s value to be applied to this pin, refer to “■ **Recommended Operating Conditions**”.

■ Equivalent Circuit of I/O Pin

This IC's I/O pin does not have an element of pull-up or pull-down. The SDA line has an open drain output. The followings are equivalent circuits.

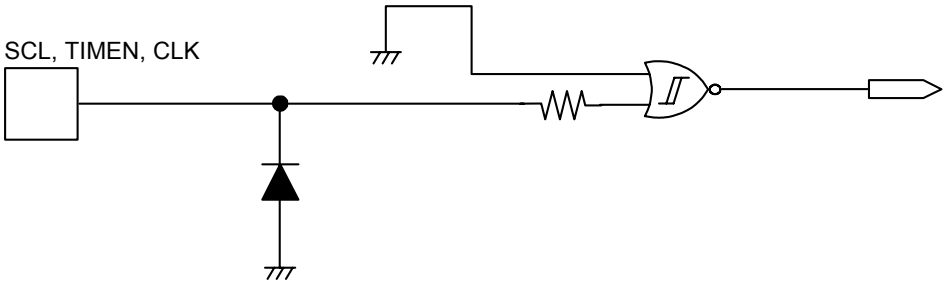


Figure 3 SCL, TIMEN, CLK Pin

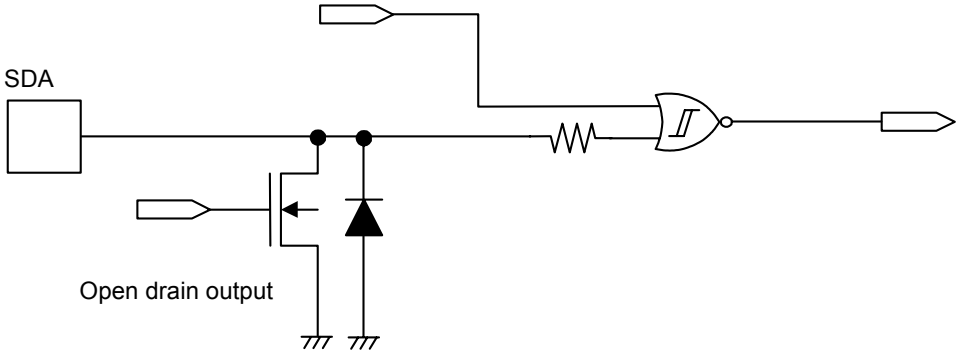


Figure 4 SDA Pin

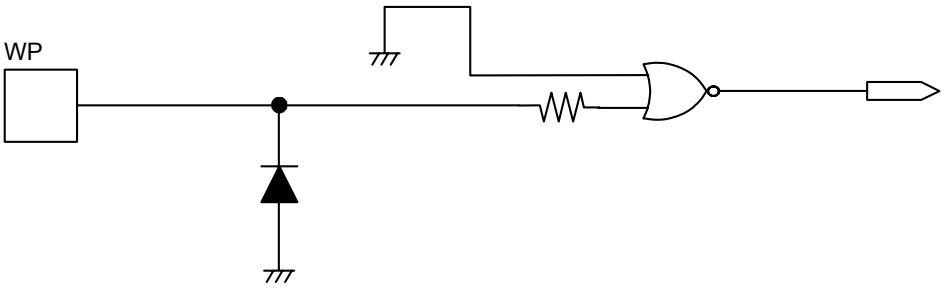


Figure 5 WP Pin

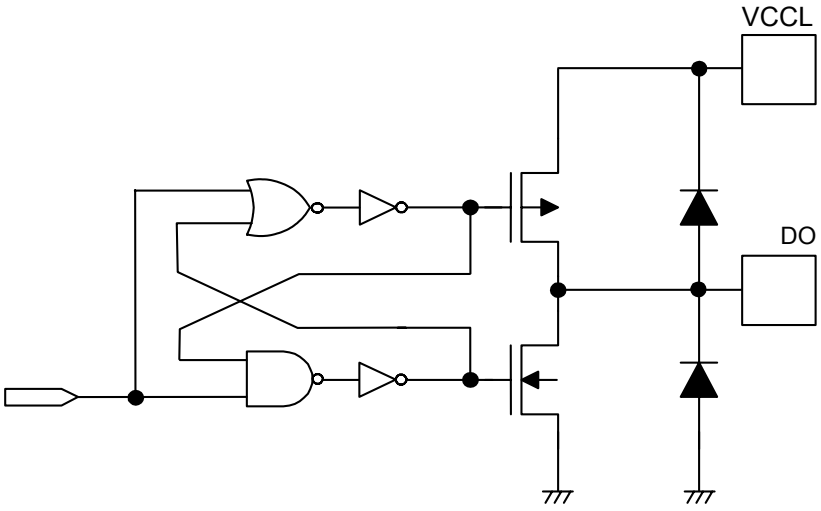


Figure 6 DO Pin and VCCL Pin

■ Absolute Maximum Ratings

Table 2

Item	Symbol	Rating	Unit
Power supply voltage1	V_{CCH}	−0.3 to +7.0	V
Power supply voltage2	V_{CCL}	−0.3 to V_{CCH}	V
Input voltage	V_{IN}	−0.3 to V_{CCH} + 0.3	V
Output voltage (SDA)	V_{OUT1}	−0.3 to V_{CCH}	V
Output voltage (DO)	V_{OUT2}	−0.3 to V_{CCL}	V
Operating ambient temperature	T_{opr}	−40 to +85	°C
Storage temperature	T_{stg}	−65 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Operating Conditions

Table 3

Item	Symbol	Option	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CCH}	Read, Write	2.3*1	–	4.5	V
Output power supply voltage	V_{CCL}	–	1.5	–	V_{CCH}*2	V
High-level input voltage	V_{IH}	V_{CCH} = 2.3 to 4.5 V	0.7 × V_{CCH}	–	V_{CCH}	V
Low-level input voltage	V_{IL}	V_{CCH} = 2.3 to 4.5 V	0.0	–	0.3 × V_{CCH}	V

***1.** Set $V_{CCH} \geq 2.5$ V when raising VCCH and TIMEN simultaneously.
***2.** Set the voltage of VCCL as $V_{CCH} \geq V_{CCL}$.

■ Pin Capacitance

Table 4

(Ta = 25°C, f = 1.0 MHz, V_{CCH} = 3 V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	SCL, WP, TIMEN, CLK	V_{IN} = 0 V	–	–	10	pF
Input / output capacitance	$C_{I/O}$	SDA, DO	$V_{I/O}$ = 0 V	–	–	10	pF

■ Endurance

Table 5

Item	Symbol	Operating Temperature	Min.	Typ.	Max.	Unit
Endurance	N_W	−40 to +85°C	10^5	–	–	cycles / word*1

***1.** For each address (Word: 8-bit)

■ DC Electrical Characteristics

Table 6 DC Characteristcs 1

Item	Symbol	Condition*1	V_{CCH} = V_{CCL} = 2.3 to 4.5 V			Unit
			Min.	Typ.	Max.	
Current consumption during standby	I_{SB}	f_{SCL} = 0 Hz, TIMEN Pin = "L"	–	–	3.0	μA
Current consumption (READ)	I_{CC1}	f_{SCL} = 400 kHz, TIMEN Pin = "L"	–	–	0.8	mA
Current consumption (WRITE)	I_{CC2}	f_{SCL} = 400 kHz, TIMEN Pin = "L"	–	–	4.0	mA
Current consumption during operation of internal oscillation circuit	I_{CC3}	–	–	–	0.8	mA

***1.** The total current consumption when V_{CCH} = V_{CCL}. No load on pins DO7 to DO0.

Table 7 DC Characteristcs 2

Item	Symbol	Condition	V_{CCH} = 2.3 to 4.5 V			Unit
			Min.	Typ.	Max.	
Input current	I_{LI}	V_{IN} = GND to V_{CCH}	–	0.1	1.0	μA
Output leakage current (SDA)	I_{LO}	V_{OUT} = GND to V_{CCH}	–	0.1	1.0	μA
Low-level output voltage (SDA)	V_{OL1}	I_{OL} = 3.2 mA	–	–	0.4	V
		I_{OL} = 1.5 mA	–	–	0.3	V
Low-level output voltage (DO)	V_{OL2}	I_{OL} = 100 μA V_{CCL} = V_{CCH} to 1.5 V	–	–	0.1	V
High-level output voltage (DO)	V_{OH2}	V_{CCL} = V_{CCH} to 2.0 V I_{OH} = −100 μA	V_{CCL}−0.3	–	–	V
		V_{CCL} = V_{CCH} to 1.5 V I_{OH} = −10 μA	V_{CCL}−0.3	–	–	V

■ AC Electrical Characteristics

Table 8 Measurement Conditions

Input pulse voltage	V_{IL} = 0.1×V_{CCH}, V_{IH} = 0.9×V_{CCH}
Rising / falling time of input pulse	20 ns
Output reference voltage	0.5×V_{CCH}
Output load	100 pF+ Pull-up resistor 1.0 kΩ

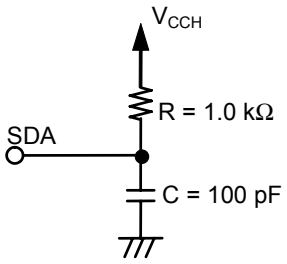


Figure 7 Output Load Circuit

Table 9 AC Electrical Characteristics

Item	Symbol	V_{CCH} = 2.3 to 4.5 V			Unit
		Min.	Typ.	Max.	
SCL clock frequency *1	f_{SCL}	0	–	400	kHz
SCL clock time "L" *1	t_{LOW}	1.0	–	–	µs
SCL clock time "H" *1	t_{HIGH}	0.9	–	–	µs
SDA output delay time *1	t_{AA}	–	–	0.9	µs
SDA output hold time *1	t_{DH}	50	–	–	ns
Start condition setup time *1	$t_{SU.STA}$	0.6	–	–	µs
Start condition hold time *1	$t_{HD.STA}$	0.6	–	–	µs
Data input setup time *1	$t_{SU.DAT}$	100	–	–	ns
Data input hold time *1	$t_{HD.DAT}$	0	–	–	ns
Stop condition setup time *1	$t_{SU.STO}$	0.6	–	–	µs
SCL, SDA rise time *1	t_R	–	–	0.3	µs
SCL, SDA fall time *1	t_F	–	–	0.3	µs
Bus release time *1	t_{BUF}	1.3	–	–	µs
Noise suppression time	t_I	–	–	50	ns
Frequency for external oscillation input *2	f_{TEX}	–	–	400	kHz

***1.** The timing is defined by 10% and 90% of the waveform.
***2.** When selecting the option for external oscillation input.

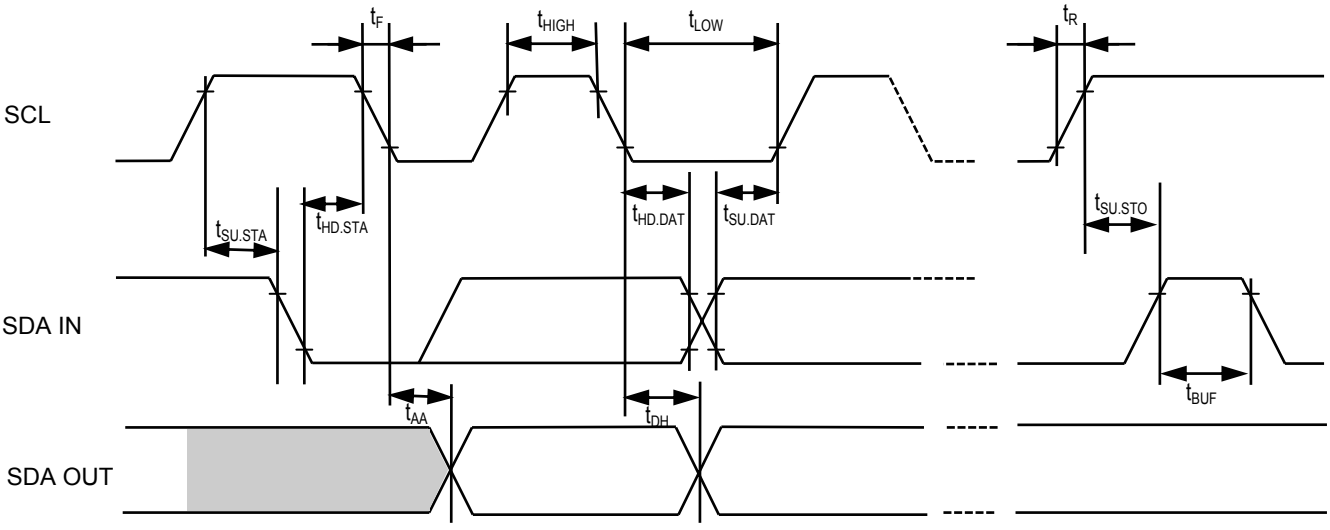


Figure 8 Bus Timing

Table 10 Characteristics of Period

Item	Symbol	Min.	Typ.	Max.	Unit
Write period to E²PROM	t_{WR}	–	2.0	5.0	ms
Delay time accuracy (short-time setting)*1	t_{DLY1}	0.8×T	T	1.2×T	µs
Delay time accuracy (long-time setting)*1	t_{DLY2}	0.8×LT	LT	1.2×LT	µs
Timeout*1	t_{OUT}	–	9×LT	–	µs

***1.** Refer to "**Figure 16 Timer Setting Register DO7 to DO0 / E²PROM**" "**Figure 17 Example of Using Timer Setting for DO7 to DO0 Register**".
T represents time reference (timer scale) in the short-time setting.
LT represents time reference (timer scale) in the long-time setting.

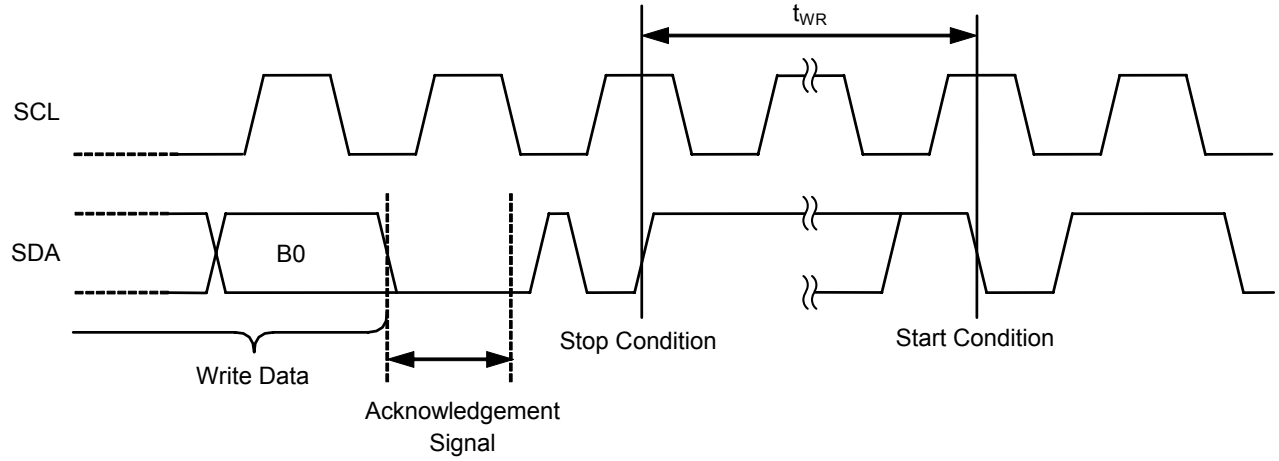


Figure 9 Write Cycle Timing

■ Device Addressing

To start communication, the master device (MPU) on the system generates a start condition for the slave device (S-7750C). After that, the master device sends a device address with 7-bit and Read / Write instruction code with 1-bit on the SDA bus. The higher 3 bits in a device address (DC2, DC1, DC0) are device codes. The fixed value which users selected by option (either one of 000, 001, 010, 011, 100, 101, 110, 111) is a device code. Command is omitted if a device code does not correspond. The next 1-bit TA / $\overline{C}$ is a bit for timer address setting / command switch. When TA / $\overline{C}$ = "1", the next 3 bits (C2, C1, C0) are used as address, when TA / $\overline{C}$ = "0", (C2, C1, C0) are used as command for the timer setting register.

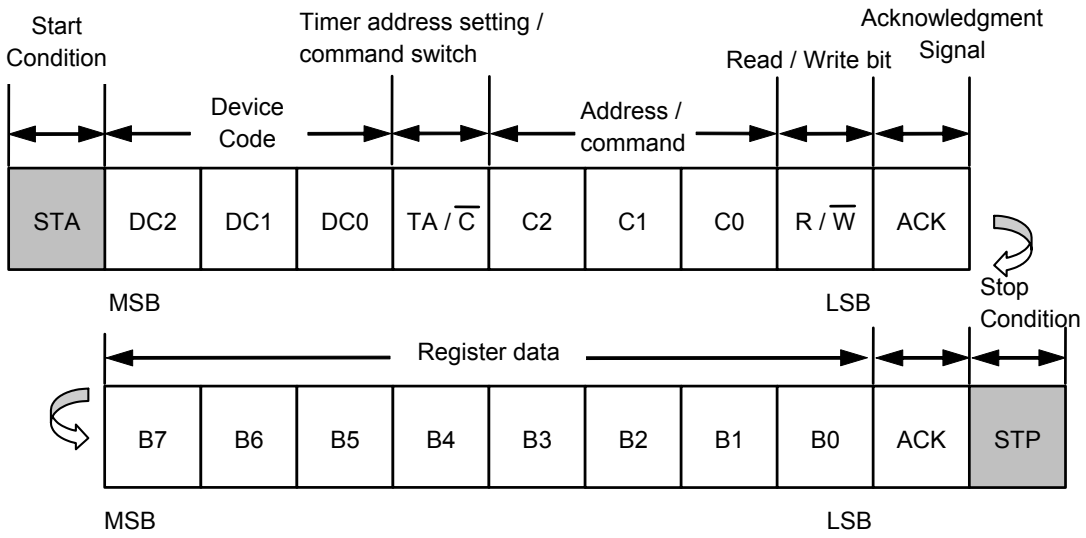


Figure 10 Device Addressing

■ Configuration of Command

If setting TA / $\overline{C}$, the bit for timer address setting / command switch, in "0", address / command (C2, C1, C0) is recognized as command. There are 8 types of command, and Read / Write in each register is done by them. If setting the bit for timer address setting / command switch (TA / $\overline{C}$) in "1", the S-7750C recognizes this command as timer setting for DO0 to DO7.

Table 11 List of Command

Command	TA / $\overline{C}$	C2	C1	C0	R / $\overline{W}$	Data							
						B7	B6	B5	B4	B3	B2	B1	B0
Reload (R / $\overline{W}$ fixed to 0)	0	0	0	0	$\overline{W}$	— *1							
Switching access to register / E²PROM	0	0	0	1	0 / 1 *2	— *1							
Timer enable register	0	0	1	0	$\overline{W}$	TEN7	TEN6	TEN5	TEN4	TEN3	TEN2	TEN1	TEN0
Do not use (Do not access)	0	0	1	1	—	—							
Free area 1 *3	0	1	0	0	R / $\overline{W}$	F17	F16	F15	F14	F13	F12	F11	F10
Control port *3	0	1	0	1	R / $\overline{W}$	CTR7	CTR6	CTR5	CTR4	CTR3	CTR2	CTR1	CTR0
Timer scale setting *3	0	1	1	0	R / $\overline{W}$	TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0
Free area 2 *3	0	1	1	1	R / $\overline{W}$	F27	F26	F25	F24	F23	F22	F21	F20
Timer setting for DO0 *3	1	0	0	0	R / $\overline{W}$	8×T	7×T	6×T	5×T	4×T	3×T	2×T	1×T
Timer setting for DO1 *3	1	0	0	1	R / $\overline{W}$	8×T	7×T	6×T	5×T	4×T	3×T	2×T	1×T
Timer setting for DO2 *3	1	0	1	0	R / $\overline{W}$	8×T	7×T	6×T	5×T	4×T	3×T	2×T	1×T
Timer setting for DO3 *3	1	0	1	1	R / $\overline{W}$	8×T	7×T	6×T	5×T	4×T	3×T	2×T	1×T
Timer setting for DO4 *3	1	1	0	0	R / $\overline{W}$	8×T	7×T	6×T	5×T	4×T	3×T	2×T	1×T
Timer setting for DO5 *3	1	1	0	1	R / $\overline{W}$	8×T	7×T	6×T	5×T	4×T	3×T	2×T	1×T
Timer setting for DO6 *3	1	1	1	0	R / $\overline{W}$	8×T	7×T	6×T	5×T	4×T	3×T	2×T	1×T
Timer setting for DO7 *3	1	1	1	1	R / $\overline{W}$	8×T	7×T	6×T	5×T	4×T	3×T	2×T	1×T

***1.** By inputting dummy data, the master device sends data in 18-bit during transmission. However, the S-7750C executes the command when it has loaded 9-bit. Regarding acknowledgment, refer to "■ **Operation 4. Acknowledgment**".

***2.** R / $\overline{W}$ = "0"; register access mode, R / $\overline{W}$ = "1"; E²PROM access mode

***3.** To switch access to register / E²PROM, use the "Switching access to register / E²PROM" command. When rewriting the E²PROM, the register is rewritten simultaneously.

■ Register and E²PROM

In the S-7750C, the register and the E²PROM correspond each other. The S-7750C maintains the default value for control despite power-off due to the included E²PROM. The data in the register is installed in the E²PROM by using the reload command. And the data in the E²PROM is automatically installed into the register when power-on and the lower power supply voltage is applied. Restoring the default value for control is possible any time due to these functions.

These 12 commands have the configuration in which the register and E²PROM correspond.

- Free area 1, 2
- Control port
- Setting for timer scale
- Timer setting for DO7 to DO0

Users are able to switch access between corresponding register and E²PROM by the "Switching access to register / E²PROM" command. Immediately after power-on, the S-7750C is in the "register access mode". In this register access mode, only the register is rewritten, the E²PROM maintains the prior data. But in the "E²PROM access mode", data both in the register and the E²PROM is rewritten. In data Read, access mode data which is being selected by user; is read.

■ Command

1. Reload

This is a 1-byte command. Set bit R / $\overline{W}$ in "0". When inputting this command, all registers to be reloaded are once set in "0", the data which correspond to the E²PROM is loaded to the register. However, the data in the E²PROM does not change. The output ports (DO7 to DO0) output "L" once regardless of the data in the control-port register / E²PROM. If the TIMEN pin is in "H", the timer starts its action. Besides, port output (DO7 to DO0) is inverted after the time has elapsed; the time set both by a timer scale setting register and a timer setting register. This is "a timer action". This is active from the start to timeout. Regarding the action, refer to "**■ Condition to start timer, Port Output and Register**".

2. Switching access to register / E²PROM

This is a 1-byte command. The mode is in the "register access mode" when R / $\overline{W}$ = "0", "E²PROM access mode" when R / $\overline{W}$ = "1". Immediately after power-on, the S-7750C is in the "register access mode". In this register access mode, only the register is rewritten, the E²PROM maintains the prior data. But in the "E²PROM access mode", both data in the register and in the E²PROM is rewritten. In data Read, access mode data which is being selected by user; is read.

3. Timer enable register

A timer enable register is an 8-bit register for Write only (it sends back "FFh" during Read). When the TIMEN pin is in "H", Write "1" in each bit in the register starts the timer action. The timer action starts at the moment that S-7750C has received all data of the timer enable command. After writing "1" in the timer enable register, the bit automatically goes back in "0". If setting this register in "00h" and the timer setting register in "00h", a timer does not work. During the timer action it is impossible to do Write in the timer enable register. A timer enable register is not the one to be reloaded, because it does not have the corresponding E²PROM.

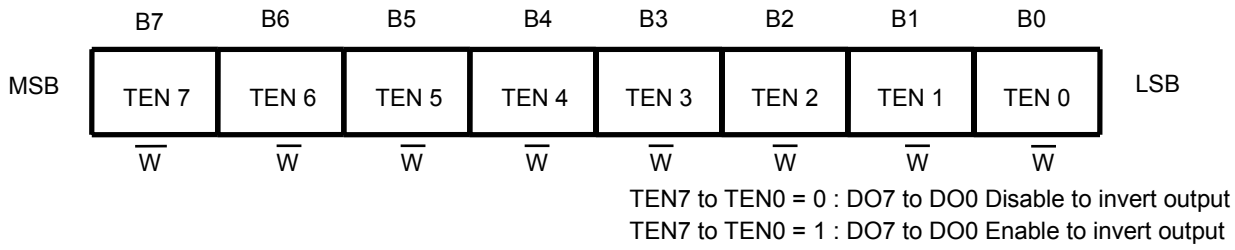
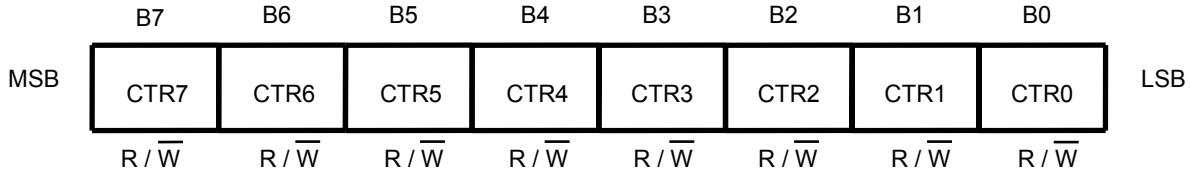


Figure 11 Timer Enable Register

4. Control port

A control port register is an 8-bit register. Users can set output at each output port (DO7 to DO0). The data in this register is “1”, output from port is “H”. If “0”, output from port is “L”. This register is the one to be reloaded by command.

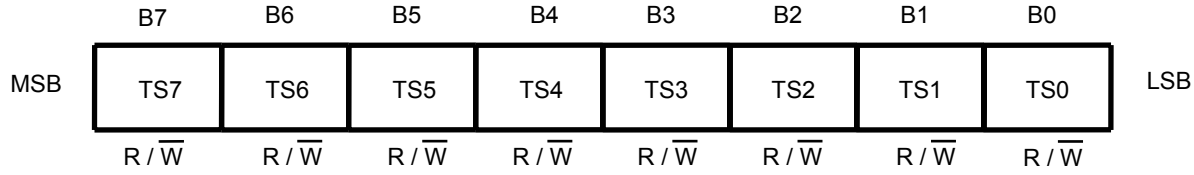


CTR7 to CTR0 = 0 : output from DO7 to DO0 = “L”
CTR7 to CTR0 = 1 : output from DO7 to DO0 = “H”

Figure 12 Control Port Register / E²PROM

5. Timer scale setting

A timer scale setting register is an 8-bit register. Output at each port (DO7 to DO0) is inverted in delay time; using this register, users can set time reference of delay time (scale) either in a short-time or a long-time setting.
Setting “0” in the data in this register, sets time reference (scale) as a long period setting, if “1”, sets time reference (scale) as a short-time setting. This register is the one to be reloaded by command.



TS7 to TS0 = 0 : Timer scale DO7 to DO0 Long-time setting
TS7 to TS0 = 1 : Timer scale DO7 to DO0 Short-time setting

Figure 13 Timer Scale Setting Register / E²PROM

6. Free area 1, Free area 2

Both of free area 1 and 2 are 8-bit registers. Users are able to use these registers freely, and these registers do not affect on other functions of the S-7750C. These free area 1 and 2 registers are the ones to be reloaded by command.

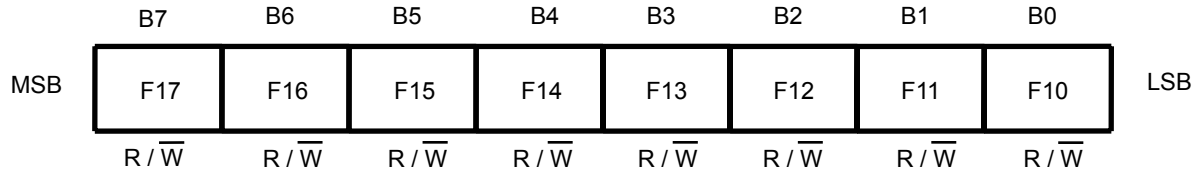


Figure 14 Free Area 1 Register / E²PROM

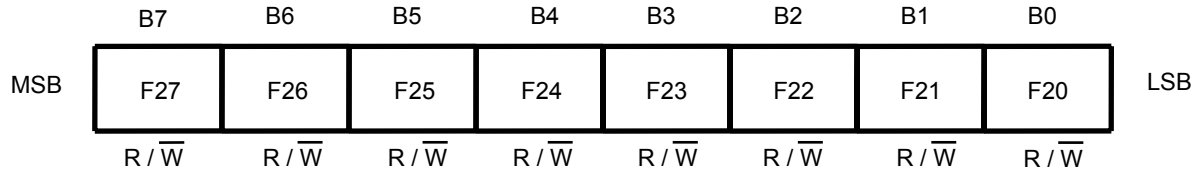


Figure 15 Free Area 2 Register / E²PROM

7. DO7 to DO0 Timer setting

A timer setting register is an 8-bit register, and for each output port (DO7 to DO0), users can set delay time which makes port output inverted after the timer action starts. Delay time at each output port (DO7 to DO0) is set as seen in **Figure 16**. Set "1" in a 1-bit only. This is the data to be set in each timer setting register.

Regarding the timer setting, the following options are selectable.

- Option to select timer clock (internal oscillation clock / external input clock)
- Option for delay time (×1 / ×2)

Time reference for timer setting register is defined by these 2 types of option and the timer scale setting register.

(1) When using an internal clock (Typ.)
Option A : (Short-time setting scale, long-time setting scale) = (T, LT) = (5 μs, 320 μs)
Option B : (Short-time setting scale, long-time setting scale) = (T, LT) = (10 μs, 640 μs)

(2) When using an external clock (Period of input clock = T')
Option A : (Short-time setting scale, long-time setting scale) = (T, LT) = (T', 64×T')
Option B : (Short-time setting scale, long-time setting scale) = (T, LT) = (2×T', 128×T')

In **Figure 16**, a timer scale setting register has a short-time setting. In the long-time setting, the port in which the timer scale setting register is set T changes into LT. For example, if setting the option to the register as seen below, in DO7, output from the port is inverted after 35 μs (7×5 μs).
Other examples are shown in **Figure 17**.

- Option to select timer clock = clock from internal oscillation circuit
- Option for delay time = ×1
- Timer scale setting register = 80 h
- DO7 timer setting register = 40 h

Setting "00h" in the register does not make port output inverted. A timer setting register is the one to be reloaded by command.

MSB	B7	B6	B5	B4	B3	B2	B1	B0	LSB
DO7	8×T	7×T	6×T	5×T	4×T	3×T	2×T	1×T	
DO6	8×T	7×T	6×T	5×T	4×T	3×T	2×T	1×T	
DO5	8×T	7×T	6×T	5×T	4×T	3×T	2×T	1×T	
DO4	8×T	7×T	6×T	5×T	4×T	3×T	2×T	1×T	
DO3	8×T	7×T	6×T	5×T	4×T	3×T	2×T	1×T	
DO2	8×T	7×T	6×T	5×T	4×T	3×T	2×T	1×T	
DO1	8×T	7×T	6×T	5×T	4×T	3×T	2×T	1×T	
DO0	8×T	7×T	6×T	5×T	4×T	3×T	2×T	1×T	
	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	

Figure 16 Timer Setting Register DO7 to DO0 / E²PROM

Example 1. When using an internal clock
Example 1-1 In case of; Timer scale register "1" (short-time setting), Delay time option "A" (×1 setting); (T = 5 μs)
Example 1-2 In case of; Timer scale register "0" (long-time setting), Delay time option "A" (×1 setting); (LT = 320 μs)

	MSB B7	B6	B5	B4	B3	B2	B1	B0 LSB
Example 1-1	40 μs	35 μs	30 μs	25 μs	20 μs	15 μs	10 μs	5 μs
Example 1-2	2.56 ms	2.24 ms	1.92 ms	1.60 ms	1.28 ms	0.96 ms	0.64 ms	0.32 ms

Example 2. When using an external clock (100 KHz, T' = 10 μs)
Example 2-1 In case of; Timer scale register "1" (short-time setting), Delay time option "B" (×2 setting); (T = 2×T' = 20 μs)
Example 2-2 In case of; Timer scale register "0" (long-time setting), Delay time option "B" (×2 setting); (LT = 128×T' = 1280 μs)

	MSB B7	B6	B5	B4	B3	B2	B1	B0 LSB
Example 2-1	160 μs	140 μs	120 μs	100 μs	80 μs	60 μs	40 μs	20 μs
Example 2-2	10.24 ms	8.96 ms	7.68 ms	6.40 ms	5.12 ms	3.84 ms	2.56 ms	1.28 ms

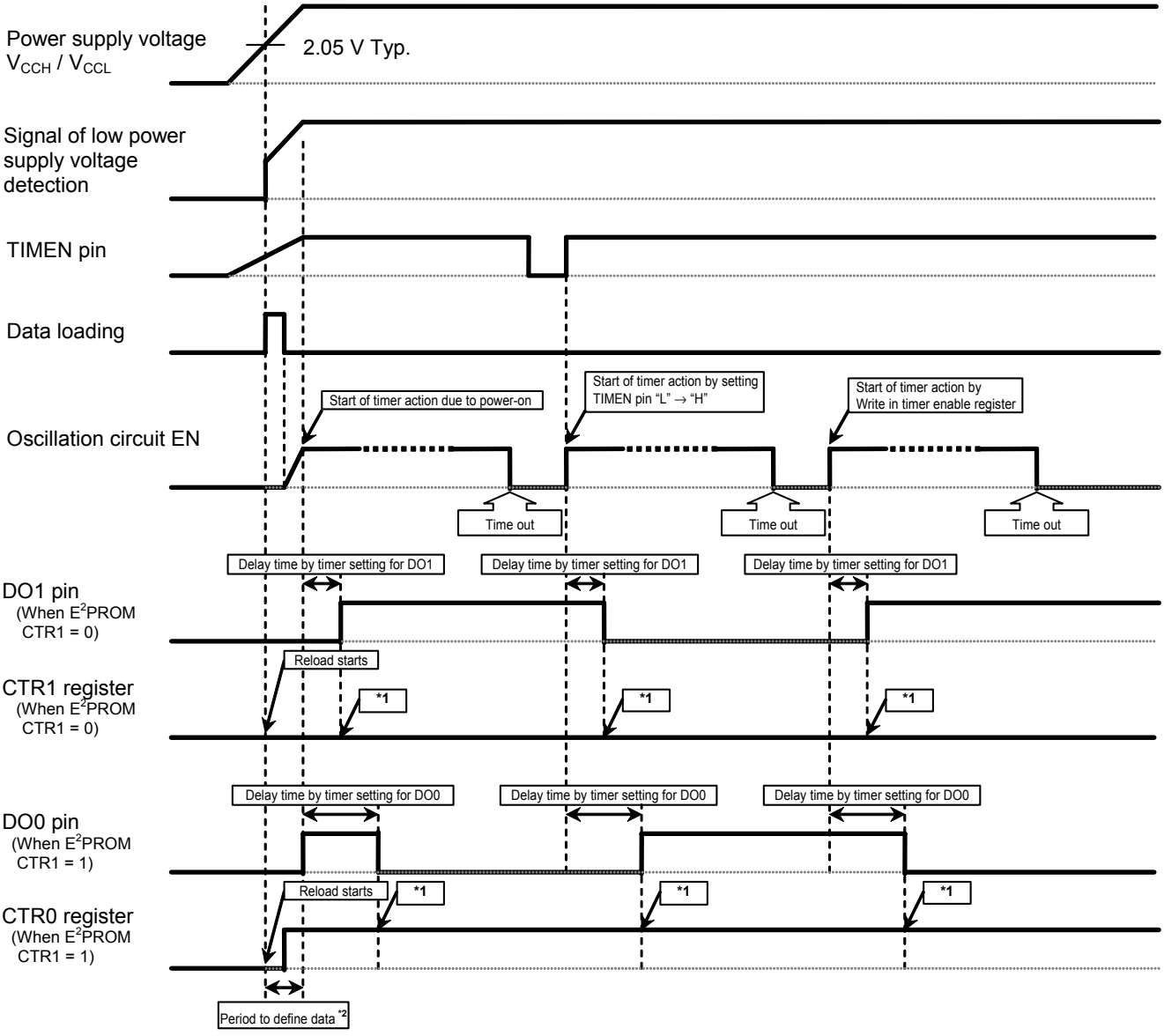
Figure 17 Example of Using Timer Setting for DO7 to DO0 Register

■ Condition to start timer, Port Output and Register

The timer action starts when either condition is satisfied. However, if “00h” is set in the timer setting register, timer action does not start.

1. When power-on (the TIMEN pin is in “H”)
2. When the TIMEN pin changes from “L” to “H”
3. While the TIMEN pin is in “H”, users do Write any commands other than “00h” in the timer enable register.
4. While the TIMEN pin is in “H”, the power supply voltage exceeds the level of release voltage of the circuit for prevention malfunction by low voltage (2.05 V typ.).
5. While the TIMEN pin is in “H”, users set the reload command.

Starting a timer action makes output from the DO7 to DO0 pins inverted after the period set by a timer has elapsed. **Figure 18** shows the timing chart of 1, 2, and 3. Set $V_{CCH} \geq 2.5V$ when raising VCCH and TIMEN simultaneously.



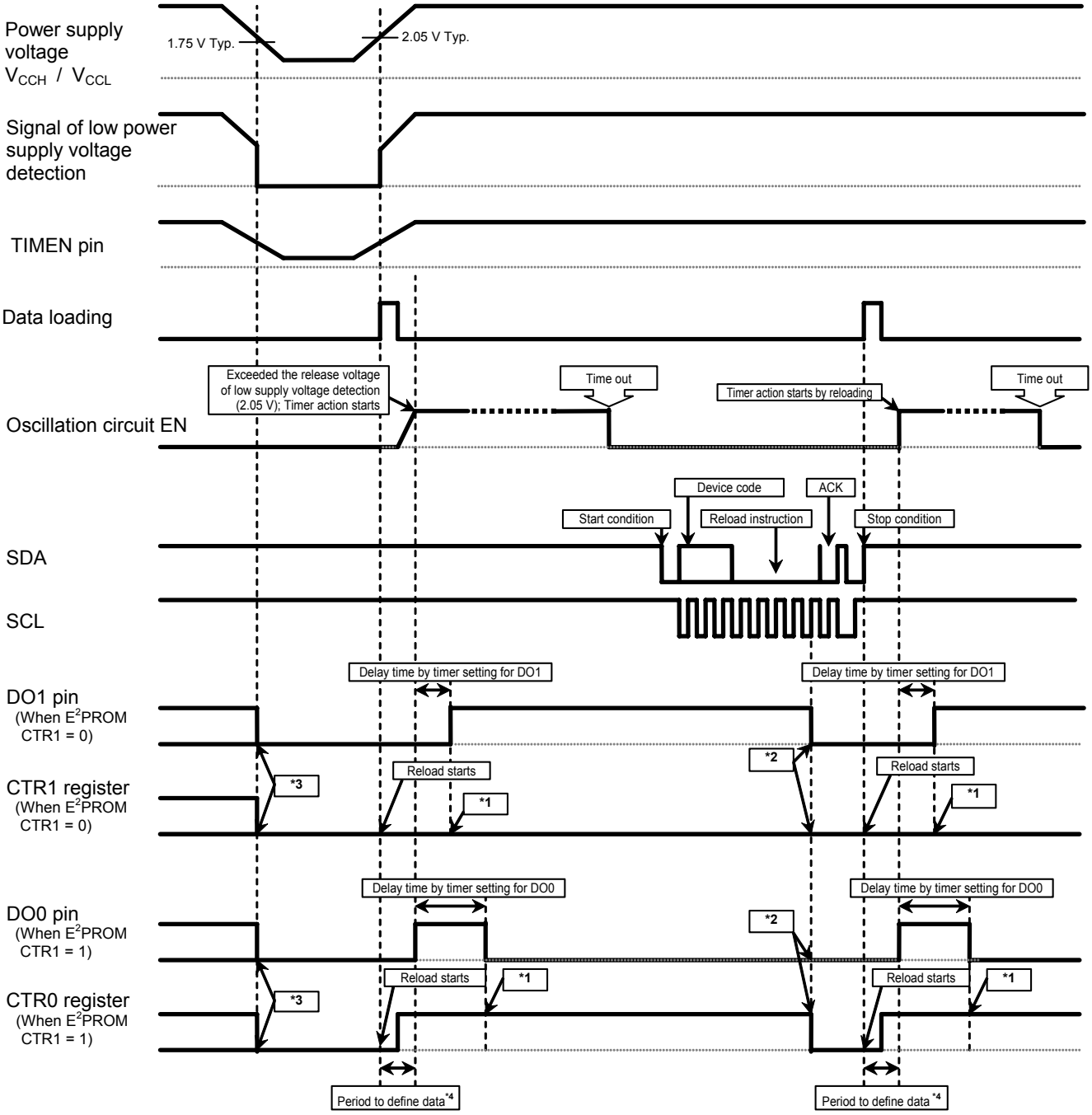
***1.** The value of control port register does not change even if the port output is inverted by timer action.
***2.** A period to define data is; the loading period from E²PROM + the period to stabilize the output from DO7 to DO0 pin = within 100 μs.

Figure 18 Example of Condition to Start Timer Action 1

Figure 19 shows the timing chart of 4 and 5.

In the S-7750C, when the power supply voltage reaches the level of detection voltage of the circuit for prevention malfunction by low voltage (1.75 V typ.), the DO7 to DO0 pins and the register go in "L". After that, the power supply voltage reaches the level of release voltage of the circuit for prevention malfunction by low voltage (2.05 V typ.), data is loaded to the register from the E^2PROM so that the timer action starts. Regarding the circuit for prevention malfunction by low voltage, refer to "■ **Action of Circuit for Prevention Malfunction by Low Voltage**".

When the S-7750C receives the reload command, the register is initialized so that the DO7 to DO0 pins once go in "L". When it receives a stop condition, data is loaded to the register from the E^2PROM so that the DO7 to DO0 pins output the default value. At this moment, the timer action starts thus output from DO7 to DO0 pins is inverted after the period set by timer.



***1.** The value of control port register does not change even if the port output is inverted by timer action.
***2.** Goes in "L" once during S-7750C recognizing the reload command to receiving a stop condition.
***3.** Goes in "L" when the power supply voltage reaches the level of the circuit for prevention malfunction by low voltage.
***4.** A period to define data is; the loading period from E^2PROM + the period to stabilize the DO7 to DO0 pin = within 100 μs.

Figure 19 Example of Condition to Start Timer Action 2

■ Flowchart of Data Loading from E^{2}PROM and Timer Action

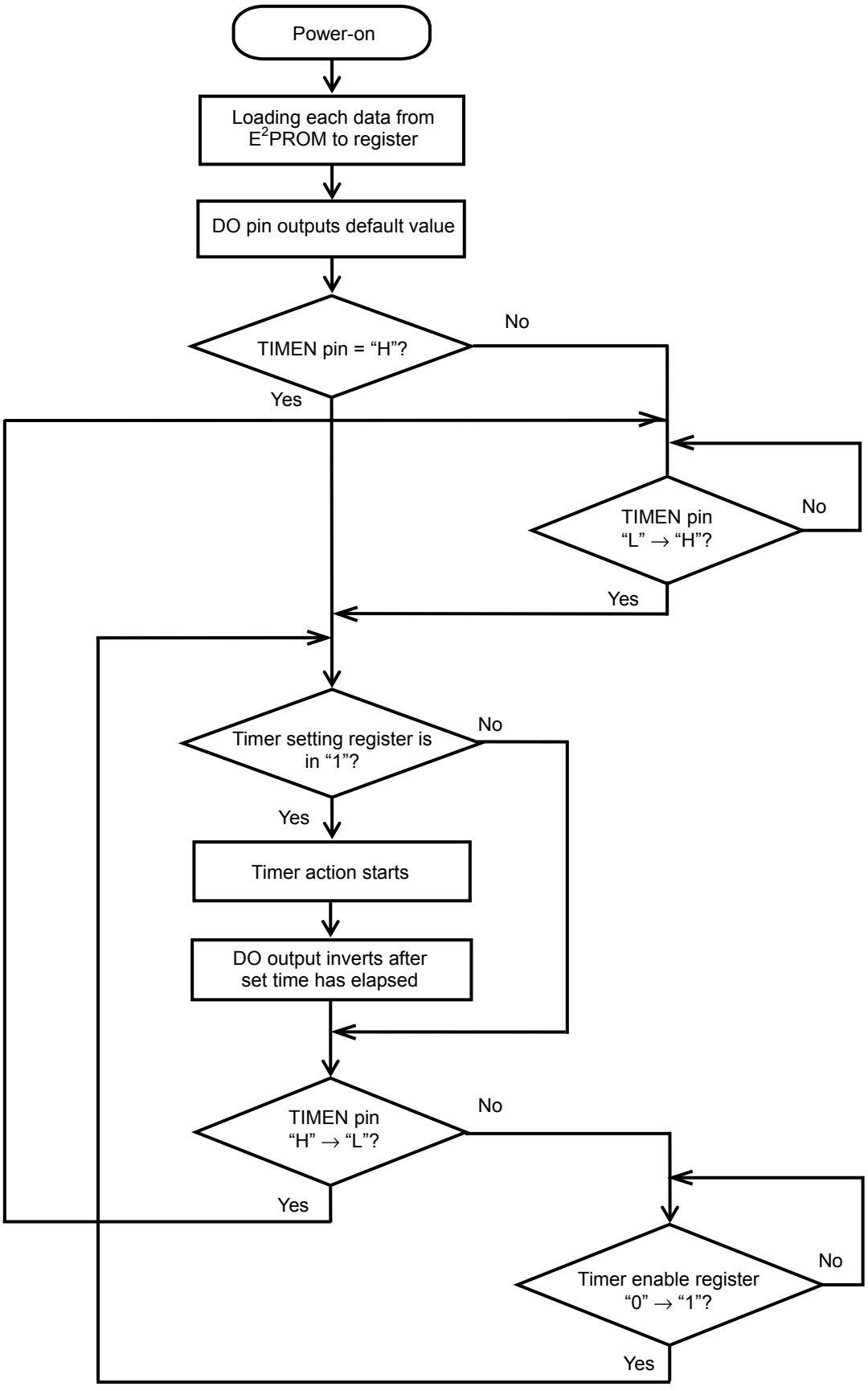


Figure 20 Flowchart of S-7750C's Action

■ Operation

1. Start condition

A start condition starts by changing the SDA line from “H” to “L” while the SCL line is “H”. Input a start condition first when inputting a command via I^{2}C-bus interface.

2. Stop condition

A stop condition starts by changing the SDA line from “L” to “H” while the SCL line is “H”. Input a stop condition in the end when inputting a command via I^{2}C-bus interface.

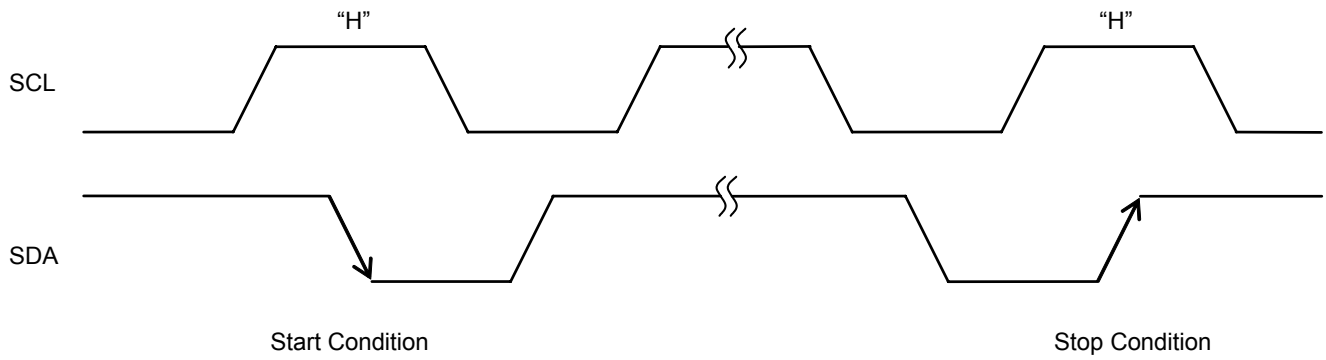


Figure 23 Start / Stop Condition

3. Data transfer

The S-7750C loads data in the SDA line at a rising edge of the SCL line.
Change the SDA line while the SCL line is “L” during the data transmission.
If changing the SDA line while the SCL line is “H”, the S-7750C goes in the start or stop condition status.

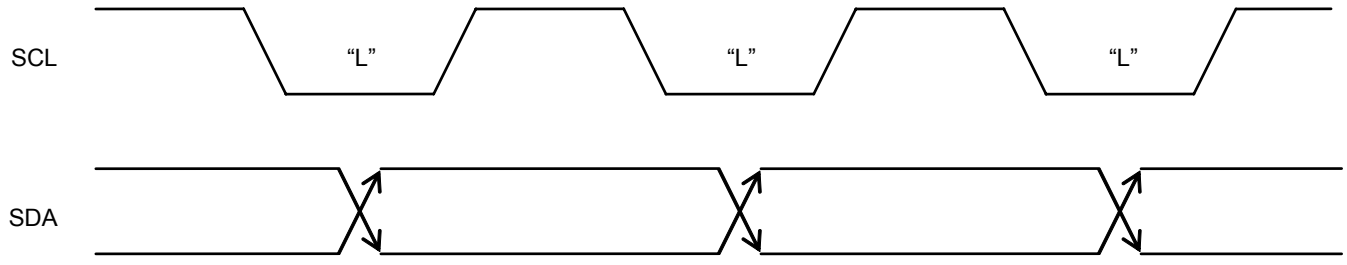


Figure 24 Data Transfer Timing

4. Acknowledgment

Data is transmitted sequentially in 8-bit. Changing the SDA line to “L” indicates that the devices on the system bus have received data, thus the devices send an acknowledgment signal back during the 9th clock of cycle.
The S-7750C does not send an acknowledgment signal back during the Write operation.

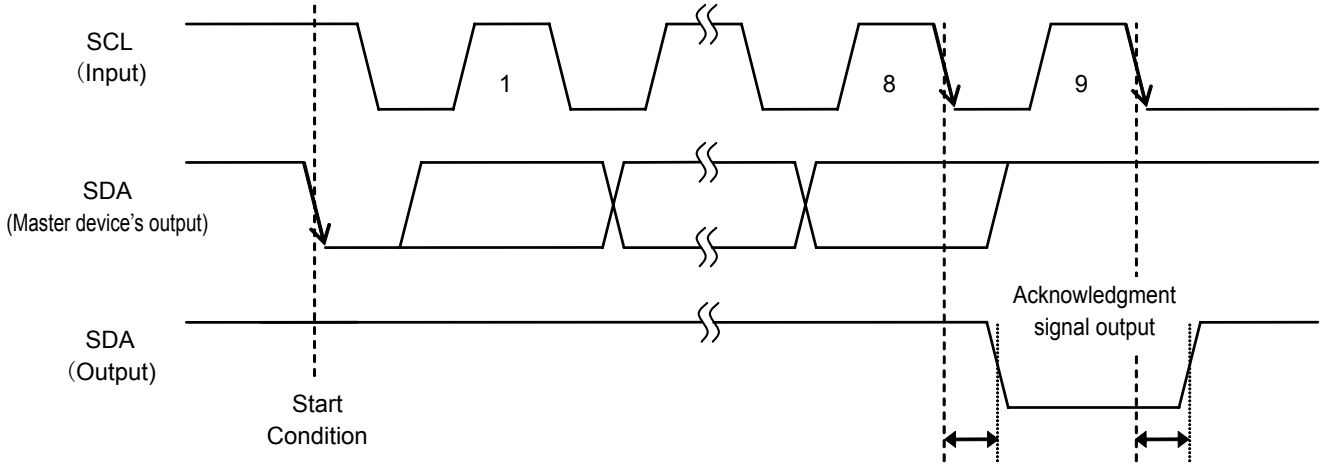


Figure 23 Acknowledgment Output Timing 1

The both commands, reload command and switching access to register / E^{2}PROM command are 1-byte, but inputting them as the command 2-byte or more is possible by adding dummy data. However, the S-7750C executes the command at the moment that it has loaded 9-bit. And in this case, inputting clock 2-byte or more after inputting these commands makes the SDA pin set in high-impedance. However, in the acknowledgment timing, S-7750C sends acknowledgment signal back regardless of the setting at R / $\overline{W}$ bit. **Figure 24** shows the output timing of acknowledgment signal.

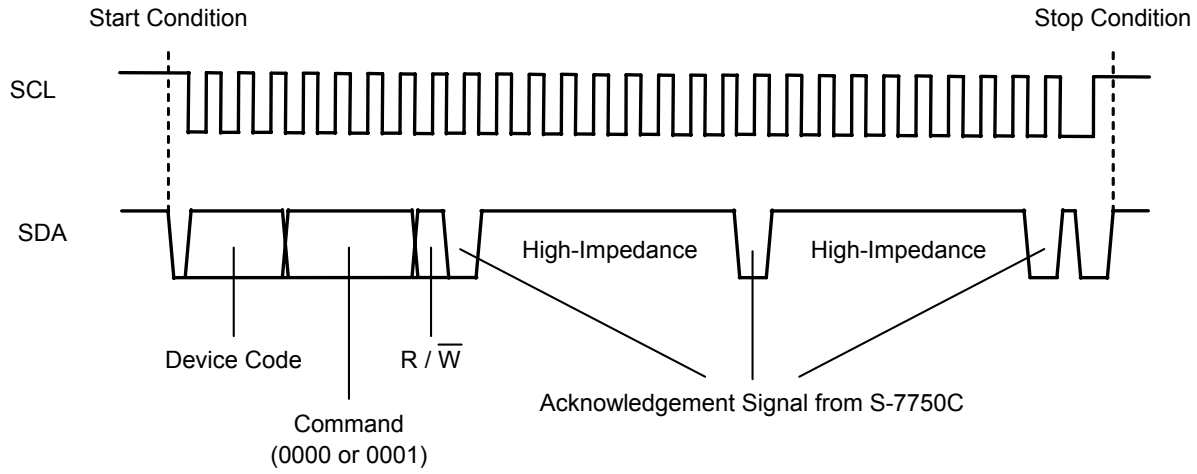


Figure 24 Acknowledgment Output Timing 2

5. Read operation

When the S-7750C receives the 7-bit device address and the Read / Write instruction code “1” after receiving a start condition, it generates an acknowledgment signal.
Next, 8-bit data is output from the S-7750C synchronizing with the SCL clock.
After that, the master device sends a stop condition, not an acknowledgment signal in order to finish the Read operation.

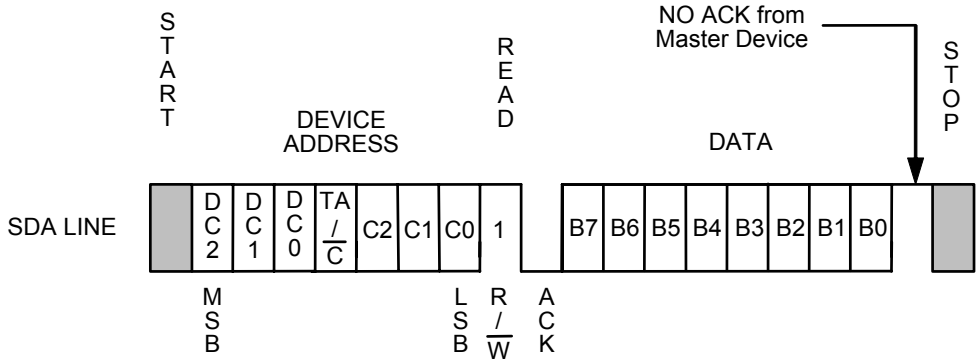
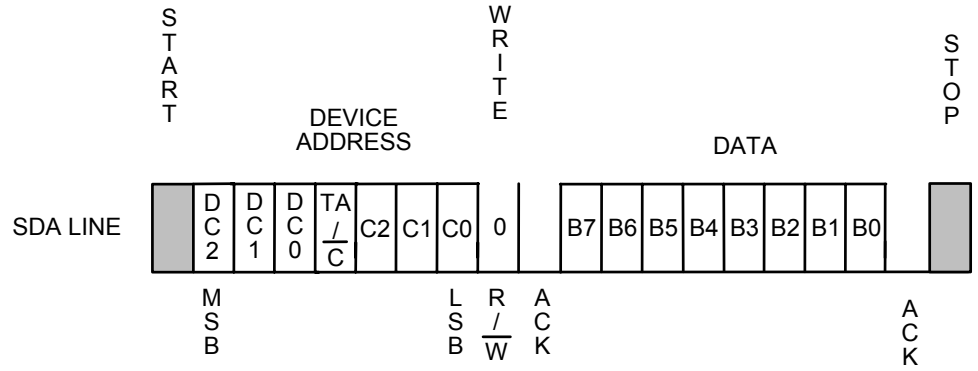


Figure 25 Read

6. Write operation

6. 1 Write

When the S-7750C receives the 7-bit device address and the Read / Write instruction code “0” after receiving a start condition, it generates an acknowledgment signal.
Next, after it receives the 8-bit word address and generates an acknowledgment signal, it receives a stop condition to finish the Write command.
In the Write operation to the E²PROM, the Write operation starts with a stop condition, the S-7750C finishes it after the period to Write (max. 5 ms) has elapsed. During Write to the E²PROM, all operations are inhibited to be performed and the S-7750C does not send back any acknowledgment signals for command inputs.



Remark Users are not necessary to input data (8-bit) and the next acknowledgment for the reload command, the switching access to register / E²PROM command. If inputting data in this timing, data is regarded as dummy, the next acknowledgement signal is generated.

Figure 26 Byte write

6. 2 Write Protect

Write protect is available in the S-7750C. When the WP pin is connected to V_{CCH}, the Write operation in all memory area is inhibited. When the WP pin is connected to GND, Write protect becomes invalid so that the Write operation in all memory area is accepted.
Fix the WP pin during the period; from rising of SCL at installing the last bit (B0) in Write data until the completion of Write period (max. 5 ms). Written data in the address is not assured if the condition of the WP pin is changed during this period. Be sure to connect the WP pin to GND when you don't use Write Protect. Write Protect is valid in the range of power supply voltage.

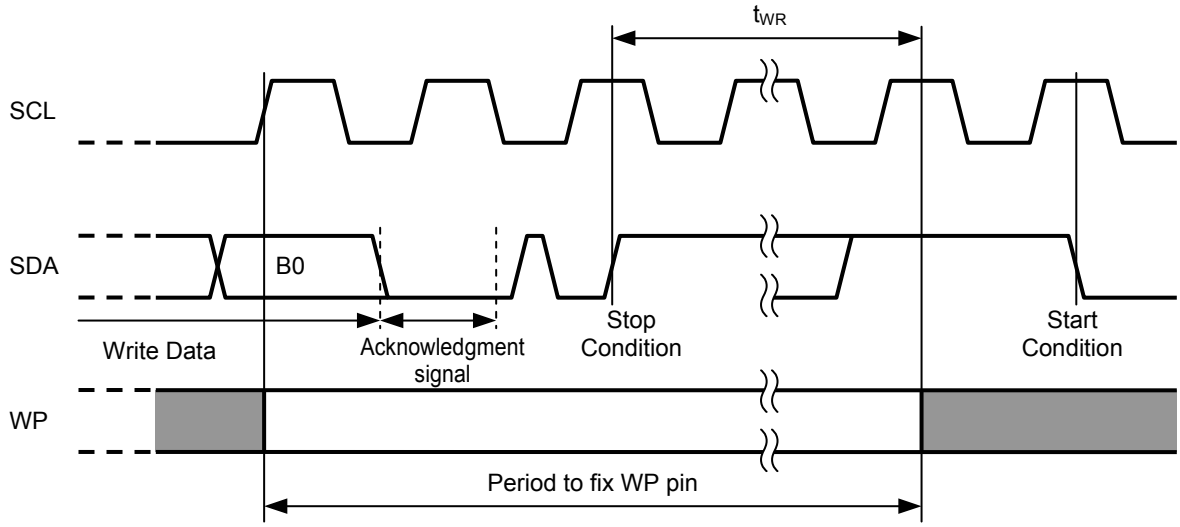


Figure 27 Period to Fix WP Pin

6. 3 Acknowledgment polling

Acknowledge polling is used to find when the Write operation has completed. After receiving a stop condition the Write operation has once started, all operations are inhibited to be performed so that the S-7750C cannot respond to the signals transmitted from the master device. The master device sends a start condition, the device address and Read / Write instruction code to the S-7750C (slave device), and detects the response from the slave device. It is possible to find when the Write operation has completed. Thus if the slave device does not send an acknowledgment signal back, the Write operation is in progress. If it sends an acknowledgment signal back, the Write operation has completed. Fix the WP pin until an acknowledgment is confirmed. It is recommended to use the Read instruction "1" for the Read / Write instruction code transmitted from the master device during acknowledgment polling.

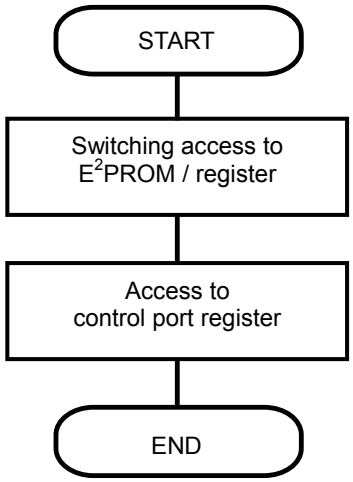
6. 4 Irregular action

In the middle of inputting Write data, if inputting a stop condition in clock less than the specified data length (8-bit), the S-7750C does not perform Write to the E²PROM. And it either does not perform Write to the E²PROM if receiving a stop condition after receiving data over 9-bit. However, data in the register has been rewritten at the point when the S-7750C has received the specified length data. Be sure not to input clock which exceeds the specified value due to noise or other causes.

■ Example of Flowchart for Software

1. Read / Write in register

The example of flowchart for software when accessing to the control port register is shown in **Figure 28**.



1-byte command

(ST, DC2 to DC0, 0001, **0**, ACK, SP)*1

2-byte command

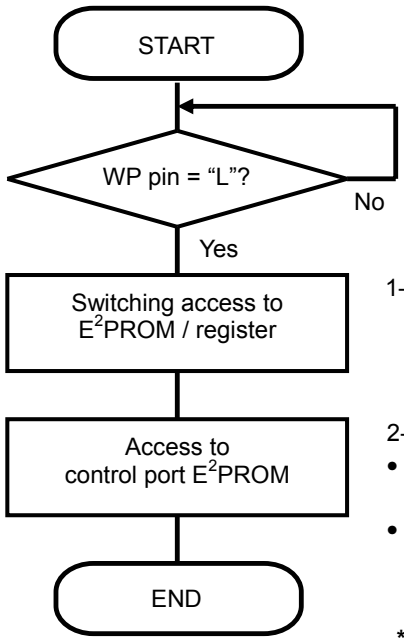
- Write
  (ST, DC2 to DC0, 0101, **0**, ACK, CTR7 to CTR0, ACK, SP)*1
- Read
  (ST, DC2 to DC0, 0101, **1**, ACK, CTR7 to CTR0, ACK, SP)*1

***1.** ST : Start condition
DC2 to DC0 : Device code
ACK : Acknowledgment
CTR7 to CTR0 : Control port register
SP : Stop condition

Figure 28 Flowchart for Software Example 1

2. Read / Write in E²PROM

The example of flowchart for software when accessing to the E²PROM is shown in **Figure 29**.



1-byte command
(ST, DC2 to DC0, 0001, **1**, ACK, SP)*1

2-byte command

- Write
  (ST, DC2 to DC0, 0101, **0**, ACK, CTR7 to CTR0, ACK, SP)*1
- Read
  (ST, DC2 to DC0, 0101, **1**, ACK, CTR7 to CTR0, ACK, SP)*1

***1.** ST : Start condition
DC2 to DC0 : Device code
ACK : Acknowledgment
CTR7 to CTR0 : Control port register
SP : Stop condition

Figure 29 Flowchart for Software Example 2

■ Action of Circuit for Prevention Malfunction by Low Voltage

The S-7750C has a detection circuit which works with the low power supply voltage, cancels Write in order to reset the internal circuit when power-on and the power supply voltage is dropping. When the power supply voltage is restored and exceeds the level of release voltage, the S-7750C automatically reloads command. The detection voltage is 1.75 V typ., the release voltage is 2.05 V typ., its hysteresis width is approx. 0.3 V. Refer to **Figure 30**.
The S-7750C cancels Write by detecting a low power supply voltage when it receives a stop condition. Both in the data transmission and the Write operation, data in the address written during the low power supply voltage is not assured.

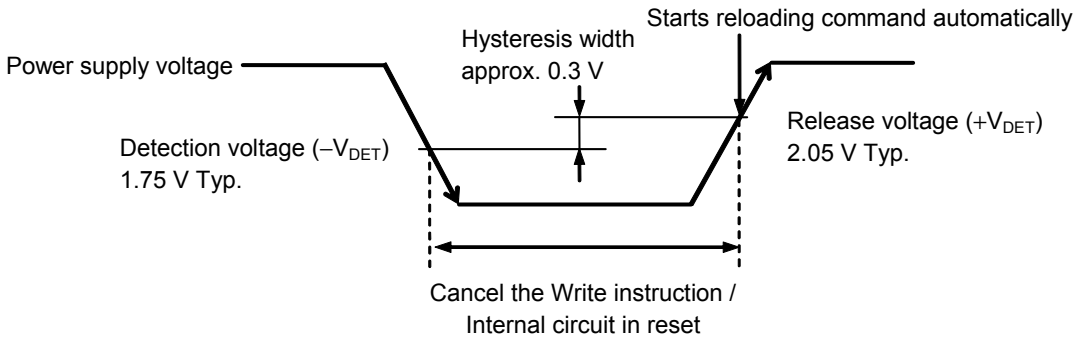


Figure 30 Action during Low Power Voltage

■ How to Use S-7750C

1. SDA I/O pin and SCL input pin

In consideration of I²C-bus protocol function, the SDA I/O and SCL input pins*1 should be connected with a pull-up resister of approx.1 to 5 kΩ.
The S-7750C cannot transmit normally without using a pull-up resistor.

***1.** In the case that the SCL input pin of the S-7750C is connected to the tri-state output pin in the master device, connect the SCL input pin with a pull-up resistor as well in order not to set the SCL input pin in high impedance. This prevents the S-7750C from error caused by high impedance from the tri-state pin when resetting the master device during the voltage drop.

2. Reset after transmission interruption

The S-7750C does not have a pin to reset, but it generally resets the internal circuit by inputting a stop or start condition. However, in case that transmission is interrupted, for example, only the master device is reset because the power supply voltage drops during transmission; the internal circuit maintains the status before interruption. If the status is that the SDA pin outputs "L" (outputs an acknowledge signal or in Read), the S-7750C does not perform the next operation because it cannot receive a start or stop condition from the master device. Therefore it is necessary to finish outputting an acknowledgment signal and the Read operation in SDA. **Figure 31** shows how to reset.
First, input a start condition. (While the SDA pin is outputting "L", the S-7750C does not go in the start condition but this "L" output does not affect on the slave device.) Next, input clock (27 clocks) which is equivalent to 3-byte data access from the SCL pin. During this procedure, pull up the SDA line which is connected closer to the master device.
Due to this, the SDA pin's I/O prior to transmission interruption ends so that the SDA pin goes in "H". After that, by inputting a stop condition, the S-7750C returns to the status possible to perform the general transmission. It is recommended to perform this reset when you initialize, after power-on the master device. A circuit for prevention malfunction by a low power supply voltage is equipped in the S-7750C, thus it automatically resets internally when a low voltage is applied to the S-7750C.

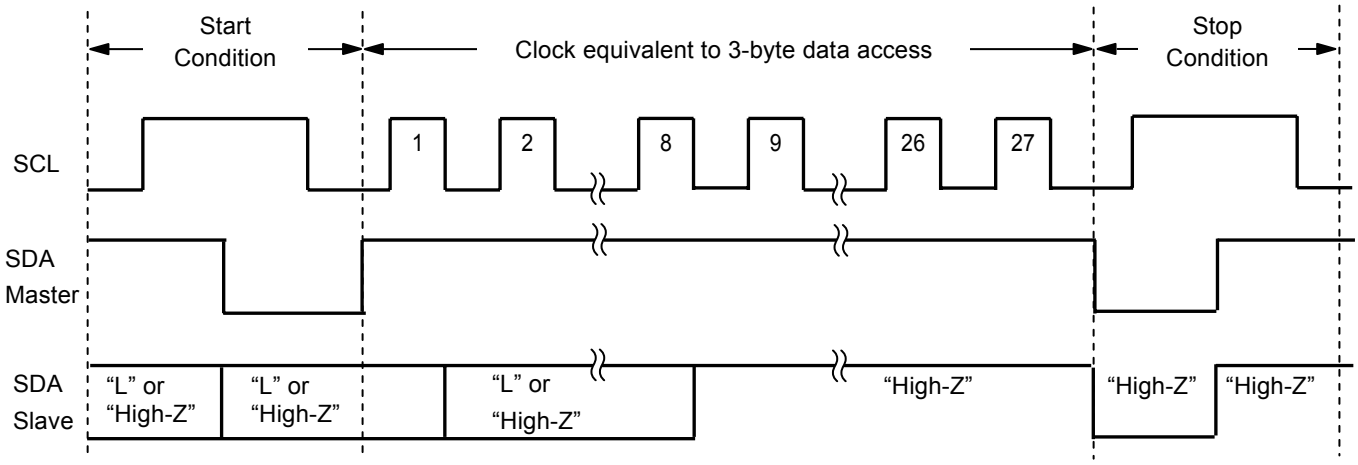


Figure 31 How to Reset S-7750C

3. Acknowledgment check

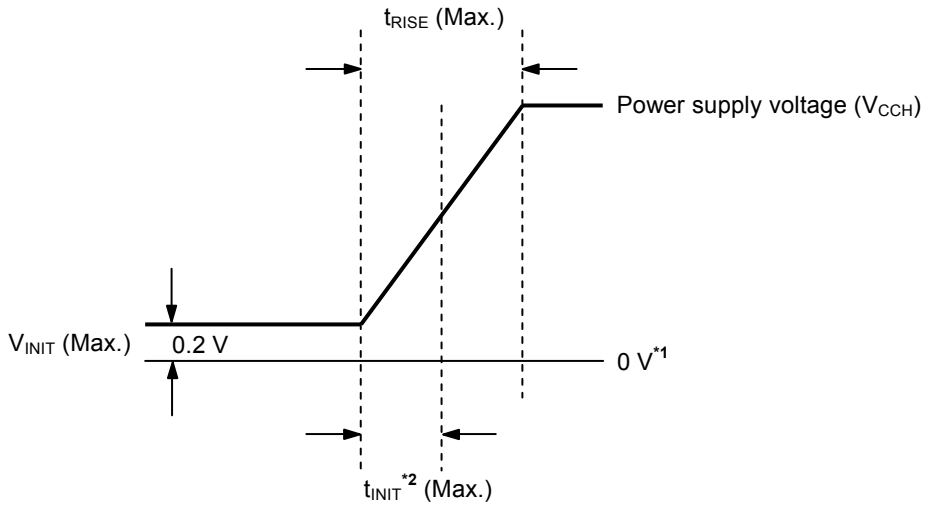
The I^2C-bus protocol includes an acknowledgment check function as a handshake function to prevent a communication error. This function allows detection of a communication failure during data communication between the master device and the S-7750C.

4. Power-on-clear circuit

The S-7750C has a power-on-clear circuit that initializes itself at the same time during power-on. Unsuccessful initialization may cause a malfunction. To operate the power-on-clear circuit normally, the following conditions must be satisfied to raise the power supply voltage.

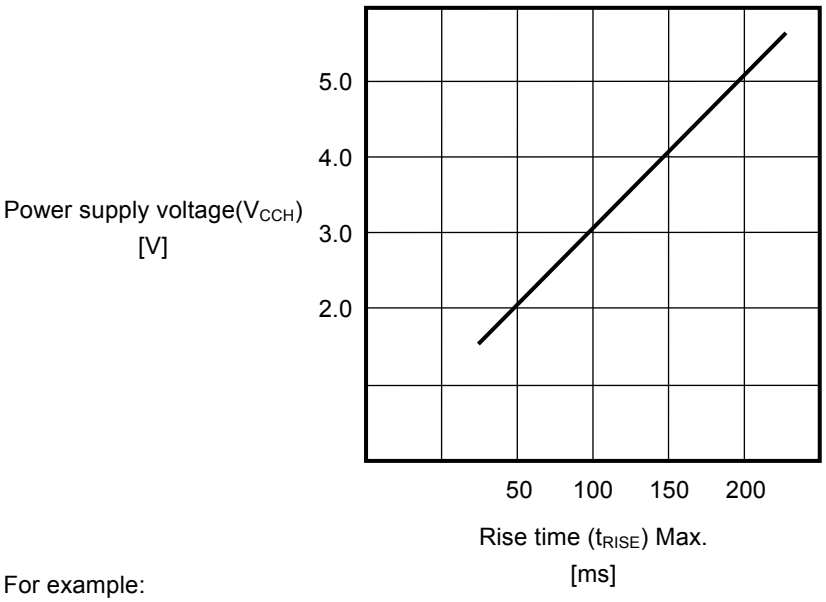
4. 1 Raising power supply voltage

As shown in **Figure 32**, raise the power supply voltage from 0.2 V max., within the time defined as t_{RISE} which is the time required to reach the power supply voltage to be set.
For example, if the power supply voltage is 3.0 V, t_{RISE} = 100 ms as seen in **Figure 33**. The power supply voltage must be raised within 100 ms.



***1.** 0 V means there is no difference in potential between the VCCH pin and the VSS pin of the S-7750C.
***2.** t_{INIT} is the time required to initialize the S-7750C. No instructions are accepted during this time.

Figure 32 Raising Power Supply Voltage



For example:

If your S-7750C's supply voltage = 3.0 V, raise the power supply voltage to 3.0 V within 100 ms.

Figure 33 Raising Time of Power Supply Voltage

When initialization is successfully completed by the power-on-clear circuit, the S-7750C enters the standby status. If the power-on-clear circuit does not operate, the followings are the possible causes.

(1) Because the S-7750C has not completed initialization, an instruction previously input is still valid or an instruction may be inappropriately recognized. In this case, S-7750C may perform the Write operation.

(2) The voltage drops due to power off while the S-7750C is being accessed. Even if the master device is reset due to the low power voltage, the S-7750C may malfunction unless the conditions for the power-on-clear operation are satisfied. Regarding the conditions for the power-on clear operation, refer to "**4.1 Raising power supply voltage**".

4. 2 Initialization time

The S-7750C initializes at the same time when the power supply voltage is raised. Input instructions to the S-7750C after initialization. The S-7750C does not accept any instruction during initialization.
Figure 34 shows the initialization time of the S-7750C.

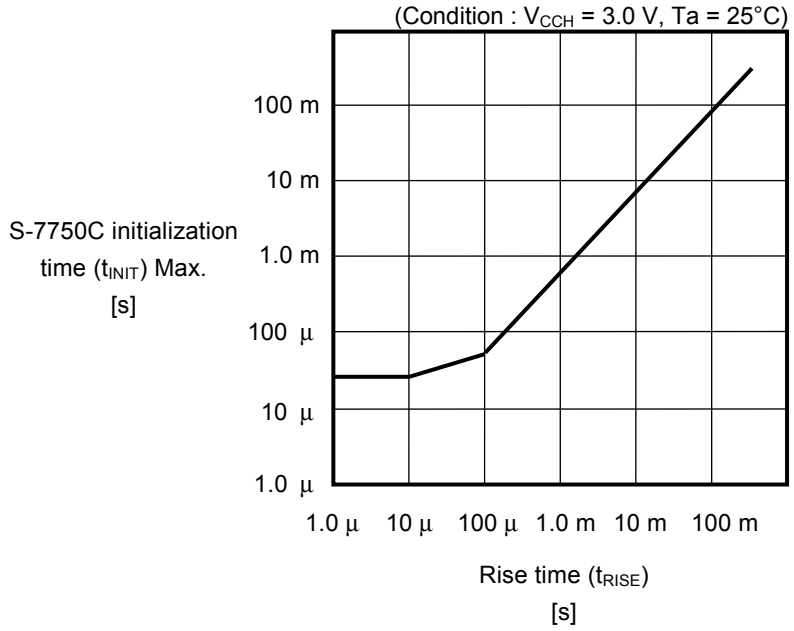


Figure 34 Initialization Time

5. Data hold time ($t_{HD.\ DAT}$ = 0 ns)

If SCL and SDA of the S-7750C are changed at the same time, the timing which takes to reach the S-7750C slightly lags due to a load on the bus line. As a result, the change in the SDA precedes a falling edge of SCL so that S-7750C may recognize a start/stop condition.
To avoid this, in the S-7750C, it is recommended to set the delay time of over 0.3 µs for a falling edge of SCL.
In its specs, it is described as the S-7750C works at 0 ns of data hold time, however, take account into the above action in actual use.

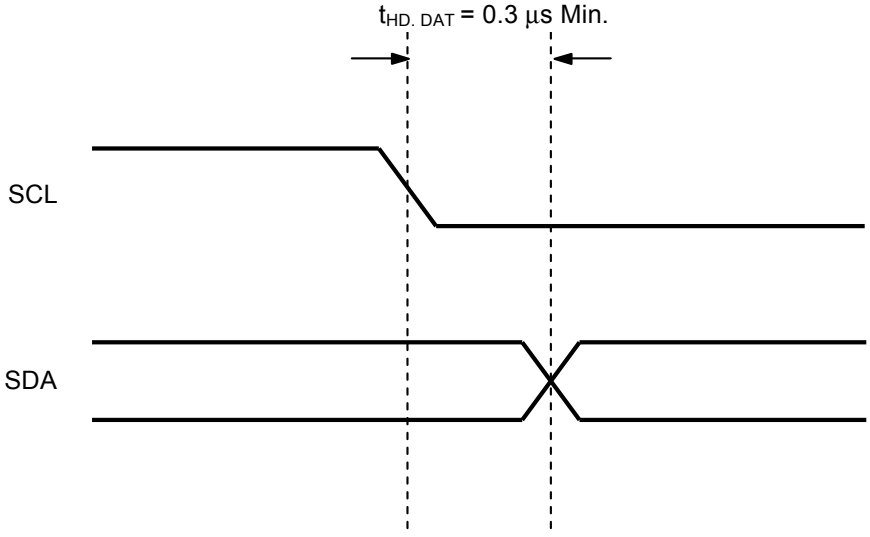


Figure 35 Data Hold Time

6. SDA pin and SCL pin noise suppression time

The S-7750C includes a built-in low-pass filter at the SDA and SCL pins to suppress noise.
This filter suppresses noise with the width of less than 130 ns when the power supply voltage is 3.0 V.
Refer to noise suppression time (t_I) in **Table 9** regarding details of the assurable value.

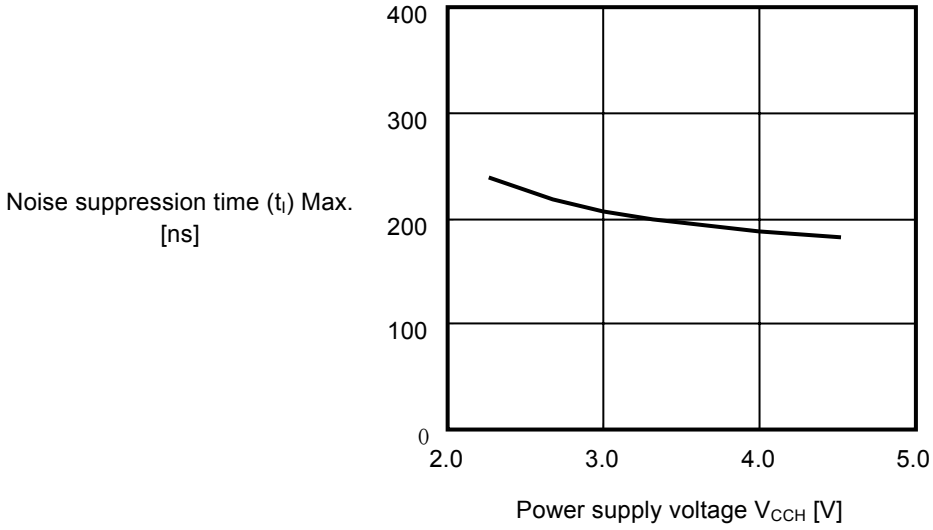


Figure 36 Noise Suppression Time for SDA and SCL Pins

■ Precautions

- Semiconductor devices must be used within the absolute maximum rating. Special caution is required for the supply voltage. A momentary surge voltage exceeding the rated value may cause latch-up and malfunction. Confirm the detailed usage conditions required for each parameter by referring to the data sheet before use.
- If the S-7750C operates with moisture remaining in the circuits, a short circuit may occur between pins, causing a malfunction. When the S-7750C is taken out of the constant-low-temperature bath during evaluation, the pins of the S-7750C may be frosted. Note that, if the S-7750C is operated with the pins frosted, the pins may be short-circuited by moisture, causing a malfunction.
  The same applies when the S-7750C is used in an environment where condensation may occur, so care is required.
- Although the IC contains a static electricity protection circuit, static electricity that exceeds the limit of the protection circuit should not be applied.
- Seiko Instruments Inc. assumes no responsibility for the way in which this IC is used in products created using this IC or for the specifications of that product, nor does Seiko Instruments Inc. assume any responsibility for any infringement of patents or copyrights by products that include this IC either in Japan or in other countries.

■ Precautions for WLP Package

- The device's silicon substrate side is exposed to the marking side of the device package. Since this portion has a lower strength against mechanical stress than a standard plastic package, take sufficient care to avoid chips and cracks when handling the package. Moreover, the exposed side of the silicon has the electrical potential of the device substrate, and needs to be kept out of contact with the external potential.
- In this package, the transistor area side is overcoated with a translucent resin. Keep in mind that the characteristics of the package may be affected if the device is exposed under an intensive light source.

■ Option

Three options which are available for the S-7750C and the option tables are shown here. When selecting the option, follow these descriptions.

1. Device code (8 types)

Selecting the arbitrary device address code is available (Refer to **Figure 10**).

Table 12 Option List of Device Code

No.	C2	C1	C0
(0)	0	0	0
(1)	0	0	1
(2)	0	1	0
(3)	0	1	1
(4)	1	0	0
(5)	1	0	1
(6)	1	1	0
(7)	1	1	1

2. Internal generation of oscillation clock / External input

The S-7750C incorporates an oscillator for generating delay time. Instead of using the oscillator, an external oscillation clock can be used for the delay time.

Table 13 Option List of Oscillation Clock

No.	Internal / External
(1)	Using an internal oscillation circuit
(2)	Using an external oscillation circuit

3. Delay time

The delay time can be selected between A: ×1 and B: ×2. (T': Oscillation clock cycle (5 μs when using the internal oscillation circuit)).

Table 14 Option List of Delay Time

No.	Delay	Timer scale setting register	
		1: Delay time for short-time setting (T)	0: Delay time for long-time setting (LT)
A	×1	T'×1	T'×64
B	×2	T'×2	T'×128

■ Option Format

When you order the option, fill these tables and contact us. Regarding the details, refer to "■ **Option**".

1. Switching of device codes

No.	C2	C1	C0

2. Switching of clock for oscillation to internal generation or external input

No.	Internal / External

3. Switching of delay time option

No.	×1 / ×2

■ Table for Write data to E^{2}PROM

Please fill this table and send to our sales office when you order Write data to E^{2}PROM.

E^{2}PROM (Command code)	Write data	Default	Remark
Free area 1 (0100)		FFH	–
Control port (0101)		00H	–
Timer scale setting (0110)		FFH	1: Short-time, 0: Long-time
Free area 2 (0111)		FFH	–
Timer setting for DO0(1000)		00H	1 for time that you select, 0 for others
Timer setting for D1 (1001)		00H	1 for time that you select, 0 for others
Timer setting for D2 (1010)		00H	1 for time that you select, 0 for others
Timer setting for D3 (1011)		00H	1 for time that you select, 0 for others
Timer setting for D4 (1100)		00H	1 for time that you select, 0 for others
Timer setting for D5 (1101)		00H	1 for time that you select, 0 for others
Timer setting for D6 (1110)		00H	1 for time that you select, 0 for others
Timer setting for D7 (1111)		00H	1 for time that you select, 0 for others

■ Product Name Structure

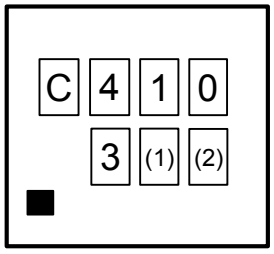
S-7750C x x xx – HCT1

- HCT1: Package name (abbreviation) and IC packing specifications
  HCT1: WLP-16A, Tape
- xx: E^{2}PROM code
- x: Clock for oscillation circuit, delay time option
  0: internal oscillation circuit, delay time; x1
  1: internal oscillation circuit, delay time; x2
  2: external oscillation circuit, delay time; x1
  3: external oscillation circuit, delay time; x2
- x: Device code : 0 to 7

■ Marking Specification

(1) WLP-16A

WLP-16A
Top view



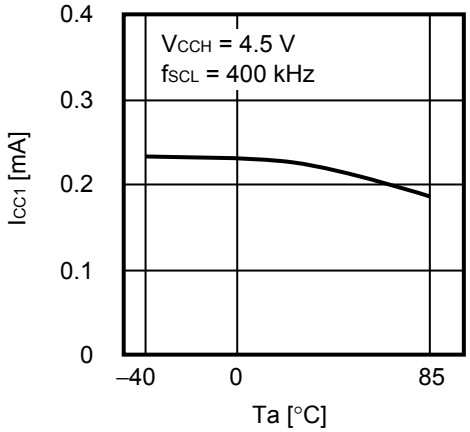
This is an example in S-7750C4103

(1), (2) : Lot number

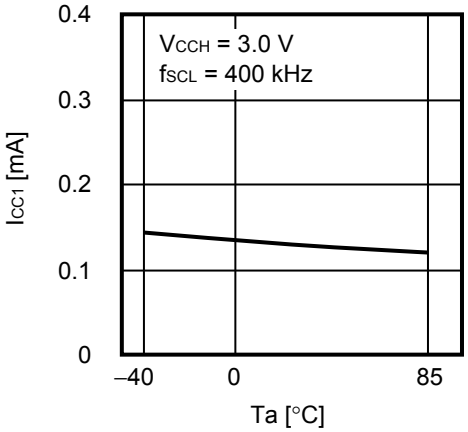
■ Characteristics (Typical Data)

1. DC Characteristics

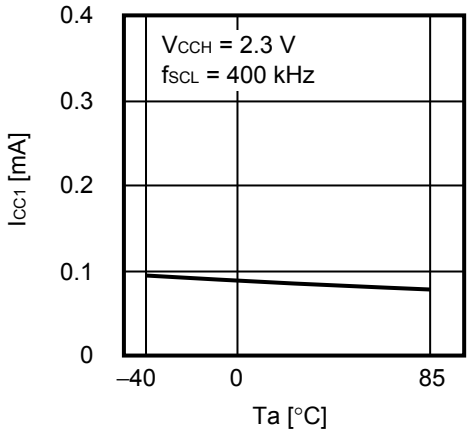
1. 1 Current consumption (READ) I_{CC1} vs. Ambient temperature Ta



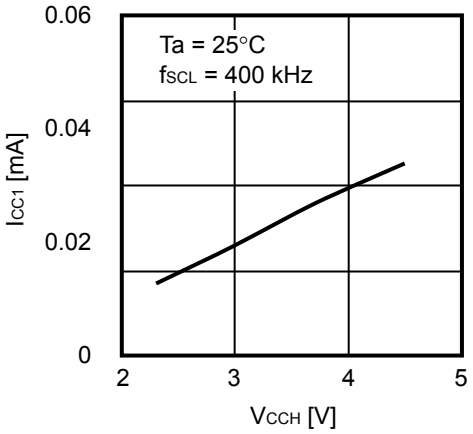
1. 2 Current consumption (READ) I_{CC1} vs. Ambient temperature Ta



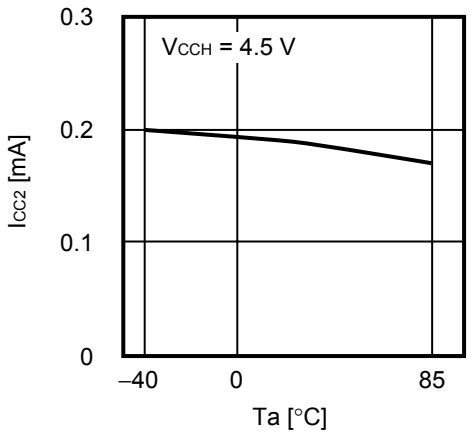
1. 3 Current consumption (READ) I_{CC1} vs. Ambient temperature Ta



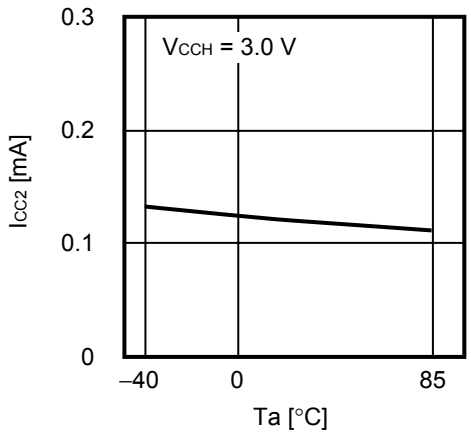
1. 4 Current consumption (READ) I_{CC1} vs. Power supply voltage V_{CCH}



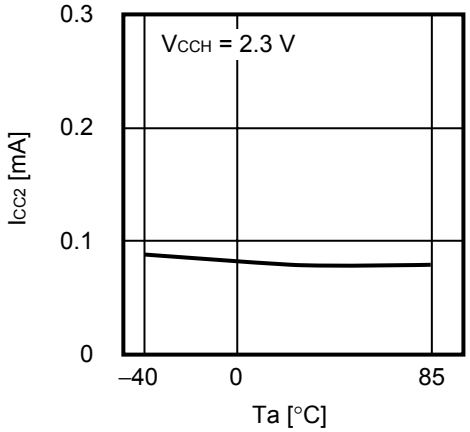
1. 5 Current consumption (PROGRAM) I_{CC2} vs. Ambient temperature Ta



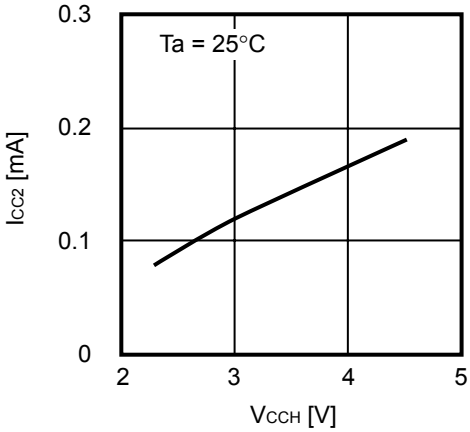
1. 6 Current consumption (PROGRAM) I_{CC2} vs. Ambient temperature Ta



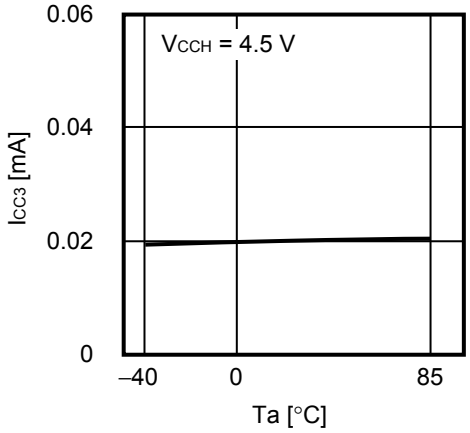
1. 7 Current consumption (PROGRAM) I_{CC2} vs. Ambient temperature Ta



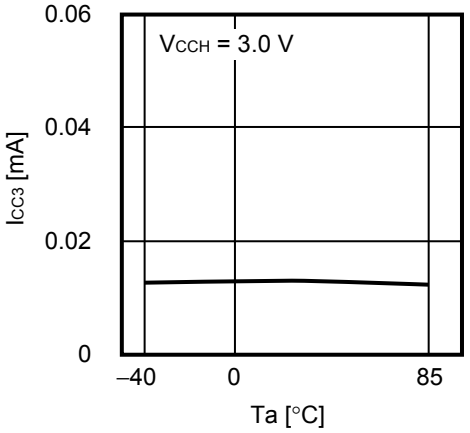
1. 8 Current consumption (PROGRAM) I_{CC2} vs. Power supply voltage V_{CCH}



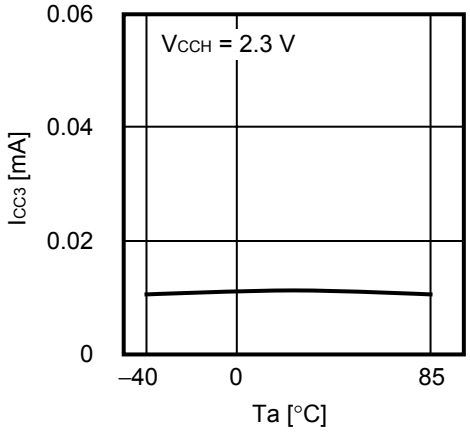
1. 9 Internal oscillator current consumption during operation I_{CC3} vs. Ambient temperature Ta



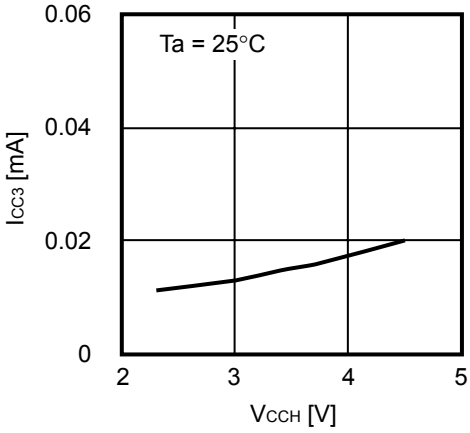
1. 10 Internal oscillator current consumption during operation I_{CC3} vs. Ambient temperature Ta



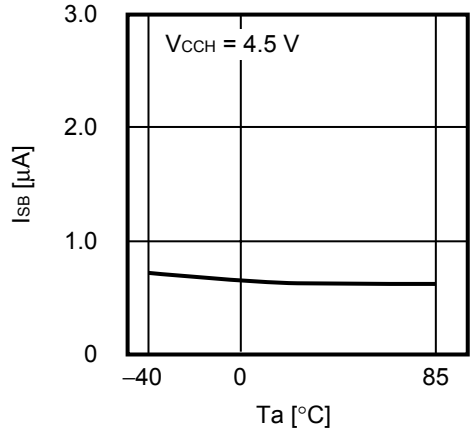
1. 11 Internal oscillator current consumption during operation I_{CC3} vs. Ambient temperature Ta



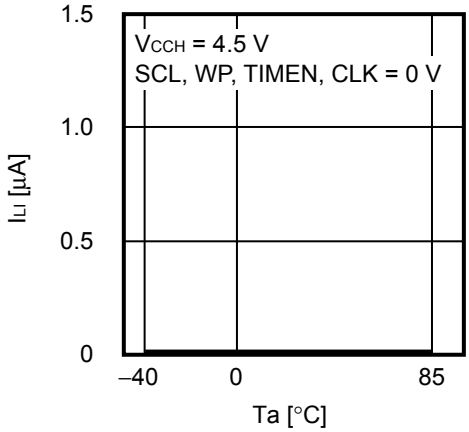
1. 12 Internal oscillator current consumption during operation I_{CC3} vs. Power supply voltage V_{CCH}



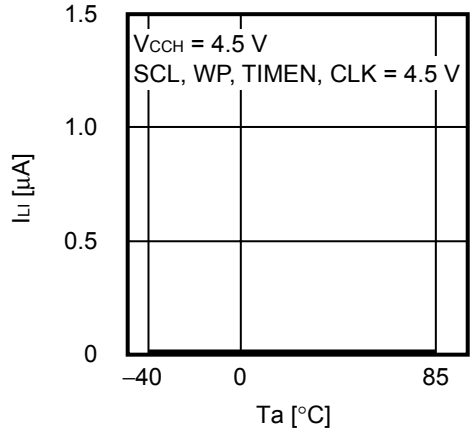
1. 13 Standby current consumption I_{SB} vs. Ambient temperature Ta



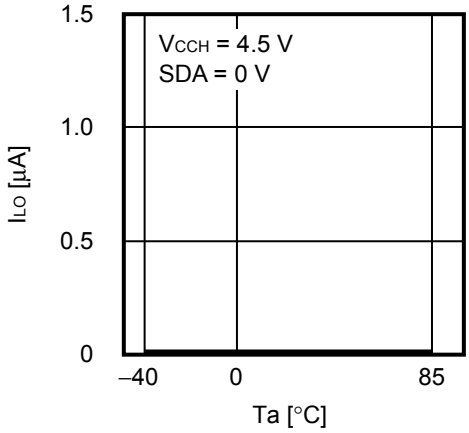
1. 14 Input leakage current I_{LI} vs. Ambient temperature Ta



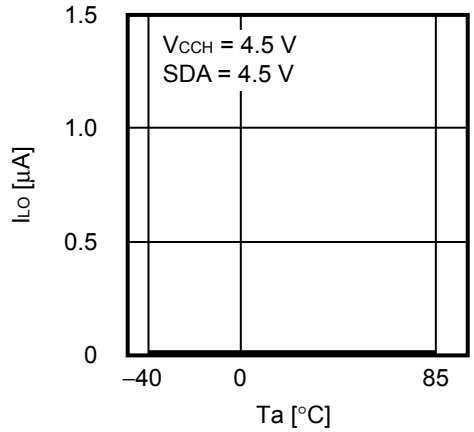
1. 15 Input leakage current I_{LI} vs. Ambient temperature Ta



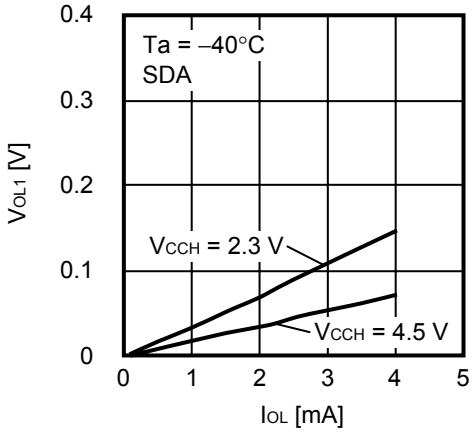
1. 16 Output leakage current I_{LO} vs. Ambient temperature Ta



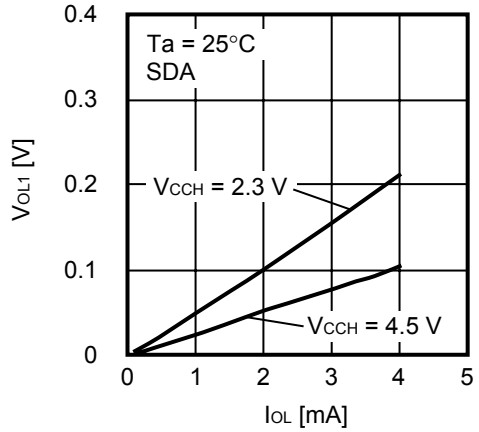
1. 17 Output leakage current I_{LO} vs. Ambient temperature Ta



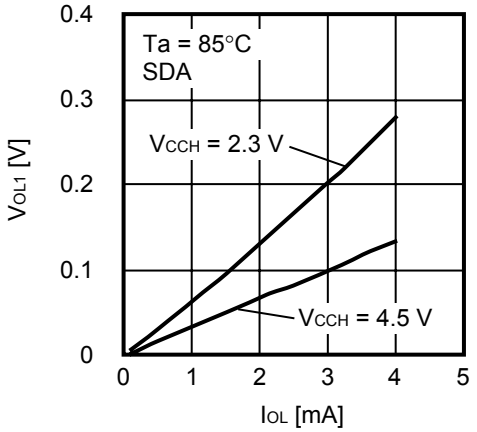
1. 18 Low level output voltage V_{OL1} vs. Low level output current I_{OL}



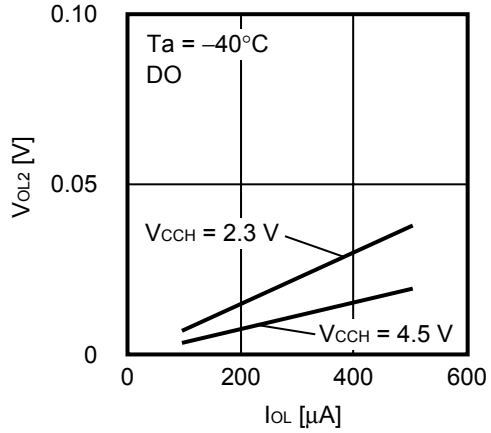
1. 19 Low level output voltage V_{OL1} vs. Low level output current I_{OL}



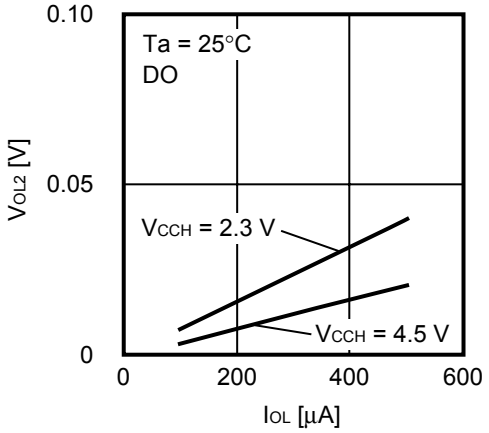
1. 20 Low level output voltage V_{OL1} vs. Low level output current I_{OL}



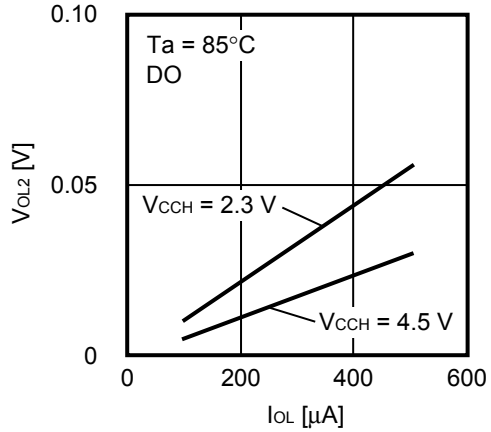
1. 21 Low level output voltage V_{OL2} vs. Low level output current I_{OL}



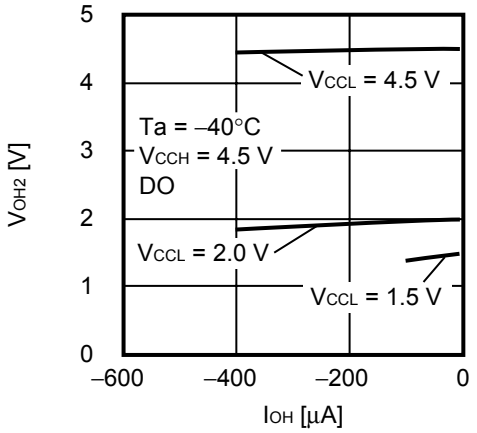
1. 22 Low level output voltage V_{OL2} vs. Low level output current I_{OL}



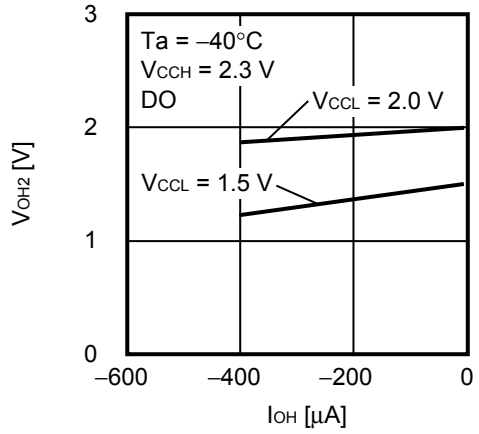
1. 23 Low level output voltage V_{OL2} vs. Low level output current I_{OL}



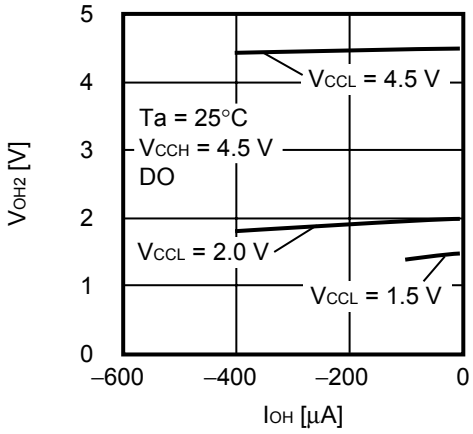
1. 24 High level output voltage V_{OH2} vs. High level output current I_{OH}



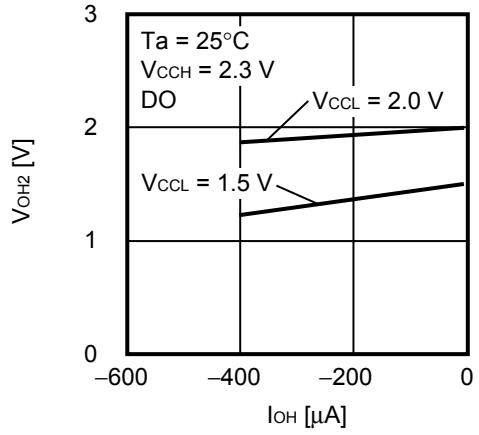
1. 25 High level output voltage V_{OH2} vs. High level output current I_{OH}



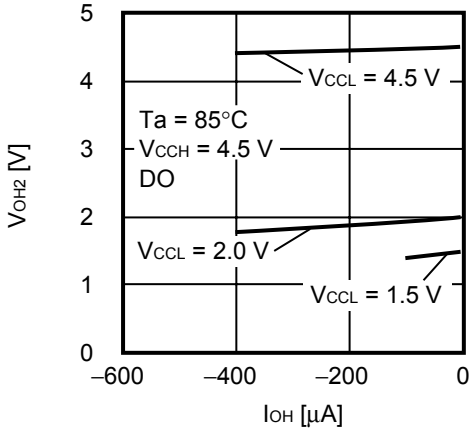
1. 26 High level output voltage V_{OH2} vs. High level output current I_{OH}



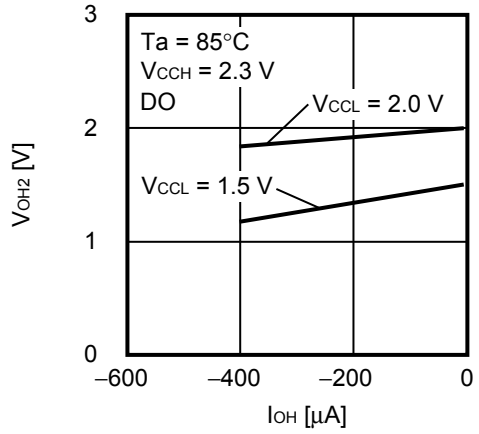
1. 27 High level output voltage V_{OH2} vs. High level output current I_{OH}



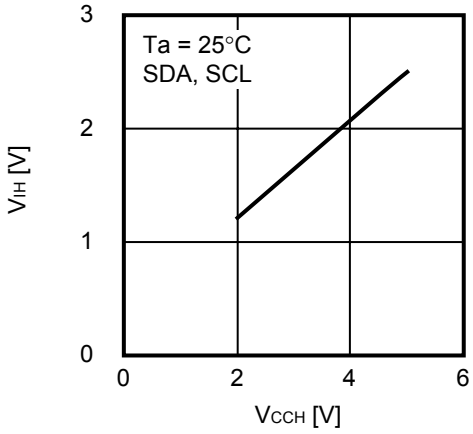
1. 28 High level output voltage V_{OH2} vs. High level output current I_{OH}



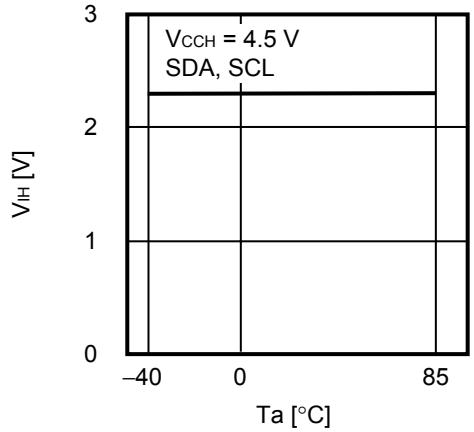
1. 29 High level output voltage V_{OH2} vs. High level output current I_{OH}



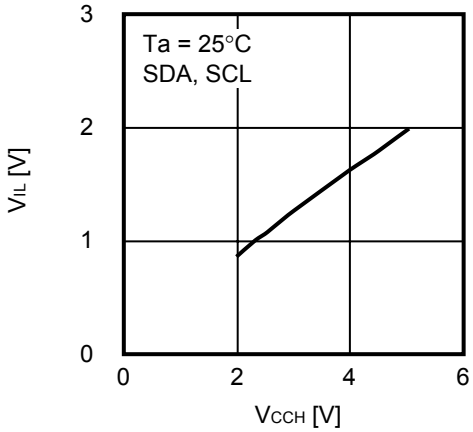
1. 30 High level input inversion voltage V_{IH} vs. Power supply voltage V_{CCH}



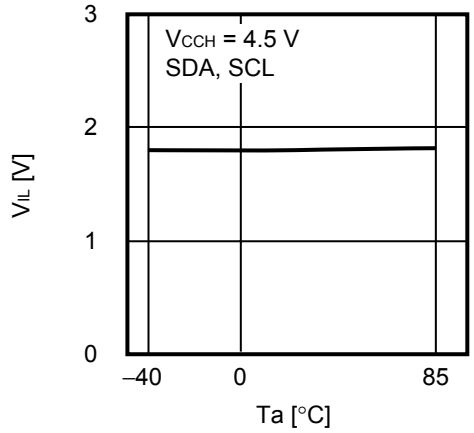
1. 31 High level input inversion voltage V_{IH} vs. Ambient temperature Ta



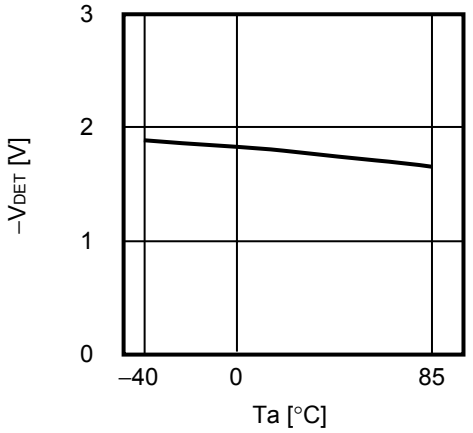
1. 32 Low level input inversion voltage V_{IL} vs. Power supply voltage V_{CCH}



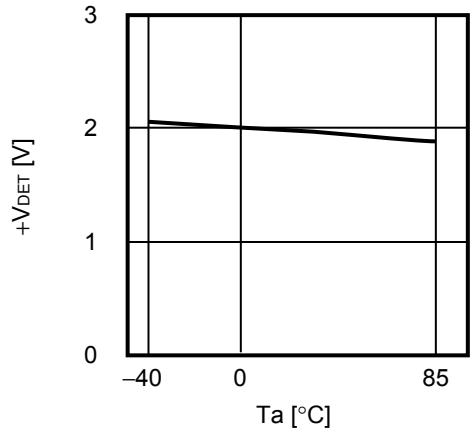
1. 33 Low level input inversion voltage V_{IL} vs. Ambient temperature Ta



1. 34 Low power supply detection voltage $-V_{DET}$ vs. Ambient temperature Ta

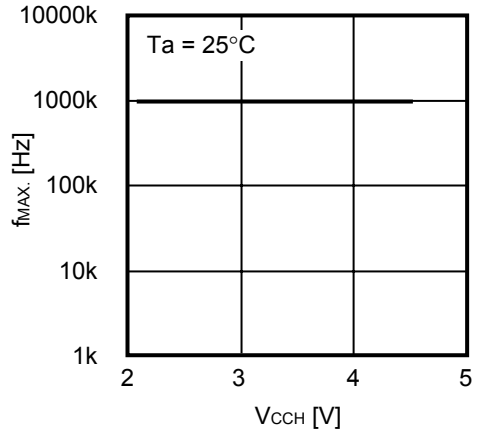


1. 35 Low power supply release voltage $+V_{DET}$ vs. Ambient temperature Ta

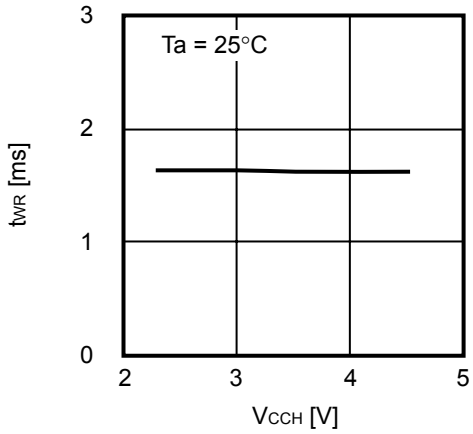


2. AC Characteristics

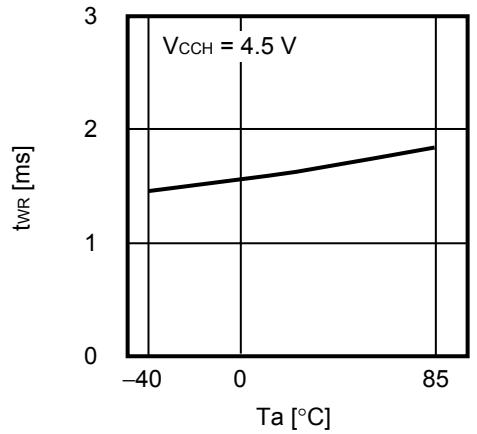
2. 1 Maximum operating frequency $f_{MAX.}$ vs. Power supply voltage V_{CCH}



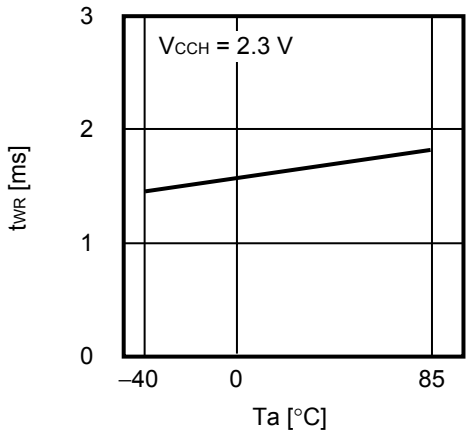
2. 2 Write time t_{WR} vs. Power supply voltage V_{CCH}



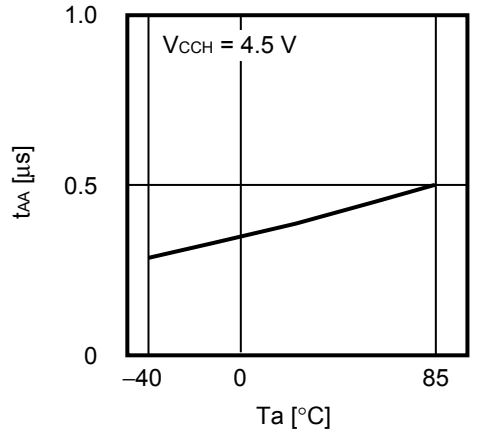
2. 3 Write time t_{WR} vs. Ambient temperature Ta



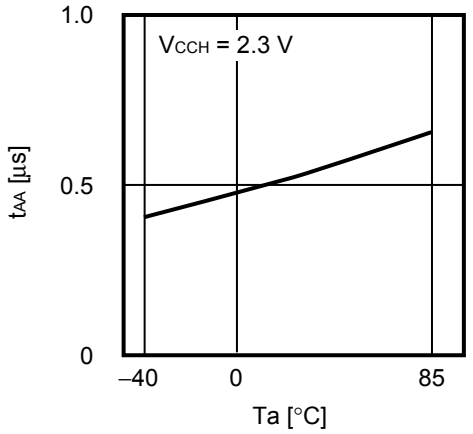
2. 4 Write time t_{WR} vs. Ambient temperature Ta

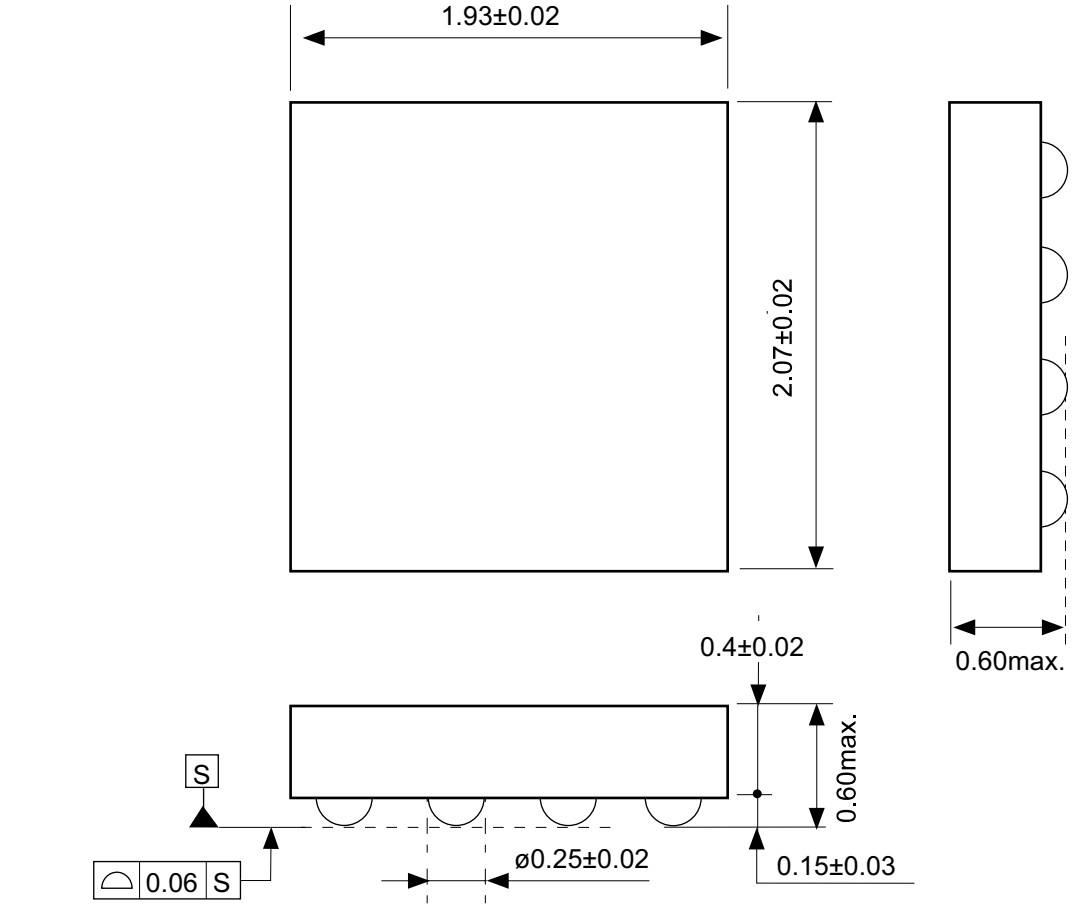


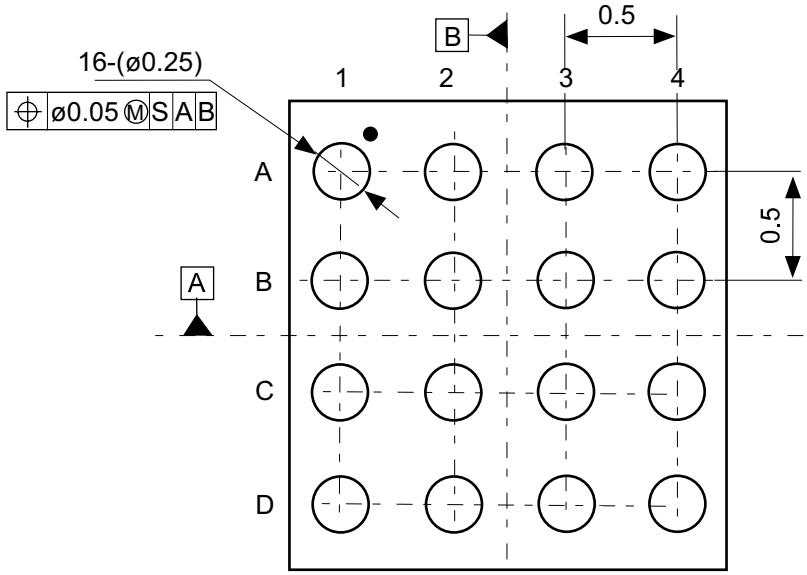
2. 5 SDA output delay time t_{AA} vs. Ambient temperature Ta



2. 6 SDA output delay time t_{AA} vs. Ambient temperature Ta

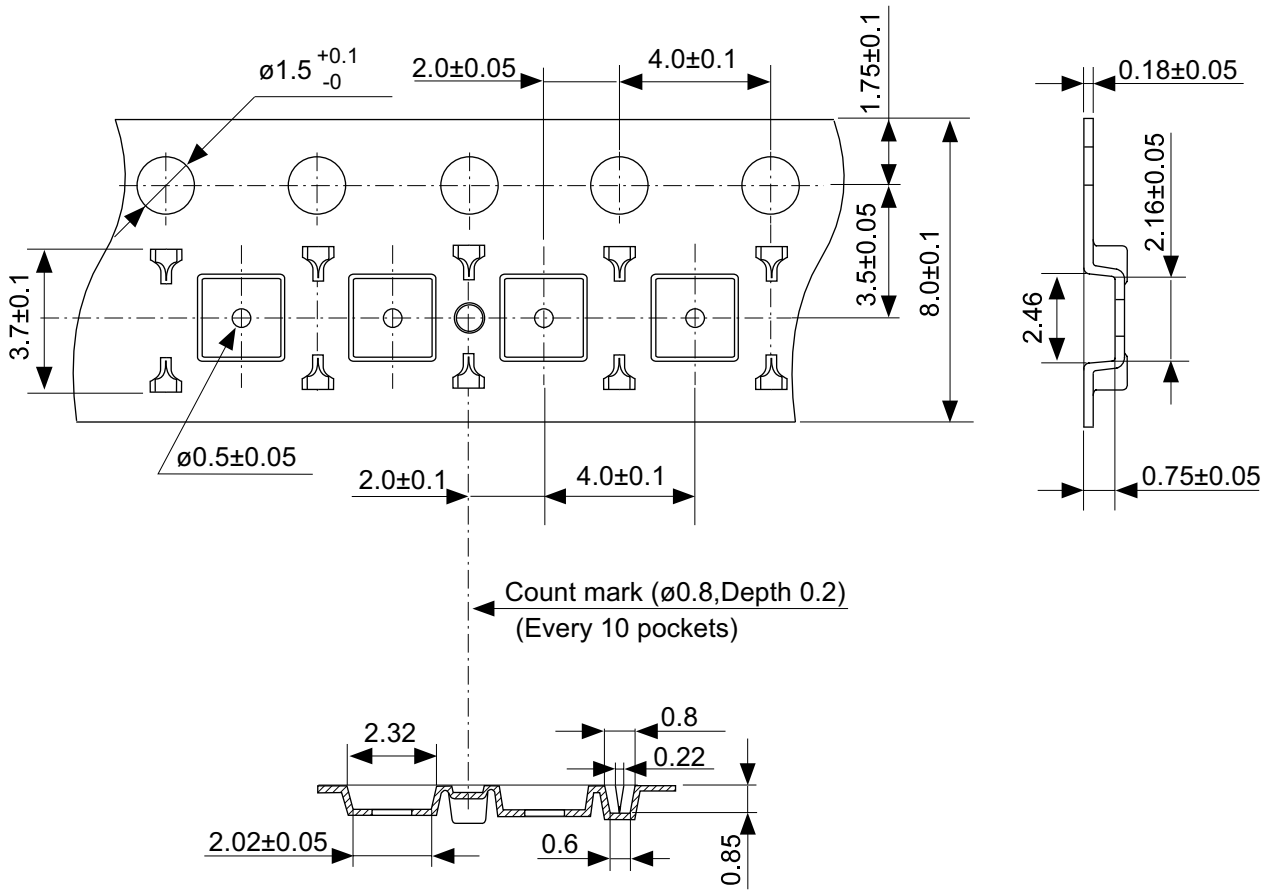


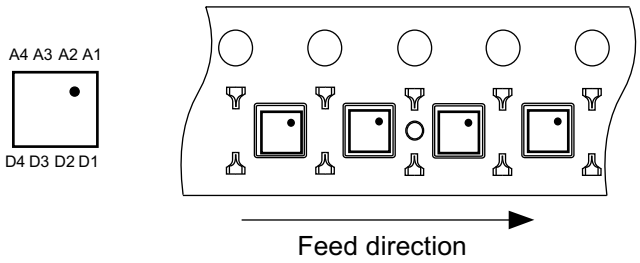




No. HA016-A-P-SD-1.1

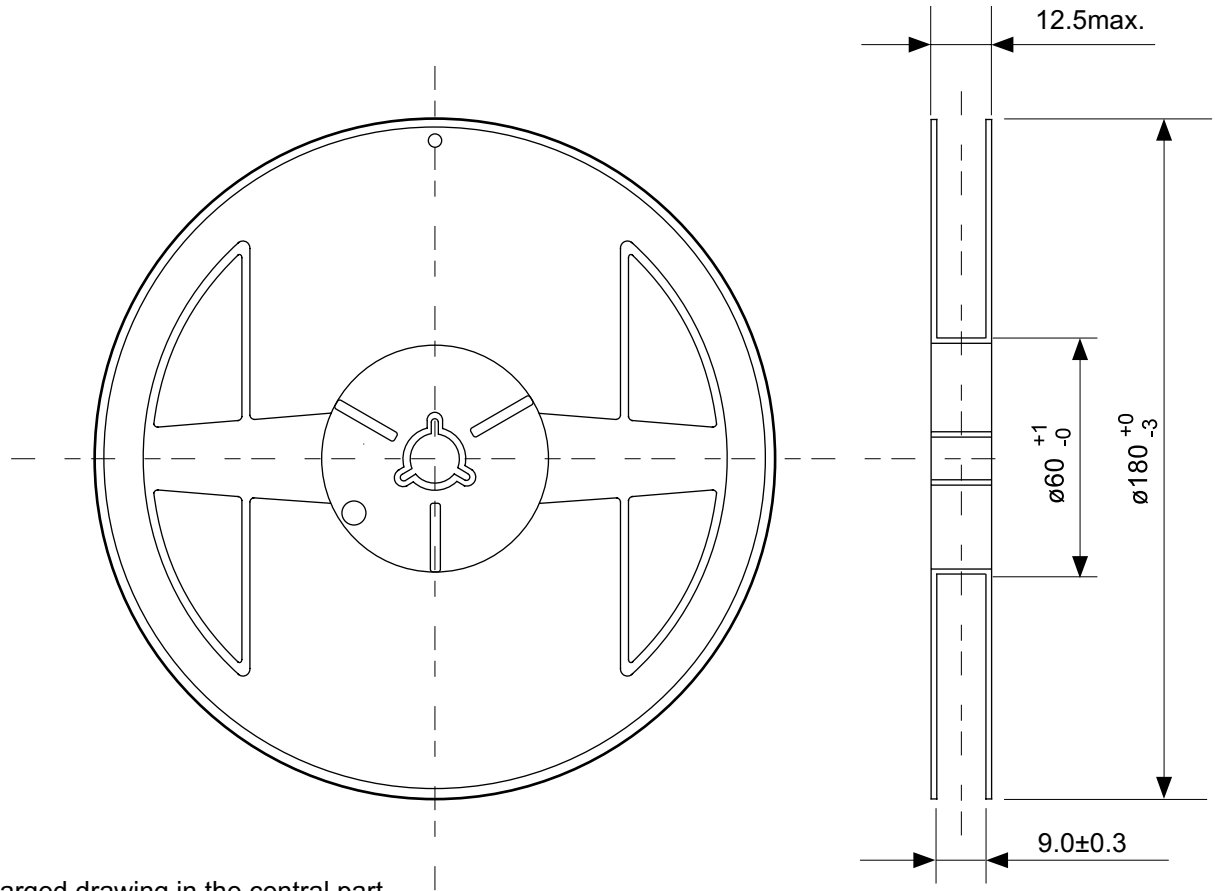
TITLE	WLP-16A-A-PKG Dimensions
No.	HA016-A-P-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	



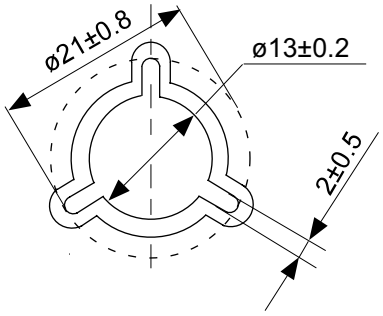


No. HA016-A-C-S2-1.0

TITLE	WLP-16A-A-Carrier Tape
No.	HA016-A-C-S2-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. HA016-A-R-SD-1.0

TITLE	WLP-16A-A-Reel		
No.	HA016-A-R-SD-1.0		
SCALE		QTY.	3,000
UNIT	mm		
Seiko Instruments Inc.			

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