



HIGH-SPEED 3.3V 64K x 18 SYNCHRONOUS PIPELINED DUAL-PORT STATIC RAM WITH 3.3V OR 2.5V INTERFACE

IDT70V3389S

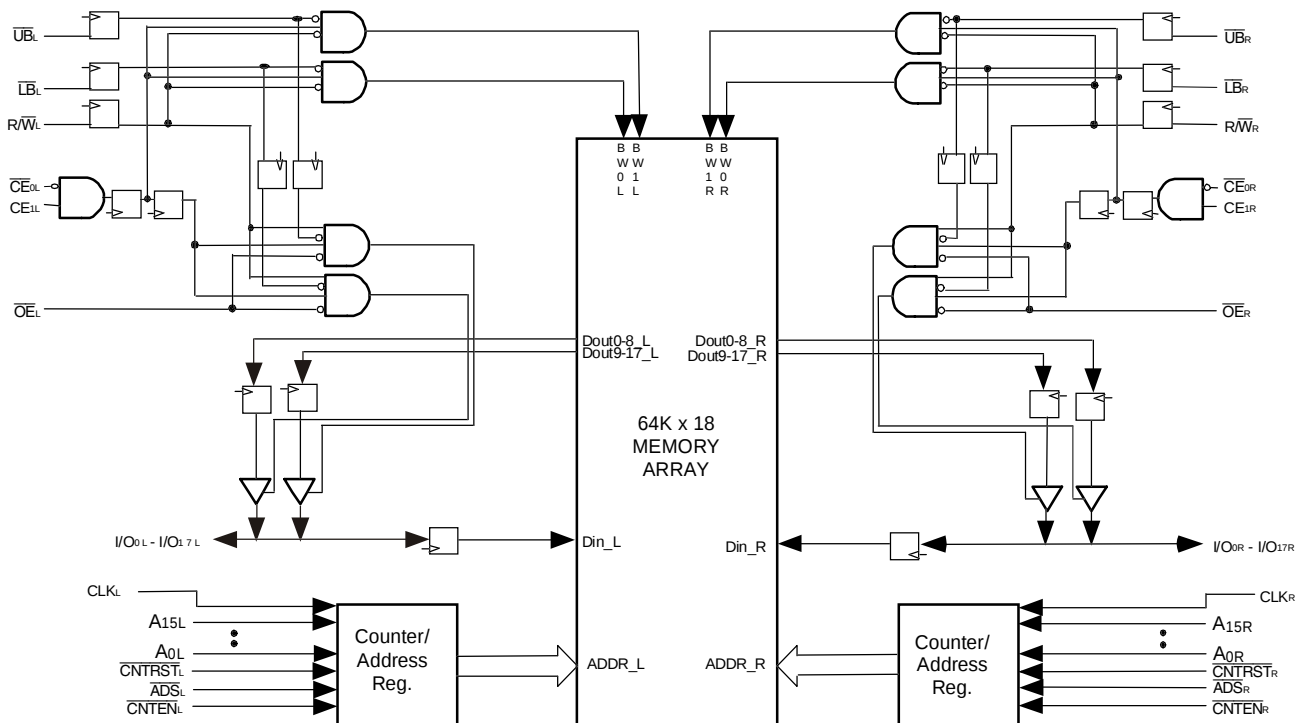
Features

- ♦ True Dual-Port memory cells which allow simultaneous access of the same memory location
- ♦ High-speed clock to data access
 - Commercial: 4.2/5/6ns (max.)
 - Industrial: 5/6ns (max)
- ♦ Pipelined output mode
- ♦ Counter enable and reset features
- ♦ Dual chip enables allow for depth expansion without additional logic
- ♦ Full synchronous operation on both ports
 - 7.5ns cycle time, 133MHz operation (9.6 Gbps bandwidth)
 - Fast 4.2ns clock to data out
 - 1.8ns setup to clock and 0.7ns hold on all control, data, and

address inputs @ 133MHz

- Data input, address, byte enable and control registers
- Self-timed write allows fast cycle time
- ♦ Separate byte controls for multiplexed bus and bus matching compatibility
- ♦ LVTTTL-compatible, single 3.3V ($\pm 150\text{mV}$) power supply for core
- ♦ LVTTTL-compatible, selectable 3.3V ($\pm 150\text{mV}$)/2.5V ($\pm 125\text{mV}$) power supply for I/Os and control signals on each port
- ♦ Industrial temperature range (-40°C to $+85^{\circ}\text{C}$) is available for selected speeds
- ♦ Available in a 128-pin Thin Quad Plastic Flatpack (TQFP), 208-pin fine pitch Ball Grid Array, and 256-pin Ball Grid Array

Functional Block Diagram



4832 tbi 01

APRIL 2001

Description:

The IDT70V3389 is a high-speed 64K x 18 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times. With an input data register, the IDT70V3389 has been optimized for applications having unidirectional or bidirectional data flow

in bursts. An automatic power down feature, controlled by $\overline{CE}_0$ and CE_1 , permits the on-chip circuitry of each port to enter a very low standby power mode.

The 70V3389 can support an operating voltage of either 3.3V or 2.5V on one or both ports, controllable by the OPT pins. The power supply for the core of the device (V_{DD}) remains at 3.3V.

Pin Configuration^(1,2,3,4)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17		
I/O _{9L}	NC	V _{SS}	NC	NC	NC	A _{12L}	A _{8L}	NC	V _{DD}	CLK _L	$\overline{\text{CNTEN}}_{\text{L}}$	A _{4L}	A _{0L}	OPT _L	NC	V _{SS}	A	
NC	V _{SS}	NC	V _{SS}	NC	A _{13L}	A _{9L}	NC	$\overline{\text{CE}}_{0\text{L}}$	V _{SS}	$\overline{\text{ADS}}_{\text{L}}$	A _{6L}	A _{1L}	V _{SS}	V _{DDQR}	I/O _{8L}	NC	B	
V _{DDQL}	I/O _{9R}	V _{DDQR}	V _{DD}	NC	A _{14L}	A _{10L}	$\overline{\text{UB}}_{\text{L}}$	CE _{1L}	V _{SS}	R/ $\overline{\text{WL}}$	A _{6L}	A _{2L}	V _{DD}	I/O _{8R}	NC	V _{SS}	C	
NC	V _{SS}	I/O _{10L}	NC	A _{15L}	A _{11L}	A _{7L}	$\overline{\text{LB}}_{\text{L}}$	V _{DD}	$\overline{\text{OE}}_{\text{L}}$	$\overline{\text{CNTRST}}_{\text{L}}$	A _{3L}	V _{DD}	NC	V _{DDQL}	I/O _{7L}	I/O _{7R}	D	
I/O _{11L}	NC	V _{DDQR}	I/O _{10R}	70V3389BF BF-208⁽⁵⁾ 208-Pin fpBGA Top View⁽⁶⁾										I/O _{6L}	NC	V _{SS}	NC	E
V _{DDQL}	I/O _{11R}	NC	V _{SS}											V _{SS}	I/O _{6R}	NC	V _{DDQR}	F
NC	V _{SS}	I/O _{12L}	NC											NC	V _{DDQL}	I/O _{5L}	NC	G
V _{DD}	NC	V _{DDQR}	I/O _{12R}											V _{DD}	NC	V _{SS}	I/O _{5R}	H
V _{DDQL}	V _{DD}	V _{SS}	V _{SS}											V _{SS}	V _{DD}	V _{SS}	V _{DDQR}	J
I/O _{14R}	V _{SS}	I/O _{13R}	V _{SS}											I/O _{3R}	V _{DDQL}	I/O _{4R}	V _{SS}	K
NC	I/O _{14L}	V _{DDQR}	I/O _{13L}											NC	I/O _{3L}	V _{SS}	I/O _{4L}	L
V _{DDQL}	NC	I/O _{15R}	V _{SS}											V _{SS}	NC	I/O _{2R}	V _{DDQR}	M
NC	V _{SS}	NC	I/O _{15L}											I/O _{1R}	V _{DDQL}	NC	I/O _{2L}	N
I/O _{16R}	I/O _{16L}	V _{DDQR}	NC	NC	NC	A _{12R}	A _{8R}	NC	V _{DD}	CLK _R	$\overline{\text{CNTEN}}_{\text{R}}$	A _{4R}	NC	I/O _{1L}	V _{SS}	NC	P	
V _{SS}	NC	I/O _{17R}	NC	NC	A _{13R}	A _{9R}	NC	$\overline{\text{CE}}_{0\text{R}}$	V _{SS}	$\overline{\text{ADS}}_{\text{R}}$	A _{6R}	A _{1R}	V _{SS}	V _{DDQL}	I/O _{0R}	V _{DDQR}	R	
NC	I/O _{17L}	V _{DDQL}	V _{SS}	NC	A _{14R}	A _{10R}	$\overline{\text{UB}}_{\text{R}}$	CE _{1R}	V _{SS}	R/ $\overline{\text{WL}}$	A _{6R}	A _{2R}	V _{SS}	NC	V _{SS}	NC	T	
V _{SS}	NC	V _{DD}	NC	A _{15R}	A _{11R}	A _{7R}	$\overline{\text{LB}}_{\text{R}}$	V _{DD}	$\overline{\text{OE}}_{\text{R}}$	$\overline{\text{CNTRST}}_{\text{R}}$	A _{3R}	A _{0R}	V _{DD}	OPT _R	NC	I/O _{0L}	U	

4832 tbl 02

NOTES:

1. All V_{DD} pins must be connected to 3.3V power supply.
2. All V_{DDQ} pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V_{IH} (3.3V), and 2.5V if OPT pin for that port is set to V_{IL} (0V).
3. All V_{SS} pins must be connected to ground supply.
4. Package body is approximately 15mm x 15mm x 1.4mm with 0.8mm ball pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Configuration^(1,2,3,4) (con't.)

70V3389BC
BC-256⁽⁵⁾

256-Pin BGA
Top View⁽⁶⁾

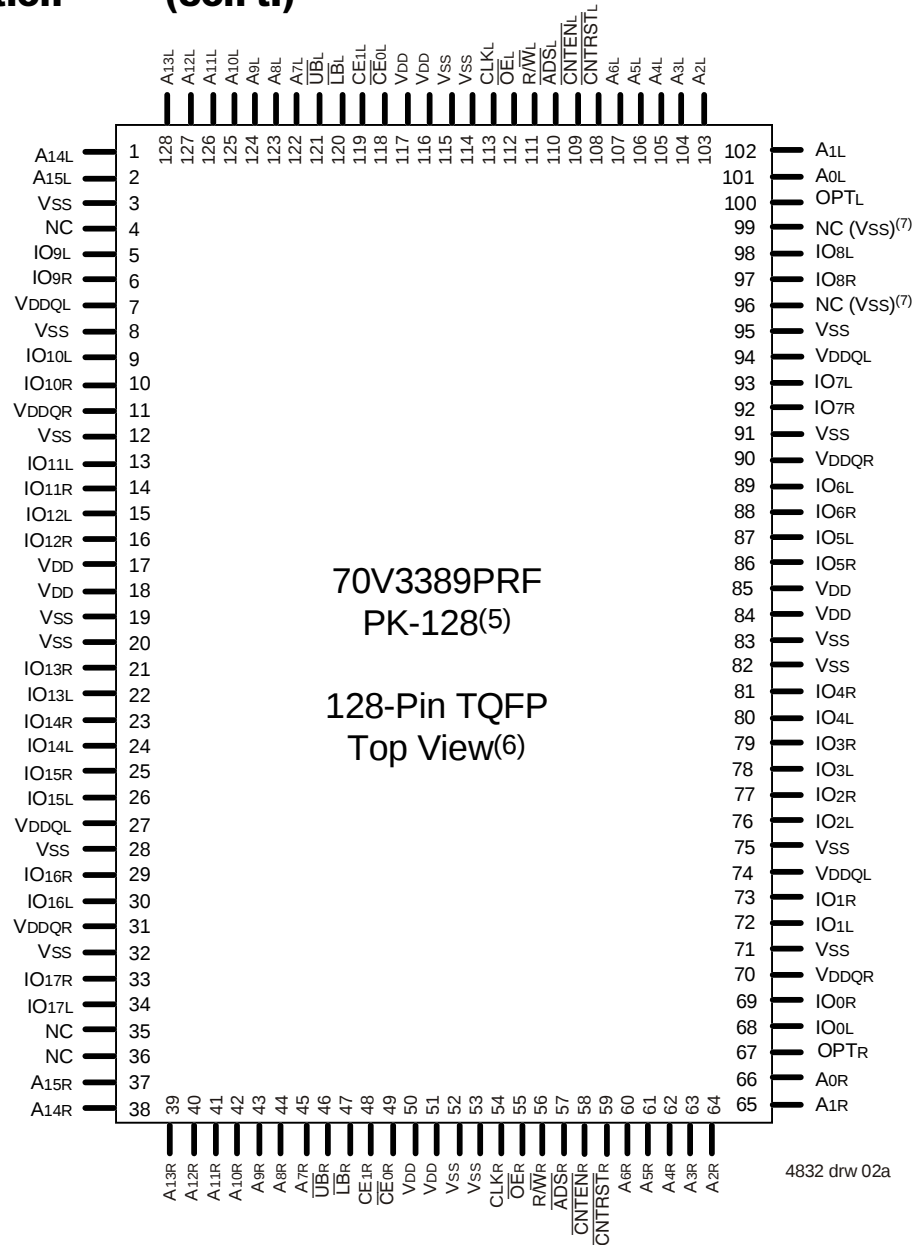
A1 NC	A2 NC	A3 NC	A4 NC	A5 A14L	A6 A11L	A7 A8L	A8 NC	A9 CE1L	A10 OE _L	A11 CNTEN _L	A12 A5L	A13 A2L	A14 A0L	A15 NC	A16 NC
B1 NC	B2 NC	B3 NC	B4 NC	B5 A15L	B6 A12L	B7 A9L	B8 UB _L	B9 CE _{0L}	B10 R/W _L	B11 CNTRST _L	B12 A4L	B13 A1L	B14 V _{DD}	B15 NC	B16 NC
C1 NC	C2 I/O _{9L}	C3 V _{SS}	C4 NC	C5 A13L	C6 A10L	C7 A7L	C8 NC	C9 LB _L	C10 CLK _L	C11 ADS _L	C12 A6L	C13 A3L	C14 OPT _L	C15 NC	C16 I/O _{8L}
D1 NC	D2 I/O _{9R}	D3 NC	D4 V _{DD}	D5 V _{DDQ} L	D6 V _{DDQ} L	D7 V _{DDQ} R	D8 V _{DDQ} R	D9 V _{DDQ} L	D10 V _{DDQ} L	D11 V _{DDQ} R	D12 V _{DDQ} R	D13 V _{DD}	D14 NC	D15 NC	D16 I/O _{8R}
E1 I/O _{10R}	E2 I/O _{10L}	E3 NC	E4 V _{DDQ} L	E5 V _{DD}	E6 V _{DD}	E7 V _{SS}	E8 V _{SS}	E9 V _{SS}	E10 V _{SS}	E11 V _{DD}	E12 V _{DD}	E13 V _{DDQ} R	E14 NC	E15 I/O _{7L}	E16 I/O _{7R}
F1 I/O _{11L}	F2 NC	F3 I/O _{11R}	F4 V _{DDQ} L	F5 V _{DD}	F6 V _{SS}	F7 V _{SS}	F8 V _{SS}	F9 V _{SS}	F10 V _{SS}	F11 V _{SS}	F12 V _{DD}	F13 V _{DDQ} R	F14 I/O _{6R}	F15 NC	F16 I/O _{6L}
G1 NC	G2 NC	G3 I/O _{12L}	G4 V _{DDQ} R	G5 V _{SS}	G6 V _{SS}	G7 V _{SS}	G8 V _{SS}	G9 V _{SS}	G10 V _{SS}	G11 V _{SS}	G12 V _{SS}	G13 V _{DDQ} L	G14 I/O _{5L}	G15 NC	G16 NC
H1 NC	H2 I/O _{12R}	H3 NC	H4 V _{DDQ} R	H5 V _{SS}	H6 V _{SS}	H7 V _{SS}	H8 V _{SS}	H9 V _{SS}	H10 V _{SS}	H11 V _{SS}	H12 V _{SS}	H13 V _{DDQ} L	H14 NC	H15 NC	H16 I/O _{5R}
J1 I/O _{13L}	J2 I/O _{14R}	J3 I/O _{13R}	J4 V _{DDQ} L	J5 V _{SS}	J6 V _{SS}	J7 V _{SS}	J8 V _{SS}	J9 V _{SS}	J10 V _{SS}	J11 V _{SS}	J12 V _{SS}	J13 V _{DDQ} R	J14 I/O _{4R}	J15 I/O _{3R}	J16 I/O _{4L}
K1 NC	K2 NC	K3 I/O _{14L}	K4 V _{DDQ} L	K5 V _{SS}	K6 V _{SS}	K7 V _{SS}	K8 V _{SS}	K9 V _{SS}	K10 V _{SS}	K11 V _{SS}	K12 V _{SS}	K13 V _{DDQ} R	K14 NC	K15 NC	K16 I/O _{3L}
L1 I/O _{15L}	L2 NC	L3 I/O _{15R}	L4 V _{DDQ} R	L5 V _{DD}	L6 V _{SS}	L7 V _{SS}	L8 V _{SS}	L9 V _{SS}	L10 V _{SS}	L11 V _{SS}	L12 V _{DD}	L13 V _{DDQ} L	L14 I/O _{2L}	L15 NC	L16 I/O _{2R}
M1 I/O _{16R}	M2 I/O _{16L}	M3 NC	M4 V _{DDQ} R	M5 V _{DD}	M6 V _{DD}	M7 V _{SS}	M8 V _{SS}	M9 V _{SS}	M10 V _{SS}	M11 V _{DD}	M12 V _{DD}	M13 V _{DDQ} L	M14 I/O _{1R}	M15 I/O _{1L}	M16 NC
N1 NC	N2 I/O _{17R}	N3 NC	N4 V _{DD}	N5 V _{DDQ} R	N6 V _{DDQ} R	N7 V _{DDQ} L	N8 V _{DDQ} L	N9 V _{DDQ} R	N10 V _{DDQ} R	N11 V _{DDQ} L	N12 V _{DDQ} L	N13 V _{DD}	N14 NC	N15 I/O _{0R}	N16 NC
P1 NC	P2 I/O _{17L}	P3 NC	P4 NC	P5 A13R	P6 A10R	P7 A7R	P8 NC	P9 LB _R	P10 CLK _R	P11 ADS _R	P12 A6R	P13 A3R	P14 NC	P15 NC	P16 I/O _{0L}
R1 NC	R2 NC	R3 NC	R4 NC	R5 A15R	R6 A12R	R7 A9R	R8 UB _R	R9 CE _{0R}	R10 R/W _R	R11 CNTRST _R	R12 A4R	R13 A1R	R14 OPT _R	R15 NC	R16 NC
T1 NC	T2 NC	T3 NC	T4 NC	T5 A14R	T6 A11R	T7 A8R	T8 NC	T9 CE1R	T10 OE _R	T11 CNTEN _R	T12 A5R	T13 A2R	T14 A0R	T15 NC	T16 NC

NOTES:

1. All V_{DD} pins must be connected to 3.3V power supply.
2. All V_{DDQ} pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V_{IH} (3.3V), and 2.5V if OPT pin for that port is set to V_{IL} (0V).
3. All V_{SS} pins must be connected to ground supply.
4. Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

4832 drw 02c

Pin Configuration^(1,2,3,4) (con't.)



NOTES:

1. All VDD pins must be connected to 3.3V power supply.
2. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
3. All VSS pins must be connected to ground supply.
4. Package body is approximately 14mm x 20mm x 1.4mm.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.
7. In the 70V3379 (32K x 18) and 70V3389 (64K x 18), pins 96 and 99 are NC. The upgrade devices 70V3399 (128K x 18) and 70V3319 (256K x 18) assign these pins as Vss. Customers who plan to take advantage of the upgrade path should treat these pins as Vss on the 70V3379 and 70V3389. If no upgrade is needed, the pins can be treated as NC.

Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$, CE_{1L}	$\overline{CE}_{0R}$, CE_{1R}	Chip Enables
$R/\overline{WL}$	$R/\overline{WR}$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - A_{15L}$	$A_{0R} - A_{15R}$	Address
$I/O_{0L} - I/O_{17L}$	$I/O_{0R} - I/O_{17R}$	Data Input/Output
CLK_L	CLK_R	Clock
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe Enable
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable
$\overline{CNTRST}_L$	$\overline{CNTRST}_R$	Counter Reset
$UB_L - LB_L$	$UB_R - LB_R$	Byte Enables (9-bit bytes)
V_{DDQL}	V_{DDQR}	Power (I/O Bus) (3.3V or 2.5V) ⁽¹⁾
OPT_L	OPT_R	Option for selecting V_{DDQX} ^(1,2)
V_{DD}		Power (3.3V) ⁽¹⁾
V_{SS}		Ground (0V)

4832 tbl 01

NOTES:

- V_{DD} , OPT_X , and V_{DDQX} must be set to appropriate operating levels prior to applying inputs on the I/Os and controls for that port.
- OPT_X selects the operating voltage levels for the I/Os and controls on that port. If OPT_X is set to VIH (3.3V), then that port's I/Os and controls will operate at 3.3V levels and V_{DDQX} must be supplied at 3.3V. If OPT_X is set to VIL (0V), then that port's I/Os and controls will operate at 2.5V levels and V_{DDQX} must be supplied at 2.5V. The OPT pins are independent of one another—both ports can operate at 3.3V levels, both can operate at 2.5V levels, or either can operate at 3.3V with the other at 2.5V.

Truth Table I—Read/Write and Enable Control^(1,2,3)

$\overline{OE}$	CLK	$\overline{CE}_0$	CE_1	$\overline{UB}$	$\overline{LB}$	$R/\overline{W}$	Upper Byte I/O ₉₋₁₈	Lower Byte I/O ₀₋₈	MODE
X	↑	L	H	H	H	X	High-Z	High-Z	All Bytes Deselected
X	↑	L	H	H	L	L	High-Z	D _N	Write to Lower Byte Only
X	↑	L	H	L	H	L	D _N	High-Z	Write to Upper Byte Only
X	↑	L	H	L	L	L	D _N	D _N	Write to Both Bytes
L	↑	L	H	H	L	H	High-Z	D _{OUT}	Read Lower Byte Only
L	↑	L	H	L	H	H	D _{OUT}	High-Z	Read Upper Byte Only
L	↑	L	H	L	L	H	D _{OUT}	D _{OUT}	Read Both Bytes
H	↑	L	H	L	L	X	High-Z	High-Z	Outputs Disabled

NOTES:

- "H" = VIH, "L" = VIL, "X" = Don't Care.
- $\overline{ADS}$, $\overline{CNTEN}$, $\overline{CNTRST}$ = VIH.
- $\overline{OE}$ is an asynchronous input signal.

4832 tbl 02

Truth Table II—Address Counter Control^(1,2)

Address	Previous Address	Addr Used	CLK	$\overline{\text{ADS}}$	$\overline{\text{CNTEN}}$	$\overline{\text{CNTRST}}$	I/O ⁽³⁾	MODE
X	X	0	↑	X	X	L ⁽⁴⁾	D _{IO} (0)	Counter Reset to Address 0
An	X	An	↑	L ⁽⁴⁾	X	H	D _{IO} (n)	External Address Used
An	Ap	Ap	↑	H	H	H	D _{IO} (p)	External Address Blocked—Counter disabled (Ap reused)
X	Ap	Ap + 1	↑	H	L ⁽⁵⁾	H	D _{IO} (p+1)	Counter Enabled—Internal Address generation

4832 tbl 03

NOTES:

- "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
- Read and write operations are controlled by the appropriate setting of R/W, $\overline{\text{CE}}_0$, CE₁, $\overline{\text{B}}\text{E}_n$ and $\overline{\text{O}}\text{E}$.
- Outputs are in Pipelined mode: the data out will be delayed by one cycle.
- $\overline{\text{ADS}}$ and $\overline{\text{CNTRST}}$ are independent of all other memory control signals including $\overline{\text{CE}}_0$, CE₁ and $\overline{\text{B}}\text{E}_n$
- The address counter advances if $\overline{\text{CNTEN}}$ = V_{IL} on the rising edge of CLK, regardless of all other memory control signals including $\overline{\text{CE}}_0$, CE₁, $\overline{\text{B}}\text{E}_n$.

Recommended Operating Temperature and Supply Voltage^(1,2)

Grade	Ambient Temperature	GND	V _{DD}
Commercial	0°C to +70°C	0V	3.3V ± 150mV
Industrial	-40°C to +85°C	0V	3.3V ± 150mV

4832 tbl 04

NOTES:

- Industrial temperature: for specific speeds, packages and powers contact your sales office.
- This is the parameter T_A. This is the "instant on" case temperature.

Recommended DC Operating Conditions with V_{DDQ} at 2.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Core Supply Voltage	3.15	3.3	3.45	V
V _{DDQ}	I/O Supply Voltage ⁽³⁾	2.375	2.5	2.625	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage ⁽³⁾ (Address & Control Inputs)	1.7	—	V _{DDQ} + 125mV ⁽²⁾	V
V _{IH}	Input High Voltage - I/O ⁽³⁾	1.7	—	V _{DDQ} + 125mV ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.7	V

4832 tbl 05a

NOTES:

- V_{IL} ≥ -1.5V for pulse width less than 10 ns.
- V_{TERM} must not exceed V_{DDQ} + 125mV.
- To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{IL} (0V), and V_{DDQX} for that port must be supplied as indicated above.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	50	mA

4832 tbl 06

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{TERM} must not exceed V_{DD} + 150mV for more than 25% of the cycle time or 4ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ V_{DD} + 150mV.

Recommended DC Operating Conditions with V_{DDQ} at 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Core Supply Voltage	3.15	3.3	3.45	V
V _{DDQ}	I/O Supply Voltage ⁽³⁾	3.15	3.3	3.45	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage (Address & Control Inputs) ⁽³⁾	2.0	—	V _{DDQ} + 150mV ⁽²⁾	V
V _{IH}	Input High Voltage - I/O ⁽³⁾	2.0	—	V _{DDQ} + 150mV ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.8	V

4832 tbl 05b

NOTES:

- V_{IL} ≥ -1.5V for pulse width less than 10 ns.
- V_{TERM} must not exceed V_{DDQ} + 150mV.
- To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{IH} (3.3V), and V_{DDQX} for that port must be supplied as indicated above.

Capacitance⁽¹⁾

(TA = +25°C, F = 1.0MHz) TQFP ONLY

Symbol	Parameter	Conditions ⁽²⁾	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	8	pF
COUT ⁽³⁾	Output Capacitance	VOUT = 3dV	10.5	pF

4832 tbl 07

NOTES:

- These parameters are determined by device characterization, but are not production tested.
- 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
- COUT also references CIO.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (VDD = 3.3V ± 150mV)

Symbol	Parameter	Test Conditions	70V3389S		Unit
			Min.	Max.	
ILI	Input Leakage Current ⁽¹⁾	VDDQ = Max., VIN = 0V to VDDQ	—	10	μA
ILO	Output Leakage Current	$\overline{CE}_0 = V_{IH}$ or $CE_1 = V_{IL}$, VOUT = 0V to VDDQ	—	10	μA
VOL (3.3V)	Output Low Voltage ⁽²⁾	IOL = +4mA, VDDQ = Min.	—	0.4	V
VOH (3.3V)	Output High Voltage ⁽²⁾	IOL = -4mA, VDDQ = Min.	2.4	—	V
VOL (2.5V)	Output Low Voltage ⁽²⁾	IOL = +2mA, VDDQ = Min.	—	0.4	V
VOH (2.5V)	Output High Voltage ⁽²⁾	IOL = -2mA, VDDQ = Min.	2.0	—	V

4832 tbl 08

NOTE:

- At VDD ≤ -2.0V input leakages are undefined.
- VDDQ is selectable (3.3V/2.5V) via OPT pins. Refer to p.4 for details.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽³⁾ ($V_{DD} = 3.3V \pm 150mV$)

Symbol	Parameter	Test Condition	Version	70V3389S4 Com'l Only		70V3389S5 Com'l & Ind		70V3389S6 Com'l & Ind		Unit
				Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.	
IDD	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R = V_{IL}$, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L S	375	460	285	360	245	310	mA
			IND S	—	—	285	415	245	360	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(1)}$	COM'L S	145	190	105	145	95	125	mA
			IND S	—	—	105	175	95	150	
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}'_A = V_{IL}$ and $\overline{CE}'_B = V_{IH}^{(5)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L S	265	325	190	260	175	225	mA
			IND S	—	—	190	300	175	260	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{DD} - 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0^{(2)}$	COM'L S	6	15	6	15	6	15	mA
			IND S	—	—	6	30	6	30	
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}'_A \leq 0.2V$ and $\overline{CE}'_B \geq V_{DD} - 0.2V^{(5)}$ $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$, Active Port, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L S	265	325	180	260	170	225	mA
			IND S	—	—	180	300	170	260	

4832 tbl 09

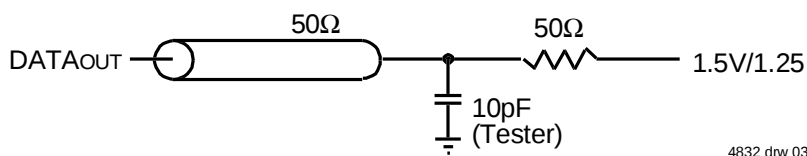
NOTES:

- At $f = f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of $1/t_{cyc}$, using "AC TEST CONDITIONS" at input levels of GND to 3V.
- $f = 0$ means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{DD} = 3.3V$, $T_A = 25^\circ C$ for Typ, and are not production tested. $I_{DD} \text{ at } f=0 = 120mA$ (Typ).
- $\overline{CE}_X = V_{IL}$ means $\overline{CE}_{0X} = V_{IL}$ and $CE_{1X} = V_{IH}$
 $\overline{CE}_X = V_{IH}$ means $\overline{CE}_{0X} = V_{IH}$ or $CE_{1X} = V_{IL}$
 $\overline{CE}_X \leq 0.2V$ means $\overline{CE}_{0X} \leq 0.2V$ and $CE_{1X} \geq V_{CC} - 0.2V$
 $\overline{CE}_X \geq V_{CC} - 0.2V$ means $\overline{CE}_{0X} \geq V_{CC} - 0.2V$ or $CE_{1X} \leq 0.2V$
 "X" represents "L" for left port or "R" for right port.

AC Test Conditions

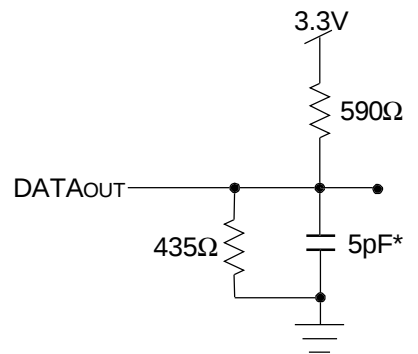
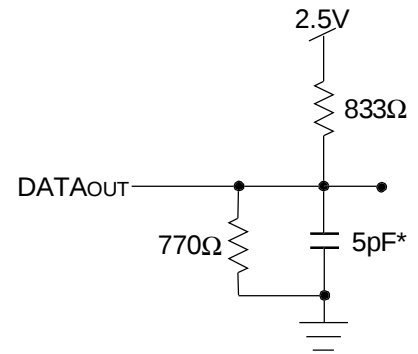
Input Pulse Levels (Address & Controls)	GND to 3.0V/GND to 2.35V
Input Pulse Levels (I/Os)	GND to 3.0V/GND to 2.35V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V/1.25V
Output Reference Levels	1.5V/1.25V
Output Load	Figures 1, 2, and 3

4832 tbl 10



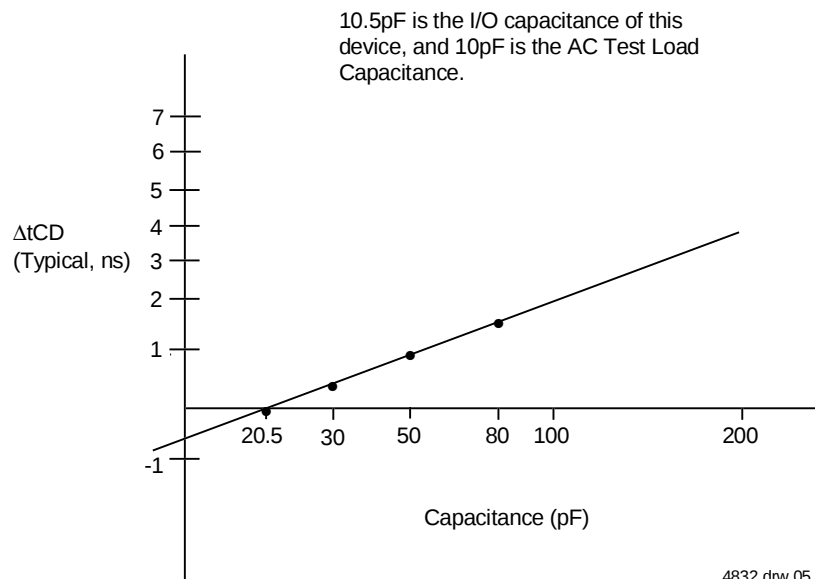
4832 drw 03

Figure 1. AC Output Test load.



4832 drw 04

Figure 2. Output Test Load
(For tckLZ, tckHZ, tolZ, and toHZ).
*Including scope and jig.



4832 drw 05

Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)^(1,2)

(V_{DD} = 3.3V ± 150mV, T_A = 0°C to +70°C)

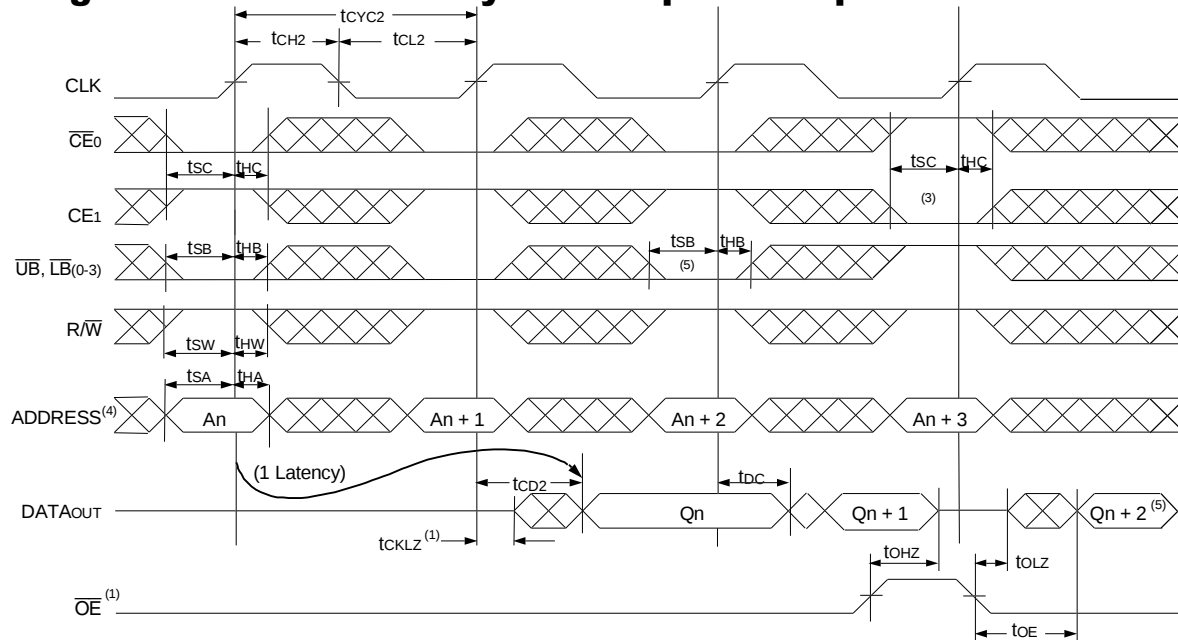
Symbol	Parameter	70V3389S4 Com'l Only		70V3389S5 Com'l & Ind		70V3389S6 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{CYC2}	Clock Cycle Time (Pipelined)	7.5	—	10	—	12	—	ns
t _{CH2}	Clock High Time (Pipelined)	3	—	4	—	5	—	ns
t _{CL2}	Clock Low Time (Pipelined)	3	—	4	—	5	—	ns
t _R	Clock Rise Time	—	3	—	3	—	3	ns
t _F	Clock Fall Time	—	3	—	3	—	3	ns
t _{SA}	Address Setup Time	1.8	—	2.0	—	2.0	—	ns
t _{HA}	Address Hold Time	0.7	—	0.7	—	1.0	—	ns
t _{SC}	Chip Enable Setup Time	1.8	—	2.0	—	2.0	—	ns
t _{HC}	Chip Enable Hold Time	0.7	—	0.7	—	1.0	—	ns
t _{SB}	Byte Enable Setup Time	1.8	—	2.0	—	2.0	—	ns
t _{HB}	Byte Enable Hold Time	0.7	—	0.7	—	1.0	—	ns
t _{SW}	R/ $\overline{W}$ Setup Time	1.8	—	2.0	—	2.0	—	ns
t _{HW}	R/ $\overline{W}$ Hold Time	0.7	—	0.7	—	1.0	—	ns
t _{SD}	Input Data Setup Time	1.8	—	2.0	—	2.0	—	ns
t _{HD}	Input Data Hold Time	0.7	—	0.7	—	1.0	—	ns
t _{SAD}	$\overline{ADS}$ Setup Time	1.8	—	2.0	—	2.0	—	ns
t _{HAD}	$\overline{ADS}$ Hold Time	0.7	—	0.7	—	1.0	—	ns
t _{SCN}	$\overline{CNTEN}$ Setup Time	1.8	—	2.0	—	2.0	—	ns
t _{HCN}	$\overline{CNTEN}$ Hold Time	0.7	—	0.7	—	1.0	—	ns
t _{SRST}	$\overline{CNTRST}$ Setup Time	1.8	—	2.0	—	2.0	—	ns
t _{HRST}	$\overline{CNTRST}$ Hold Time	0.7	—	0.7	—	1.0	—	ns
t _{OE} ⁽¹⁾	Output Enable to Data Valid	—	4	—	5	—	6	ns
t _{OLZ}	Output Enable to Output Low-Z	0	—	0	—	0	—	ns
t _{OHZ}	Output Enable to Output High-Z	1	4	1	4.5	1	5	ns
t _{CD2}	Clock to Data Valid (Pipelined)	—	4.2	—	5	—	6	ns
t _{DC}	Data Output Hold After Clock High	1	—	1	—	1	—	ns
t _{CKHZ}	Clock High to Output High-Z	1	3	1	4.5	1.5	6	ns
t _{CKLZ}	Clock High to Output Low-Z	1	—	1	—	1	—	ns
Port-to-Port Delay								
t _{CO}	Clock-to-Clock Offset	6	—	8	—	10	—	ns

NOTES:

1. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ($\overline{OE}$).
2. These values are valid for either level of V_{DDQ} (3.3V/2.5V). See page 4 for details on selecting the desired I/O voltage levels for each port.

4830 tbl 11

Timing Waveform of Read Cycle for Pipelined Operation⁽²⁾

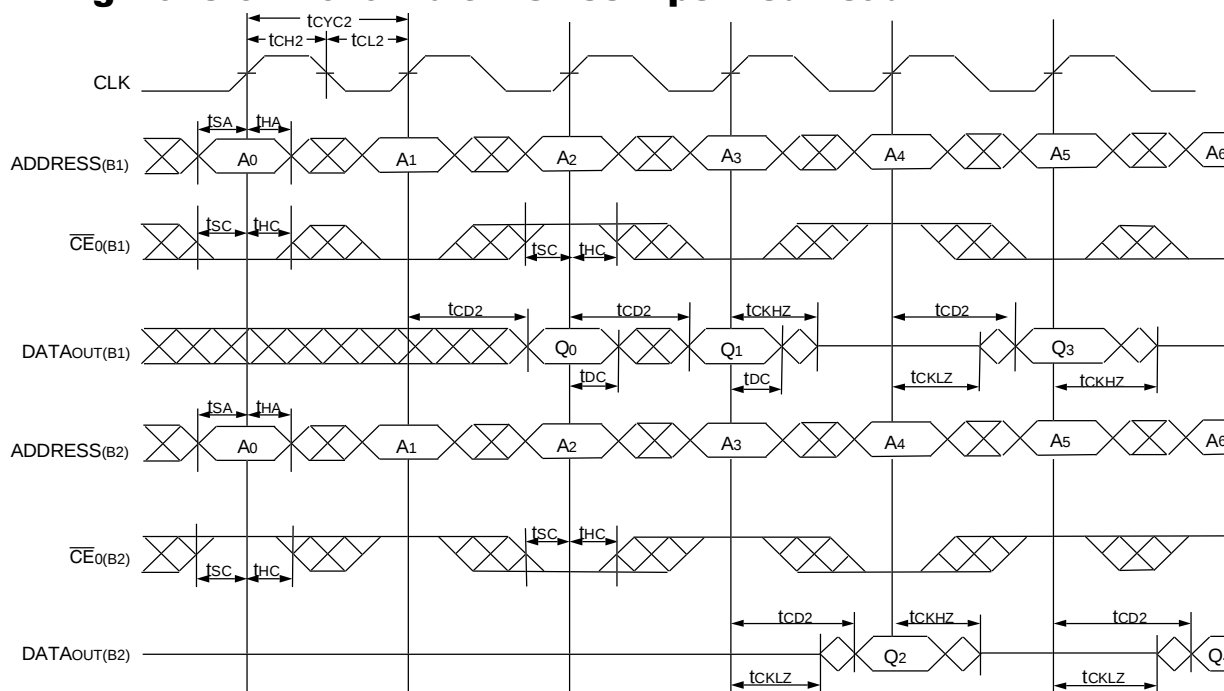


NOTES:

1. $\overline{OE}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
2. $\overline{ADS} = V_{IL}$, $\overline{CNTEN}$ and $\overline{CNTRST} = V_{IH}$.
3. The output is disabled (High-Impedance state) by $\overline{CE}_0 = V_{IH}$, $CE_1 = V_{IL}$, $\overline{UB}$, $\overline{LB} = V_{IH}$ following the next rising edge of the clock. Refer to Truth Table 1.
4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. If $\overline{UB}$ or $\overline{LB}$ was HIGH, then the appropriate Byte of DATAout for Q_{n+2} would be disabled (High-Impedance state).

4832 dnr 06

Timing Waveform of a Multi-Device Pipelined Read^(1,2)

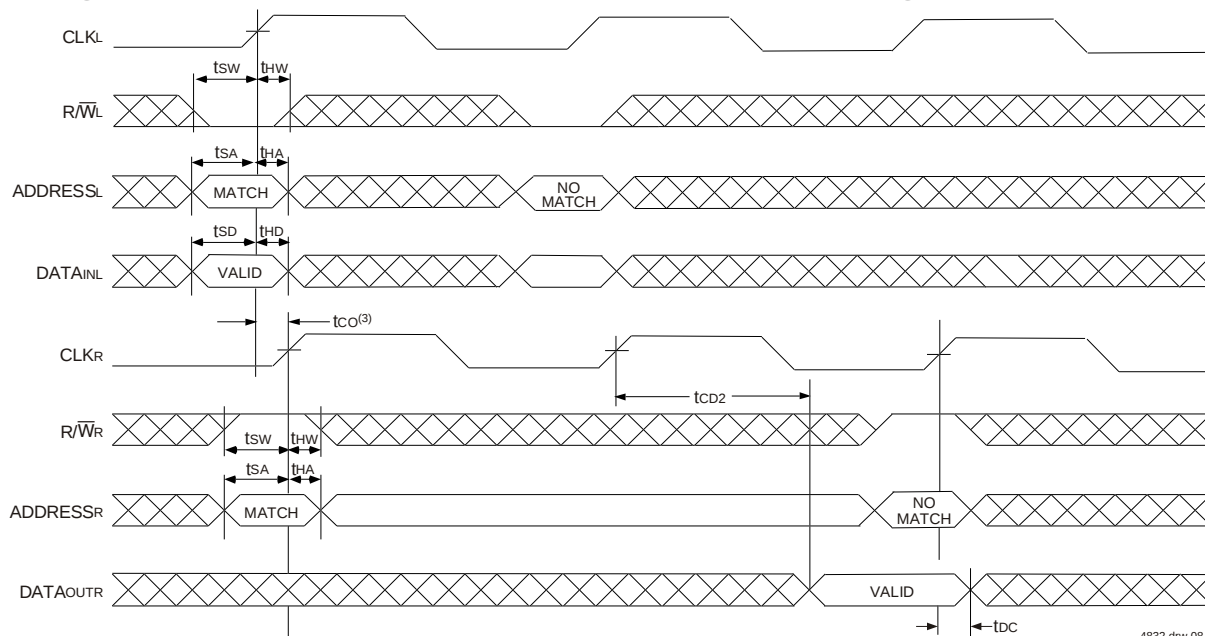


NOTES:

1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70V3389 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. $\overline{UB}$, $\overline{LB}$, $\overline{OE}$, and $\overline{ADS} = V_{IL}$; $CE_1(B1)$, $CE_1(B2)$, $R/\overline{W}$, $\overline{CNTEN}$, and $\overline{CNTRST} = V_{IH}$.

4832 dnr 07

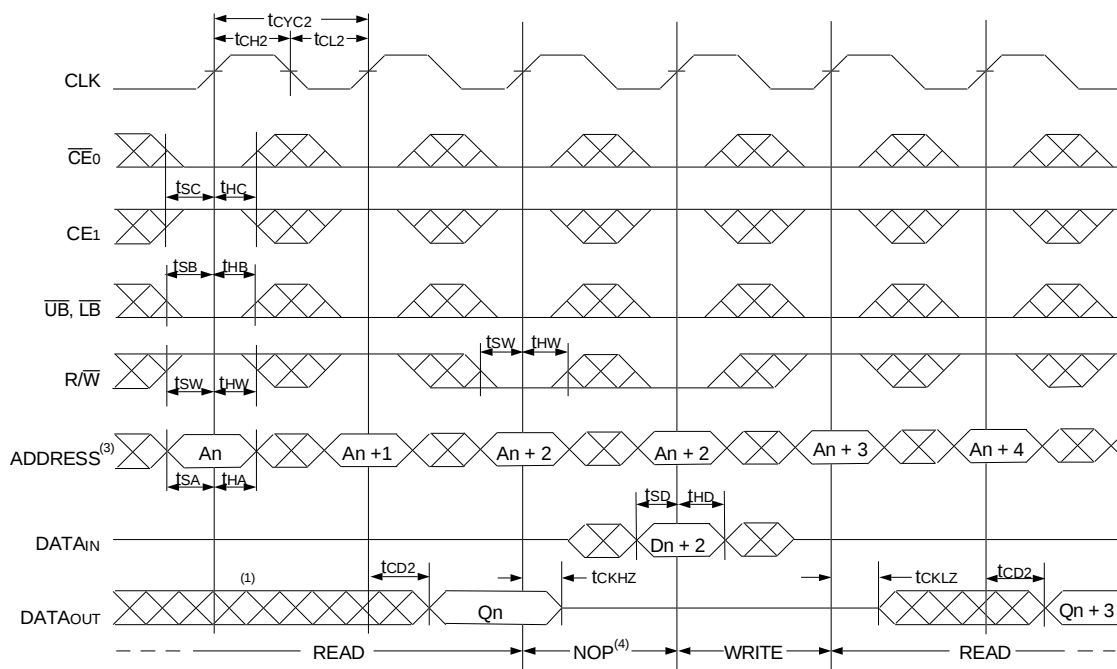
Timing Waveform of Left Port Write to Pipelined Right Port Read^(1,2)



NOTES:

1. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS} = V_{IL}$; $\overline{CE_1}$, $\overline{CNTEN}$, and $\overline{CNTRST} = V_{IH}$.
2. $\overline{OE} = V_{IL}$ for the Right Port, which is being read from. $\overline{OE} = V_{IH}$ for the Left Port, which is being written to.
3. If $t_{CO} \leq$ minimum specified, then data from right port read is not valid until following right port clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + 2 \text{ tCYC2} + t_{CD2}$). If $t_{CO} >$ minimum, then data from right port read is available on first right port clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + t_{CYC} + t_{CD2}$).

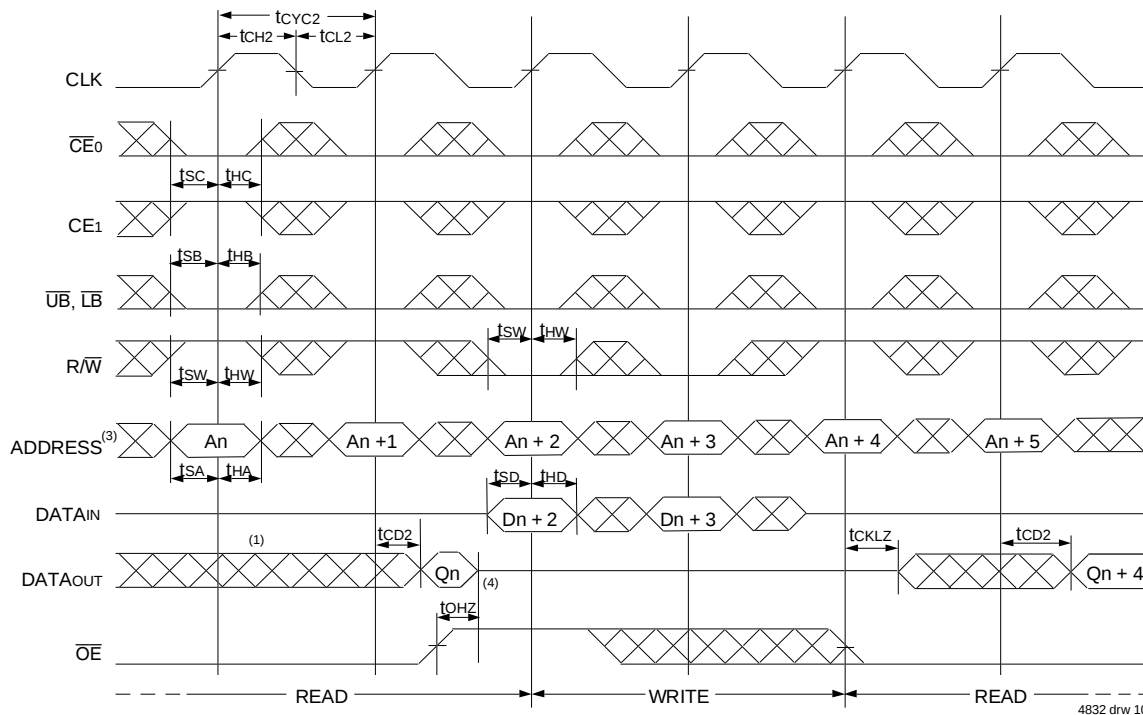
Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)⁽²⁾



NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS} = V_{IL}$; $\overline{CE_1}$, $\overline{CNTEN}$, and $\overline{CNTRST} = V_{IH}$. "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

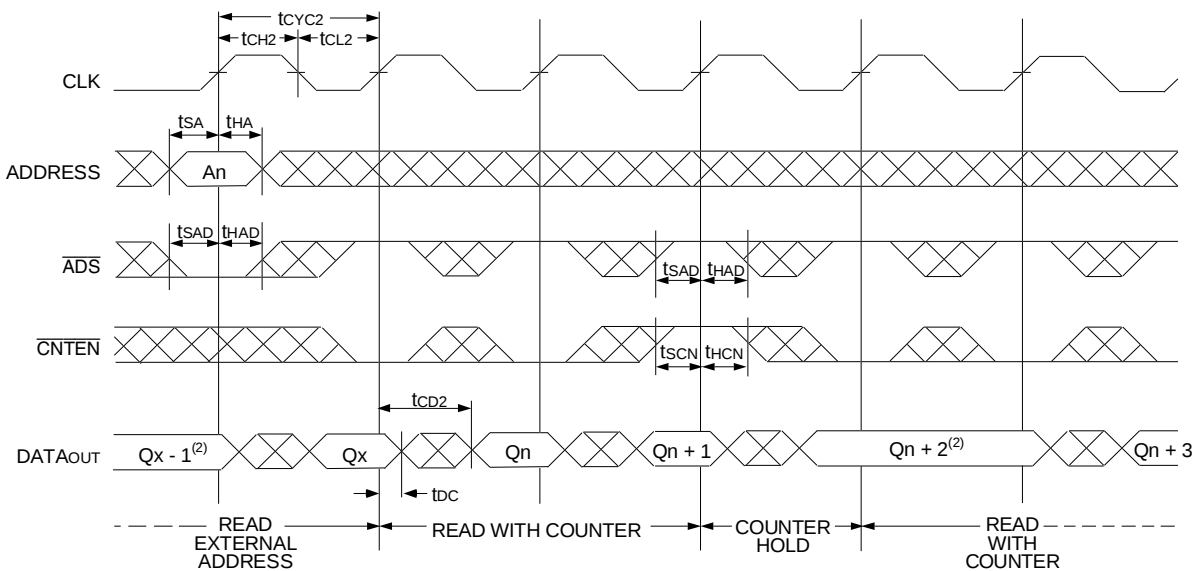
Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ Controlled)⁽²⁾



NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE0}$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS} = V_{IL}$; $\overline{CE1}$, $\overline{CNTEN}$, and $\overline{CNTRST} = V_{IH}$.
3. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.

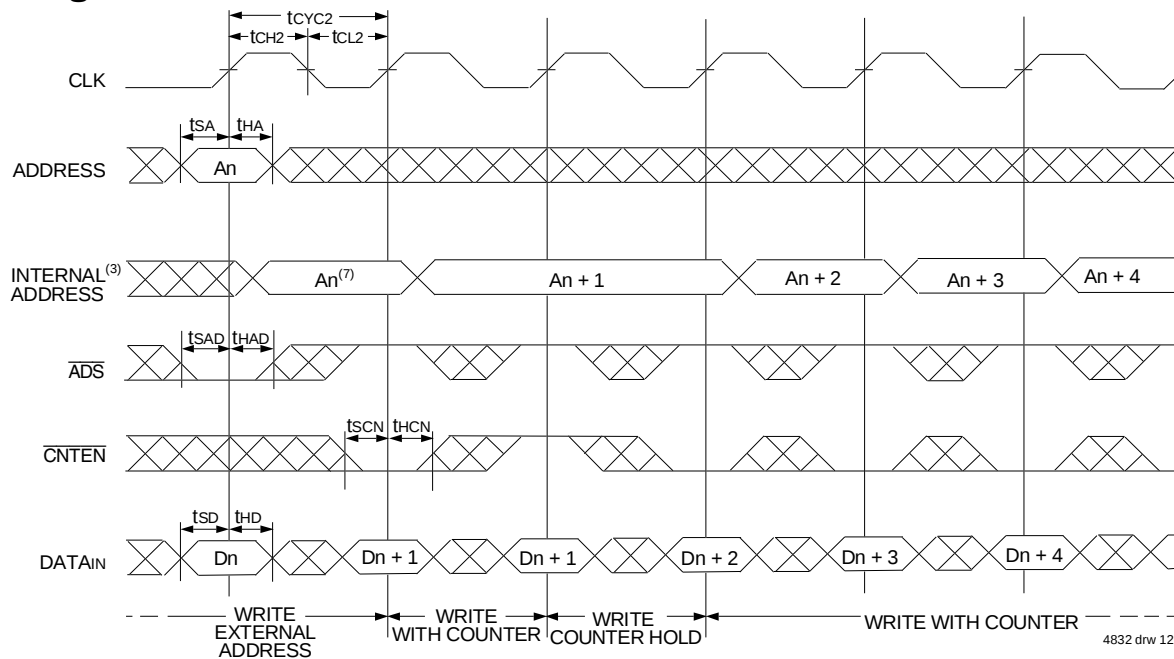
Timing Waveform of Pipelined Read with Address Counter Advance⁽¹⁾



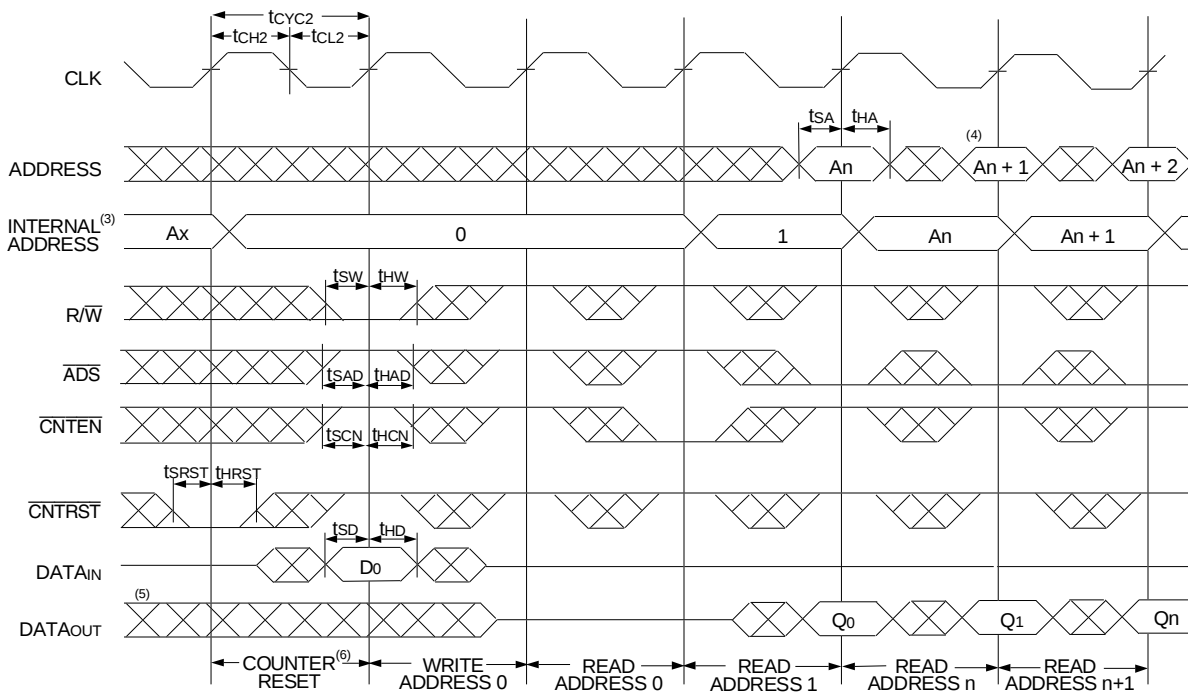
NOTES:

1. $\overline{CE0}$, $\overline{OE}$, $\overline{UB}$, $\overline{LB} = V_{IL}$; $\overline{CE1}$, $\overline{R/W}$, and $\overline{CNTRST} = V_{IH}$.
2. If there is no address change via $\overline{ADS} = V_{IL}$ (loading a new address) or $\overline{CNTEN} = V_{IL}$ (advancing the address), i.e. $\overline{ADS} = V_{IH}$ and $\overline{CNTEN} = V_{IH}$, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance⁽¹⁾



Timing Waveform of Counter Reset⁽²⁾



NOTES:

1. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, and $R/\overline{W}$ = V_{IL} ; CE_1 and $\overline{CNTRST}$ = V_{IH} .
2. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$ = V_{IL} ; CE_1 = V_{IH} .
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS}$ = V_{IL} and equals the counter output when $\overline{ADS}$ = V_{IH} .
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset cycle: ADDR 0 will be accessed. Extra cycles are shown here simply for clarification.
7. $\overline{CNTEN}$ = V_{IL} advances Internal Address from 'An' to 'An + 1'. The transition shown indicates the time required for the counter to advance. The 'An + 1' Address is written to during this cycle.

Functional Description

The IDT70V3389 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on $\overline{CE_0}$ or a LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70V3389s for depth expansion configurations. Two cycles are required with $\overline{CE_0}$ LOW and CE_1 HIGH to re-activate the outputs.

Depth and Width Expansion

The IDT70V3389 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V3389 can also be used in applications requiring expanded width, as indicated in Figure 4. Through combining the control signals, the devices can be grouped as necessary to accommodate applications needing 36-bits or wider.

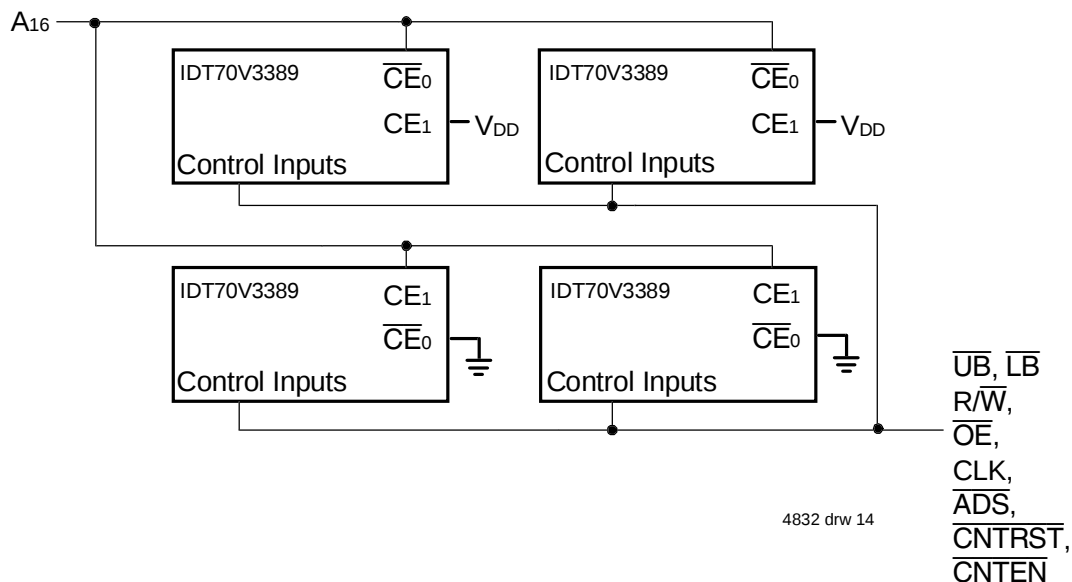


Figure 4. Depth and Width Expansion with IDT70V3389

Ordering Information

IDT	XXXXX	A	99	A	A		
	Device Type	Power	Speed	Package	Process/ Temperature Range		
						Blank I	Commercial (0°C to +70°C) Industrial (-40°C to +85°C)
						BF PRF BC	208-pin fpBGA (BF-208) 128-pin TQFP (PK-128) 256-pin BGA (BC-256)
						4 5 6	Commercial Only Commercial & Industrial Commercial & Industrial
						S	Standard Power
						70V3389	1Mbit (64K x 18-Bit) Synchronous Dual-Port RAM

} Speed in nanosecond

4832 dw 15A

Datasheet Document History

1/18/99:	Initial Public Release
3/15/99:	Page 9 Additional notes
4/28/99:	Added fpBGA package
6/8/99:	Page 2 Changed package body height from 1.5mm to 1.4mm
6/15/99:	Page 5 Deleted note 6 for Table II
7/14/99:	Page 2 Corrected pin T3 to VDDQL
8/4/99:	Page 6 Improved power numbers
10/1/99:	Upgraded speed to 133MHz, added 2.5V I/O capability
11/12/99:	Replaced IDT logo
2/28/00:	Added new BGA package, added full 2.5V interface capability
5/1/00:	Page 2 Added ball pitch
	Page 3 Renamed pins
	Page 6 Made corrections to Truth Table
	Page 9 Changed Ω numbers in figure 2
1/10/01:	Page 4 Added information to pin and pin notes
	Page 6 Increased storage temperature parameter
	Clarified TA Parameter
	Page 8 DC Electrical parameters—changed wording from "open" to "disabled"
	Removed note 7 on DC Characteristics table
	Removed Preliminary status
4/10/01:	Added Industrial Temperature Ranges and removed related notes



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