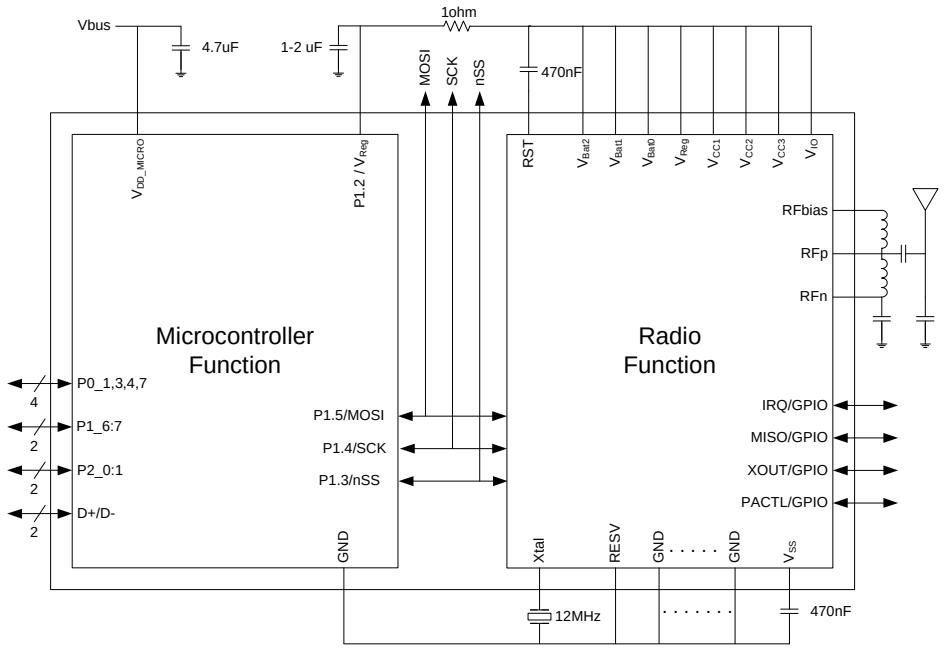
CYRF69213

Programmable Radio on Chip Low Power

PRoC™ LP Features

- USB 2.0-USB-IF certified (TID # 40000552)
- Single Device, Two Functions
  - 8-bit, Flash based USB peripheral MCU function and 2.4 GHz radio transceiver function in a single device
- Flash Based Microcontroller Function
  - M8C based 8-bit CPU, optimized for Human Interface Devices (HID) applications
  - 256 bytes of SRAM
  - 8 Kbytes of Flash memory with EEPROM emulation
  - In-System reprogrammable through D+/D– pins
  - 16-bit free running timer
  - Low power wake up timer
  - 12-bit Programmable Interval Timer with interrupts
  - Watchdog timer
- Industry-Leading 2.4 GHz Radio Transceiver Function
  - Operates in the unlicensed worldwide Industrial, Scientific and Medical (ISM) band (2.4 GHz to 2.483 GHz)
  - DSSS data rates of up to 250 Kbps
  - GFSK data rate of 1 Mbps
  - –97 dBm receive sensitivity
  - Programmable output power of up to +4 dBm
  - Auto Transaction Sequencer (ATS)
  - Framing CRC and Auto ACK
  - Received Signal Strength Indication (RSSI)
  - Automatic Gain Control (AGC)
- Component Reduction
  - Integrated 3.3 V regulator
  - Integrated pull up on D–
  - GPIOs that require no external components
  - Operates off a single crystal
- Flexible I/O
  - 2 mA source current on all GPIO pins. Configurable 8 mA or 50 mA/pin current sink on designated pins
  - Each GPIO pin supports high impedance inputs, configurable pull up, open-drain output, CMOS/TTL inputs and CMOS output
  - Maskable interrupts on all I/O pins
- USB Specification Compliance
  - Conforms to USB Specification Version 2.0
  - Conforms to USB HID Specification Version 1.1
  - Supports one Low Speed USB device address
  - Supports one control endpoint and two data end points
  - Integrated USB Transceiver
- Operating Voltage from 4.0 V to 5.5 V DC
- Operating Temperature from 0 to 70°C
- Pb-free 40-pin QFN Package
- Advanced Development Tools Based on Cypress's PSoC® Tools

Block Diagram



Contents

Applications 3
Functional Description 3
Functional Overview 3
2.4 GHz Radio Function 3
Data Transmission Modes 3
USB Microcontroller Function 3
Pinouts 4
Pin Configurations 5
PRoC LP Functional Overview 6
DDR Mode 6
SDR Mode 7
Functional Block Overview 8
2.4 GHz Radio 8
Frequency Synthesizer 8
Baseband and Framer 8
Packet Buffers 9
Auto Transaction Sequencer (ATS) 9
Interrupts 9
Clocks 9
GPIO Interface 10
Power On Reset/Low Voltage Detect 10
Power Management 10
Timers 10
USB Interface 10
Low Noise Amplifier (LNA) and Received Signal Strength Indication (RSSI) 10
SPI Interface 11
3-Wire SPI Interface 11
4-Wire SPI Interface 11
SPI Communication and Transactions 11
SPI I/O Voltage References 12
SPI Connects to External Devices 12
CPU Architecture 12
CPU Registers 13
Flags Register 13
Accumulator Register 13
Index Register 14
Stack Pointer Register 14
CPU Program Counter High Register 14
CPU Program Counter Low Register 14
Addressing Modes 15
Source Immediate 15
Source Direct 15
Source Indexed 15
Destination Direct 15
Destination Indexed 16
Destination Direct Source Immediate 16
Destination Indexed Source Immediate 16
Source Indirect Post Increment 17
Destination Indirect Post Increment 17
Instruction Set Summary 18
Memory Organization 19
Flash Program Memory Organization 19
Data Memory Organization 20
Flash 20
SROM 20
SROM Function Descriptions 21
SROM Table Read Description 24
Clocking 25
Clock Architecture Description 26
CPU Clock During Sleep Mode 32
Reset 32
Power on Reset 34
Watchdog Timer Reset 34
Sleep Mode 34
Sleep Sequence 34
Wakeup Sequence 35
Low Voltage Detect Control 37
POR Compare State 37
ECO Trim Register 38
General-Purpose I/O Ports 38
Port Data Registers 38
GPIO Port Configuration 39
GPIO Configurations for Low Power Mode: 44
Serial Peripheral Interface (SPI) 45
SPI Data Register 46
SPI Configure Register 46
Timer Registers 48
Registers 48
Interrupt Controller 51
Architectural Description 51
Interrupt Processing 52
Interrupt Latency 52
Interrupt Registers 52
USB Transceiver 56
USB Transceiver Configuration 56
VREG Control 56
USB Serial Interface Engine (SIE) 57
USB Device 57
Endpoint 0 Mode 59
Endpoint Data Buffers 60
USB Mode Tables 62
Mode Column 62
Encoding Column 62
SETUP, IN, and OUT Columns 62
Details of Mode for Differing Traffic Conditions 63
Register Summary 66
Radio Function Register Descriptions 69
Absolute Maximum Ratings 70
DC Characteristics 70
RF Characteristics 73
AC Test Loads and Waveforms for Digital Pins 74
AC Electrical Characteristics 75
Ordering Information 81
Package Diagram 82
Document History Page 84
Sales, Solutions, and Legal Information 85
Worldwide Sales and Design Support 85
Products 85
PSoC Solutions 85

Applications

The CYRF69213 PRoC LP Low Speed is targeted for the following applications:

- USB Bridge for Human Interface Devices (HID)
  - Wireless mice
  - Wireless keyboards
  - Remote controls
  - Gaming applications
- USB Bridge for General Purpose Applications
  - Consumer electronics
  - Industrial applications
  - White goods
  - Home automation
  - Personal health

Functional Description

PRoC LP devices are integrated radio and microcontroller functions in the same package to provide a dual role single-chip solution.

Communication between the microcontroller and the radio is via the SPI interface between both functions.

Functional Overview

The CYRF69213 is a complete Radio System-on-Chip device, providing a complete RF system solution with a single device and a few discrete components. The CYRF69213 is designed to implement low cost wireless systems operating in the worldwide 2.4 GHz Industrial, Scientific, and Medical (ISM) frequency band (2.400 GHz–2.4835 GHz).

2.4 GHz Radio Function

The radio meets the following world wide regulatory requirements:

- Europe
  - ETSI EN 301 489-1 V1.4.1
  - ETSI EN 300 328-1 V1.3.1
- North America
  - FCC CFR 47 Part 15
- Japan
  - ARIB STD-T66

Data Transmission Modes

The radio supports four different data transmission modes:

- In GFSK mode, data is transmitted at 1 Mbps without any DSSS
- In 8DR mode, 1 byte is encoded in each PN code symbol transmitted
- In DDR mode, 2 bits are encoded in each PN code symbol transmitted
- In SDR mode, a single bit is encoded in each PN code symbol transmitted

Both 64-chip and 32-chip data PN codes are supported. The four data transmission modes apply to the data after the Start of Packet (SOP). In particular, the packet length, data and CRC are all sent in the same mode.

USB Microcontroller Function

The microcontroller function is based on the powerful CYRF69213 microcontroller. It is an 8-bit Flash programmable microcontroller with integrated low speed USB interface.

The microcontroller has up to 14 GPIO pins to support USB, PS/2 and other applications. Each GPIO port supports high impedance inputs, configurable pull up, open drain output, CMOS/TTL inputs and CMOS output. Up to two pins support programmable drive strength of up to 50 mA. Additionally each I/O pin can be used to generate a GPIO interrupt to the microcontroller. Each GPIO port has its own GPIO interrupt vector with the exception of GPIO Port 0.

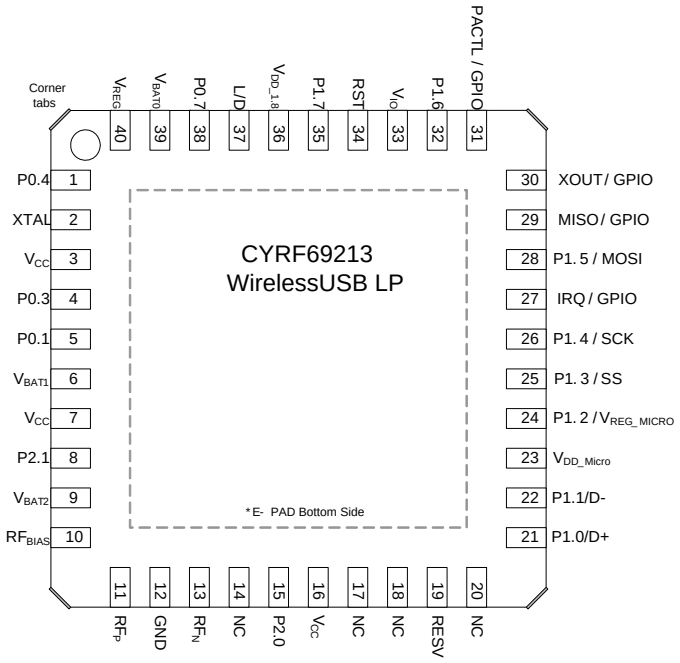
The microcontroller features an internal oscillator. With the presence of USB traffic, the internal oscillator can be set to precisely tune to USB timing requirements (24 MHz ± 1.5%).

The PRoC LP has up to 8 Kbytes of Flash for user's firmware code and up to 256 bytes of RAM for stack space and user variables.

The PRoC LP includes a Watchdog timer, a vectored interrupt controller, a 12-bit programmable interval timer with configurable 1 ms interrupt and a 16-bit free running timer with capture registers.

Pinouts

Figure 1. 40-pin QFN pinout



Pin Configurations

Pin	Name	Function
1	P0.4	Individually configured GPIO
2	Xtal_in	12 MHz Crystal. External clock in
3, 7, 16	V_{CC}	Connected to pin 24 via 0.047 µF capacitor
4	P0.3	Individually configured GPIO
5	P0.1	Individually configured GPIO
6, 9, 39	V_{bat}	Connected to pin 24 via 0.047 µFshunt capacitor
8	P2.1	GPIO. Port 2 Bit 1
10	RF Bias	RF pin voltage reference
11	RF_p	Differential RF input to/from antenna
12	GND	Ground
13	RF_n	Differential RF to/from antenna
14, 17, 18, 20, 36	NC	
15	P2.0	GPIO. Port 2 Bit 0
19	RESV	Reserved. Must connect to GND
21	P1.0 / D+	GPIO 1.0 / Low speed USB I/O
22	P1.1 / D–	GPIO 1.1 / Low speed USB I/O
23	V_{DD_micro}	4.0–5.5 for 12 MHz CPU/4.75–5.5 for 24 MHz CPU
24	P1.2 / V_{REG}	Must be configured as 3.3 V output. It must have a 1–2 µF output capacitor
25	P1.3 / nSS	Slave select SPI Pin
26	P1.4 / SCK	Serial Clock Pin from MCU function to radio function
27	IRQ	Interrupt output, configure high/low or GPIO
28	P1.5 / MOSI	Master Out Slave In
29	MISO	Master In Slave Out, from radio function. Can be configured as GPIO
30	XOUT	Bufferd CLK, PACTL_n or GPIO
31	PACTL	Control for external PA or GPIO
32	P1.6	GPIO. Port 1 Bit 6
33	V_{IO}	I/O interface voltage. Connected to pin 24 via 0.047 µF
34	Reset	Radio Reset. Connected to V_{DD} via 0.47 µF capacitor or to microcontroller GPIO pin. Must have a RESET = HIGH event the very first time power is applied to the radio otherwise the state of the radio function control registers is unknown
35	P1.7	GPIO. Port 1 Bit 7
36	$V_{DD_1.8}$	Regulated logic bypass. Connected via 0.47 µF to GND
37	L/D	Connected to GND
38	P0.7	GPIO. Port 0 Bit 7
40	V_{reg}	Connected to pin 24
41	E-pad	Must be connected to GND
42	Corner Tabs	Do not connect corner tabs

PRoC LP Functional Overview

The SoC is designed to implement wireless device links operating in the worldwide 2.4 GHz ISM frequency band. It is intended for systems compliant with worldwide regulations covered by ETSI EN 301 489-1 V1.41, ETSI EN 300 328-1 V1.3.1 (Europe), FCC CFR 47 Part 15 (USA and Industry Canada) and TELEC ARIB_T66_March, 2003 (Japan).

The SoC contains a 2.4 GHz 1 Mbps GFSK radio transceiver, packet data buffering, packet framer, DSSS baseband controller, Received Signal Strength Indication (RSSI), and SPI interface for data transfer and device configuration.

The radio supports 98 discrete 1 MHz channels (regulations may limit the use of some of these channels in certain jurisdictions). In DSSS modes the baseband performs DSSS spreading/despreading, while in GFSK Mode (1 Mb/s - GFSK) the baseband performs Start of Frame (SOF), End of Frame (EOF) detection and CRC16 generation and checking. The baseband may also be configured to automatically transmit Acknowledge (ACK) handshake packets whenever a valid packet is received.

When in receive mode, with packet framing enabled, the device is always ready to receive data transmitted at any of the supported bit rates, except SDR, enabling the implementation of mixed-rate systems in which different devices use different data rates. This also enables the implementation of dynamic data rate systems, which use high data rates at shorter distances and/or in a low moderate interference environment, and change to lower data rates at longer distances and/or in high interference environments.

The MCU function is an 8-bit Flash programmable microcontroller with integrated low speed USB interface. The instruction set has been optimized specifically for USB operations, although it can be used for a variety of other embedded applications.

The MCU function has up to eight Kbytes of Flash for user's code and up to 256 bytes of RAM for stack space and user variables.

In addition, the MCU function includes a Watchdog timer, a vectored interrupt controller, a 16-bit Free-Running Timer, and 12-bit Programmable Interrupt Timer.

The MCU function supports in-system programming by using the D+ and D– pins as the serial programming mode interface. The programming protocol is not USB.

DDR Mode

Table 1. DDR Mode

Register	Value	Description
TX_CFG_ADR	0X16	32 chip PN Code, DDR, PA = 6
RX_CFG_ADR	0X4B	AGC is enabled. LNA and attenuator are disabled. Fast turn around is disabled, the device uses high side receive injection and Hi-Lo is disabled. Overwrite to receive buffer is enabled and the RX buffer is configured to receive eight bytes maximum.
XACT_CFG_ADR	0X05	AutoACK is disabled. Forcing end state is disabled. The device is configured to transition to Idle mode after a Receive or Transmit. ACK timeout is set to 128 µs.
FRAMING_CFG_ADR	0X00	All SOP and framing features are disabled. Disable LEN_EN=0 if EOP is needed.
TX_OVERRIDE_ADR	0X04	Disable Transmit CRC-16.
RX_OVERRIDE_ADR	0X14	The receiver rejects packets with a zero seed. The Rx CRC-16 Checker is disabled and the receiver accepts bad packets that do not match the seed in CRC_seed registers. Basically this helps in communication with the first generation radio that does not have CRC capabilities.
ANALOG_CTRL_ADR	0X01	Set ALL SLOW. When set, the synthesizer settle time for all channels is the same as the slow channels in the first generation radio.
DATA32_THOLD_ADR	0X03	Sets the number of allowed corrupted bits to 3.
EOP_CTRL_ADR	0x01	Sets the number of consecutive symbols for non correlation to detect end of packet.
PREAMBLE_ADR	0xAAAA05	AAAA are the two preamble bytes.Other Bytes can also be written into the preamble register file. The number of preamble bytes to be sent should be >4.

SDR Mode

Table 2. SDR Mode

Register	Value	Description
TX_CFG_ADR	0X3E	64 chip PN code, SDR mode, PA = 6.
RX_CFG_ADR	0X4B	AGC is enabled. LNA and attenuator are disabled. Fast turn around is disabled, the device uses high side receive injection and Hi-Lo is disabled. Overwrite to receive buffer is enabled and RX buffer is configured to receive eight bytes maximum. Enables RXOW to allow new packets to be loaded into the receive buffer. This also enables the VALID bit which is used by the first generation radio's error correction firmware.
XACT_CFG_ADR	0X05	AutoACK is disabled. Forcing end state is disabled. The device is configured to transition to Idle mode after Receive or Transmit. ACK timeout is set to 128 µs.
FRAMING_CFG_ADR	0X00	All SOP and framing features are disabled. Disable LEN_EN=0 if EOP is needed.
TX_OVERRIDE_ADR	0X04	Disable Transmit CRC-16.
RX_OVERRIDE_ADR	0X14	The receiver rejects packets with a zero seed. The RX CRC-16 checker is disabled and the receiver accepts bad packets that do not match the seed in the CRC_seed registers. Basically this helps in communication with the first generation radio that does not have CRC capabilities.
ANALOG_CTRL_ADR	0X01	Set ALL SLOW. When set, the synthesizer settle time for all channels is the same as the slow channels in the first generation radio, for manual ACK consistency
DATA64_THOLD_ADR	0X07	Sets the number of allowed corrupted bits to 7 which is close to the recommended 12% value.
EOP_CTRL_ADR	0xA1	Sets the number of consecutive symbols for non correlation to detect end of packet.
PREAMBLE_ADR	0xAAAA09	AAAA are the two preamble bytes. Any other byte can also be written into the preamble register file. The number of preamble bytes to be sent should be >8.

Functional Block Overview

All the blocks that make up the PRoC LP are presented here.

2.4 GHz Radio

The radio transceiver is a dual conversion low IF architecture optimized for power and range/robustness. The radio employs channel-matched filters to achieve high performance in the presence of interference. An integrated Power Amplifier (PA) provides up to +4 dBm transmit power, with an output power control range of 34 dB in 7 steps. The supply current of the device is reduced as the RF output power is reduced.

Table 3. Internal PA Output Power Step Table

PA Setting	Typical Output Power (dBm)
7	+4
6	0
5	–5
4	–10
3	–15
2	–20
1	–25
0	–30

Frequency Synthesizer

Before transmission or reception may commence, it is necessary for the frequency synthesizer to settle. The settling time varies depending on channel; 25 fast channels are provided with a maximum settling time of 100 µs.

The ‘fast channels’ (<100 µs settling time) are every third frequency, starting at 2400 MHz up to and including 2472 MHz (for example, 0,3,6,9…....69 & 72).

Baseband and Framer

The baseband and framer blocks provide the DSSS encoding and decoding, SOP generation and reception and CRC16 generation and checking, and EOP detection and length field.

Data Rates and Data Transmission Modes

The SoC supports four different data transmission modes:

- In GFSK mode, data is transmitted at 1 Mbps, without any DSSS.
- In 8DR mode, 8 bits are encoded in each DATA_CODE_ADR derived code symbol transmitted.
- In DDR mode, 2-bits are encoded in each DATA_CODE_ADR derived code symbol transmitted. (As in the CYWUSB6934 DDR mode).
- In SDR mode, 1 bit is encoded in each DATA_CODE_ADR derived code symbol transmitted. (As in the CYWUSB6934 standard modes.)

Both 64-chip and 32-chip DATA_CODE_ADR codes are supported. The four data transmission modes apply to the data after the SOP. In particular the length, data, and CRC16 are all sent in the same mode. In general, lower data rates reduces packet error rate in any given environment.

By combining the DATA_CODE_ADR code lengths and data transmission modes described above, the CYRF69213 IC supports the following data rates:

- 1000 kbps (GFSK)
- 250 kbps (32-chip 8DR)
- 125 kbps (64-chip 8DR)
- 62.5 kbps (32-chip DDR)
- 31.25 kbps (64-chip DDR)
- 15.625 kbps (64-chip SDR)

Lower data rates typically provide longer range and/or a more robust link.

Link Layer Modes

The CYRF69213 IC device supports the following data packet framing features:

SOP – Packets begin with a 2-symbol Start of Packet (SOP) marker. This is required in GFSK and 8DR modes, but is optional in DDR mode and is not supported in SDR mode; if framing is disabled then an SOP event is inferred whenever two successive correlations are detected. The SOP_CODE_ADR code used for the SOP is different from that used for the ‘body’ of the packet, and if desired may be a different length. SOP must be configured to be the same length on both sides of the link.

EOP – There are two options for detecting the end of a packet. If SOP is enabled, then a packet length field may be enabled. GFSK and 8DR must enable the length field. This is the first 8 bits after the SOP symbol, and is transmitted at the payload data rate. If the length field is enabled, an End of Packet (EOP) condition is inferred after reception of the number of bytes defined in the length field, plus two bytes for the CRC16 (if enabled—see below). The alternative to using the length field is to infer an EOP condition from a configurable number of successive non correlations; this option is not available in GFSK mode and is only recommended when using SDR mode.

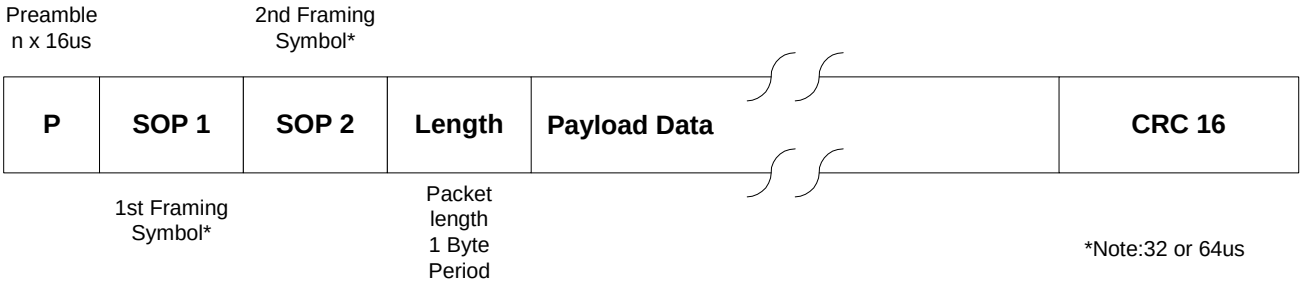
CRC16 – The device may be configured to append a 16-bit CRC16 to each packet. The CRC16 uses the USB CRC polynomial with the added programmability of the seed. If enabled, the receiver verifies the calculated CRC16 for the payload data against the received value in the CRC16 field. The starting value for the CRC16 calculation is configurable, and the CRC16 transmitted may be calculated using either the loaded seed value or a zero seed; the received data CRC16 is checked against both the configured and zero CRC16 seeds.

CRC16 detects the following errors:

- Any one bit in error
- Any two bits in error (irrespective of how far apart, which column, and so on)
- Any odd number of bits in error (irrespective of the location)
- An error burst as wide as the checksum itself

Figure 2 on page 9 shows an example packet with SOP, CRC16 and lengths fields enabled.

Figure 2. Example Default Packet Format



Packet Buffers

Packet data and configuration registers are accessed through the SPI interface. All configuration registers are directly addressed through the address field in the SPI packet. Configuration registers are provided to allow configuration of DSSS PN codes, data rate, operating mode, interrupt masks, interrupt status, and others.

Packet Buffers

All data transmission and reception uses the 16-byte packet buffers—one for transmission and one for reception.

The transmit buffer allows a complete packet of up to 16 bytes of payload data to be loaded in one burst SPI transaction.This is then transmitted with no further MCU intervention. Similarly, the receive buffer allows an entire packet of payload data up to 16 bytes to be received with no firmware intervention required until packet reception is complete.

The CYRF69213 IC supports packet length of up to 40 bytes; interrupts are provided to allow an MCU to use the transmit and receive buffers as FIFOs. When transmitting a packet longer than 16 bytes, the MCU can load 16 bytes initially, and add further bytes to the transmit buffer as transmission of data creates space in the buffer. Similarly, when receiving packets longer than 16 bytes, the MCU function must fetch received data from the FIFO periodically during packet reception to prevent it from overflowing.

Auto Transaction Sequencer (ATS)

The CYRF69213 IC provides automated support for transmission and reception of acknowledged data packets.

When transmitting a data packet, the device automatically starts the crystal and synthesizer, enters transmit mode, transmits the packet in the transmit buffer, and then automatically switches to receive mode and waits for a handshake packet — and then automatically reverts to sleep mode or idle mode when either an ACK packet is received, or a timeout period expires.

Similarly, when receiving in transaction mode, the device waits in receive mode for a valid packet to be received, then automatically transitions to transmit mode, transmits an ACK packet, and then switches back to receive mode to await the next packet. The contents of the packet buffers are not affected by the transmission or reception of ACK packets.

In each case, the entire packet transaction takes place without any need for MCU firmware action; to transmit data the MCU simply needs to load the data packet to be transmitted, set the length, and set the TX GO bit. Similarly, when receiving packets in transaction mode, firmware simply needs to retrieve the fully received packet in response to an interrupt request indicating reception of a packet.

Interrupts

The radio function provides an interrupt (IRQ) output, which is configurable to indicate the occurrence of various different events. The IRQ pin may be programmed to be either active high or active low, and be either a CMOS or open drain output. The IRQ pin can be multiplexed on the SPI if routed to an external pin.

The radio function features three sets of interrupts: transmit, receive, and system interrupts. These interrupts all share a single pin (IRQ), but can be independently enabled/disabled. In transmit mode, all receive interrupts are automatically disabled, and in receive mode all transmit interrupts are automatically disabled. However, the contents of the enable registers are preserved when switching between transmit and receive modes.

If more than one radio interrupt is enabled at any time, it is necessary to read the relevant status register to determine which event caused the IRQ pin to assert. Even when a given interrupt source is disabled, the status of the condition that would otherwise cause an interrupt can be determined by reading the appropriate status register. It is therefore possible to use the devices without making use of the IRQ pin by polling the status register(s) to wait for an event, rather than using the IRQ pin.

The microcontroller function supports 23 maskable interrupts in the vectored interrupt controller. Interrupt sources include a USB bus reset, LVR/POR, a programmable interval timer, a 1.024-ms output from the Free Running Timer, three USB endpoints, two capture timers, five GPIO Ports, three GPIO pins, two SPI, a 16-bit free running timer wrap, an internal wakeup timer, and a bus active interrupt. The wakeup timer causes periodic interrupts when enabled. The USB endpoints interrupt after a USB transaction complete is on the bus. The capture timers interrupt whenever a new timer value is saved due to a selected GPIO edge event. A total of eight GPIO interrupts support both TTL or CMOS thresholds. For additional flexibility, on the edge sensitive GPIO pins, the interrupt polarity is programmable to be either rising or falling.

Clocks

The radio function has a 12 MHz crystal (30-ppm or better) directly connected between XTAL and GND without the need for external capacitors. A digital clock out function is provided, with selectable output frequencies of 0.75, 1.5, 3, 6, or 12 MHz. This output may be used to clock an external microcontroller (MCU) or ASIC. This output is enabled by default, but may be disabled.

Following are the requirements for the crystal to be directly connected to XTAL pin and GND:

- Nominal Frequency: 12 MHz
- Operating Mode: Fundamental Mode
- Resonance Mode: Parallel Resonant
- Frequency Stability: ±30 ppm
- Series Resistance: ≤60 ohms
- Load Capacitance: 10 pF
- Drive Level:100 µW

The MCU function features an internal oscillator. With the presence of USB traffic, the internal oscillator can be set to precisely tune to USB timing requirements (24 MHz ±1.5%). The clock generator provides the 12 MHz and 24 MHz clocks that remain internal to the microcontroller.

GPIO Interface

The MCU function features up to 20 general purpose I/O (GPIO) pins to support USB, PS/2, and other applications. The I/O pins are grouped into five ports (Port 0 to 4). The pins on Port 0 and Port 1 may each be configured individually while the pins on Ports 2, 3, and 4 may only be configured as a group. Each GPIO port supports high impedance inputs, configurable pull up, open drain output, CMOS/TTL inputs, and CMOS output with up to five pins that support programmable drive strength of up to 50 mA sink current. GPIO Port 1 features four pins that interface at a voltage level of 3.3 volts. Additionally, each I/O pin can be used to generate a GPIO interrupt to the microcontroller. Each GPIO port has its own GPIO interrupt vector with the exception of GPIO Port 0. GPIO Port 0 has three dedicated pins that have independent interrupt vectors (P0.3–P0.4).

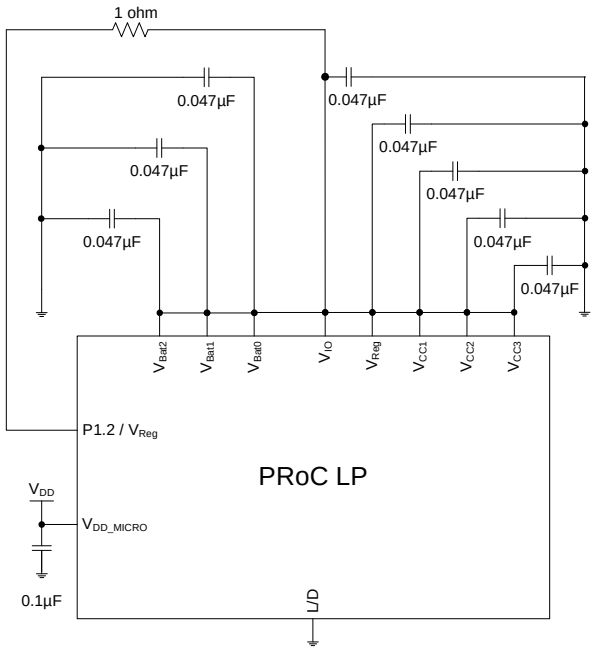
Power On Reset/Low Voltage Detect

The power on reset circuit detects logic when power is applied to the device, resets the logic to a known state, and begins executing instructions at Flash address 0x0000. When power falls below a programmable trip voltage, it generates reset or may be configured to generate interrupt. There is a low voltage detect circuit that detects when V_{CC} drops below a programmable trip voltage. It may be configurable to generate an LVD interrupt to inform the processor about the low voltage event. POR and LVD share the same interrupt. There is not a separate interrupt for each. The Watchdog timer can be used to ensure the firmware never gets stalled in an infinite loop.

Power Management

The device draws its power supply from the USB V_{bus} line. The V_{bus} supplies power to the MCU function, which has an internal 3.3 V regulator. This 3.3 V is supplied to the radio function via P1.2/V_{REG} after proper filtering as shown in Figure 3.

Figure 3. Power Management From Internal Regulator



Timers

The free-running 16-bit timer provides two interrupt sources: the programmable interval timer with 1 µs resolution and the 1.024 ms outputs. The timer can be used to measure the duration of an event under firmware control by reading the timer at the start and at the end of an event, then calculating the difference between the two values.

USB Interface

The MCU function includes an integrated USB serial interface engine (SIE) that allows the chip to easily interface to a USB host. The hardware supports one USB device address with three endpoints.

Low Noise Amplifier (LNA) and Received Signal Strength Indication (RSSI)

The gain of the receiver may be controlled directly by clearing the AGC EN bit and writing to the Low Noise Amplifier (LNA) bit of the RX_CFG_ADR register. When the LNA bit is cleared, the receiver gain is reduced by approximately 20 dB, allowing accurate reception of very strong received signals (for example when operating a receiver very close to the transmitter). An additional 20 dB of receiver attenuation can be added by setting the Attenuation (ATT) bit; this allows data reception to be limited to devices at very short ranges. Disabling AGC and enabling LNA is recommended unless receiving from a device using external PA.

The RSSI register returns the relative signal strength of the on-channel signal power.

When receiving, the device may be configured to automatically measure and store the relative strength of the signal being received as a 5-bit value. When enabled, an RSSI reading is taken and may be read through the SPI interface. An RSSI

reading is taken automatically when the start of a packet is detected. In addition, a new RSSI reading is taken every time the previous reading is read from the RSSI register, allowing the background RF energy level on any given channel to be easily measured when RSSI is read when no signal is being received. A new reading can occur as fast as once every 12 µs.

Receive Spurious Response

The transmitter may exhibit spurs around 50MHz offset at levels approximately 50dB to 60dB below the carrier power. Receivers operating at the transmit spur frequency may receive the spur if the spur level power is greater than the receive sensitivity level.

The workaround for this is to program an additional byte in the packet header which contains the transmitter channel number. After the packet is received, the channel number can be checked. If the channel number does not match the receive channel then the packet is rejected.

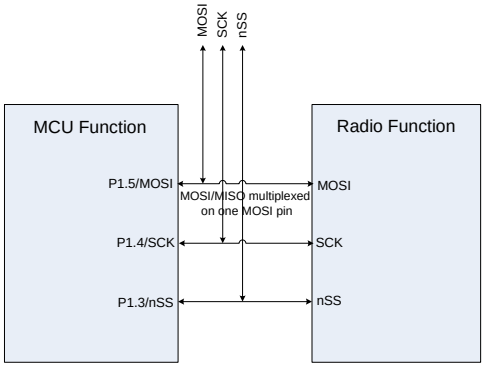
SPI Interface

The SPI interface between the MCU function and the radio function is a 3-wire SPI Interface. The three pins are MOSI (Master Out Slave In), SCK (Serial Clock), SS (Slave Select). There is an alternate 4-wire MISO Interface that requires the connection of two external pins. The SPI interface is controlled by configuring the SPI Configure Register (SICR Address: 0x3D).

3-Wire SPI Interface

The radio function receives a clock from the MCU function on the SCK pin. The MOSI pin is multiplexed with the MISO pin. Bidirectional data transfer takes place between the MCU function and the radio function through this multiplexed MOSI pin. When using this mode the user firmware should ensure that the MOSI pin on the MCU function is in a high impedance state, except when the MCU is actively transmitting data. Firmware must also control the direction of data flow and switch directions between MCU function and radio function by setting the SWAP bit [Bit 7] of the SPI Configure Register. The SS pin is asserted prior to initiating a data transfer between the MCU function and the radio function. The IRQ function may be optionally multiplexed with the MOSI pin; when this option is enabled the IRQ function is not available while the SS pin is low. When using this configuration, user firmware should ensure that the MOSI function on MCU function is in a high impedance state whenever SS is high.

Figure 4. 3-Wire SPI Mode

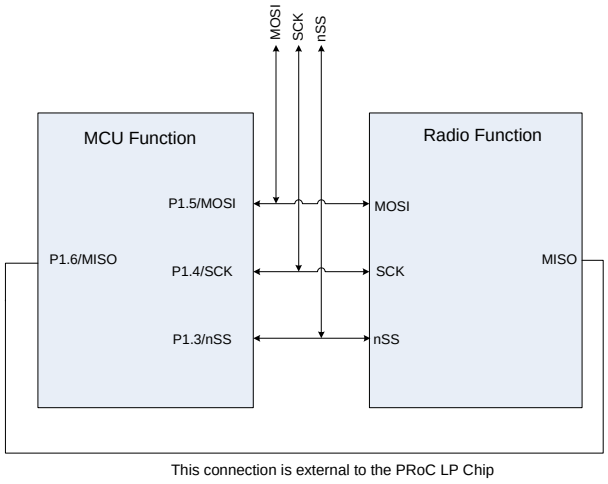


4-Wire SPI Interface

The 4-wire SPI communications interface consists of MOSI, MISO, SCK, and SS.

The device receives SCK from the MCU function on the SCK pin. Data from the MCU function is shifted in on the MOSI pin. Data to the MCU function is shifted out on the MISO pin. The active low SS pin must be asserted for the two functions to communicate. The IRQ function may be optionally multiplexed with the MOSI pin; when this option is enabled the IRQ function is not available while the SS pin is low. When using this configuration, user firmware should ensure that the MOSI function on MCU function is in a high impedance state whenever SS is high.

Figure 5. 4-WIRE SPI Mode



SPI Communication and Transactions

The SPI transactions can be single byte or multi-byte. The MCU function initiates a data transfer through a Command/Address byte. The following bytes are data bytes. The SPI transaction format is shown in Figure 6.

The DIR bit specifies the direction of data transfer. 0 = Master reads from slave. 1 = Master writes to slave.

The INC bit helps to read or write consecutive bytes from contiguous memory locations in a single burst mode operation.

If Slave Select is asserted and INC = 1, then the master MCU function reads a byte from the radio, the address is incremented by a byte location, and then the byte at that location is read, and so on. If Slave Select is asserted and INC = 0, then the MCU function reads/writes the bytes in the same register in burst mode, but if it is a register file then it reads/writes the bytes in that register file.

The SPI interface between the radio function and the MCU is not dependent on the internal 12 MHz oscillator of the radio. Therefore, radio function registers can be read from or written into while the radio is in sleep mode.

SPI I/O Voltage References

The SPI interfaces between MCU function and the radio and the IRQ and RST have a separate voltage reference V_{IO}, enabling the radio function to directly interface with the MCU function, which operates at higher supply voltage. The internal SPIO pins between the MCU function and radio function should be connected with a regulated voltage of 3.3 V (by setting [bit4] of Registers P13CR, P14CR, P15CR, and P16CR of the MCU function) and the internal 3.3 V regulator of the MCU function should be turned on.

SPI Connects to External Devices

The three SPI wires, MOSI, SCK, and SS are also drawn out of the package as external pins to allow the user to interface their own external devices (such as optical sensors and others) through SPI. The radio function also has its own SPI wires MISO and IRQ, which can be used to send data back to the MCU function or send an interrupt request to the MCU function. They can also be configured as GPIO pins.

Figure 6. SPI Transaction Format

	Byte 1			Byte 1+N
Bit#	7	6	[5:0]	[7:0]
Bit Name	DIR	INC	Address	Data

CPU Architecture

This family of microcontroller is based on a high performance, 8-bit, Harvard-architecture microprocessor. Five registers control the primary operation of the CPU core. These registers are affected by various instructions, but are not directly accessible through the register space by the user.

Table 4. CPU Registers and Register Names

Register	Register Name
Flags	CPU_F
Program Counter	CPU_PC
Accumulator	CPU_A
Stack Pointer	CPU_SP
Index	CPU_X

The 16-bit Program Counter Register (CPU_PC) allows for direct addressing of the full eight Kbytes of program memory space.

The Accumulator Register (CPU_A) is the general purpose register that holds the results of instructions that specify any of the source addressing modes.

The Index Register (CPU_X) holds an offset value that is used in the indexed addressing modes. Typically, this is used to address a block of data within the data memory space.

The Stack Pointer Register (CPU_SP) holds the address of the current top-of-stack in the data memory space. It is affected by the PUSH, POP, LCALL, CALL, RETI, and RET instructions, which manage the software stack. It can also be affected by the SWAP and ADD instructions.

The Flag Register (CPU_F) has three status bits: Zero Flag bit [1]; Carry Flag bit [2]; Supervisory State bit [3]. The Global Interrupt Enable bit [0] is used to globally enable or disable interrupts. The user cannot manipulate the Supervisory State status bit [3]. The flags are affected by arithmetic, logic, and shift operations. The manner in which each flag is changed is dependent upon the instruction being executed (for example, AND, OR, XOR). See Table 21 on page 18.

CPU Registers

Flags Register

The Flags Register can only be set or reset with logical instruction.

Table 5. CPU Flags Register (CPU_F) [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Reserved			XIO	Super	Carry	Zero	Global IE
Read/Write	–	–	–	R/W	R	RW	RW	RW
Default	0	0	0	0	0	0	1	0

Bits 7:5 Reserved

Bit 4 XIO

Set by the user to select between the register banks
0 = Bank 0
1 = Bank 1

Bit 3 Super

Indicates whether the CPU is executing user code or Supervisor Code. (This code cannot be accessed directly by the user.)
0 = User Code
1 = Supervisor Code

Bit 2 Carry

Set by CPU to indicate whether there has been a carry in the previous logical/arithmetic operation
0 = No Carry
1 = Carry

Bit 1 Zero

Set by CPU to indicate whether there has been a zero result in the previous logical/arithmetic operation
0 = Not Equal to Zero
1 = Equal to Zero

Bit 0 Global IE

Determines whether all interrupts are enabled or disabled
0 = Disabled
1 = Enabled

Note CPU_F register is only readable with explicit register address 0xF7. The *OR F, expr and AND F, expr* instructions must be used to set and clear the CPU_F bits

Accumulator Register

Table 6. CPU Accumulator Register (CPU_A)

Bit #	7	6	5	4	3	2	1	0
Field	CPU Accumulator [7:0]							
Read/Write	–	–	–	–	–	–	–	–
Default	0	0	0	0	0	0	0	0

Bits 7:0 CPU Accumulator [7:0]
8-bit data value holds the result of any logical/arithmetic instruction that uses a source addressing mode

Index Register

Table 7. CPU X Register (CPU_X)

Bit #	7	6	5	4	3	2	1	0
Field	X [7:0]							
Read/Write	–	–	–	–	–	–	–	–
Default	0	0	0	0	0	0	0	0

Bits 7:0X [7:0]
8-bit data value holds an index for any instruction that uses an indexed addressing mode

Stack Pointer Register

Table 8. CPU Stack Pointer Register (CPU_SP)

Bit #	7	6	5	4	3	2	1	0
Field	Stack Pointer [7:0]							
Read/Write	–	–	–	–	–	–	–	–
Default	0	0	0	0	0	0	0	0

Bits 7:0 Stack Pointer [7:0]
8-bit data value holds a pointer to the current top-of-stack

CPU Program Counter High Register

Table 9. CPU Program Counter High Register (CPU_PCH)

Bit #	7	6	5	4	3	2	1	0
Field	Program Counter [15:8]							
Read/Write	–	–	–	–	–	–	–	–
Default	0	0	0	0	0	0	0	0

Bits 7:0 Program Counter [15:8]
8-bit data value holds the higher byte of the program counter

CPU Program Counter Low Register

Table 10. CPU Program Counter Low Register (CPU_PCL)

Bit #	7	6	5	4	3	2	1	0
Field	Program Counter [7:0]							
Read/Write	–	–	–	–	–	–	–	–
Default	0	0	0	0	0	0	0	0

Bits 7:0 Program Counter [7:0]
8-bit data value holds the lower byte of the program counter

Addressing Modes

Examples of the different addressing modes are discussed in this section and example code is given.

Source Immediate

The result of an instruction using this addressing mode is placed in the A register, the F register, the SP register, or the X register, which is specified as part of the instruction opcode. Operand 1 is an immediate value that serves as a source for the instruction. Arithmetic instructions require two sources. Instructions using this addressing mode are two bytes in length.

Table 11. Source Immediate

Opcode	Operand 1
Instruction	Immediate Value

Examples

```
ADD   A,   7   ;In this case, the immediate value
               ;of 7 is added with the Accumulator,
               ;and the result is placed in the
               ;Accumulator.
MOV   X,   8   ;In this case, the immediate value
               ;of 8 is moved to the X register.
AND   F,   9   ;In this case, the immediate value
               ;of 9 is logically ANDed with the F
               ;register and the result is placed
               ;in the F register.
```

Source Direct

The result of an instruction using this addressing mode is placed in either the A register or the X register, which is specified as part of the instruction opcode. Operand 1 is an address that points to a location in either the RAM memory space or the register space that is the source for the instruction. Arithmetic instructions require two sources; the second source is the A register or X register specified in the opcode. Instructions using this addressing mode are two bytes in length.

Table 12. Source Direct

Opcode	Operand 1
Instruction	Source Address

Examples

```
ADD   A,   [7]     ;In this case, the value in
                   ;the RAM memory location at
                   ;address 7 is added with the
                   ;Accumulator, and the result
                   ;is placed in the Accumulator.
MOV   X,   REG[8]  ;In this case, the value in
                   ;the register space at address
                   ;8 is moved to the X register.
```

Source Indexed

The result of an instruction using this addressing mode is placed in either the A register or the X register, which is specified as part of the instruction opcode. Operand 1 is added to the X register forming an address that points to a location in either the RAM memory space or the register space that is the source for the instruction. Arithmetic instructions require two sources; the second source is the A register or X register specified in the opcode. Instructions using this addressing mode are two bytes in length.

Table 13. Source Indexed

Opcode	Operand 1
Instruction	Source Index

Examples

```
ADD   A,   [X+7]     ;In this case, the value in
                     ;the memory location at
                     ;address X + 7 is added with
                     ;the Accumulator, and the
                     ;result is placed in the
                     ;Accumulator.
MOV   X,   REG[X+8]  ;In this case, the value in
                     ;the register space at
                     ;address X + 8 is moved to
                     ;the X register.
```

Destination Direct

The result of an instruction using this addressing mode is placed within either the RAM memory space or the register space. Operand 1 is an address that points to the location of the result. The source for the instruction is either the A register or the X register, which is specified as part of the instruction opcode. Arithmetic instructions require two sources; the second source is the location specified by Operand 1. Instructions using this addressing mode are two bytes in length.

Table 14. Destination Direct

Opcode	Operand 1
Instruction	Destination Address

Examples

```
ADD   [7],     A   ;In this case, the value in
                   ;the memory location at
                   ;address 7 is added with the
                   ;Accumulator, and the result
                   ;is placed in the memory
                   ;location at address 7. The
                   ;Accumulator is unchanged.
MOV   REG[8],  A   ;In this case, the Accumula-
                   ;tor is moved to the regis-
                   ;ter space location at
                   ;address 8. The Accumulator
                   ;is unchanged.
```

Destination Indexed

The result of an instruction using this addressing mode is placed within either the RAM memory space or the register space. Operand 1 is added to the X register forming the address that points to the location of the result. The source for the instruction is the A register. Arithmetic instructions require two sources; the second source is the location specified by Operand 1 added with the X register. Instructions using this addressing mode are two bytes in length.

Table 15. Destination Indexed

Opcode	Operand 1
Instruction	Destination Index

Example

```
ADD   [X+7],    A    ;In this case, the value in the
                     ;memory location at address X+7
                     ;is added with the Accumulator,
                     ;and the result is placed in
                     ;the memory location at address
                     ;x+7. The Accumulator is
                     ;unchanged.
```

Destination Direct Source Immediate

The result of an instruction using this addressing mode is placed within either the RAM memory space or the register space. Operand 1 is the address of the result. The source for the instruction is Operand 2, which is an immediate value. Arithmetic instructions require two sources; the second source is the location specified by Operand 1. Instructions using this addressing mode are three bytes in length.

Table 16. Destination Direct Immediate

Opcode	Operand 1	Operand 2
Instruction	Destination Address	Immediate Value

Examples

```
ADD   [7],     5    ;In this case, value in the mem-
                    ;ory location at address 7 is
                    ;added to the immediate value of
                    ;5, and the result is placed in
                    ;the memory location at address 7.
MOV   REG[8],  6    ;In this case, the immediate
                    ;value of 6 is moved into the
                    ;register space location at
                    ;address 8.
```

Destination Indexed Source Immediate

The result of an instruction using this addressing mode is placed within either the RAM memory space or the register space. Operand 1 is added to the X register to form the address of the result. The source for the instruction is Operand 2, which is an immediate value. Arithmetic instructions require two sources; the second source is the location specified by Operand 1 added with the X register. Instructions using this addressing mode are three bytes in length.

Table 17. Destination Indexed Immediate

Opcode	Operand 1	Operand 2
Instruction	Destination Index	Immediate Value

Examples

```
ADD    [X+7],     5    ;In this case, the value in
                       ;the memory location at
                       ;address X+7 is added with
                       ;the immediate value of 5,
                       ;and the result is placed
                       ;in the memory location at
                       ;address X+7.
MOV    REG[X+8],  6    ;In this case, the immedi-
                       ;ate value of 6 is moved
                       ;into the location in the
                       ;register space at
                       ;address X+8.
```

Destination Direct Source Direct

The result of an instruction using this addressing mode is placed within the RAM memory. Operand 1 is the address of the result. Operand 2 is an address that points to a location in the RAM memory that is the source for the instruction. This addressing mode is only valid on the MOV instruction. The instruction using this addressing mode is three bytes in length.

Table 18. Destination Direct Source Direct

Opcode	Operand 1	Operand 2
Instruction	Destination Address	Source Address

Example

```
MOV   [7],  [8]  ;In this case, the value in the
                 ;memory location at address 8 is
                 ;moved to the memory location at
                 ;address 7.
```

Source Indirect Post Increment

The result of an instruction using this addressing mode is placed in the Accumulator. Operand 1 is an address pointing to a location within the memory space, which contains an address (the indirect address) for the source of the instruction. The indirect address is incremented as part of the instruction execution. This addressing mode is only valid on the MVI instruction. The instruction using this addressing mode is two bytes in length. Refer to the *PSoC Designer: Assembly Language User Guide* for further details on MVI instruction.

Table 19. Source Indirect Post Increment

Opcode	Operand 1
Instruction	Source Address Address

Example

```
MVI   A,   [8]  ;In this case, the value in the
                ;memory location at address 8 is
                ;an indirect address. The memory
                ;location pointed to by the indi-
                ;rect address is moved into the
                ;Accumulator. The indirect
                ;address is then incremented.
```

Destination Indirect Post Increment

The result of an instruction using this addressing mode is placed within the memory space. Operand 1 is an address pointing to a location within the memory space, which contains an address (the indirect address) for the destination of the instruction. The indirect address is incremented as part of the instruction execution. The source for the instruction is the Accumulator. This addressing mode is only valid on the MVI instruction. The instruction using this addressing mode is two bytes in length.

Table 20. Destination Indirect Post Increment

Opcode	Operand 1
Instruction	Destination Address Address

Example

```
MVI    [8],   A     ;In this case, the value in
                    ;the memory location at
                    ;address 8 is an indirect
                    ;address. The Accumulator is
                    ;moved into the memory loca-
                    ;tion pointed to by the indi-
                    ;rect address. The indirect
                    ;address is then incremented.
```

Instruction Set Summary

The instruction set is summarized in Table 21 numerically and serves as a quick reference. If more information is needed, the Instruction Set Summary tables are described in detail in the *PSoC Designer Assembly Language User Guide* (available on www.cypress.com).

Table 21. Instruction Set Summary Sorted Numerically by Opcode Order [1, 2]

Opcode Hex	Cycles	Bytes	Instruction Format	Flags	Opcode Hex	Cycles	Bytes	Instruction Format	Flags	Opcode Hex	Cycles	Bytes	Instruction Format	Flags
00	15	1	SSC		2D	8	2	OR [X+expr], A	Z	5A	5	2	MOV [expr], X	
01	4	2	ADD A, expr	C, Z	2E	9	3	OR [expr], expr	Z	5B	4	1	MOV A, X	Z
02	6	2	ADD A, [expr]	C, Z	2F	10	3	OR [X+expr], expr	Z	5C	4	1	MOV X, A	
03	7	2	ADD A, [X+expr]	C, Z	30	9	1	HALT		5D	6	2	MOV A, reg[expr]	Z
04	7	2	ADD [expr], A	C, Z	31	4	2	XOR A, expr	Z	5E	7	2	MOV A, reg[X+expr]	Z
05	8	2	ADD [X+expr], A	C, Z	32	6	2	XOR A, [expr]	Z	5F	10	3	MOV [expr], [expr]	
06	9	3	ADD [expr], expr	C, Z	33	7	2	XOR A, [X+expr]	Z	60	5	2	MOV reg[expr], A	
07	10	3	ADD [X+expr], expr	C, Z	34	7	2	XOR [expr], A	Z	61	6	2	MOV reg[X+expr], A	
08	4	1	PUSH A		35	8	2	XOR [X+expr], A	Z	62	8	3	MOV reg[expr], expr	
09	4	2	ADC A, expr	C, Z	36	9	3	XOR [expr], expr	Z	63	9	3	MOV reg[X+expr], expr	
0A	6	2	ADC A, [expr]	C, Z	37	10	3	XOR [X+expr], expr	Z	64	4	1	ASL A	C, Z
0B	7	2	ADC A, [X+expr]	C, Z	38	5	2	ADD SP, expr		65	7	2	ASL [expr]	C, Z
0C	7	2	ADC [expr], A	C, Z	39	5	2	CMP A, expr	if (A=B) Z=1 if (A<B) C=1	66	8	2	ASL [X+expr]	C, Z
0D	8	2	ADC [X+expr], A	C, Z	3A	7	2	CMP A, [expr]		67	4	1	ASR A	C, Z
0E	9	3	ADC [expr], expr	C, Z	3B	8	2	CMP A, [X+expr]		68	7	2	ASR [expr]	C, Z
0F	10	3	ADC [X+expr], expr	C, Z	3C	8	3	CMP [expr], expr		69	8	2	ASR [X+expr]	C, Z
10	4	1	PUSH X		3D	9	3	CMP [X+expr], expr		6A	4	1	RLC A	C, Z
11	4	2	SUB A, expr	C, Z	3E	10	2	MVI A, [[expr]++]	Z	6B	7	2	RLC [expr]	C, Z
12	6	2	SUB A, [expr]	C, Z	3F	10	2	MVI [[expr]++], A		6C	8	2	RLC [X+expr]	C, Z
13	7	2	SUB A, [X+expr]	C, Z	40	4	1	NOP		6D	4	1	RRC A	C, Z
14	7	2	SUB [expr], A	C, Z	41	9	3	AND reg[expr], expr	Z	6E	7	2	RRC [expr]	C, Z
15	8	2	SUB [X+expr], A	C, Z	42	10	3	AND reg[X+expr], expr	Z	6F	8	2	RRC [X+expr]	C, Z
16	9	3	SUB [expr], expr	C, Z	43	9	3	OR reg[expr], expr	Z	70	4	2	AND F, expr	C, Z
17	10	3	SUB [X+expr], expr	C, Z	44	10	3	OR reg[X+expr], expr	Z	71	4	2	OR F, expr	C, Z
18	5	1	POP A	Z	45	9	3	XOR reg[expr], expr	Z	72	4	2	XOR F, expr	C, Z
19	4	2	SBB A, expr	C, Z	46	10	3	XOR reg[X+expr], expr	Z	73	4	1	CPL A	Z
1A	6	2	SBB A, [expr]	C, Z	47	8	3	TST [expr], expr	Z	74	4	1	INC A	C, Z
1B	7	2	SBB A, [X+expr]	C, Z	48	9	3	TST [X+expr], expr	Z	75	4	1	INC X	C, Z
1C	7	2	SBB [expr], A	C, Z	49	9	3	TST reg[expr], expr	Z	76	7	2	INC [expr]	C, Z
1D	8	2	SBB [X+expr], A	C, Z	4A	10	3	TST reg[X+expr], expr	Z	77	8	2	INC [X+expr]	C, Z
1E	9	3	SBB [expr], expr	C, Z	4B	5	1	SWAP A, X	Z	78	4	1	DEC A	C, Z
1F	10	3	SBB [X+expr], expr	C, Z	4C	7	2	SWAP A, [expr]	Z	79	4	1	DEC X	C, Z
20	5	1	POP X		4D	7	2	SWAP X, [expr]		7A	7	2	DEC [expr]	C, Z
21	4	2	AND A, expr	Z	4E	5	1	SWAP A, SP	Z	7B	8	2	DEC [X+expr]	C, Z
22	6	2	AND A, [expr]	Z	4F	4	1	MOV X, SP		7C	13	3	LCALL	
23	7	2	AND A, [X+expr]	Z	50	4	2	MOV A, expr	Z	7D	7	3	LJMP	
24	7	2	AND [expr], A	Z	51	5	2	MOV A, [expr]	Z	7E	10	1	RETI	C, Z
25	8	2	AND [X+expr], A	Z	52	6	2	MOV A, [X+expr]	Z	7F	8	1	RET	
26	9	3	AND [expr], expr	Z	53	5	2	MOV [expr], A		8x	5	2	JMP	
27	10	3	AND [X+expr], expr	Z	54	6	2	MOV [X+expr], A		9x	11	2	CALL	
28	11	1	ROMX	Z	55	8	3	MOV [expr], expr		Ax	5	2	JZ	
29	4	2	OR A, expr	Z	56	9	3	MOV [X+expr], expr		Bx	5	2	JNZ	
2A	6	2	OR A, [expr]	Z	57	4	2	MOV X, expr		Cx	5	2	JC	
2B	7	2	OR A, [X+expr]	Z	58	6	2	MOV X, [expr]		Dx	5	2	JNC	
2C	7	2	OR [expr], A	Z	59	7	2	MOV X, [X+expr]		Ex	7	2	JACC	
										Fx	13	2	INDEX	Z

Notes
1. Interrupt routines take 13 cycles before execution resumes at interrupt vector table.
2. The number of cycles required by an instruction is increased by one for instructions that span 256-byte boundaries in the Flash memory space.

Memory Organization

Flash Program Memory Organization

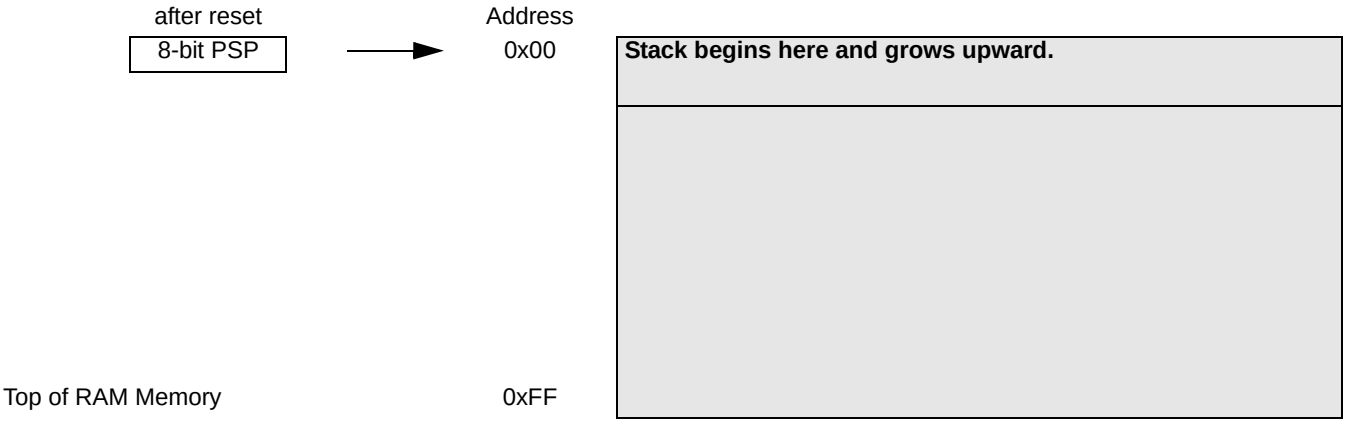
Table 22. Program Memory Space with Interrupt Vector Table

after reset	Address	
16-bit PC →	0x0000	Program execution begins here after a reset
	0x0004	POR/LVD
	0x0008	INT0
	0x000C	SPI Transmitter Empty
	0x0010	SPI Receiver Full
	0x0014	GPIO Port 0
	0x0018	GPIO Port 1
	0x001C	INT1
	0x0020	EP0
	0x0024	EP1
	0x0028	EP2
	0x002C	USB Reset
	0x0030	USB Active
	0x0034	1 ms Interval Timer
	0x0038	Programmable Interval Timer
	0x003C	Reserved
	0x0040	Reserved
	0x0044	16-bit Free Running Timer Wrap
	0x0048	INT2
	0x004C	Reserved
	0x0050	GPIO Port 2
	0x0054	Reserved
	0x0058	Reserved
	0x005C	Reserved
	0x0060	Reserved
	0x0064	Sleep Timer
	0x0068	**Program Memory begins here (if below interrupts not used, program memory can start lower)**
	0x1FFF	**8 KB ends here**

Data Memory Organization

The MCU function has 256 bytes of data RAM.

Table 23. Data Memory Organization



Flash

This section describes the Flash block of the CYRF69213. Much of the user-visible Flash functionality, including programming and security, are implemented in the M8C Supervisory Read Only Memory (SROM). CYRF69213 Flash has an endurance of 1000 cycles and 10 year data retention.

Flash Programming and Security

All Flash programming is performed by code in the SROM. The registers that control the Flash programming are only visible to the M8C CPU when it is executing out of SROM. This makes it impossible to read, write, or erase the Flash by bypassing the security mechanisms implemented in the SROM.

Customer firmware can only program the Flash via SROM calls. The data or code images can be sourced by way of any interface with the appropriate support firmware. This type of programming requires a 'boot-loader' — a piece of firmware resident on the Flash. For safety reasons this boot-loader should not be overwritten during firmware rewrites.

The Flash provides four auxiliary rows that are used to hold Flash block protection flags, boot time calibration values, configuration tables, and any device values. The routines for accessing these auxiliary rows are documented in the SROM section. The auxiliary rows are not affected by the device erase function.

In-System Programming

Most designs that include an CYRF69213 part have a USB connector attached to the USB D+/D– pins on the device. These designs require the ability to program or reprogram a part through these two pins alone.

CYRF69213 device enables this type of in-system programming by using the D+ and D– pins as the serial programming mode interface. This allows an external controller to cause the CYRF69213 part to enter serial programming mode and then to use the test queue to issue Flash access functions in the SROM. The programming protocol is not USB.

SROM

The SROM holds code that is used to boot the part, calibrate circuitry, and perform Flash operations. (Table 24 lists the SROM functions.) The functions of the SROM may be accessed in normal user code or operating from Flash. The SROM exists in a separate memory space from user code. The SROM functions are accessed by executing the Supervisory System Call instruction (SSC), which has an opcode of 00h. Prior to executing the SSC, the M8C's accumulator needs to be loaded with the desired SROM function code from Table 24. Undefined functions causes a HALT if called from user code. The SROM functions are executing code with calls; therefore, the functions require stack space. With the exception of Reset, all of the SROM functions have a *parameter block* in SRAM that must be configured before executing the SSC. Table 25 lists all possible parameter block variables. The meaning of each parameter, with regards to a specific SROM function, is described later in this section.

Table 24. SROM Function Codes

Function Code	Function Name	Stack Space
00h	SWBootReset	0
01h	ReadBlock	7
02h	WriteBlock	10
03h	EraseBlock	9
05h	EraseAll	11
06h	TableRead	3
07h	CheckSum	3

Two important variables that are used for all functions are KEY1 and KEY2. These variables are used to help discriminate between valid SSCs and inadvertent SSCs. KEY1 must always have a value of 3Ah, while KEY2 must have the same value as the stack pointer when the SROM function begins execution. This would be the Stack Pointer value when the SSC opcode is

executed, plus three. If either of the keys do not match the expected values, the M8C halts (with the exception of the SWBootReset function). The following code puts the correct value in KEY1 and KEY2. The code starts with a halt, to force the program to jump directly into the setup code and not run into it.

```
halt
SSCOP: mov [KEY1], 3ah
mov X, SP
mov A, X
add A, 3
mov [KEY2], A
```

Table 25. SROM Function Parameters

Variable Name	SRAM Address
Key1/Counter/Return Code	0,F8h
Key2/TMP	0,F9h
BlockID	0,FAh
Pointer	0,FBh
Clock	0,FCh
Mode	0,FDh
Delay	0,FEh
PCL	0,FFh

The SROM also features Return Codes and Lockouts.

Return Codes

Return codes aid in the determination of success or failure of a particular function. The return code is stored in KEY1's position in the parameter block. The CheckSum and TableRead functions do not have return codes because KEY1's position in the parameter block is used to return other data.

Table 26. SROM Return Codes

Return Code	Description
00h	Success
01h	Function not allowed due to level of protection on block
02h	Software reset without hardware reset
03h	Fatal error, SROM halted

Read, write, and erase operations may fail if the target block is read or write protected. Block protection levels are set during device programming.

The EraseAll function overwrites data in addition to leaving the entire user Flash in the erase state. The EraseAll function loops through the number of Flash macros in the product, executing the following sequence: erase, bulk program all zeros, erase. After all the user space in all the Flash macros are erased, a second loop erases and then programs each protection block with zeros.

SROM Function Descriptions

All SROM functions are described in the following sections.

SWBootReset Function

The SROM function, SWBootReset, is the function that is responsible for transitioning the device from a reset state to running user code. The SWBootReset function is executed whenever the SROM is entered with an M8C accumulator value of 00h; the SRAM parameter block is not used as an input to the function. This happens, by design, after a hardware reset, because the M8C's accumulator is reset to 00h or when user code executes the SSC instruction with an accumulator value of 00h. The SWBootReset function does not execute when the SSC instruction is executed with a bad key value and a nonzero function code. A CYRF69213 device executes the HALT instruction if a bad value is given for either KEY1 or KEY2.

The SWBootReset function verifies the integrity of the calibration data by way of a 16-bit checksum, before releasing the M8C to run user code.

ReadBlock Function

The ReadBlock function is used to read 64 contiguous bytes from Flash — a block.

The first thing this function does is to check the protection bits and determine if the desired BLOCKID is readable. If read protection is turned on, the ReadBlock function exits, setting the accumulator and KEY2 back to 00h. KEY1 has a value of 01h, indicating a read failure. If read protection is not enabled, the function reads 64 bytes from the Flash using a ROMX instruction and store the results in SRAM using an MVI instruction. The first of the 64 bytes is stored in SRAM at the address indicated by the value of the POINTER parameter. When the ReadBlock completes successfully, the accumulator, KEY1, and KEY2 all have a value of 00h.

Table 27. ReadBlock Parameters

Name	Address	Description
KEY1	0,F8h	3Ah
KEY2	0,F9h	Stack Pointer value, when SSC is executed
BLOCKID	0,FAh	Flash block number
POINTER	0,FBh	First of 64 addresses in SRAM where returned data should be stored

WriteBlock Function

The WriteBlock function is used to store data in the Flash. Data is moved 64 bytes at a time from SRAM to Flash using this function. The first thing the WriteBlock function does is to check the protection bits and determine if the desired BLOCKID is writable. If write protection is turned on, the WriteBlock function exits, setting the accumulator and KEY2 back to 00h. KEY1 has a value of 01h, indicating a write failure. The configuration of the WriteBlock function is straightforward. The BLOCKID of the Flash block, where the data is stored, must be determined and stored at SRAM address FAh.

The SRAM address of the first of the 64 bytes to be stored in Flash must be indicated using the POINTER variable in the parameter block (SRAM address FBh). Finally, the CLOCK and DELAY values must be set correctly. The CLOCK value determines the length of the write pulse that is used to store the data in the Flash. The CLOCK and DELAY values are dependent on the CPU speed. Refer to 'Clocking' Section for additional information.

Table 28. WriteBlock Parameters

Name	Address	Description
KEY1	0,F8h	3Ah
KEY2	0,F9h	Stack Pointer value, when SSC is executed
BLOCKID	0,FAh	8 KB Flash block number (00h–7Fh) 4 KB Flash block number (00h–3Fh) 3 KB Flash block number (00h–2Fh)
POINTER	0,FBh	First of 64 addresses in SRAM, where the data to be stored in Flash is located prior to calling WriteBlock
CLOCK	0,FCh	Clock divider used to set the write pulse width
DELAY	0,FEh	For a CPU speed of 12 MHz set to 56h

EraseBlock Function

The EraseBlock function is used to erase a block of 64 contiguous bytes in Flash. The first thing the EraseBlock function does is to check the protection bits and determine if the desired BLOCKID is writable. If write protection is turned on, the EraseBlock function exits, setting the accumulator and KEY2 back to 00h. KEY1 has a value of 01h, indicating a write failure. The EraseBlock function is only useful as the first step in programming. Erasing a block does not cause data in a block to be one hundred percent unreadable. If the objective is to obliterate data in a block, the best method is to perform an EraseBlock followed by a WriteBlock of all zeros.

To set up the parameter block for the EraseBlock function, correct key values must be stored in KEY1 and KEY2. The block number to be erased must be stored in the BLOCKID variable and the CLOCK and DELAY values must be set based on the current CPU speed.

Table 29. EraseBlock Parameters

Name	Address	Description
KEY1	0,F8h	3Ah
KEY2	0,F9h	Stack Pointer value when SSC is executed
BLOCKID	0,FAh	Flash block number (00h–7Fh)
CLOCK	0,FCh	Clock divider used to set the erase pulse width
DELAY	0,FEh	For a CPU speed of 12 MHz set to 56h

ProtectBlock Function

The CYRF69213 device offers Flash protection on a block-by-block basis. Table 30 lists the protection modes available. In the table, ER and EW are used to indicate the ability to perform external reads and writes. For internal writes, IW is used. Internal reading is always permitted by way of the ROMX instruction. The ability to read by way of the SROM ReadBlock function is indicated by SR. The protection level is stored in two bits according to Table 30. These bits are bit packed into the 64 bytes of the protection block. Therefore, each protection block byte stores the protection level for four Flash blocks. The bits are packed into a byte, with the lowest numbered block's protection level stored in the lowest numbered bits.

The first address of the protection block contains the protection level for blocks 0 through 3; the second address is for blocks 4 through 7. The 64th byte stores the protection level for blocks 252 through 255.

Table 30. Protection Modes

Mode	Settings	Description	Marketing
00b	SR ER EW IW	Unprotected	Unprotected
01b	SR ER EW IW	Read protect	Factory upgrade
10b	SR ER EW IW	Disable external write	Field upgrade
11b	SR ER EW IW	Disable internal write	Full protection

7	6	5	4	3	2	1	0
Block n+3		Block n+2		Block n+1		Block n	

The level of protection is only decreased by an EraseAll, which places zeros in all locations of the protection block. To set the level of protection, the ProtectBlock function is used. This function takes data from SRAM, starting at address 80h, and ORs it with the current values in the protection block. The result of the OR operation is then stored in the protection block. The EraseBlock function does not change the protection level for a block. Because the SRAM location for the protection data is fixed and there is only one protection block per Flash macro, the ProtectBlock function expects very few variables in the parameter block to be set prior to calling the function. The parameter block values that must be set, besides the keys, are the CLOCK and DELAY values.

Table 31. ProtectBlock Parameters

Name	Address	Description
KEY1	0,F8h	3Ah
KEY2	0,F9h	Stack Pointer value when SSC is executed
CLOCK	0,FCh	Clock divider used to set the write pulse width
DELAY	0,FEh	For a CPU speed of 12 MHz set to 56h

EraseAll Function

The EraseAll function performs a series of steps that destroy the user data in the Flash macros and resets the protection block in each Flash macro to all zeros (the unprotected state). The EraseAll function does not affect the three hidden blocks above the protection block in each Flash macro. The first of these four hidden blocks is used to store the protection table for its eight Kbytes of user data.

The EraseAll function begins by erasing the user space of the Flash macro with the highest address range. A bulk program of all zeros is then performed on the same Flash macro, to destroy all traces of the previous contents. The bulk program is followed by a second erase that leaves the Flash macro in a state ready for writing. The erase, program, erase sequence is then performed on the next lowest Flash macro in the address space if it exists. Following the erase of the user space, the protection block for the Flash macro with the highest address range is erased. Following the erase of the protection block, zeros are written into every bit of the protection table. The next lowest Flash macro in the address space then has its protection block erased and filled with zeros.

The end result of the EraseAll function is that all user data in the Flash is destroyed and the Flash is left in an unprogrammed state, ready to accept one of the various write commands. The protection bits for all user data are also reset to the zero state.

The parameter block values that must be set, besides the keys, are the CLOCK and DELAY values.

Table 32. EraseAll Parameters

Name	Address	Description
KEY1	0,F8h	3Ah
KEY2	0,F9h	Stack Pointer value when SSC is executed
CLOCK	0,FCh	Clock divider used to set the write pulse width
DELAY	0,FEh	For a CPU speed of 12 MHz set to 56h

TableRead Function

The TableRead function gives the user access to part specific data stored in the Flash during manufacturing. It also returns a Revision ID for the die (not to be confused with the Silicon ID).

Table 33. Table Read Parameters

Name	Address	Description
KEY1	0,F8h	3Ah
KEY2	0,F9h	Stack Pointer value when SSC is executed
BLOCKID	0,FAh	Table number to read

The table space for the CYRF69213 is simply a 64-byte row broken up into eight tables of eight bytes. The tables are numbered zero through seven. All user and hidden blocks in the CYRF69213 parts consist of 64 bytes.

An internal table holds the Silicon ID and returns the Revision ID. The Silicon ID is returned in SRAM, while the Revision ID is returned in the CPU_A and CPU_X registers. The Silicon ID is a value placed in the table by programming the Flash and is controlled by Cypress Semiconductor Product Engineering. The Revision ID is hard coded into the SROM. The Revision ID is discussed in more detail later in this section.

An internal table holds alternate trim values for the device and returns a one-byte internal revision counter. The internal revision counter starts out with a value of zero and is incremented each time one of the other revision numbers is not incremented. It is reset to zero each time one of the other revision numbers is incremented. The internal revision count is returned in the CPU_A register. The CPU_X register is always set to FFh when trim values are read. The BLOCKID value, in the parameter block, is used to indicate which table should be returned to the user. Only the three least significant bits of the BLOCKID parameter are used by the TableRead function for the CYRF69213. The upper five bits are ignored. When the function is called, it transfers bytes from the table to SRAM addresses F8h–FFh.

The M8C's A and X registers are used by the TableRead function to return the die's Revision ID. The Revision ID is a 16-bit value hard coded into the SROM that uniquely identifies the die's design.

Checksum Function

The Checksum function calculates a 16-bit checksum over a user specifiable number of blocks, within a single Flash macro (Bank) starting from block zero. The BLOCKID parameter is used to pass in the number of blocks to calculate the checksum over. A BLOCKID value of 1 calculates the checksum of only block 0, while a BLOCKID value of 0 calculates the checksum of all 256 user blocks. The 16-bit checksum is returned in KEY1 and KEY2. The parameter KEY1 holds the lower eight bits of the checksum and the parameter KEY2 holds the upper eight bits of the checksum.

The checksum algorithm executes the following sequence of three instructions over the number of blocks times 64 to be checksummed.

```
romx
  add [KEY1], A
adc [KEY2], 0
```

Table 34. Checksum Parameters

Name	Address	Description
KEY1	0,F8h	3Ah
KEY2	0,F9h	Stack Pointer value when SSC is executed
BLOCKID	0,FAh	Number of Flash blocks to calculate checksum on

SROM Table Read Description

Figure 7. SROM Table

	F8h	F9h	F8h	F8h	F8h	F8h	F8h	F8h
Table 0	Silicon ID [15-8]	Silicon ID [7-0]						
Table 1								
Table 2								
Table 3								
Table 4								
Table 5								
Table 6								
Table 7								

The Silicon IDs for enCoRe II devices are stored in SROM tables in the part, as shown in Figure 7.

The Silicon ID can be read out from the part using SROM Table reads. This is demonstrated in the following pseudo code. As mentioned in the section SROM on page 20, the SROM variables occupy address F8h through FFh in the SRAM. Each of the variables and their definition in given in the section SROM on page 20.

```
AREA SSCParmBlkA(RAM,ABS)

    org  F8h // Variables are defined starting at address F8h

SSC_KEY1:                 ; F8h  supervisory key
SSC_RETURNCODE:     blk 1 ; F8h  result code
SSC_KEY2 :          blk 1  ;F9h  supervisory stack ptr key
SSC_BLOCKID:        blk 1 ; FAh  block ID
SSC_POINTER:        blk 1 ; FBh  pointer to data buffer
SSC_CLOCK:          blk 1 ; FCh  Clock
SSC_MODE:           blk 1 ; FDh  ClockW ClockE multiplier
SSC_DELAY:          blk 1 ; FEh  flash macro sequence delay count
SSC_WRITE_ResultCode: blk 1 ; FFh  temporary result code

_main:
           mov   A, 0
           mov   [SSC_BLOCKID], A// To read from Table 0 - Silicon ID is stored in Table 0
//Call SROM operation to read the SROM table
          mov   X, SP      ; copy SP into X
          mov   A, X       ; A temp stored in X
          add   A, 3               ; create 3 byte stack frame (2 + pushed A)
          mov   [SSC_KEY2], A      ; save stack frame for supervisory code

   ; load the supervisory code for flash operations
          mov   [SSC_KEY1], 3Ah  ;FLASH_OPER_KEY - 3Ah

          mov   A,6        ; load A with specific operation. 06h is the code for Table read Table 24
          SSC              ; SSC call the supervisory ROM

// At the end of the SSC command the silicon ID is stored in F8 (MSB) and F9(LSB) of the SRAM
.terminate:
    jmp .terminate
```

Clocking

The CYRF69213 internal oscillator outputs two frequencies, the Internal 24 MHz Oscillator and the 32 kHz Low power Oscillator.

The Internal 24 MHz Oscillator is designed such that it may be trimmed to an output frequency of 24 MHz over temperature and voltage variation. With the presence of USB traffic, the Internal 24 MHz Oscillator can be set to precisely tune to USB timing requirements (24 MHz ± 1.5%). Without USB traffic, the Internal 24 MHz Oscillator accuracy is 24 MHz ± 5% (between 0 °C–70 °C). No external components are required to achieve this level of accuracy.

The internal low speed oscillator of nominally 32 KHz provides a slow clock source for the CYRF69213 in suspend mode, particularly to generate a periodic wakeup interrupt and also to provide a clock to sequential logic during power up and power down events when the main clock is stopped. In addition, this oscillator can also be used as a clocking source for the Interval Timer clock (ITMRCLK) and Capture Timer clock (TCAPCLK). The 32 kHz Low power Oscillator can operate in low power mode or can provide a more accurate clock in normal mode. The Internal 32 kHz Low power Oscillator accuracy ranges (between 0° C–70° C) as follows:

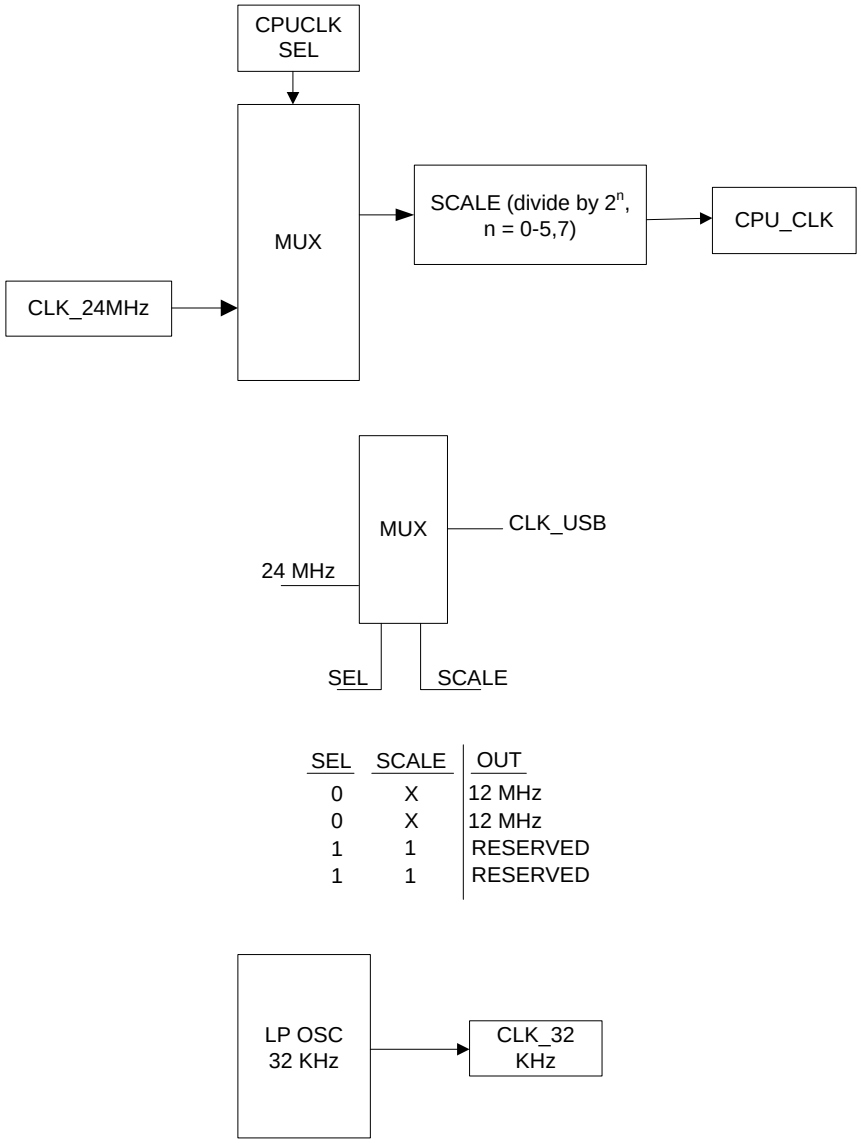
5 V Normal mode: –8% to + 16%

5 V LP mode: +12% to + 48%

When using the 32 kHz oscillator the PITMRL/H should be read until two consecutive readings match before sending/receiving data. The following firmware example assumes the developer is interested in the lower byte of the PIT.

```
Read_PIT_counter:
mov A, reg[PITMRL]
mov [57h], A
mov A, reg[PITMRL]
mov [58h], A
mov [59h], A
mov A, reg{PITMRL]
mov [60h], A
;;;Start comparison
mov A, [60h]
mov X, [59h]
sub A, [59h]
jz done
mov A, [59h]
mov X, [58h]
sub A, [58h]
jz done
mov X, [57h]
;;;correct data is in memory location 57h
done:
mov [57h], X
ret
```

Figure 8. Clock Block Diagram



SEL	SCALE	OUT
0	X	12 MHz
0	X	12 MHz
1	1	RESERVED
1	1	RESERVED

Clock Architecture Description

The CYRF69213 clock selection circuitry allows the selection of independent clocks for the CPU, USB, Interval Timers, and Capture Timers.

The CPU clock, CPUCLK, can be sourced from the Internal 24 MHz Oscillator. This clock source can optionally be divided by 2^n where *n* is 0–5,7 (see Table 38 on page 29).

USBCLK, which must be 12 MHz for the USB SIE to function properly, can be sourced by the Internal 24 MHz Oscillator. An optional divide-by-two allows the use of the 24 MHz source.

The Interval Timer clock (ITMRCLK), can be sourced from the Internal 24 MHz Oscillator, the Internal 32 kHz Low power Oscillator, except when in sleep mode, or from the timer capture clock (TCAPCLK). A programmable prescaler of 1, 2, 3, 4 then divides the selected source.

The Timer Capture clock (TCAPCLK) can be sourced from the Internal 24 MHz Oscillator, or the Internal 32 kHz Low power Oscillator except when in sleep mode.

The CLKOUT pin (P0.1) can be driven from one of many sources. This is used for test and can also be used in some applications.

The sources that can drive the CLKOUT are:

- CLKIN after the optional EFTB filter
- Internal 24 MHz Oscillator
- Internal 32 kHz Low power Oscillator except when in sleep mode
- CPUCLK after the programmable divider

Table 35. IOSC Trim (IOSCTR) [0x34] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	foffset[2:0]			Gain[4:0]				
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	D	D	D	D	D

The I/OSC Calibrate register is used to calibrate the internal oscillator. The reset value is undefined, but during boot the SROM writes a calibration value that is determined during manufacturing test. This value should not require change during normal use. This is the meaning of 'D' in the Default field

Bits 7:5 foffset [2:0]

This value is used to trim the frequency of the internal oscillator. These bits are not used in factory calibration and is zero. Setting each of these bits causes the appropriate fine offset in oscillator frequency
foffset bit 0 = 7.5 kHz
foffset bit 1 = 15 kHz
foffset bit 2 = 30 kHz

Bits 4:0 Gain [4:0]

The effective frequency change of the offset input is controlled through the gain input. A lower value of the gain setting increases the gain of the offset input. This value sets the size of each offset step for the internal oscillator. Nominal gain change (KHz/offsetStep) at each bit, typical conditions (24 MHz operation):
Gain bit 0 = –1.5 kHz
Gain bit 1 = –3.0 kHz
Gain bit 2 = –6 kHz
Gain bit 3 = –12 kHz
Gain bit 4 = –24 kHz

Table 36. LPOSC Trim (LPOSCTR) [0x36] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	32 kHz Low Power	Reserved	32 kHz Bias Trim [1:0]		32 kHz Freq Trim [3:0]			
Read/Write	R/W	–	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	D	D	D	D	D	D	D

This register is used to calibrate the 32 kHz Low speed Oscillator. The reset value is undefined, but during boot the SROM writes a calibration value that is determined during manufacturing test. This value should not require change during normal use. This is the meaning of 'D' in the Default field. If the 32 kHz Low power bit needs to be written, care should be taken not to disturb the 32 kHz Bias Trim and the 32 kHz Freq Trim fields from their factory calibrated values

Bit 7 32 kHz Low Power

0 = The 32 kHz Low speed Oscillator operates in normal mode
1 = The 32 kHz Low speed Oscillator operates in a low power mode. The oscillator continues to function normally but with reduced accuracy

Bit 6 Reserved

Bits 5:4 32 kHz Bias Trim [1:0]

These bits control the bias current of the low power oscillator.
0 0 = Mid bias
0 1 = High bias
1 0 = Reserved
1 1 = Reserved

Important Note Do not program the 32 kHz Bias Trim [1:0] field with the reserved 10b value, as the oscillator does not oscillate at all corner conditions with this setting

Bits 3:0 32 kHz Freq Trim [3:0]

These bits are used to trim the frequency of the low power oscillator

Table 37. CPU/USB Clock Config CPUCLKCR) [0x30] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Reserved							
Read/Write	–	R/W	R/W	–	–	–	–	R/W
Default	0	0	0	0	0	0	0	0

Bit 7 Reserved
Bit 6 Reserved
Bit 5 Reserved
Bits 4:1 Reserved
Bit 0 Reserved
Note The CPU speed selection is configured using the OSC_CR0 Register (Table 38 on page 29)

Table 38. OSC Control 0 (OSC_CR0) [0x1E0] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Reserved		No Buzz	Sleep Timer [1:0]		CPU Speed [2:0]		
Read/Write	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bits 7:6 Reserved

Bit 5 No Buzz

During sleep (the Sleep bit is set in the CPU_SCR Register — Table 42 on page 33), the LVD and POR detection circuit is turned on periodically to detect any POR and LVD events on the V_{CC} pin (the Sleep Duty Cycle bits in the ECO_TR are used to control the duty cycle — Table 46 on page 38). To facilitate the detection of POR and LVD events, the No Buzz bit is used to force the LVD and POR detection circuit to be continuously enabled during sleep. This results in a faster response to an LVD or POR event during sleep at the expense of a slightly higher than average sleep current

0 = The LVD and POR detection circuit is turned on periodically as configured in the Sleep Duty Cycle

1 = The Sleep Duty Cycle value is overridden. The LVD and POR detection circuit is always enabled

Note The periodic Sleep Duty Cycle enabling is independent with the sleep interval shown in the Sleep [1:0] bits below

Bits 4:3 Sleep Timer [1:0]

Sleep Timer [1:0]	Sleep Timer Clock Frequency (Nominal)	Sleep Period (Nominal)	Watchdog Period (Nominal)
00	512 Hz	1.95 ms	6 ms
01	64 Hz	15.6 ms	47 ms
10	8 Hz	125 ms	375 ms
11	1 Hz	1 sec	3 sec

Note Sleep intervals are approximate

Bits 2:0 CPU Speed [2:0]

The CYRF69213 may operate over a range of CPU clock speeds. The reset value for the CPU Speed bits is zero; therefore, the default CPU speed is one-eighth of the internal 24 MHz, or 3 MHz

Regardless of the CPU Speed bit's setting, if the actual CPU speed is greater than 12 MHz, the 24 MHz operating requirements apply. The operating voltage requirements are not relaxed until the CPU speed is at 12 MHz or less

CPU Speed [2:0]	CPU
000	3 MHz (Default)
001	6 MHz
010	12 MHz
011	24 MHz
100	1.5 MHz
101	750 KHz
110	187 KHz
111	Reserved

Important Note Correct USB operations require the CPU clock speed be at least 1.5 MHz or not less than USB clock/8. If the two clocks have the same source then the CPU clock divider should not be set to divide by more than 8. If the two clocks have different sources, care must be taken to ensure that the maximum ratio of USB Clock/CPU Clock can never exceed 8 across the full specification range of both clock sources

Table 39. USB Osclock Clock Configuration (OSCLCKCR) [0x39] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Reserved						Fine Tune Only	USB Osclock Disable
Read/Write	–	–	–	–	–	–	R/W	R/W
Default	0	0	0	0	0	0	0	0

This register is used to trim the Internal 24 MHz Oscillator using received low speed USB packets as a timing reference. The USB Osclock circuit is active when the Internal 24 MHz Oscillator provides the USB clock

Bits 7:2 Reserved

Bit 1 Fine Tune Only

0 = Enable

1 = Disable the oscillator lock from performing the course-tune portion of its retuning. The oscillator lock must be allowed to perform a course tuning to tune the oscillator for correct USB SIE operation. After the oscillator is properly tuned this bit can be set to reduce variance in the internal oscillator frequency that would be caused by course tuning

Bit 0 USB Osclock Disable

0 = Enable. With the presence of USB traffic, the Internal 24 MHz Oscillator precisely tunes to 24 MHz ± 1.5%

1 = Disable. The Internal 24 MHz Oscillator is not trimmed based on USB packets. This setting is useful when the internal oscillator is not sourcing the USBSIE clock

Table 40. Timer Clock Config (TMRCLKCR) [0x31] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	TCAPCL Divider		TCAPCLK Select		ITMRCLK Divider		ITMRCLK Select	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	1	1	0	0

Bits 7:6 TCAPCLK Divider

TCAPCLK Divider controls the TCAPCLK divisor

00 = Divide by 2

01 = Divide by 4

10 = Divide by 6

11 = Divide by 8

Bits 5:4 TCAPCLK Select

The TCAPCLK Select field controls the source of the TCAPCLK

0 0 = Internal 24 MHz Oscillator

0 1 = Reserved)

1 0 = Internal 32 kHz Low power Oscillator. However this configuration is not used in sleep mode.

1 1 = TCAPCLK Disabled

Note The 1024-µs interval timer is based on the assumption that TCAPCLK is running at 4 MHz. Changes in TCAPCLK frequency causes a corresponding change in the 1024 µs interval timer frequency

Bits 3:2 ITMRCLK Divider

ITMRCLK Divider controls the ITMRCLK divisor.

0 0 = Divider value of 1

0 1 = Divider value of 2

1 0 = Divider value of 3

1 1 = Divider value of 4

Bits 1:0 ITMRCLK Select

0 0 = Internal 24 MHz Oscillator

0 1 = Reserved

1 0 = Internal 32 kHz Low power Oscillator. However this configuration is not used in sleep mode.

1 1 = TCAPCLK

Interval Timer Clock (ITMRCLK)

The Interval Timer Clock (ITMRCLK) can be sourced from the Internal 24 MHz oscillator, the internal 32 kHz low power oscillator except when in sleep mode, or the timer capture clock. A programmable prescaler of 1, 2, 3, or 4 then divides the selected source. The 12-bit Programmable Interval Timer is a simple down counter with a programmable reload value. It provides a 1 μs resolution by default. When the down counter reaches zero, the next clock is spent reloading. The reload value can be read and written while the counter is running, but care should be taken to ensure that the counter does not unintentionally reload while the 12-bit reload value is only partially stored — for example, between the two writes of the 12-bit value. The programmable interval timer generates an interrupt to the CPU on each reload.

The parameters to be set appears on the device editor view of PSoC Designer after you place the CYRF69213 Timer User Module. The parameters are PITIMER_Source and PITIMER_Divider. The PITIMER_Source is the clock to the timer and the PITMER_Divider is the value the clock is divided by.

The interval register (PITMR) holds the value that is loaded into the PIT counter on terminal count. The PIT counter is a down counter.

The Programmable Interval Timer resolution is configurable. For example:

TCAPCLK divide by x of CPU clock (for example TCAPCLK divide by 2 of a 24 MHz CPU clock gives a frequency of 12 MHz)

ITMRCLK divide by x of TCAPCLK (for example, ITMRCLK divide by 3 of TCAPCLK is 4 MHz so resolution is 0.25 μs)

Timer Capture Clock (TCAPCLK)

The Timer Capture clock can be sourced from the internal 24 MHz oscillator or the Internal 332 kHz low power oscillator except when in sleep mode. A programmable prescaler of 2, 4, 6, or 8 then divides the selected source.

Figure 9. Programmable Interval Timer Block Diagram

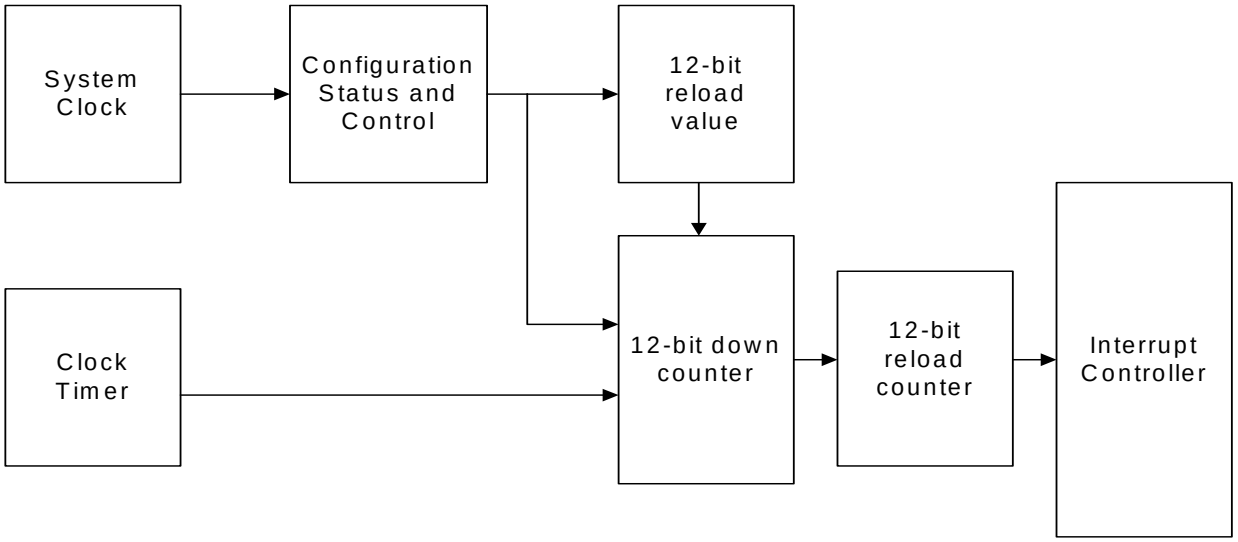


Figure 10. Timer Capture Block Diagram

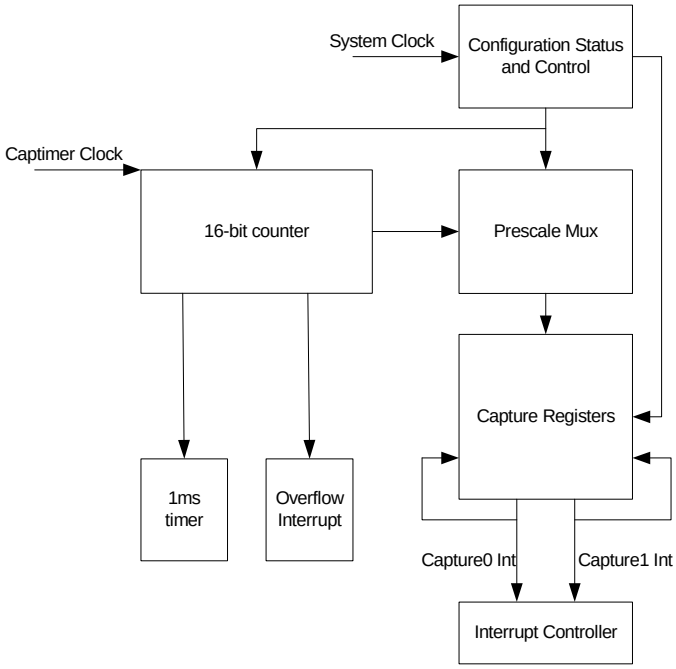


Table 41. Clock I/O Config (CLKIOCR) [0x32] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Reserved						CLKOUT Select	
Read/Write	–	–	–	–	–	–	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bits 7:2 Reserved

Bits 1:0 CLKOUT Select

0 0 = Internal 24 MHz Oscillator
0 1 = Reserved
1 0 = Internal 32 kHz Low power Oscillator.However this configuration is not used in sleep mode.
1 1 = CPUCLK

CPU Clock During Sleep Mode

When the CPU enters sleep mode the CPUCLK Select (Bit [0], Table 37) is forced to the internal oscillator, and the oscillator is stopped. When the CPU comes out of sleep mode it is running on the internal oscillator. The internal oscillator recovery time is three clock cycles of the Internal 32 kHz Low power Oscillator.

Reset

The microcontroller supports two types of resets: Power on Reset (POR) and Watchdog Reset (WDR). When reset is initiated, all registers are restored to their default states and all interrupts are disabled.

The occurrence of a reset is recorded in the System Status and Control Register (CPU_SCR). Bits within this register record the occurrence of POR and WDR Reset respectively. The firmware can interrogate these bits to determine the cause of a reset.

The microcontroller resumes execution from Flash address 0x0000 after a reset. The internal clocking mode is active after a reset.

Note The CPU clock defaults to 3 MHz (Internal 24 MHz Oscillator divide-by-8 mode) at POR to guarantee operation at the low V_{CC} that might be present during the supply ramp.

Table 42. System Status and Control Register (CPU_SCR) [0xFF] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	GIES	Reserved	WDRS	PORS	Sleep	Reserved		Stop
Read/Write	R	–	R/C[3]	R/C[3]	R/W	–	–	R/W
Default	0	0	0	1	0	0	0	0

The bits of the CPU_SCR register are used to convey status and control of events for various functions of an CYRF69213 device

Bit 7 GIES

The Global Interrupt Enable Status bit is a read only status bit and its use is discouraged. The GIES bit is a legacy bit, which was used to provide the ability to read the GIE bit of the CPU_F register. However, the CPU_F register is now readable. When this bit is set, it indicates that the GIE bit in the CPU_F register is also set which, in turn, indicates that the microprocessor services interrupts

0 = Global interrupts disabled

1 = Global interrupt enabled

Bit 6 Reserved

Bit 5 WDRS

The WDRS bit is set by the CPU to indicate that a WDR event has occurred. The user can read this bit to determine the type of reset that has occurred. The user can clear but not set this bit

0 = No WDR

1 = A WDR event has occurred

Bit 4 PORS

The PORS bit is set by the CPU to indicate that a POR event has occurred. The user can read this bit to determine the type of reset that has occurred. The user can clear but not set this bit

0 = No POR

1 = A POR event has occurred. (Note that WDR events does not occur until this bit is cleared)

Bit 3 SLEEP

Set by the user to enable CPU sleep state. CPU remains in sleep mode until any interrupt is pending. The Sleep bit is covered in more detail in the Sleep Mode section

0 = Normal operation

1 = Sleep

Bit 2:1 Reserved

Bit 0 STOP

This bit is set by the user to halt the CPU. The CPU remains halted until a reset (WDR, POR, or external reset) has taken place. If an application wants to stop code execution until a reset, the preferred method would be to use the HALT instruction rather than writing to this bit

0 = Normal CPU operation

1 = CPU is halted (not recommended)

Note

3. C = Clear. This bit can only be cleared by the user and cannot be set by firmware

Power on Reset

POR occurs every time the power to the device is switched on. POR is released when the supply is typically 2.6 V for the upward supply transition, with typically 50 mV of hysteresis during the power on transient. Bit 4 of the System Status and Control Register (CPU_SCR) is set to record this event (the register contents are set to 00010000 by the POR). After a POR, the microprocessor is held off for approximately 20 ms for the V_{CC} supply to stabilize before executing the first instruction at address 0x00 in the Flash. If the V_{CC} voltage drops below the POR downward supply trip point, POR is reasserted. The V_{CC} supply needs to ramp linearly from 0 to 4 V in 0 to 200 ms.

Important The PORS status bit is set at POR and can only be cleared by the user. It cannot be set by firmware.

Watchdog Timer Reset

The user has the option to enable the WDT. The WDT is enabled by clearing the PORS bit. When the PORS bit is cleared, the WDT cannot be disabled. The only exception to this is if a POR event takes place, which disables the WDT.

The sleep timer is used to generate the sleep time period and the Watchdog time period. The sleep timer is clocked by the Internal 32 kHz Low power Oscillator system clock. The user can program the sleep time period using the Sleep Timer bits of the OSC_CR0 Register (Table 38 on page 29). When the sleep time elapses (sleep timer overflows), an interrupt to the Sleep Timer Interrupt Vector is generated.

The Watchdog Timer period is automatically set to be three counts of the Sleep Timer overflows. This represents between two and three sleep intervals depending on the count in the Sleep Timer at the previous WDT clear. When this timer reaches three, a WDR is generated.

The user can either clear the WDT, or the WDT and the Sleep Timer. Whenever the user writes to the Reset WDT Register (RES_WDT), the WDT is cleared. If the data that is written is the hex value 0x38, the Sleep Timer is also cleared at the same time.

Table 43. Reset Watchdog Timer (RESWDT) [0xE3] [W]

Bit #	7	6	5	4	3	2	1	0
Field	Reset Watchdog Timer [7:0]							
Read/Write	W	W	W	W	W	W	W	W
Default	0	0	0	0	0	0	0	0

Any write to this register clears Watchdog Timer, a write of 0x38 also clears the Sleep Timer

Bits 7:0 Reset Watchdog Timer [7:0]

Sleep Mode

The CPU can only be put to sleep by the firmware. This is accomplished by setting the Sleep bit in the System Status and Control Register (CPU_SCR). This stops the CPU from executing instructions, and the CPU remains asleep until an interrupt comes pending, or there is a reset event (either a Power on Reset, or a Watchdog Timer Reset).

The Low voltage Detection circuit (LVD) drops into fully functional power reduced states, and the latency for the LVD is increased. The actual latency can be traded against power consumption by changing the Sleep Duty Cycle field of the ECO_TR Register.

The Internal 32 kHz Low speed Oscillator remains running. Prior to entering suspend mode, firmware can optionally configure the 32 kHz Low speed Oscillator to operate in a low power mode to help reduce the overall power consumption (using Bit 7, Table 36 on page 27). This helps save approximately 5 µA; however, the trade off is that the 32 kHz Low speed Oscillator is less accurate.

All interrupts remain active. Only the occurrence of an interrupt wakes the part from sleep. The Stop bit in the System Status and Control Register (CPU_SCR) must be cleared for a part to resume out of sleep. The Global Interrupt Enable bit of the CPU Flags Register (CPU_F) does not have any effect. Any unmasked interrupt wakes the system up. As a result, any interrupts not intended for waking must be disabled through the Interrupt Mask Registers.

When the CPU exits sleep mode the CPUCLK Select (Bit 1, Table 37 on page 28) is forced to the Internal Oscillator. The internal oscillator recovery time is three clock cycles of the Internal 32 kHz Low power Oscillator. The Internal 24 MHz Oscillator restarts immediately on exiting Sleep mode.

On exiting sleep mode, when the clock is stable and the delay time has expired, the instruction immediately following the sleep instruction is executed before the interrupt service routine (if enabled).

The Sleep interrupt allows the microcontroller to wake up periodically and poll system components while maintaining very low average power consumption. The Sleep interrupt may also be used to provide periodic interrupts during non sleep modes.

Sleep Sequence

The SLEEP bit is an input into the sleep logic circuit. This circuit is designed to sequence the device into and out of the hardware sleep state. The hardware sequence to put the device to sleep is shown in Figure 11 and is defined as follows.

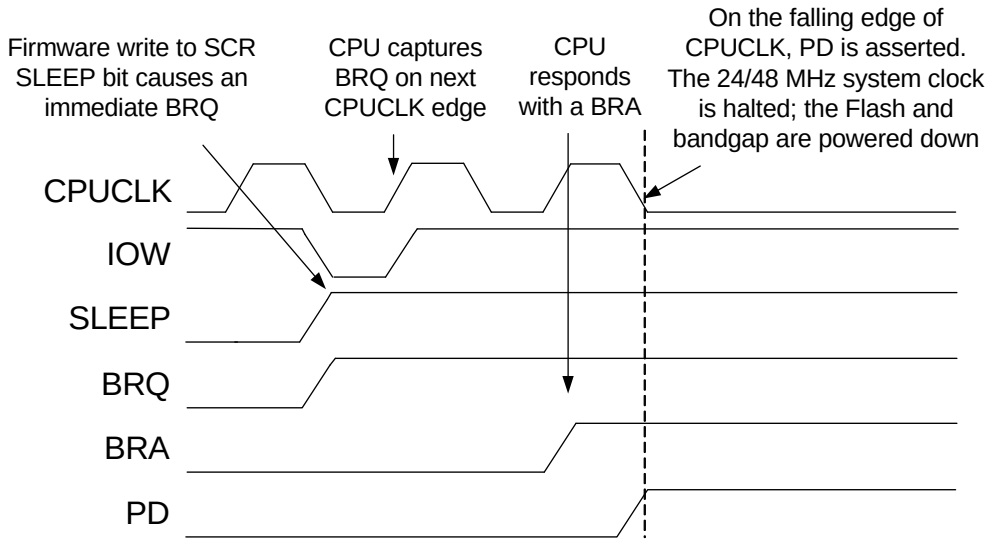
1. Firmware sets the SLEEP bit in the CPU_SCR0 register. The Bus Request (BRQ) signal to the CPU is immediately asserted. This is a request by the system to halt CPU operation at an instruction boundary. The CPU samples BRQ on the positive edge of CPUCLK.
2. Due to the specific timing of the register write, the CPU issues a Bus Request Acknowledge (BRA) on the following positive edge of the CPU clock. The sleep logic waits for the following negative edge of the CPU clock and then asserts a system-wide Power Down (PD) signal. In Figure 11 the CPU is halted and the system-wide power down signal is asserted.
3. The system-wide PD (power down) signal controls several major circuit blocks: The Flash memory module, the internal

24 MHz oscillator, the EFTB filter and the bandgap voltage reference. These circuits transition into a zero power state. The only operational circuits on chip are the Low Power oscillator, the bandgap refresh circuit, and the supply voltage monitor (POR/LVD) circuit.

Note To achieve the lowest possible power consumption during suspend/sleep, the following conditions must be observed in addition to considerations for the sleep timer.

- All GPIOs must be set to outputs and driven low
- The USB pins P1.0 and P1.1 should be configured as inputs with their pull ups enabled.

Figure 11. Sleep Timing



Wakeup Sequence

When asleep, the only event that can wake the system up is an interrupt. The global interrupt enable of the CPU flag register does not need to be set. Any unmasked interrupt wakes the system up. It is optional for the CPU to actually take the interrupt after the wakeup sequence. The wakeup sequence is synchronized to the 32 kHz clock for purposes of sequencing a startup delay, to allow the Flash memory module enough time to power up before the CPU asserts the first read access. Another reason for the delay is to allow the oscillator, Bandgap, and LVD/POR circuits time to settle before actually being used in the system. As shown in Figure 12 on page 36, the wakeup sequence is as follows:

1. The wakeup interrupt occurs and is synchronized by the negative edge of the 32 kHz clock.
2. At the following positive edge of the 32 kHz clock, the system-wide PD signal is negated. The Flash memory module, internal oscillator, EFTB, and bandgap circuit are all powered up to a normal operating state.
3. At the following positive edge of the 32 kHz clock, the current values for the precision POR and LVD have settled and are sampled.
4. At the following negative edge of the 32 kHz clock (after about 15 µs nominal), the BRQ signal is negated by the sleep logic circuit. On the following CPUCLK, BRA is negated by the CPU and instruction execution resumes. Note that in Figure 12 on page 36 fixed function blocks, such as Flash, internal oscillator, EFTB, and bandgap, have about 15 µs start up. The wakeup times (interrupt to CPU operational) ranges from 75 µs to 105 µs.

Low Power in Sleep Mode

The following steps are mandatory before configuring the system into suspend mode to meet the specifications:

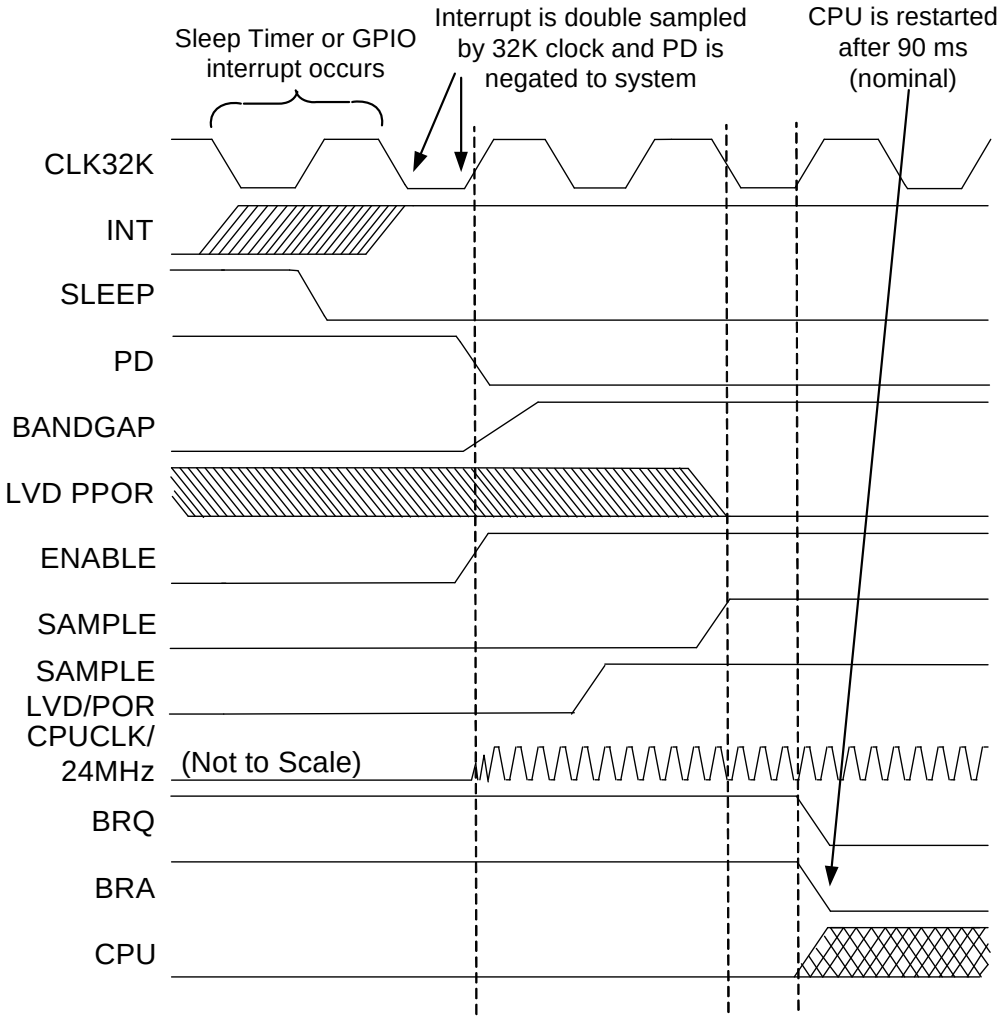
1. Clear P11CR[0], P10CR[0] - during USB and Non-USB operations
2. Clear the USB Enable USBCR[7] - during USB mode operations
3. Set P10CR[1] - during non-USB mode operations
4. To avoid current consumption make sure ITMRCLK, TCPCLK, and USBCLK are not sourced by either low power 32KHz oscillator or 24 MHz crystal-less oscillator.

All the other blocks go to the power down mode automatically on suspend.

The following steps are user configurable and help in reducing the average suspend mode power consumption.

1. Configure the power supply monitor at a large regular intervals, control register bits are 1,EB[7:6] (Power system sleep duty cycle PSSDC[1:0]).
2. Configure the Low power oscillator into low power mode, control register bit is LOPSCTR[7].

Figure 12. Wakeup Timing



Low Voltage Detect Control

Table 44. Low voltage Control Register (LVDCR) [0x1E3] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Reserved		PORLEV[1:0]		Reserved	VM[2:0]		
Read/Write	–	–	R/W	R/W	–	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

This register controls the configuration of the Power on Reset/Low voltage Detection block

Bits 7:6 Reserved

Bits 5:4 PORLEV[1:0]

This field controls the level below which the precision power-on-reset (PPOR) detector generates a reset
0 0 = 2.7 V Range (trip near 2.6 V)
0 1 = 3 V Range (trip near 2.9 V)
1 0 = 5 V Range, ≥4.75 V (trip near 4.65 V). This setting must be used when operating the CPU above 12 MHz.
1 1 = PPOR does not generate a reset, but values read from the Voltage Monitor Comparators Register (Table 45) give the internal PPOR comparator state with trip point set to the 3 V range setting

Bit 3 Reserved

Bits 2:0 VM[2:0]

This field controls the level below which the low voltage-detect trips — possibly generating an interrupt and the level at which the Flash is enabled for operation.

VM[2:0]	LVD Trip Point (V)		
	Min.	Typical	Max.
000	Reserved	Reserved	Reserved
001	Reserved	Reserved	Reserved
010	Reserved	Reserved	Reserved
011	Reserved	Reserved	Reserved
100	4.439	4.48	4.528
101	4.597	4.64	4.689
110	4.680	4.73	4.774
111	4.766	4.82	4.862

POR Compare State

Table 45. Voltage Monitor Comparators Register (VLTCMP) [0x1E4] [R]

Bit #	7	6	5	4	3	2	1	0
Field	Reserved						LVD	PPOR
Read/Write	–	–	–	–	–	–	R	R
Default	0	0	0	0	0	0	0	0

This read-only register allows reading the current state of the Low voltage-Detection and Precision-Power-On-Reset comparators

Bits 7:2 Reserved

Bit 1 LVD

This bit is set to indicate that the low voltage-detect comparator has tripped, indicating that the supply voltage has gone below the trip point set by VM[2:0] (See Table 44)
0 = No low voltage-detect event
1 = A low voltage-detect has tripped

Bit 0 PPOR

This bit is set to indicate that the precision-power-on-reset comparator has tripped, indicating that the supply voltage is below the trip point set by PORLEV[1:0]
0 = No precision-power-on-reset event
1 = A precision-power-on-reset event has tripped

ECO Trim Register

Table 46. ECO (ECO_TR) [0x1EB] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Sleep Duty Cycle [1:0]		Reserved					
Read/Write	R/W	R/W	–	–	–	–	–	–
Default	0	0	0	0	0	0	0	0

This register controls the ratios (in numbers of 32 kHz clock periods) of ‘on’ time versus ‘off’ time for LVD and POR detection circuit

Bits 7:6 Sleep Duty Cycle [1:0]

0 0 = 1/128 periods of the Internal 32 kHz Low speed Oscillator
0 1 = 1/512 periods of the Internal 32 kHz Low speed Oscillator
1 0 = 1/32 periods of the Internal 32 kHz Low speed Oscillator
1 1 = 1/8 periods of the Internal 32 kHz Low speed Oscillator

General-Purpose I/O Ports

The general purpose I/O ports are discussed in the following sections.

Port Data Registers

Table 47. P0 Data Register (P0DATA)[0x00] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	P0.7	Reserved	Reserved	P0.4/INT2	P0.3/INT1	Reserved	P0.1	Reserved
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

This register contains the data for Port 0. Writing to this register sets the bit values to be output on output enabled pins. Reading from this register returns the current state of the Port 0 pins

Bit 7 P0.7 Data

Bits 6:5 Reserved

The use of the pins as the P0.6–P0.5 GPIOs and the alternative functions exist in the CYRF69213

Bits 4:3 P0.4–P0.3 Data/INT2 – INT1

In addition to their use as the P0.4–P0.3 GPIOs, these pins can also be used for the alternative functions as the Interrupt pins (INT0–INT2). To configure the P0.4–P0.3 pins, refer to the P0.3/INT1–P0.4/INT2 Configuration Register (Table 51)

The use of the pins as the P0.4–P0.3 GPIOs and the alternative functions exist in the CYRF69213

Bit 2 Reserved

Bit 1 P0.1

Bit 0 Reserved

Table 48. P1 Data Register (P1DATA) [0x01] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	P1.7	P1.6/SMISO	P1.5/SMOSI	P1.4/SCLK	P1.3/SSEL	P1.2/VREG	P1.1/D–	P1.0/D+
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

This register contains the data for Port 1. Writing to this register sets the bit values to be output on output enabled pins. Reading from this register returns the current state of the Port 1 pins

Bit 7 P1.7 Data

Bits 6:3 P1.6–P1.3 Data/SPI Pins (SMISO, SMOSI, SCLK, SSEL)

In addition to their use as the P1.6–P1.3 GPIOs, these pins can also be used for the alternative function as the SPI interface pins. To configure the P1.6–P1.3 pins, refer to the P1.3–P1.6 Configuration Register (Table 56 on page 43)

The use of the pins as the P1.6–P1.3 GPIOs and the alternative functions exist in all the CYRF69213 parts

Bit 2 P1.2/VREG

This pin is used as the regulator output. The 3.3 V VREG output must be enabled by setting Bit 0 of VREGCR register (Table 80 on page 56). A 1 mF min, 2 mF max capacitor is required on VREG output.

Bits 1:0 P1.1–P1.0/D– and D+

When USB mode is disabled (Bit 7 in Table 81 on page 57 is clear), the P1.1 and P1.0 bits are used to control the state of the P1.0 and P1.1 pins. When the USB mode is enabled, the P1.1 and P1.0 pins are used as the D– and D+ pins, respectively. If the USB Force State bit (Bit 0 in Table 79 on page 56) is set, the state of the D– and D+ pins can be controlled by writing to the D– and D+ bits

Table 49. P2 Data Register (P2DATA) [0x02] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Reserved						P2.1–P2.0	
Read/Write	–	–	–	–	–	–	R/W	R/W
Default	0	0	0	0	0	0	0	0

This register contains the data for Port 2. Writing to this register sets the bit values to be output on output enabled pins. Reading from this register returns the current state of the Port 2 pins

Bits 7:2 Reserved Data [7:2]

Bits 1:0 P2 Data [1:0]

GPIO Port Configuration

All the GPIO configuration registers have common configuration controls. The following are the bit definitions of the GPIO configuration registers.

Int Enable

When set, the Int Enable bit allows the GPIO to generate interrupts. Interrupt generate can occur regardless of whether the pin is configured for input or output. All interrupts are edge sensitive, however for any interrupt that is shared by multiple sources (that is, Ports 2, 3, and 4) all inputs must be deasserted before a new interrupt can occur.

When clear, the corresponding interrupt is disabled on the pin.

It is possible to configure GPIOs as outputs, enable the interrupt on the pin and then to generate the interrupt by driving the appropriate pin state. This is useful in test and may have value in applications as well.

Int Act Low

When set, the corresponding interrupt is active on the falling edge.

When clear, the corresponding interrupt is active on the rising edge.

TTL Thresh

When set, the input has TTL threshold. When clear, the input has standard CMOS threshold.

High Sink

When set, the output can sink up to 50 mA.

When clear, the output can sink up to 8 mA.

On the CYRF69213, only the P1.7–P1.3 have 50 mA sink drive capability. Other pins have 8 mA sink drive capability.

Open Drain

When set, the output on the pin is determined by the Port Data Register. If the corresponding bit in the Port Data Register is set,

the pin is in high impedance state. If the corresponding bit in the Port Data Register is clear, the pin is driven low.

When clear, the output is driven LOW or HIGH.

Pull up Enable

When set the pin has a 7K pull up to V_{CC} (or VREG for ports with V3.3 enabled).

When clear, the pull up is disabled.

Output Enable

When set, the output driver of the pin is enabled.

When clear, the output driver of the pin is disabled.

For pins with shared functions there are some special cases.

VREG Output/SPI Use

The P1.2 (VREG), P1.3 (SSEL), P1.4 (SCLK), P1.5 (SMOSI) and P1.6 (SMISO) pins can be used for their dedicated functions or for GPIO.

To enable the pin for GPIO, clear the corresponding VREG Output or SPI Use bit. The SPI function controls the output enable for its dedicated function pins when their GPIO enable bit is clear.

3.3 V Drive

The P1.3 (SSEL), P1.4 (SCLK), P1.5 (SMOSI) and P1.6 (SMISO) pins have an alternate voltage source from the voltage regulator. If the 3.3 V Drive bit is set a high level is driven from the voltage regulator instead of from V_{CC}.

Setting the 3.3 V Drive bit does not enable the voltage regulator. That must be done explicitly by setting the VREG Enable bit in the VREGCR Register (Table 80 on page 56).

Figure 13. Block Diagram of a GPIO

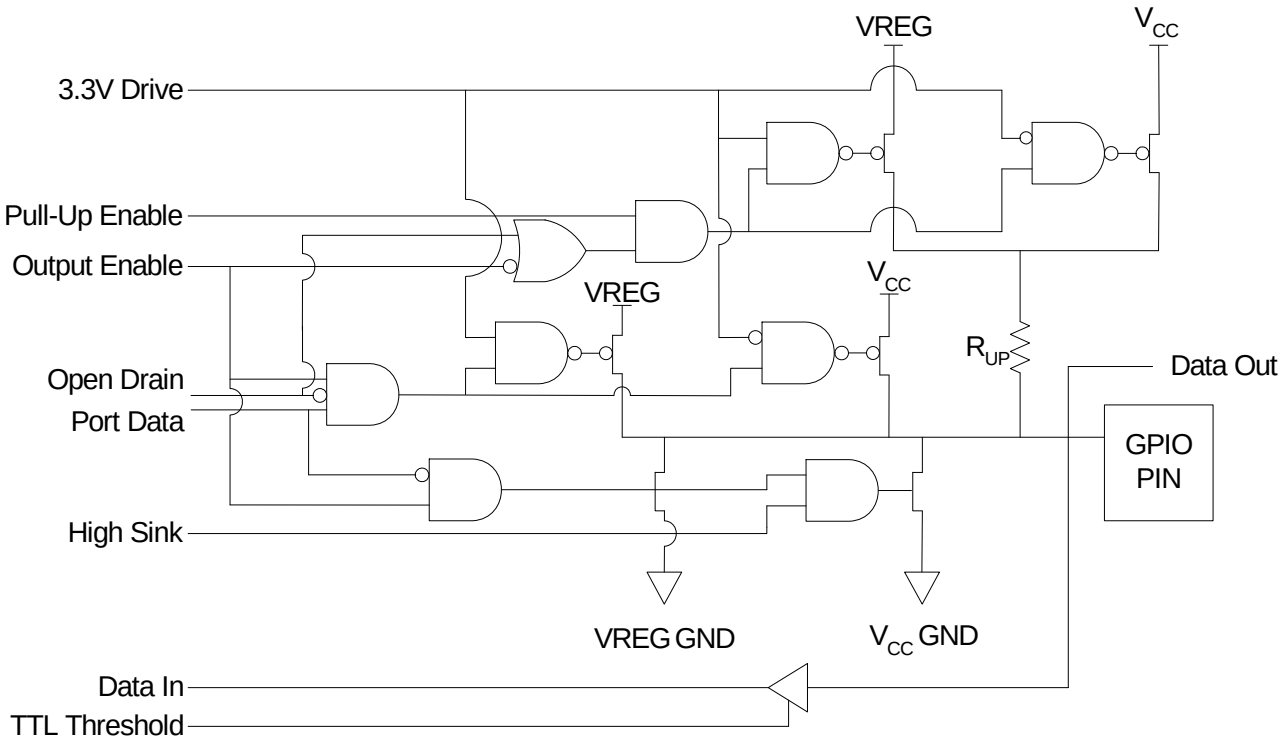


Table 50. P0.1 Configuration (P01CR) [0x06] R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Reserved	Int Enable	Int Act Low	TTL Thresh	High Sink	Open Drain	Pull up Enable	Output Enable
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

This register is used to configure P0.1 In the CYRF69213, only 8 mA sink drive capability is available on this pin regardless of the setting of the High Sink bit
Bit 7: Reserved

Table 51. P0.3/INT1–P0.4/INT2 Configuration (P03CR–P04CR) [0x08–0x09] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Reserved		Int Act Low	TTL Thresh	Reserved	Open Drain	Pull up Enable	Output Enable
Read/Write	–	–	R/W	R/W	–	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

These registers control the operation of pins P0.3–P0.4, respectively. These pins are shared between the P0.3–P0.4 GPIOs and the INT0–INT2. These registers exist in all CYRF69213 parts. The INT0–INT2 interrupts are different than all the other GPIO interrupts. These pins are connected directly to the interrupt controller to provide three edge-sensitive interrupts with independent interrupt vectors. These interrupts occur on a rising edge when Int act Low is clear and on a falling edge when Int act Low is set. These pins are enabled as interrupt sources in the interrupt controller registers (Table 77 and Table 75)

To use these pins as interrupt inputs configure them as inputs by clearing the corresponding Output Enable. If the INT0–INT2 pins are configured as outputs with interrupts enabled, firmware can generate an interrupt by writing the appropriate value to the P0.3 and P0.4 data bits in the P0 Data Register

Regardless of whether the pins are used as Interrupt or GPIO pins the Int Enable, Int act Low, TTL Threshold, Open Drain, and Pull up Enable bits control the behavior of the pin

The P0.3/INT1–P0.4/INT2 pins are individually configured with the P03CR (0x08), and P04CR (0x09), respectively.

Note Changing the state of the Int Act Low bit can cause an unintentional interrupt to be generated. When configuring these interrupt sources, it is best to follow the following procedure:

1. Disable interrupt source
2. Configure interrupt source
3. Clear any pending interrupts from the source
4. Enable interrupt source

Table 52. P0.7 Configuration (P07CR) [0x0C] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Reserved	Int Enable	Int Act Low	TTL Thresh	Reserved	Open Drain	Pull up Enable	Output Enable
Read/Write	–	R/W	R/W	R/W	–	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

This register controls the operation of pin P0.7.

Table 53. P1.0/D+ Configuration (P10CR) [0x0D] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Reserved	Int Enable	Int Act Low	Reserved			5K pull up enable	Output Enable
Read/Write	R/W	R/W	R/W	–	–	–	–	R/W
Default	0	0	0	0	0	0	0	0

This register controls the operation of the P1.0 (D+) pin when the USB interface is not enabled, allowing the pin to be used as a GPIO pin which is pulled up. See Table 81 for information on enabling USB. When USB is enabled, none of the controls in this register have any effect on the P1.0 pin

Note The P1.0 is an open drain only output. It can actively drive a signal low, but cannot actively drive a signal high

Bit 1 5K Pull up Enable

0 = Disable the 5 Kohm pull up resistors

1 = Enable 5 Kohm pull up resistors for both P1.0 and P1.1. Enable the use of the P1.0 (D+) and P1.1 (D–) pins as pulled up GPIOs

Bit 0 This bit enables the output on P1.0/D+. This bit should be cleared in sleep mode.

Table 54. P1.1/D– Configuration (P11CR) [0x0E] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Reserved	Int Enable	Int Act Low	Reserved		Open Drain	Reserved	Output Enable
Read/Write	–	R/W	R/W	–	–	R/W	–	R/W
Default	0	0	0	0	0	0	0	0

This register controls the operation of the P1.1 (D–) pin when the USB interface is not enabled, allowing the pin to be used as a GPIO. See Table 81 for information on enabling USB. When USB is enabled, none of the controls in this register have any effect on the P1.1 pin. When USB is disabled, the 5 Kohm pull up resistor on this pin can be enabled by the 5K Pull up Enable bit of the P10CR Register (Table 53)

Bit 0This bit enables the output on P1.1/D-. This bit should be cleared in sleep mode.

Note There is no 2 mA sourcing capability on this pin. The pin can only sink 5 mA at V_{OL3}

Table 55. P1.2 Configuration (P12CR) [0x0F] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	CLK Output	Int Enable	Int Act Low	TTL Threshold	Reserved	Open Drain	Pull up Enable	Output Enable
Read/Write	R/W	R/W	R/W	R/W	–	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

This register controls the operation of the P1.2

Bit 7 CLK Output

0 = The internally selected clock is not sent out onto P1.2 pin

1 = When CLK Output is set, the internally selected clock is sent out onto P1.2 pin

Table 56. P1.3 Configuration (P13CR) [0x10] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Reserved	Int Enable	Int Act Low	3.3 V Drive	High Sink	Open Drain	Pull up Enable	Output Enable
Read/Write	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

This register controls the operation of the P1.3 pin. This register exists in all CYRF69213 parts

The P1.3 GPIO's threshold is always set to TTL

When the SPI hardware is enabled, the output enable and output state of the pin is controlled by the SPI circuitry. When the SPI hardware is disabled, the pin is controlled by the Output Enable bit and the corresponding bit in the P1 data register

Regardless of whether the pin is used as an SPI or GPIO pin the Int Enable, Int act Low, 3.3 V Drive, High Sink, Open Drain, and Pull up Enable control the behavior of the pin

The 50 mA sink drive capability is only available in the CY7C638xx.

Table 57. P1.4–P1.6 Configuration (P14CR–P16CR) [0x11–0x13] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	SPI Use	Int Enable	Int Act Low	3.3 V Drive	High Sink	Open Drain	Pull up Enable	Output Enable
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

These registers control the operation of pins P1.4–P1.6, respectively

The P1.4–P1.6 GPIO's threshold is always set to TTL

When the SPI hardware is enabled, pins that are configured as SPI Use have their output enable and output state controlled by the SPI circuitry. When the SPI hardware is disabled or a pin has its SPI Use bit clear, the pin is controlled by the Output Enable bit and the corresponding bit in the P1 data register

Regardless of whether any pin is used as an SPI or GPIO pin the Int Enable, Int act Low, 3.3 V Drive, High Sink, Open Drain, and Pull up Enable control the behavior of the pin

Bit 7 SPI Use

0 = Disable the SPI alternate function. The pin is used as a GPIO

1 = Enable the SPI function. The SPI circuitry controls the output of the pin

Important Note for Comm Modes 01 or 10 (SPI Master or SPI Slave, see Table 61)

When configured for SPI (SPI Use = 1 and Comm Modes [1:0] = SPI Master or SPI Slave mode), the input/output direction of pins P1.3, P1.5, and P1.6 is set automatically by the SPI logic. However, pin P1.4's input/output direction is NOT automatically set; it must be explicitly set by firmware. For SPI Master mode, pin P1.4 must be configured as an output; for SPI Slave mode, pin P1.4 must be configured as an input

Table 58. P1.7 Configuration (P17CR) [0x14] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Reserved	Int Enable	Int Act Low	TTL Thresh	High Sink	Open Drain	Pull up Enable	Output Enable
Read/Write	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

This register controls the operation of pin P1.7. This register only exists in CY7C638xx

The 50 mA sink drive capability is only available in the CY7C638xx. The P1.7 GPIO's threshold is always set to TTL

Table 59. P2 Configuration (P2CR) [0x15] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Reserved	Int Enable	Int Act Low	TTL Thresh	High Sink	Open Drain	Pull up Enable	Output Enable
Read/Write	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
This register only exists in CY7C638xx. This register controls the operation of pins P2.0–P2.1. In the CY7C638xx, only 8 mA sink drive capability is available on this pin regardless of the setting of the High Sink bit								

GPIO Configurations for Low Power Mode:

To ensure low power mode, unbonded GPIO pins in CYRF69213 must be placed in a non floating state. The following assembly code snippet shows how this is achieved. This snippet can be added as a part of the initialization routine.

```
//Code Snippet for addressing unbonded GPIOs

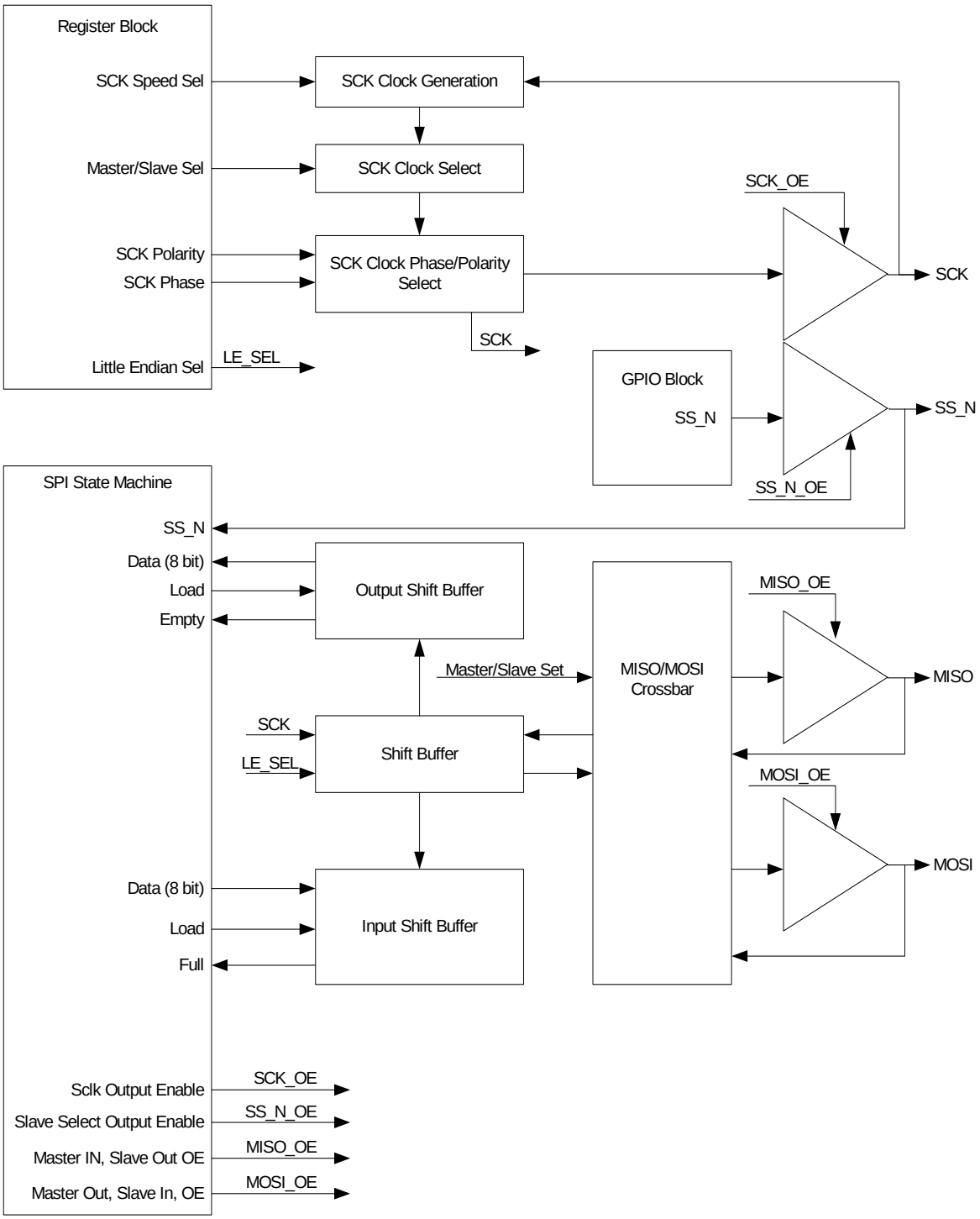
mov A, 00h
mov reg[1Fh],A
mov A, 01h
mov reg[16h],A // Port3 Configuration register - Enable ouptut
mov A, 00h
mov reg[03h],A // Asserting P3.0 and P3.1 outputs to '0'
mov A, 01h
mov reg[05h],A // Port0.0 Configuration register - Enable output
mov reg[07h],A // Port0.2 Configuration register - Enable output
mov reg[0Ah],A // Port0.5 Configuration register - Enable output
mov reg[0Bh],A // Port0.6 Configuration register - Enable output
mov A,reg[00h]
mov A,00h
and A,9Ah
mov reg[00h], A // Asserting outputs '0' to pins in port 1
```

When writing to port 0 , to access GPIOs P0.1,3,4,7 , mask bits 0,2,5,6 .Failing to do so will void the low power.

Serial Peripheral Interface (SPI)

The SPI Master/Slave Interface core logic runs on the SPI clock domain, making its functionality independent of system clock speed. SPI is a four pin serial interface comprised of a clock, an enable and two data pins.

Figure 14. SPI Block Diagram



SPI Data Register

Table 60. SPI Data Register (SPIDATA) [0x3C] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	SPIData[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

When read, this register returns the contents of the receive buffer. When written, it loads the transmit holding register

Bits 7:0 SPI Data [7:0]

When an interrupt occurs to indicate to firmware that a byte of receive data is available, or the transmitter holding register is empty, firmware has 7 SPI clocks to manage the buffers — to empty the receiver buffer, or to refill the transmit holding register. Failure to meet this timing requirement results in incorrect data transfer.

SPI Configure Register

Table 61. SPI Configure Register (SPICR) [0x3D] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Swap	LSB First	Comm Mode		CPOL	CPHA	SCLK Select	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit 7 Swap

0 = Swap function disabled

1 = The SPI block swaps its use of SMOSI and SMISO. Among other things, this can be useful in implementing single wire SPI-like communications

Bit 6 LSB First

0 = The SPI transmits and receives the MSB (Most Significant Bit) first

1 = The SPI transmits and receives the LSB (Least Significant Bit) first.

Bits 5:4 Comm Mode [1:0]

0 0: All SPI communication disabled

0 1: SPI master mode

1 0: SPI slave mode

1 1: Reserved

Bit 3 CPOL

This bit controls the SPI clock (SCLK) idle polarity

0 = SCLK idles low

1 = SCLK idles high

Bit 2 CPHA

The Clock Phase bit controls the phase of the clock on which data is sampled. Table 62 on page 47 shows the timing for the various combinations of LSB First, CPOL, and CPHA

Bits 1:0 SCLK Select

This field selects the speed of the master SCLK. When in master mode, SCLK is generated by dividing the base CPUCLK

Important Note for Comm Modes 01b or 10b (SPI Master or SPI Slave):

When configured for SPI, (SPI Use = 1 — Table 57 on page 43), the input/output direction of pins P1.3, P1.5, and P1.6 is set automatically by the SPI logic. However, pin P1.4's input/output direction is NOT automatically set; it must be explicitly set by firmware. For SPI Master mode, pin P1.4 must be configured as an output; for SPI Slave mode, pin P1.4 must be configured as an input

Table 62. SPI Mode Timing vs. LSB First, CPOL and CPHA

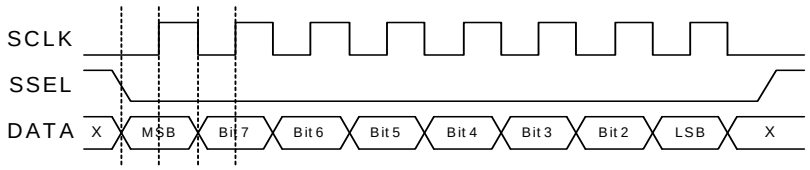
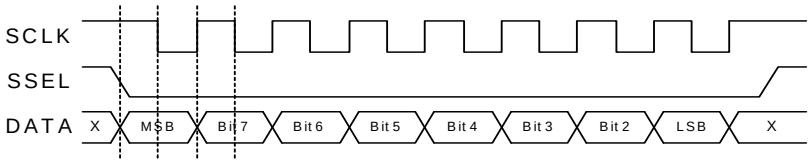
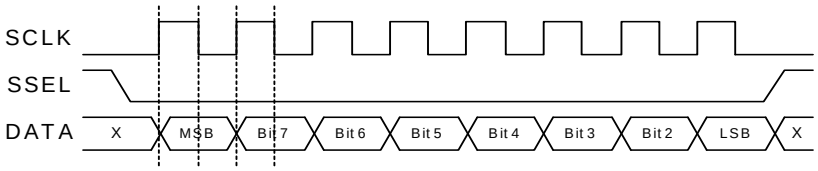
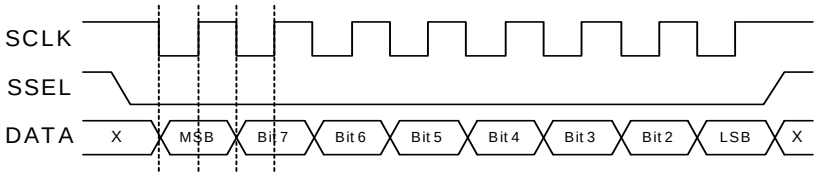
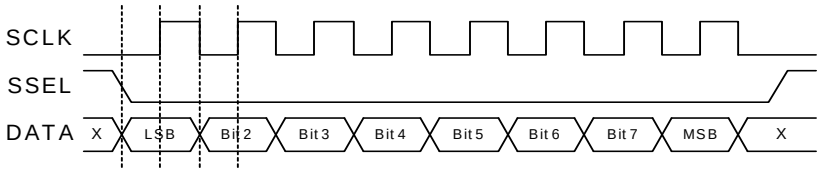
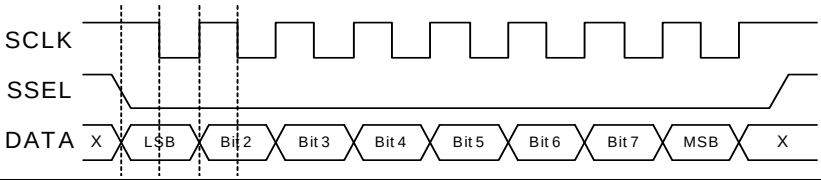
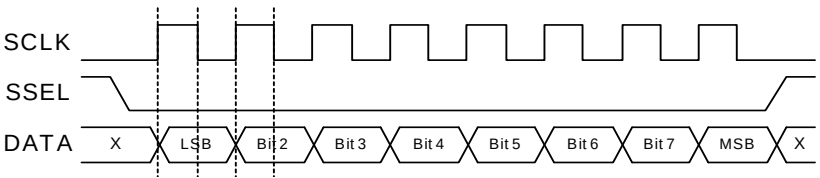
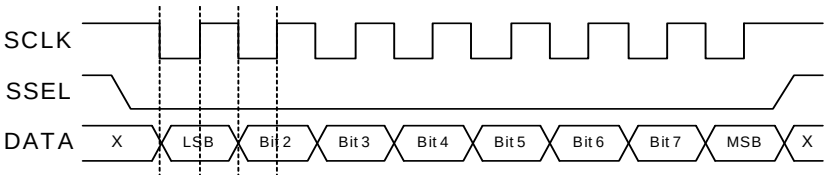
LSB First	CPHA	CPOL	Diagram
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Table 63. SPI SCLK Frequency

SCLK Select	CPUCLK Divisor	SCLK Frequency	
		CPUCLK = 12 MHz	CPUCLK = 24 MHz
00	6	2 MHz	4 MHz
01	12	1 MHz	2 MHz
10	48	250 KHz	500 KHz
11	96	125 KHz	250 KHz

Timer Registers

All timer functions of the CYRF69213 are provided by a single timer block. The timer block is asynchronous from the CPU clock.

Registers

Free-Running Counter

The 16-bit free-running counter is clocked by a 4/6 MHz source. It can be read in software for use as a general purpose time base. When the low order byte is read, the high order byte is registered. Reading the high order byte reads this register allowing the CPU to read the 16-bit value atomically (loads all bits at one time). The free-running timer generates an interrupt at a 1024 µs rate. It can also generate an interrupt when the free-running counter overflow occurs — every 16.384 ms. This allows extending the length of the timer in software.

Figure 15. 16-Bit Free-Running Counter Block Diagram

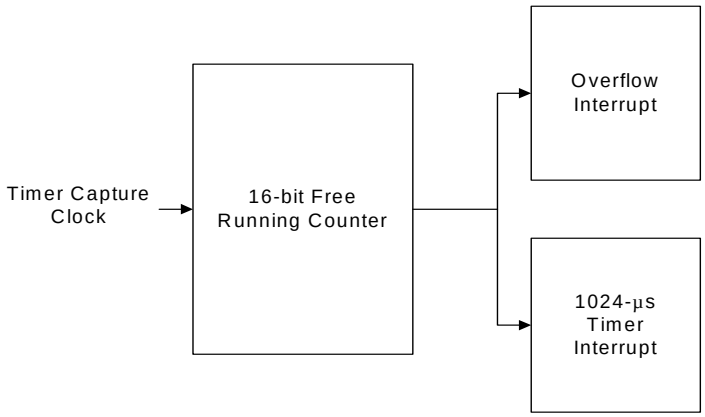


Table 64. Free-Running Timer Low Order Byte (FRTMRL) [0x20] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Free-running Timer [7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bits 7:0 Free-running Timer [7:0]

This register holds the low order byte of the 16-bit free-running timer. Reading this register causes the high order byte to be moved into a holding register allowing an automatic read of all 16 bits simultaneously.

For reads, the actual read occurs in the cycle when the low order is read. For writes, the actual time the write occurs is the cycle when the high order is written

When reading the free-running timer, the low order byte should be read first and the high order second. When writing, the low order byte should be written first then the high order byte

Table 65. Free-Running Timer High Order Byte (FRTMRH) [0x21] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Free-running Timer [15:8]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bits 7:0 Free-running Timer [15:8]

When reading the free-running timer, the low order byte should be read first and the high order second. When writing, the low order byte should be written first then the high order byte

Table 66. Programmable Interval Timer Low (PITMRL) [0x26] [R]

Bit #	7	6	5	4	3	2	1	0
Field	Prog Interval Timer [7:0]							
Read/Write	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bits 7:0 ‘Prog Interval Timer [7:0]

This register holds the low order byte of the 12-bit programmable interval timer. Reading this register causes the high order byte to be moved into a holding register allowing an automatic read of all 12 bits simultaneously

Table 67. Programmable Interval Timer High (PITMRH) [0x27] [R]

Bit #	7	6	5	4	3	2	1	0
Field	Reserved				Prog Interval Timer [11:8]			
Read/Write	–	–	–	–	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bits 7:4 Reserved

Bits 3:0 Prog Internal Timer [11:8]

This register holds the high order nibble of the 12-bit programmable interval timer. Reading this register returns the high order nibble of the 12-bit timer at the instant that the low order byte was last read

Table 68. Programmable Interval Reload Low (PIRL) [0x28] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Prog Interval [7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bits 7:0 Prog Interval [7:0]

This register holds the lower 8 bits of the timer. While writing into the 12-bit reload register, write lower byte first then the higher nibble

Table 69. Programmable Interval Reload High (PIRH) [0x29] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Reserved				Prog Interval[11:8]			
Read/Write	–	–	–	–	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bits 7:4 Reserved

Bits 3:0 Prog Interval [11:8]

This register holds the higher 4 bits of the timer. While writing into the 12-bit reload register, write lower byte first then the higher nibble

Figure 16. 16-Bit Free-Running Counter Loading Timing Diagram

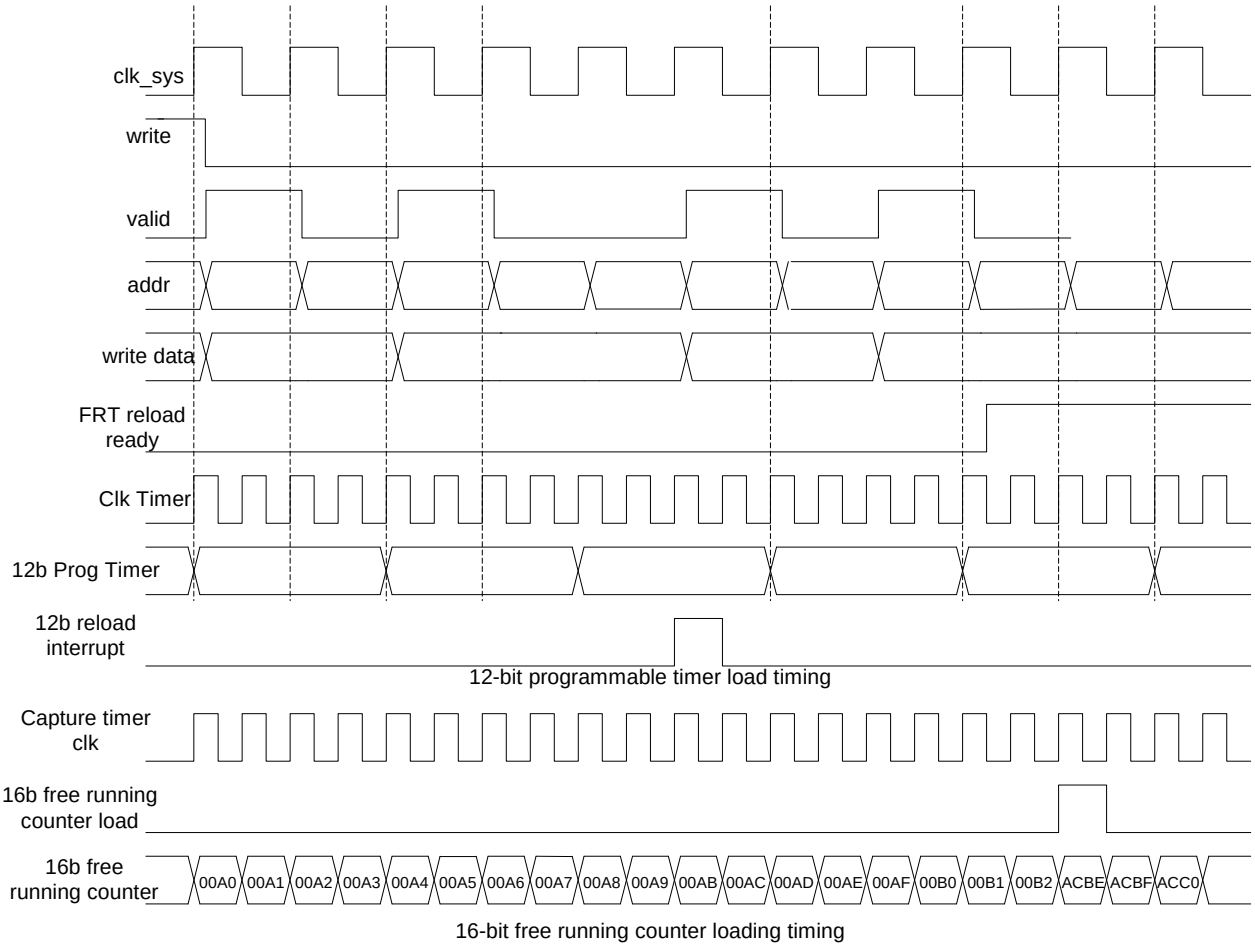
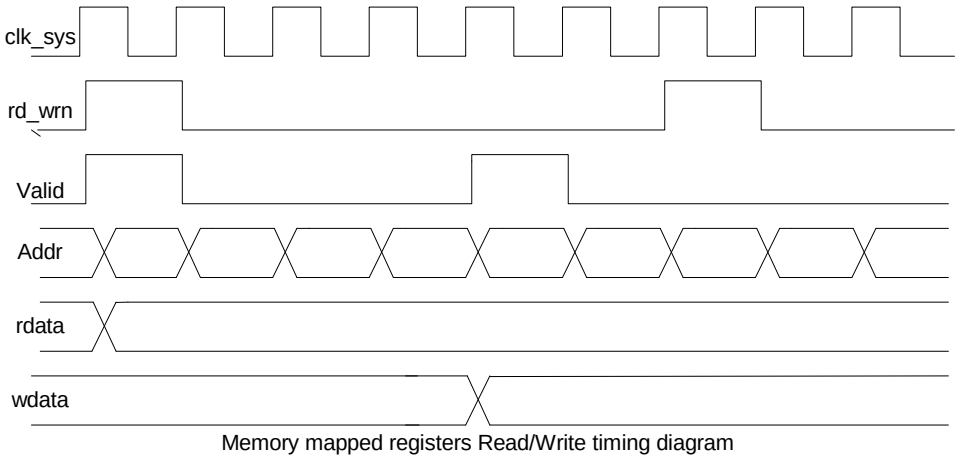


Figure 17. Memory Mapped Registers Read/Write Timing Diagram



Interrupt Controller

The interrupt controller and its associated registers allow the user's code to respond to an interrupt from almost every functional block in the CYRF69213 devices. The registers associated with the interrupt controller allow interrupts to be disabled either globally or individually. The registers also provide a mechanism by which a user may clear all pending and posted interrupts, or clear individual posted or pending interrupts.

The following table lists all interrupts and the priorities that are available in the CYRF69213.

Table 70. Interrupt Numbers, Priorities, Vectors

Interrupt Priority	Interrupt Address	Name
0	0000h	Reset
1	0004h	POR/LVD
2	0008h	INT0
3	000Ch	SPI Transmitter Empty
4	0010h	SPI Receiver Full
5	0014h	GPIO Port 0
6	0018h	GPIO Port 1
7	001Ch	INT1
8	0020h	EP0
9	0024h	EP1
10	0028h	EP2
11	002Ch	USB Reset
12	0030h	USB Active
13	0034h	1 ms Interval timer
14	0038h	Programmable Interval Timer
15	003Ch	Reserved
16	0040h	Reserved

Table 70. Interrupt Numbers, Priorities, Vectors (continued)

Interrupt Priority	Interrupt Address	Name
17	0044h	16-bit Free Running Timer Wrap
18	0048h	INT2
19	004Ch	Reserved
20	0050h	GPIO Port 2
21	0054h	Reserved
22	0058h	Reserved
23	005Ch	Reserved
24	0060h	Reserved
25	0064h	Sleep Timer

Architectural Description

An interrupt is posted when its interrupt conditions occur. This results in the flip-flop in Figure 18 clocking in a '1'. The interrupt remains posted until the interrupt is taken or until it is cleared by writing to the appropriate INT_CLRx register.

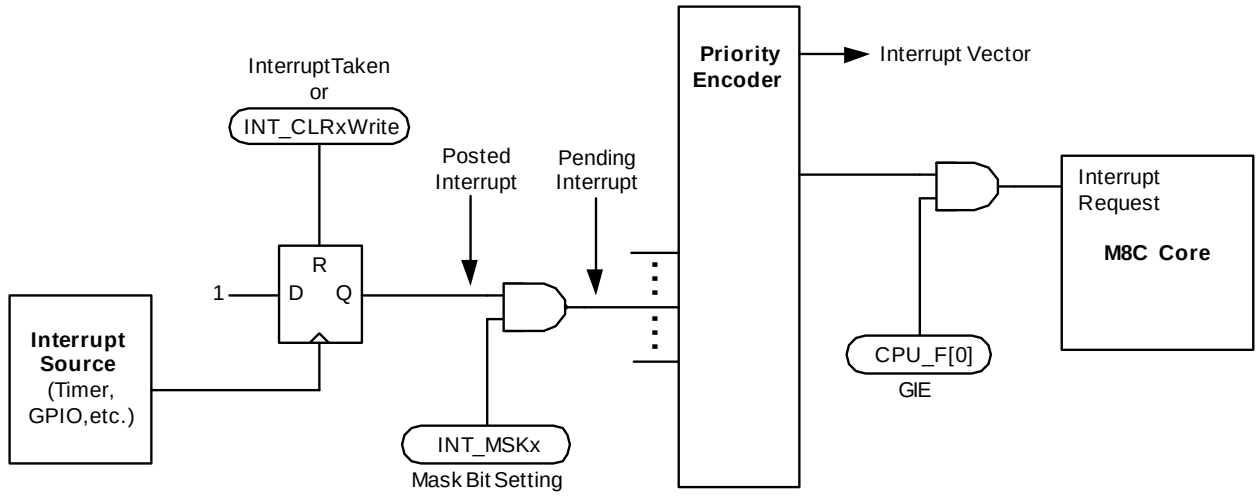
A posted interrupt is not pending unless it is enabled by setting its interrupt mask bit (in the appropriate INT_MSKx register). All pending interrupts are processed by the Priority Encoder to determine the highest priority interrupt which is taken by the M8C if the Global Interrupt Enable bit is set in the CPU_F register.

Disabling an interrupt by clearing its interrupt mask bit (in the INT_MSKx register) does not clear a posted interrupt, nor does it prevent an interrupt from being posted. It simply prevents a posted interrupt from becoming pending.

Nested interrupts can be accomplished by re-enabling interrupts inside an interrupt service routine. To do this, set the IE bit in the Flag Register.

A block diagram of the CYRF69213 Interrupt Controller is shown in Figure 18.

Figure 18. Interrupt Controller Block Diagram



Interrupt Processing

The sequence of events that occur during interrupt processing is as follows:

- An interrupt becomes active, either because:
  a. The interrupt condition occurs (for example, a timer expires).
  b. A previously posted interrupt is enabled through an update of an interrupt mask register.
  c. An interrupt is pending and GIE is set from 0 to 1 in the CPU Flag register.
  d. The GPIO interrupts are edge triggered.
- The current executing instruction finishes.
- The internal interrupt is dispatched, taking 13 cycles. During this time, the following actions occur:
  a. The MSB and LSB of Program Counter and Flag registers (CPU_PC and CPU_F) are stored onto the program stack by an automatic CALL instruction (13 cycles) generated during the interrupt acknowledge process.
  b. The PCH, PCL, and Flag register (CPU_F) are stored onto the program stack (in that order) by an automatic CALL instruction (13 cycles) generated during the interrupt acknowledge process.
  c. The CPU_F register is then cleared. Because this clears the GIE bit to 0, additional interrupts are temporarily disabled
  d. The PCH (PC[15:8]) is cleared to zero.
  e. The interrupt vector is read from the interrupt controller and its value placed into PCL (PC[7:0]). This sets the program counter to point to the appropriate address in the interrupt table (for example, 0004h for the POR/LVD interrupt).
- Program execution vectors to the interrupt table. Typically, a LJMP instruction in the interrupt table sends execution to the user's Interrupt Service Routine (ISR) for this interrupt.
- The ISR executes. Note that interrupts are disabled because GIE = 0. In the ISR, interrupts can be re-enabled if desired by setting GIE = 1 (care must be taken to avoid stack overflow).
- The ISR ends with a RETI instruction which restores the Program Counter and Flag registers (CPU_PC and CPU_F). The restored Flag register re-enables interrupts, because GIE = 1 again.
- Execution resumes at the next instruction, after the one that occurred before the interrupt. However, if there are more pending interrupts, the subsequent interrupts are processed before the next normal program instruction.

Interrupt Latency

The time between the assertion of an enabled interrupt and the start of its ISR can be calculated from the following equation.

Latency = Time for current instruction to finish + Time for internal interrupt routine to execute + Time for LJMP instruction in interrupt table to execute.

For example, if the 5 cycle JMP instruction is executing when an interrupt becomes active, the total number of CPU clock cycles before the ISR begins would be as follows:

(1 to 5 cycles for JMP to finish) + (13 cycles for interrupt routine) + (7 cycles for LJMP) = 21 to 25 cycles.

In the example above, at 24 MHz, 25 clock cycles take 1.042 μs.

Interrupt Registers

The Interrupt Registers are discussed it the following sections.

Interrupt Clear Register

The Interrupt Clear Registers (INT_CLRx) are used to enable the individual interrupt sources' ability to clear posted interrupts.

When an INT_CLRx register is read, any bits that are set indicates an interrupt has been posted for that hardware resource. Therefore, reading these registers gives the user the ability to determine all posted interrupts.

Table 71. Interrupt Clear 0 (INT_CLR0) [0xDA] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	GPIO Port 1	Sleep Timer	INT1	GPIO Port 0	SPI Receive	SPI Transmit	INT0	POR/LVD
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

When reading this register,
0 = There's no posted interrupt for the corresponding hardware
1 = Posted interrupt for the corresponding hardware present

Writing a '0' to the bits clears the posted interrupts for the corresponding hardware. Writing a '1' to the bits and to the ENSWINT (Bit 7 of the INT_MSK3 Register) posts the corresponding hardware interrupt

Table 72. Interrupt Clear 1 (INT_CLR1) [0xDB] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Reserved	Prog Interval Timer	1 ms Timer	USB Active	USB Reset	USB EP2	USB EP1	USB EP0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

When reading this register,
0 = There's no posted interrupt for the corresponding hardware
1 = Posted interrupt for the corresponding hardware present

Writing a '0' to the bits clears the posted interrupts for the corresponding hardware. Writing a '1' to the bits AND to the ENSWINT (Bit 7 of the INT_MSK3 Register) posts the corresponding hardware interrupt

Bit 7 Reserved

Table 73. Interrupt Clear 2 (INT_CLR2) [0xDC] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	GPIO Port 2	Reserved	INT2	16-bit Counter Wrap	Reserved
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

When reading this register,
0 = There's no posted interrupt for the corresponding hardware
1 = Posted interrupt for the corresponding hardware present

Writing a '0' to the bits clears the posted interrupts for the corresponding hardware. Writing a '1' to the bits AND to the ENSWINT (Bit 7 of the INT_MSK3 Register) posts the corresponding hardware interrupt

Bits 7,6,5,3,0Reserved

Interrupt Mask Registers

The Interrupt Mask Registers (INT_MSKx) are used to enable the individual interrupt sources' ability to create pending interrupts.

There are four Interrupt Mask Registers (INT_MSK0, INT_MSK1, INT_MSK2, and INT_MSK3), which may be referred to in general as INT_MSKx. If cleared, each bit in an INT_MSKx register prevents a posted interrupt from becoming a pending interrupt (input to the priority encoder). However, an interrupt can still post even if its mask bit is zero. All INT_MSKx bits are independent of all other INT_MSKx bits.

If an INT_MSKx bit is set, the interrupt source associated with that mask bit may generate an interrupt that becomes a pending interrupt.

The Enable Software Interrupt (ENSWINT) bit in INT_MSK3[7] determines the way an individual bit value written to an INT_CLRx register is interpreted. When is cleared, writing 1's to an INT_CLRx register has no effect. However, writing 0's to an INT_CLRx register, when ENSWINT is cleared, causes the corresponding interrupt to clear. If the ENSWINT bit is set, any 0's written to the INT_CLRx registers are ignored. However, 1's written to an INT_CLRx register, while ENSWINT is set, causes an interrupt to post for the corresponding interrupt.

Software interrupts can aid in debugging interrupt service routines by eliminating the need to create system level interactions that are sometimes necessary to create a hardware-only interrupt.

Table 74. Interrupt Mask 3 (INT_MSK3) [0xDE] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	ENSWINT	Reserved						
Read/Write	R/W	–	–	–	–	–	–	–
Default	0	0	0	0	0	0	0	0

Bit 7 Enable Software Interrupt (ENSWINT)
0 = Disable. Writing 0's to an INT_CLRx register, when ENSWINT is cleared, causes the corresponding interrupt to clear
1 = Enable. Writing 1's to an INT_CLRx register, when ENSWINT is set, causes the corresponding interrupt to post

Bits 6:0 Reserved

Table 75. Interrupt Mask 2 (INT_MSK2) [0xDF] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	GPIO Port 2 Int Enable	Reserved	INT2 Int Enable	16-bit Counter Wrap Int Enable	Reserved
Read/Write	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit 7 Reserved

Bit 6 Reserved

Bit 5 Reserved

Bit 4 GPIO Port 2 Interrupt Enable
0 = Mask GPIO Port 2 interrupt
1 = Unmask GPIO Port 2 interrupt

Bit 3 Reserved

Bit 2 INT2 Interrupt Enable
0 = Mask INT2 interrupt
1 = Unmask INT2 interrupt

Bit 1 16-bit Counter Wrap Interrupt Enable
0 = Mask 16-bit Counter Wrap interrupt
1 = Unmask 16-bit Counter Wrap interrupt

Bit 0 Reserved

Table 76. Interrupt Mask 1 (INT_MSK1) [0xE1] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Reserved	Prog Interval Timer Int Enable	1 ms Timer Int Enable	USB Active Int Enable	USB Reset Int Enable	USB EP2 Int Enable	USB EP1 Int Enable	USB EP0 Int Enable
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit 7 Reserved

Bit 6 Prog Interval Timer Interrupt Enable
0 = Mask Prog Interval Timer interrupt
1 = Unmask Prog Interval Timer interrupt

Bit 5 1 ms Timer Interrupt Enable
0 = Mask 1 ms interrupt
1 = Unmask 1 ms interrupt

Bit 4 USB Active Interrupt Enable
0 = Mask USB Active interrupt
1 = Unmask USB Active interrupt

Bit 3 USB Reset Interrupt Enable
0 = Mask USB Reset interrupt
1 = Unmask USB Reset interrupt

Bit 2 USB EP2 Interrupt Enable
0 = Mask EP2 interrupt
1 = Unmask EP2 interrupt

Bit 1 USB EP1 Interrupt Enable
0 = Mask EP1 interrupt
1 = Unmask EP1 interrupt

Bit 0 USB EP0 Interrupt Enable
0 = Mask EP0 interrupt
1 = Unmask EP0 interrupt

Table 77. Interrupt Mask 0 (INT_MSK0) [0xE0] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	GPIO Port 1 Int Enable	Sleep Timer Int Enable	INT1 Int Enable	GPIO Port 0 Int Enable	SPI Receive Int Enable	SPI Transmit Int Enable	INT0 Int Enable	POR/LVD Int Enable
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit 7 GPIO Port 1 Interrupt Enable
0 = Mask GPIO Port 1 interrupt
1 = Unmask GPIO Port 1 interrupt

Bit 6 Sleep Timer Interrupt Enable
0 = Mask Sleep Timer interrupt
1 = Unmask Sleep Timer interrupt

Bit 5 INT1 Interrupt Enable
0 = Mask INT1 interrupt
1 = Unmask INT1 interrupt

Bit 4 GPIO Port 0 Interrupt Enable
0 = Mask GPIO Port 0 interrupt
1 = Unmask GPIO Port 0 interrupt

Bit 3 SPI Receive Interrupt Enable
0 = Mask SPI Receive interrupt
1 = Unmask SPI Receive interrupt

Bit 2 SPI Transmit Interrupt Enable
0 = Mask SPI Transmit interrupt
1 = Unmask SPI Transmit interrupt

Bit 1 INT0 Interrupt Enable
0 = Mask INT0 interrupt
1 = Unmask INT0 interrupt

Bit 0 POR/LVD Interrupt Enable
0 = Mask POR/LVD interrupt
1 = Unmask POR/LVD interrupt

Interrupt Vector Clear Register

Table 78. Interrupt Vector Clear Register (INT_VC) [0xE2] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Pending Interrupt [7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

The Interrupt Vector Clear Register (INT_VC) holds the interrupt vector for the highest priority pending interrupt when read, and when written clears all pending interrupts

Bits 7:0 Pending Interrupt [7:0]
8-bit data value holds the interrupt vector for the highest priority pending interrupt. Writing to this register clears all pending interrupts

USB Transceiver

USB Transceiver Configuration

Table 79. USB Transceiver Configure Register (USBXCR) [0x74] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	USB Pull up Enable	Reserved						USB Force State
Read/Write	R/W	–	–	–	–	–	–	R/W
Default	0	0	0	0	0	0	0	0

Bit 7 USB Pull up Enable
0 = Disable the pull up resistor on D–
1 = Enable the pull up resistor on D–. This pull up is to V_{CC} IF VREG is not enabled or to the internally generated 3.3 V when VREG is enabled. This bit should be cleared in sleep mode.

Bits 6:1 Reserved

Bit 0 USB Force State
This bit allows the state of the USB I/O pins DP and D+ to be forced to a state while USB is enabled
0 = Disable USB Force State
1 = Enable USB Force State. Allows the D– and D+ pins to be controlled by P1.1 and P1.0 respectively when the USBIO is in USB mode. Refer to Table 48 for more information

Note The USB transceiver has a dedicated 3.3 V regulator for USB signalling purposes and to provide for the 1.5K D– pull up. Unlike the other 3.3 V regulator, this regulator cannot be controlled/accessed by firmware. When the device is suspended, this regulator is disabled along with the bandgap (which provides the reference voltage to the regulator) and the D– line is pulled up to 5 V through an alternate 6.5K resistor. During wakeup following a suspend, the band gap and the regulator are switched on in any order. Under an extremely rare case when the device wakes up following a bus reset condition and the voltage regulator and the band gap turn on in that particular order, there is possibility of a glitch/low pulse occurring on the D– line. The host can misinterpret this as a deattach condition. This condition, although rare, can be avoided by keeping the bandgap circuitry enabled during sleep. This is achieved by setting the 'No Buzz' bit, bit[5] in the OSC_CR0 register. This is an issue only if the device is put to sleep during a bus reset condition

VREG Control

Table 80. VREG Control Register (VREGCR) [0x73] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Reserved						Keep Alive	VREG Enable
Read/Write	–	–	–	–	–	–	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bits 7:2 Reserved

Bit 1 Keep Alive
Keep Alive when set allows the voltage regulator to source up to 20 µA of current when voltage regulator is disabled, P12CR[0],P12CR[7] should be cleared.
0 = Disabled
1 = Enabled

Bit 0 VREG Enable
This bit turns on the 3.3 V voltage regulator. The voltage regulator only functions within specifications when V_{CC} is above 4.35 V. This block should not be enabled when V_{CC} is below 4.35 V — although no damage or irregularities occurs if it is enabled below 4.35 V
0 = Disable the 3.3 V voltage regulator output on the VREG/P1.2 pin
1 = Enable the 3.3 V voltage regulator output on the VREG/P1.2 pin. GPIO functionality of P1.2 is disabled

Note Use of the alternate drive on pins P1.3–P1.6 requires that the VREG Enable bit be set to enable the regulator and provide the alternate voltage

USB Serial Interface Engine (SIE)

The SIE allows the microcontroller to communicate with the USB host at low speed data rates (1.5 Mbps). The SIE simplifies the interface between the microcontroller and USB by incorporating hardware that handles the following USB bus activity independently of the microcontroller:

- Translating the encoded received data and formatting the data to be transmitted on the bus
- CRC checking and generation. Flagging the microcontroller if errors exist during transmission
- Address checking. Ignoring the transactions not addressed to the device
- Sending appropriate ACK/NAK/STALL handshakes
- Identifying token type (SETUP, IN, or OUT). Setting the appropriate token bit after a valid token is received
- Placing valid received data in the appropriate endpoint FIFOs
- Sending and updating the data toggle bit (Data1/0)
- Bit stuffing/unstuffing.

Firmware is required to handle the rest of the USB interface with the following tasks:

- Coordinate enumeration by decoding USB device requests
- Fill and empty the FIFOs
- Suspend/Resume coordination
- Verify and select Data toggle values

USB Device

Table 81. USB Device Address (USBCR) [0x40] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	USB Enable	Device Address[6:0]						
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

The content of this register is cleared when a USB Bus Reset condition occurs

Bit 7 USB Enable
This bit must be enabled by firmware before the serial interface engine (SIE) responds to USB traffic at the address specified in Device Address [6:0]. When this bit is cleared, the USB transceiver enters power down state. User's firmware should clear this bit prior to entering sleep mode to save power
0 = Disable USB device address and put the USB transceiver into power down state
1 = Enable USB device address and put the USB transceiver into normal operating mode

Bits 6:0 Device Address [6:0]
These bits must be set by firmware during the USB enumeration process (for example, SetAddress) to the non-zero address assigned by the USB host

Table 82. Endpoint 0, 1, and 2 Count (EP0CNT–EP2CNT) [0x41, 0x43, 0x45] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Data Toggle	Data Valid	Reserved		Byte Count[3:0]			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit 7 Data Toggle
This bit selects the DATA packet's toggle state. For IN transactions, firmware must set this bit to the select the transmitted Data Toggle. For OUT or SETUP transactions, the hardware sets this bit to the state of the received Data Toggle bit.
0 = DATA0
1 = DATA1

Bit 6 Data Valid
This bit is used for OUT and SETUP tokens only. This bit is cleared to ‘0’ if CRC, bitstuff, or PID errors have occurred. This bit does not update for some endpoint mode settings
0 = Data is invalid. If enabled, the endpoint interrupt occurs even if invalid data is received
1 = Data is valid

Bits 5:4 Reserved

Bits 3:0 Byte Count Bit [3:0]
Byte Count Bits indicate the number of data bytes in a transaction: For IN transactions, firmware loads the count with the number of bytes to be transmitted to the host from the endpoint FIFO. Valid values are 0 to 8 inclusive. For OUT or SETUP transactions, the count is updated by hardware to the number of data bytes received, plus 2 for the CRC bytes. Valid values are 2–10 inclusive.

For Endpoint 0 Count Register, whenever the count updates from a SETUP or OUT transaction, the count register locks and cannot be written by the CPU. Reading the register unlocks it. This prevents firmware from overwriting a status update on it

Endpoint 0 Mode

Because both firmware and the SIE are allowed to write to the Endpoint 0 Mode and Count Registers the SIE provides an interlocking mechanism to prevent accidental overwriting of data.

When the SIE writes to these registers they are locked and the processor cannot write to them until after it has read them. Writing to this register clears the upper four bits regardless of the value written.

Table 83. Endpoint 0 Mode (EP0MODE) [0x44] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Setup Received	IN Received	OUT Received	ACK'd Trans	Mode[3:0]			
Read/Write	R/C[3]	R/C[3]	R/C[3]	R/C[3]	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit 7 SETUP Received
This bit is set by hardware when a valid SETUP packet is received. It is forced HIGH from the start of the data packet phase of the SETUP transactions until the end of the data phase of a control write transfer and cannot be cleared during this interval. While this bit is set to '1', the CPU cannot write to the EP0 FIFO. This prevents firmware from overwriting an incoming SETUP transaction before firmware has a chance to read the SETUP data
This bit is cleared by any non-locked writes to the register
0 = No SETUP received
1 = SETUP received

Bit 6 IN Received
This bit, when set, indicates a valid IN packet has been received. This bit is updated to '1' after the host acknowledges an IN data packet.When clear, it indicates that either no IN has been received or that the host didn't acknowledge the IN data by sending an ACK handshake
This bit is cleared by any non-locked writes to the register.
0 = No IN received
1 = IN received

Bit 5 OUT Received
This bit, when set, indicates a valid OUT packet has been received and ACKed. This bit is updated to '1' after the last received packet in an OUT transaction. When clear, it indicates no OUT received
This bit is cleared by any non-locked writes to the register
0 = No OUT received
1 = OUT received

Bit 4 ACK'd Transaction
The ACK'd transaction bit is set whenever the SIE engages in a transaction to the register's endpoint that completes with a ACK packet
This bit is cleared by any non-locked writes to the register
1 = The transaction completes with an ACK
0 = The transaction does not complete with an ACK

Bits 3:0 Mode [3:0]
The endpoint modes determine how the SIE responds to USB traffic that the host sends to the endpoint. The mode controls how the USB SIE responds to traffic and how the USB SIE changes the mode of that endpoint as a result of host packets to the endpoint

Table 84. Endpoint 1 and 2 Mode (EP1MODE – EP2MODE) [0x45, 0x46] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Stall	Reserved	NAK Int Enable	ACK'd Transaction	Mode[3:0]			
Read/Write	R/W	R/W	R/W	R/C (Note 3)	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit 7 Stall
When this bit is set the SIE stalls an OUT packet if the Mode Bits are set to ACK-OUT, and the SIE stalls an IN packet if the mode bits are set to ACK-IN. This bit must be clear for all other modes

Bit 6 Reserved

Bit 5 NAK Int Enable
This bit, when set, causes an endpoint interrupt to be generated even when a transfer completes with a NAK. Unlike enCoRe, CYRF69213 family members do not generate an endpoint interrupt under these conditions unless this bit is set
0 = Disable interrupt on NAK'd transactions
1 = Enable interrupt on NAK'd transaction

Bit 4 ACK'd Transaction
The ACK'd transaction bit is set whenever the SIE engages in a transaction to the register's endpoint that completes with an ACK packet
This bit is cleared by any writes to the register
0 = The transaction does not complete with an ACK
1 = The transaction completes with an ACK

Bits 3:0 Mode [3:0]
The endpoint modes determine how the SIE responds to USB traffic that the host sends to the endpoint. The mode controls how the USB SIE responds to traffic and how the USB SIE changes the mode of that endpoint as a result of host packets to the endpoint.

Note When the SIE writes to the EP1MODE or the EP2MODE register it blocks firmware writes to the EP2MODE or the EP1MODE registers, respectively (if both writes occur in the same clock cycle). This is because the design employs only one common 'update' signal for both EP1MODE and EP2MODE registers. Thus, when SIE writes to the EP1MODE register, the update signal is set and this prevents firmware writes to EP2MODE register. SIE writes to the endpoint mode registers have higher priority than firmware writes. This mode register write block situation can put the endpoints in incorrect modes. Firmware must read the EP1/2MODE registers immediately following a firmware write and rewrite if the value read is incorrect

Endpoint Data Buffers

The three data buffers are used to hold data for both IN and OUT transactions. Each data buffer is 8 bytes long. The reset values of the Endpoint Data Registers are unknown. Unlike past enCoRe parts the USB data buffers are only accessible in the I/O space of the processor.

Table 85. Endpoint 0 Data (EP0DATA) [0x50-0x57] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Endpoint 0 Data Buffer [7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	Unknown	Unknown	Unknown	Unknown	Unknown	Unknown	Unknown	Unknown

The Endpoint 0 buffer is comprised of 8 bytes located at address 0x50 to 0x57

Table 86. Endpoint 1 Data (EP1DATA) [0x58-0x5F] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Endpoint 1 Data Buffer [7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	Unknown	Unknown	Unknown	Unknown	Unknown	Unknown	Unknown	Unknown

The Endpoint 1buffer is comprised of 8 bytes located at address 0x58 to 0x5F

Table 87. Endpoint 2 Data (EP2DATA) [0x60-0x67] [R/W]

Bit #	7	6	5	4	3	2	1	0
Field	Endpoint 2 Data Buffer [7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	Unknown	Unknown	Unknown	Unknown	Unknown	Unknown	Unknown	Unknown

The Endpoint 2 buffer is comprised of 8 bytes located at address 0x60 to 0x67

USB Mode Tables

Mode	Encoding	SETUP	IN	OUT	Comments
DISABLE	0000	Ignore	Ignore	Ignore	Ignore all USB traffic to this endpoint. Used by Data and Control endpoints
NAK IN/OUT	0001	Accept	NAK	NAK	NAK IN and OUT token. Control endpoint only
STATUS OUT ONLY	0010	Accept	STALL	Check	STALL IN and ACK zero byte OUT. Control endpoint only
STALL IN/OUT	0011	Accept	STALL	STALL	STALL IN and OUT token. Control endpoint only
STATUS IN ONLY	0110	Accept	TX0 byte	STALL	STALL OUT and send zero byte data for IN token. Control endpoint only
ACK OUT – STATUS IN	1011	Accept	TX0 byte	ACK	ACK the OUT token or send zero byte data for IN token. Control endpoint only
ACK IN – STATUS OUT	1111	Accept	TX Count	Check	Respond to IN data or Status OUT. Control endpoint only
NAK OUT	1000	Ignore	Ignore	NAK	Send NAK handshake to OUT token. Data endpoint only
ACK OUT (STALL = 0)	1001	Ignore	Ignore	ACK	This mode is changed by the SIE to mode 1000 on issuance of ACK handshake to an OUT. Data endpoint only
ACK OUT (STALL = 1)	1001	Ignore	Ignore	STALL	STALL the OUT transfer
NAK IN	1100	Ignore	NAK	Ignore	Send NAK handshake for IN token. Data endpoint only
ACK IN (STALL = 0)	1101	Ignore	TX Count	Ignore	This mode is changed by the SIE to mode 1100 after receiving ACK handshake to an IN data. Data endpoint only
ACK IN (STALL = 1)	1101	Ignore	STALL	Ignore	STALL the IN transfer. Data endpoint only
Reserved	0101	Ignore	Ignore	Ignore	These modes are not supported by SIE. Firmware should not use this mode in Control and Data endpoints
Reserved	0111	Ignore	Ignore	Ignore	
Reserved	1010	Ignore	Ignore	Ignore	
Reserved	0100	Ignore	Ignore	Ignore	
Reserved	1110	Ignore	Ignore	Ignore	

Mode Column

The 'Mode' column contains the mnemonic names given to the modes of the endpoint. The mode of the endpoint is determined by the four-bit binaries in the 'Encoding' column as discussed in the following section. The Status IN and Status OUT represent the status IN or OUT stage of the control transfer.

Encoding Column

The contents of the 'Encoding' column represent the Mode Bits [3:0] of the Endpoint Mode Registers (Table 83 on page 59 and Table 84 on page 60). The endpoint modes determine how the SIE responds to different tokens that the host sends to the endpoints. For example, if the Mode Bits [3:0] of the Endpoint 0 Mode Register are set to '0001', which is NAK IN/OUT mode, the SIE sends an ACK handshake in response to SETUP tokens and NAK any IN or OUT tokens.

SETUP, IN, and OUT Columns

Depending on the mode specified in the 'Encoding' column, the 'SETUP', 'IN', and 'OUT' columns contain the SIE's responses when the endpoint receives SETUP, IN, and OUT tokens, respectively.

A 'Check' in the Out column means that upon receiving an OUT token the SIE checks to see whether the OUT is of zero length and has a Data Toggle (Data1/0) of 1. If these conditions are true, the SIE responds with an ACK. If any of the above conditions is not met, the SIE responds with either a STALL or Ignore.

A 'TX Count' entry in the IN column means that the SIE transmits the number of bytes specified in the Byte Count Bit [3:0] of the Endpoint Count Register (Table 82 on page 58) in response to any IN token.

Details of Mode for Differing Traffic Conditions

SIE	Bus Event				SIE	EP0 Mode Register					EP0 Count Register			EP0	Interrupt	Comments
Mode	Token	Count	Dval	D0/1	Response	S	I	O	A	MODE	DTOG	DVAL	COUNT	FIFO		
Control Endpoint																
DISABLED																
0000	x	x	x	x												Ignore All
STALL_IN_OUT																
0011	SETUP	> 10	x	x										junk		Ignore
0011	SETUP	≤ 10	invalid	x										junk		Ignore
0011	SETUP	≤ 10	valid	x	ACK	1			1	0001	update	1	update	data	Yes	ACK SETUP
0011	IN	x	x	x	STALL											Stall IN
0011	OUT	> 10	x	x												Ignore
0011	OUT	≤ 10	invalid	x												Ignore
0011	OUT	≤ 10	valid	x	STALL											Stall OUT
NAK_IN_OUT																
0001	SETUP	> 10	x	x										junk		Ignore
0001	SETUP	≤ 10	invalid	x										junk		Ignore
0001	SETUP	≤ 10	valid	x	ACK	1			1	0001	update	1	update	data	Yes	ACK SETUP
0001	IN	x	x	x	NAK											NAK IN
0001	OUT	>10	x	x												Ignore
0001	OUT	≤ 10	invalid	x												Ignore
0001	OUT	≤ 10	valid	x	NAK											NAK OUT
ACK_IN_STATUS_OUT																
1111	SETUP	> 10	x	x										junk		Ignore
1111	SETUP	≤ 10	invalid	x										junk		Ignore
1111	SETUP	≤ 10	valid	x	ACK	1			1	0001	update	1	update	data	Yes	ACK SETUP
1111	IN	x	x	x	TX											Host Not ACK'd
1111	IN	x	x	x	TX		1		1	0001					Yes	Host ACK'd
1111	OUT	> 10	x	x												Ignore
1111	OUT	≤ 10	invalid	x												Ignore
1111	OUT	≤ 10, <>2	valid	x	STALL					0011					Yes	Bad Status
1111	OUT	2	valid	0	STALL					0011					Yes	Bad Status
1111	OUT	2	valid	1	ACK			1	1	0010	1	1	2		Yes	Good Status
STATUS_OUT																
0010	SETUP	>10	x	x										junk		Ignore
0010	SETUP	≤ 10	invalid	x										junk		Ignore
0010	SETUP	≤ 10	valid	x	ACK	1			1	0001	update	1	update	data	Yes	ACK SETUP
0010	IN	x	x	x	STALL					0011					Yes	Stall IN
0010	OUT	>10	x	x												Ignore
0010	OUT	≤ 10	invalid	x												Ignore
0010	OUT	≤ 10, <>2	valid	x	STALL					0011					Yes	Bad Status

Details of Mode for Differing Traffic Conditions (continued)

SIE	Bus Event				SIE	EP0 Mode Register					EP0 Count Register			EP0	Interrupt	Comments
Mode	Token	Count	Dval	D0/1	Response	S	I	O	A	MODE	DTOG	DVAL	COUNT	FIFO		
0010	OUT	2	valid	0	STALL					0011					Yes	Bad Status
0010	OUT	2	valid	1	ACK			1	1		1	1	2		Yes	Good Status
ACK_OUT_STATUS_IN																
1011	SETUP	>10	x	x										junk		Ignore
1011	SETUP	≤ 10	invalid	x										junk		Ignore
1011	SETUP	≤ 10	valid	x	ACK	1			1	0001	update	1	update	data	Yes	ACK SETUP
1011	IN	x	x	x	TX 0											Host Not ACK'd
1011	IN	x	x	x	TX 0		1		1	0011					Yes	Host ACK'd
1011	OUT	>10	x	x										junk		Ignore
1011	OUT	≤ 10	invalid	x										junk		Ignore
1011	OUT	≤ 10	valid	x	ACK			1	1	0001	update	1	update	data	Yes	Good OUT
STATUS_IN																
0110	SETUP	>10	x	x										junk		Ignore
0110	SETUP	≤ 10	invalid	x										junk		Ignore
0110	SETUP	≤ 10	valid	x	ACK	1			1	0001	update	1	update	data	Yes	ACK SETUP
0110	IN	x	x	x	TX 0											Host Not ACK'd
0110	IN	x	x	x	TX 0		1		1	0011					Yes	Host ACK'd
0110	OUT	>10	x	x												Ignore
0110	OUT	≤ 10	invalid	x												Ignore
0110	OUT	≤ 10	valid	x	STALL					0011					Yes	Stall OUT
Data Out Endpoints																
ACK OUT (STALL Bit = 0)																
1001	IN	x	x	x												Ignore
1001	OUT	> MAX	x	x										junk		Ignore
1001	OUT	≤ MAX	invalid	invalid										junk		Ignore
1001	OUT	≤ MAX	valid	valid	ACK				1	1000	update	1	update	data	Yes	ACK OUT
ACK OUT (STALL Bit = 1)																
1001	IN	x	x	x												Ignore
1001	OUT	> MAX	x	x												Ignore
1001	OUT	≤ MAX	invalid	invalid												Ignore
1001	OUT	≤ MAX	valid	valid	STALL											Stall OUT
NAK OUT																
1000	IN	x	x	x												Ignore
1000	OUT	> MAX	x	x												Ignore
1000	OUT	≤ MAX	invalid	invalid												Ignore
1000	OUT	≤ MAX	valid	valid	NAK										If Enabled	NAK OUT

Details of Mode for Differing Traffic Conditions (continued)

SIE	Bus Event				SIE	EP0 Mode Register					EP0 Count Register			EP0	Interrupt	Comments
Mode	Token	Count	Dval	D0/1	Response	S	I	O	A	MODE	DTOG	DVAL	COUNT	FIFO		
Data In Endpoints																
ACK IN (STALL Bit = 0)																
1101	OUT	x	x	x												Ignore
1101	IN	x	x	x												Host Not ACK'd
1101	IN	x	x	x	TX				1	1100					Yes	Host ACK'd
ACK IN (STALL Bit = 1)																
1101	OUT	x	x	x												Ignore
1101	IN	x	x	x	STALL											Stall IN
NAK IN																
1100	OUT	x	x	x												Ignore
1100	IN	x	x	x	NAK										If Enabled	NAK IN

Register Summary

Addr	Name	7	6	5	4	3	2	1	0	R/W	Default
00	P0DATA	P0.7	Reserved	Reserved	P0.4 / INT2	P0.3 / INT1	Reserved	P0.1	Reserved	b--bbb--	00000000
01	P1DATA	P1.7	P1.6/SMISO	P1.5/SMOSI	P1.4 / SCLK	P1.3 / SSEL	P1.2 / VREG	P1.1/D–	P1.0/D+	bbbbbbbb	00000000
02	P2DATA	Res						P2.1–P2.0		bbbbbbbb	00000000
06	P01CR	Reserved	Int Enable	Int Act Low	TTL Thresh	High Sink	Open Drain	Pull up Enable	Output Enable	--bbbbbb	00000000
08–09	P03CR–P04CR	Reserved	Reserved	Int Act Low	TTL Thresh	Reserved	Open Drain	Pull up Enable	Output Enable	--bbbbbb	00000000
0C	P07CR	Reserved	Int Enable	Int Act Low	TTL Thresh	Reserved	Open Drain	Pull up Enable	Output Enable	-bbbbbbb	00000000
0D	P10CR	Reserved	Int Enable	Int Act Low	Reserved			5K pull up enable	Output Enable	-bb----b	00000000
0E	P11CR	Reserved	Int Enable	Int Act Low	Reserved		Open Drain	Reserved	Output Enable	-bb--b-b	00000000
0F	P12CR	CLK Output	Int Enable	Int Act Low	TTL Thresh	Reserved	Open Drain	Pull up Enable	Output Enable	bbbbbbbb	00000000
10	P13CR	Reserved	Int Enable	Int Act Low	3.3 V Drive	High Sink	Open Drain	Pull up Enable	Output Enable	-bbbbbbb	00000000
11–13	P14CR–P16CR	SPI Use	Int Enable	Int Act Low	3.3 V Drive	High Sink	Open Drain	Pull up Enable	Output Enable	bbbbbbbb	00000000
14	P17CR	Reserved	Int Enable	Int Act Low	TTL Thresh	High Sink	Open Drain	Pull up Enable	Output Enable	-bbbbbbb	00000000
15	P2CR	Reserved	Int Enable	Int Act Low	TTL Thresh	Reserved	Open Drain	Pull up Enable	Output Enable	-bbbbbbb	00000000
20	FRTMRL	Free-Running Timer [7:0]								bbbbbbbb	00000000
21	FRTMRH	Free-Running Timer [15:8]								bbbbbbbb	00000000
26	PITMRL	Prog Interval Timer [7:0]								bbbbbbbb	00000000
27	PITMRH	Reserved				Prog Interval Timer [11:8]				----bbbb	00000000
28	PIRL	Prog Interval [7:0]								bbbbbbbb	00000000
29	PIRH	Reserved				Prog Interval [11:8]				----bbbb	00000000
30	CPUCLKCR	Reserved								--------	00010000
31	ITMRCLKCR	TCAPCLK Divider		TCAPCLK Select		ITMRCLK Divider		ITMRCLK Select		bbbbbbbb	10001111
32	CLKIOCR	Reserved			Reserved			CLKOUT Select		---bbbbb	00000000
34	IOSCTR	foffset[2:0]			Gain[4:0]					bbbbbbbb	000ddddd
35	XOSCTR	Reserved			Reserved			Reserved	Mode	---bbb-b	000ddd0d
36	LPOSCTR	32 kHz Low Power	Reserved	32 kHz Bias Trim [1:0]	32 kHz Freq Trim [3:0]					b-bbbbbb	dddddddd
39	OSCLCKCR	Reserved						Fine Tune Only	USB Osclock Disable	------bb	00000000
3C	SPIDATA	SPIData[7:0]								bbbbbbbb	00000000
3D	SPICR	Swap	LSB First	Comm Mode		CPOL	CPHA	SCLK Select		bbbbbbbb	00000000
40	USBCR	USB Enable	Device Address[6:0]							bbbbbbbb	00000000

Register Summary (continued)

Addr	Name	7	6	5	4	3	2	1	0	R/W	Default
41	EP0CNT	Data Toggle	Data Valid	Reserved		Byte Count[3:0]				bbbbbbbb	00000000
42	EP1CNT	Data Toggle	Data Valid	Reserved		Byte Count[3:0]				bbbbbbbb	00000000
43	EP2CNT	Data Toggle	Data Valid	Reserved		Byte Count[3:0]				bbbbbbbb	00000000
44	EP0MODE	Setup rcv'd	IN rcv'd	OUT rcv'd	ACK'd trans	Mode[3:0]				ccccbbbb	00000000
45	EP1MODE	Stall	Reserved	NAK Int Enable	Ack'd trans	Mode[3:0]				b-bcbbbb	00000000
46	EP2MODE	Stall	Reserved	NAK Int Enable	Ack'd trans	Mode[3:0]				b-bcbbbb	00000000
50–57	EP0DATA	Endpoint 0 Data Buffer [7:0]								bbbbbbbb	????????
58–5F	EP1DATA	Endpoint 1 Data Buffer [7:0]								bbbbbbbb	????????
60–67	EP2DATA	Endpoint 2 Data Buffer [7:0]								bbbbbbbb	????????
73	VREGCR	Reserved						Keep Alive	VREG Enable	------bb	00000000
74	USBXCR	USB Pull up Enable	Reserved						USB Force State	b------b	00000000
DA	INT_CLR0	GPIO Port 1	Sleep Timer	INT1	GPIO Port 0	SPI Receive	SPI Transmit	INT0	POR/LVD	bbbbbbbb	00000000
DB	INT_CLR1	Reserved	Prog Interval Timer	1-ms Timer	USB Active	USB Reset	USB EP2	USB EP1	USB EP0	-bbbbbbb	00000000
DC	INT_CLR2	Reserved	Reserved	Reserved	GPIO Port 2	Reserved	INT2	16-bit Counter Wrap	Reserved	-bbbbbb-	00000000
DE	INT_MSK3	ENSWINT	Reserved							b-------	00000000
DF	INT_MSK2	Reserved	Reserved	Reserved	GPIO Port 2 Int Enable	Reserved	INT2 Int Enable	16-bit Counter Wrap Int Enable	Reserved	---bbbb-	00000000
E0	INT_MSK0	GPIO Port 1 Int Enable	Sleep Timer Int Enable	INT1 Int Enable	GPIO Port 0 Int Enable	SPI Receive Int Enable	SPI Transmit Int Enable	INT0 Int Enable	POR/LVD Int Enable	bbbbbbbb	00000000
E1	INT_MSK1	Reserved	Prog Interval Timer Int Enable	1-ms Timer Int Enable	USB Active Int Enable	USB Reset Int Enable	USB EP2 Int Enable	USB EP1 Int Enable	USB EP0 Int Enable	bbbbbbbb	00000000
E2	INT_VC	Pending Interrupt [7:0]								bbbbbbbb	00000000
E3	RESWDT	Reset Watchdog Timer [7:0]								wwwwwwww	00000000
--	CPU_A	Temporary Register T1 [7:0]								--------	00000000
--	CPU_X	X[7:0]								--------	00000000
--	CPU_PCL	Program Counter [7:0]								--------	00000000
--	CPU_PCH	Program Counter [15:8]								--------	00000000
--	CPU_SP	Stack Pointer [7:0]								--------	00000000
--	CPU_F	Reserved			XOI	Super	Carry	Zero	Global IE	---brwww	00000010
FF	CPU_SCR	GIES	Reserved	WDRS	PORS	Sleep	Reserved	Reserved	Stop	r-ccb--b	00010000

Register Summary (continued)

Addr	Name	7	6	5	4	3	2	1	0	R/W	Default
1E0	OSC_CR0	Reserved		No Buzz	Sleep Timer [1:0]		CPU Speed [2:0]			--bbbbbb	00000000
1E3	LVDCR	Reserved		PORLEV[1:0]		Reserved	VM[2:0]			--bb-bbbb	00000000
1E4	VLTCMP	Reserved						LVD	PPOR	------rr	00000000
1EB	ECO_TR	Sleep Duty Cycle [1:0]		Reserved						bb------	00000000

LEGEND
In the R/W column,
b = Both Read and Write
r = Read Only
w = Write Only
c = Read/Clear
? = Unknown
d = calibration value. Should not change during normal use

Radio Function Register Descriptions

All registers are read and writeable, except where noted. Registers may be written to or read from either individually or in sequential groups. A single-byte read or write reads or writes from the addressed register. Incrementing burst read and write is a sequence that begins with an address, and then reads or writes to/from each register in address order for as long as clocking continues. It is possible to repeatedly read (poll) a single register using a non-incrementing burst read. These registers are managed and configured over SPI by the user firmware running in the microcontroller function.

Table 88. Register Map Summary

Address	Mnemonic	b7	b6	b5	b4	b3	b2	b1	b0	Default[4]	Access[4]
0x00	CHANNEL_ADR	Not Used	Channel							-1001000	-bbbbbbb
0x01	TX_LENGTH_ADR	TX Length								00000000	bbbbbbbb
0x02	TX_CTRL_ADR	TX GO	TX CLR	TXB15 IRQEN	TXB8 IRQEN	TXB0 IRQEN	TXBERR IRQEN	TXC IRQEN	TXE IRQEN	00000011	bbbbbbbb
0x03	TX_CFG_ADR	Not Used	Not Used	DATA CODE LENGTH	DATA MODE		PA SETTING			--000101	--bbbbbb
0x04	TX_IRQ_STATUS_ADR	OS IRQ	LV IRQ	TXB15 IRQ	TXB8 IRQ	TXB0 IRQ	TXBERR IRQ	TXC IRQ	TXE IRQ	10111000	rrrrrrrr
0x05	RX_CTRL_ADR	RX GO	RSVD	RXB16 IRQEN	RXB8 IRQEN	RXB1 IRQEN	RXBERR IRQEN	RXC IRQEN	RXE IRQEN	00000111	bbbbbbbb
0x06	RX_CFG_ADR	AGC EN	LNA	ATT	HILO	FAST TURN EN	Not Used	RXOW EN	VLD EN	10010-10	bbbbb-bb
0x07	RX_IRQ_STATUS_ADR	RXOW IRQ	SOFDET IRQ	RXB16 IRQ	RXB8 IRQ	RXB1 IRQ	RXBERR IRQ	RXC IRQ	RXE IRQ	00000000	brrrrrrr
0x08	RX_STATUS_ADR	RX ACK	PKT ERR	EOP ERR	CRC0	Bad CRC	RX Code	RX Data Mode		00001---	rrrrrrrr
0x09	RX_COUNT_ADR	RX Count								00000000	rrrrrrrr
0x0A	RX_LENGTH_ADR	RX Length								00000000	rrrrrrrr
0x0B	PWR_CTRL_ADR	PMU EN	LVIRQ EN	PMU MODE FORCE	RSVD	LVI TH		PMU OUTV		10100000	bbb-bbbb
0x0C	XTAL_CTRL_ADR	XOUT FN		XSIRQ EN	Not Used	Not Used	FREQ			000--100	bbb--bbb
0x0D	IO_CFG_ADR	IRQ OD	IRQ POL	MISO OD	XOUT OD	PACTL OD	PACTL GPIO	SPI 3PIN	IRQ GPIO	00000000	bbbbbbbb
0x0E	GPIO_CTRL_ADR	XOUT OP	MISO OP	PACTL OP	IRQ OP	XOUT IP	MISO IP	PACTL IP	IRQ IP	0000----	bbbbrrrr
0x0F	XACT_CFG_ADR	ACK EN	Not Used	FRC END	END STATE			ACK TO		1-000000	b-bbbbbb
0x10	FRAMING_CFG_ADR	SOP EN	SOP LEN	LEN EN	SOP TH					10100101	bbbbbbbb
0x11	DATA32_THOLD_ADR	Not Used	Not Used	Not Used	Not Used	TH32				----0100	----bbbb
0x12	DATA64_THOLD_ADR	Not Used	Not Used	Not Used	TH64					---01010	---bbbbb
0x13	RSSI_ADR	SOP	Not Used	LNA	RSSI					0-100000	r-rrrrrr
0x14	EOP_CTRL_ADR	HEN	HINT		EOP					10100100	bbbbbbbb
0x15	CRC_SEED_LSB_ADR	CRC SEED LSB								00000000	bbbbbbbb
0x16	CRC_SEED_MSB_ADR	CRC SEED MSB								00000000	bbbbbbbb
0x17	TX_CRC_LSB_ADR	CRC LSB								--------	rrrrrrrr
0x18	TX_CRC_MSB_ADR	CRC MSB								--------	rrrrrrrr
0x19	RX_CRC_LSB_ADR	CRC LSB								11111111	rrrrrrrr
0x1A	RX_CRC_MSB_ADR	CRC MSB								11111111	rrrrrrrr
0x1B	TX_OFFSET_LSB_ADR	STRIM LSB								00000000	bbbbbbbb
0x1C	TX_OFFSET_MSB_ADR	Not Used	Not Used	Not Used	Not Used	STRIM MSB				----0000	----bbbb
0x1D	MODE_OVERRIDE_ADR	RSVD	RSVD	FRC SEN	FRC AWAKE		Not Used	Not Used	RST	00000--0	wwwww--w
0x1E	RX_OVERRIDE_ADR	ACK RX	RXTX DLY	MAN RXACK	FRC RXDR	DIS CRC0	DIS RXCRC	ACE	Not Used	0000000-	bbbbbbb-
0x1F	TX_OVERRIDE_ADR	ACK TX	FRC PRE	RSVD	MAN TXACK	OVRD ACK	DIS TXCRC	RSVD	TX INV	00000000	bbbbbbbb
0x27	CLK_OVERRIDE_ADR	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RXF	RSVD	00000000	wwwwwwww
0x28	CLK_EN_ADR	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RXF	RSVD	00000000	wwwwwwww
0x29	RX_ABORT_ADR	RSVD	RSVD	ABORT EN	RSVD	RSVD	RSVD	RSVD	RSVD	00000000	wwwwwwww
0x32	AUTO_CAL_TIME_ADR	AUTO_CAL_TIME_MAX								00000011	wwwwwwww
0x35	AUTO_CAL_OFFSET_ADR	AUTO_CAL_OFFSET_MINUS_4								00000000	wwwwwwww
0x39	ANALOG_CTRL_ADR	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	ALL SLOW	00000000	wwwwwwww
Register Files											
0x20	TX_BUFFER_ADR	TX Buffer File								--------	wwwwwwww
0x21	RX_BUFFER_ADR	RX Buffer File								--------	rrrrrrrr
0x22	SOP_CODE_ADR	SOP Code File								Note 5	bbbbbbbb
0x23	DATA_CODE_ADR	Data Code File								Note 6	bbbbbbbb
0x24	PREAMBLE_ADR	Preamble File								Note 7	bbbbbbbb
0x25	MFG_ID_ADR	MFG ID File								NA	rrrrrrrr

Notes
4. b = read/write; r = read only; w = write only; '-' = not used, default value is undefined.
5. SOP_CODE_ADR default = 0x17FF9E213690C782.
6. DATA_CODE_ADR default = 0x02F9939702FA5CE3012BF1DB0132BE6F.
7. PREAMBLE_ADR default = 0x333302;The count value should be great than 4 for DDR and greater than 8 for SDR.

Absolute Maximum Ratings

Storage Temperature ..... –40 °C to +90 °C

Ambient Temperature with Power Applied ..... 0 °C to +70 °C

Supply Voltage on any power supply pin relative to V_{SS} .....–0.3 V to +3.9 V

DC Voltage to Logic Inputs [8] ..... –0.3 V to V_{IO} + 0.3 V

DC Voltage applied to Outputs in High Z State ..... –0.3 V to V_{IO} + 0.3 V

Static Discharge Voltage (Digital) [9] .....>2000 V

Static Discharge Voltage (RF) [9] ..... 1100 V

Latch up Current .....+200 mA, –200 mA

Ground Voltage ..... 0 V

F_{OSC} (Crystal Frequency) ..... 12 MHz ±30 ppm

DC Characteristics

(T = 25 °C)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Radio Function Operating Voltages (For RF activity, V_{cc} = V_{bat} = 3.0 V to 3.6 V)						
V_{BAT}	Battery Voltage	0 °C–70 °C	2.4	–	3.6	V
V_{IO}	V_{IO} Voltage		1.8	–	3.6	V
V_{CC}	V_{CC} Voltage	0 °C–70 °C	2.4	–	3.6	V
MCU Function Operating Voltages						
V_{DD_MICRO1}	Operating Voltage	No USB activity, CPU speed ≤ 12 MHz	4.0	–	5.25	V
V_{DD_MICRO2}	Operating Voltage	USB activity, CPU speed ≤ 12 MHz. Flash programming	4.35	–	5.25	V
V_{LVD}	Low voltage Detect Trip Voltage (8 programmable trip points)		2.68	–	4.87	V
Device Current (For total current consumption in different modes, for example Radio, active, MCU, sleep, etc., add Radio Function Current and MCU Function Current)						
I_{DD} (GFSK)[10]	Average I_{DD}, 1 Mbps, slow channel	PA = 5, 2-way, 4 bytes/10 ms	–	10.87	–	mA
I_{DD} (32-8DR)[10]	Average I_{DD}, 250 kbps, fast channel	PA = 5, 2-way, 4 bytes/10 ms	–	11.2	–	mA
I_{SB}	Sleep Mode I_{DD}	Radio function and MCU function in Sleep mode, V_{REG} in Keep Alive.	–	40.1	–	µA
Radio Function Current (V_{DD_Micro} = 5.0 V, V_{REG} enabled, MCU sleep)						
IDLE I_{CC}	Radio Off, XTAL Active	XOUT disabled	–	2.1	–	mA
I_{synth}	I_{CC} during Synth Start		–	9.8	–	mA
TX I_{CC}	I_{CC} during Transmit	PA = 5 (–5 dBm)	–	22.4	–	mA
TX I_{CC}	I_{CC} during Transmit	PA = 6 (0 dBm)	–	27.7	–	mA
TX I_{CC}	I_{CC} during Transmit	PA = 7 (+4 dBm)	–	36.6	–	mA
RX I_{CC}	I_{CC} during Receive	LNA off, ATT on	–	20.2	–	mA
RX I_{CC}	I_{CC} during Receive	LNA on, ATT off	–	23.4	–	mA

Notes

8. It is permissible to connect voltages above V_{IO} to inputs through a series resistor limiting input current to 1 mA. AC timing not guaranteed.
9. Human Body Model (HBM).
10. Includes current drawn while starting crystal, starting synthesizer, transmitting packet (including SOP and CRC16), changing to receive mode, and receiving ACK handshake. Device is in sleep except during this transaction.

DC Characteristics (continued)

(T = 25 °C)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
MCU Function Current (V_{DD_Micro} = 5.0 V, V_{REG} disabled)						
I_{DD_MICRO1}	V_{DD_MICRO} Operating Supply Current	No GPIO loading, 6 MHz	–	10	–	mA
I_{SB1}	Standby Current	Internal Oscillators, Bandgap, Flash, CPU Clock, Timer Clock, USB Clock all disabled	–	4	10	µA
USB Interface						
V_{ON}	Static Output High	15K ± 5% Ohm to V_{SS}	2.8	–	3.6	V
V_{OFF}	Static Output Low	R_{UP} is enabled	–	–	0.3	V
V_{DI}	Differential Input Sensitivity		0.2	–	–	V
V_{CM}	Differential Input Common Mode Range		0.8	–	2.5	V
V_{SE}	Single Ended Receiver Threshold		0.8	–	2	V
C_{IN}	Transceiver Capacitance		–	–	20	pF
I_{IO}	Hi-Z State Data Line Leakage	0 V < V_{IN} < 3.3 V	–10	–	10	µA
Radio Function GPIO Interface						
V_{OH1}	Output High Voltage Condition 1	At I_{OH} = –100.0 µA	V_{IO} – 0.1	V_{IO}	–	V
V_{OH2}	Output High Voltage Condition 2	At I_{OH} = –2.0 mA	V_{IO} – 0.4	V_{IO}	–	V
V_{OL}	Output Low Voltage	At I_{OL} = 2.0 mA	–	0	0.4	V
V_{IH}	Input High Voltage		0.76 V_{IO}	–	V_{IO}	V
V_{IL}	Input Low Voltage		0	–	0.24 V_{IO}	V
I_{IL}	Input Leakage Current	0 < V_{IN} < V_{IO}	–1	0.26	+1	µA
C_{IN}	Pin Input Capacitance	except XTAL, RF_N, RF_P, RF_{BIAS}	–	3.5	10	pF
MCU Function GPIO Interface						
R_{UP}	Pull up Resistance		4	–	12	KΩ
V_{ICR}	Input Threshold Voltage Low, CMOS mode	Low to High edge	40%	–	65%	V_{CC}
V_{ICF}	Input Threshold Voltage Low, CMOS mode	High to Low edge	30%	–	55%	V_{CC}
V_{HC}	Input Hysteresis Voltage, CMOS Mode	High to Low edge	3%	–	10%	V_{CC}
V_{ILTTL}	Input Low Voltage, TTL Mode	IO-pin Supply = 2.9–3.6 V	–	–	0.8	V
V_{IHTTL}	Input High Voltage, TTL Mode	IO-pin Supply = 4.0–5.5 V	2.0	–	–	V
V_{OL1}	Output Low Voltage, High Drive [11]	I_{OL1} = 50 mA	–	–	0.8	V
V_{OL2}	Output Low Voltage, High Drive [11]	I_{OL1} = 25 mA	–	–	0.4	V
V_{OL3}	Output Low Voltage, Low Drive [11]	I_{OL2} = 8 mA	–	–	0.4	V
V_{OH}	Output High Voltage[11]	I_{OH} = 2 mA	V_{CC} – 0.5	–	–	V

Note
11. Except for pins P1.0, P1.1 in GPIO mode.

DC Characteristics (continued)

(T = 25 °C)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
3.3 V Regulator						
I_{VREG}	Max Regulator Output Current	$V_{CC} \geq 4.35$ V	–	–	125	mA
I_{KA}	Keep Alive Current	When regulator is disabled with 'keep alive' enable	–	–	20	µA
V_{REG1}	V_{REG} Output Voltage	$V_{CC} \geq 4.35$ V, 0 < temp < 40 °C, 25 mA $\leq I_{VREG} \leq$ 125 mA	3.0	–	3.6	V
V_{REG2}	V_{REG} Output Voltage	$V_{CC} \geq 4.35$ V, 0 < temp < 40 °C, 1 mA $\leq I_{VREG} \leq$ 25 mA	3.15	–	3.45	V
V_{KA}	Keep Alive Voltage	Keep Alive bit set in VREGCR	2.35	–	3.9	V

RF Characteristics

Table 89. Radio Parameters

Parameter Description	Conditions	Min.	Typ.	Max.	Unit
RF Frequency Range	Subject to regulations.	2.400	–	2.497	GHz
Receiver (T = 25 °C, V_{CC} = V_{bat} = 3.0 V, f_{OSC} = 12.000 MHz, BER < 10^{-3})					
Sensitivity 125 kbps 64-8DR	BER 1E-3	–	–97	–	dBm
Sensitivity 250 kbps 32-8DR	BER 1E-3	–	–93	–	dBm
Sensitivity	CER 1E-3	–80	–87	–	dBm
Sensitivity GFSK	BER 1E-3, ALL SLOW = 1	–	–84	–	dBm
LNA gain		–	22.8	–	dB
ATT gain		–	–31.7	–	dB
Maximum Received Signal	LNA On	–15	–6	–	dBm
RSSI value for PWR_{in} –60 dBm[13]	LNA On	–	21	–	Count
RSSI slope		–	1.9	–	dB/Count
Interference Performance (CER 1E-3)					
Co-channel Interference rejection Carrier-to-Interference (C/I)	C = –60 dBm	–	9	–	dB
Adjacent (±1 MHz) channel selectivity C/I 1 MHz	C = –60 dBm	–	3	–	dB
Adjacent (±2 MHz) channel selectivity C/I 2 MHz	C = –60 dBm	–	–30	–	dB
Adjacent ($\geq$ 3 MHz) channel selectivity C/I $\geq$ 3 MHz	C = –67 dBm	–	–38	–	dB
Out-of-Band Blocking 30 MHz–12.75 MHz[12]	C = –67 dBm	–	–30	–	dBm
Intermodulation	C = –64 dBm, Δf = 5,10 MHz	–	–36	–	dBm
Receive Spurious Emission					
800 MHz	100 kHz ResBW	–	–79	–	dBm
1.6 GHz	100 kHz ResBW	–	–71	–	dBm
3.2 GHz	100 kHz ResBW	–	–65	–	dBm
Transmitter (T = 25 °C, V_{CC} = V_{bat} = 3.0 V, f_{OSC} = 12.000 MHz)					
Maximum RF Transmit Power	PA = 7	+2	4	+6	dBm
Maximum RF Transmit Power	PA = 6	–2	0	+2	dBm
Maximum RF Transmit Power	PA = 5	–7	–5	–3	dBm
Maximum RF Transmit Power	PA = 0	–	–35	–	dBm
RF Power Control Range		–	39	–	dB
RF Power Range Control Step Size	seven steps, monotonic	–	5.6	–	dB
Frequency Deviation Min	PN Code Pattern 10101010	–	270	–	kHz
Frequency Deviation Max	PN Code Pattern 11110000	–	323	–	kHz
Error Vector Magnitude (FSK error)	>0 dBm	–	10	–	%rms
Occupied Bandwidth	–6 dBc, 100 kHz ResBW	500	876	–	kHz

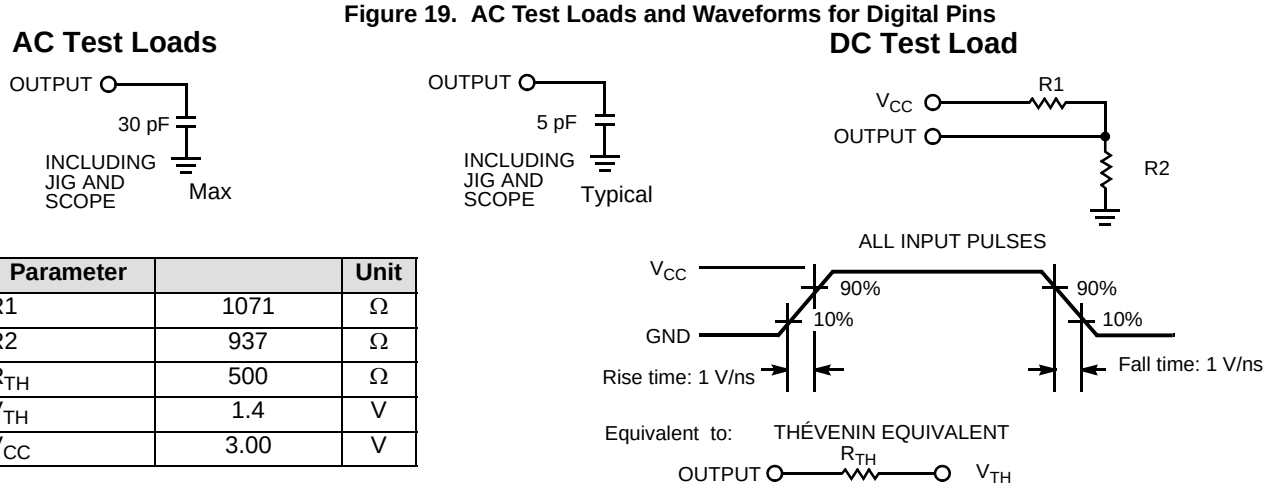
Notes
12. Exceptions F/3 & 5C/3.
13. RSSI value is not guaranteed. Extensive variation from part to part.

Table 89. Radio Parameters (continued)

Parameter Description	Conditions	Min.	Typ.	Max.	Unit
Transmit Spurious Emission (PA = 7)					
In-band Spurious Second Channel Power (±2 MHz)		–	–38	–	dBm
In-band Spurious Third Channel Power (≥ 3 MHz)		–	–44	–	dBm
Non-Harmonically Related Spurs (8.000 GHz)		–	–38	–	dBm
Non-Harmonically Related Spurs (1.6 GHz)		–	–34	–	dBm
Non-Harmonically Related Spurs (3.2 GHz)		–	–47	–	dBm
Harmonic Spurs (Second Harmonic)		–	–43	–	dBm
Harmonic Spurs (Third Harmonic)		–	–48	–	dBm
Fourth and Greater Harmonics		–	–59	–	dBm
Power Management (Crystal PN# eCERA GF-1200008)					
Crystal start to 10 ppm		–	0.7	1.3	ms
Crystal start to IRQ	XSIRQ EN = 1	–	0.6	–	ms
Synth Settle	Slow channels	–	–	270	µs
Synth Settle	Medium channels	–	–	180	µs
Synth Settle	Fast channels	–	–	100	µs
Link turnaround time	GFSK	–	–	30	µs
Link turnaround time	250 kbps	–	–	62	µs
Link turnaround time	125 kbps	–	–	94	µs
Link turnaround time	<125 kbps	–	–	31	µs
Max. packet length	< 60 ppm crystal-to-crystal all modes except 64-DDR and 64-SDR	–	–	40	bytes
Max. packet length	< 60 ppm crystal-to-crystal 64-DDR and 64-SDR	–	–	16	bytes

AC Test Loads and Waveforms for Digital Pins

Figure 19. AC Test Loads and Waveforms for Digital Pins



Parameter		Unit
R1	1071	Ω
R2	937	Ω
R_{TH}	500	Ω
V_{TH}	1.4	V
V_{CC}	3.00	V

AC Electrical Characteristics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Clock						
F_{IMO}	Internal Main Oscillator Frequency	No USB present	22.8	–	25.2	MHz
		With USB present	23.64	–	24.36	
F_{ILO}	Internal Low Power Oscillator	Normal Mode	29.44	–	37.12	kHz
		Low Power Mode	35.84	–	47.36	
3.3 V Regulator						
V_{ORIP}	Output Ripple Voltage		45	–	55	%
USB Driver						
T_{R1}	Transition Rise Time	C_{LOAD} = 200 pF	75	–	–	ns
T_{R2}	Transition Rise Time	C_{LOAD} = 600 pF	–	–	300	ns
T_{F1}	Transition Fall Time	C_{LOAD} = 200 pF	75	–	–	ns
T_{F2}	Transition Fall Time	C_{LOAD} = 600 pF	–	–	300	ns
T_R	Rise/Fall Time Matching		80	–	125	%
V_{CRS}	Output Signal Crossover Voltage		1.3	–	2.0	V
USB Data Timing						
T_{DRATE}	Low speed Data Rate	Ave. Bit Rate (1.5 Mbps ± 1.5%)	1.4775	–	1.5225	Mbps
T_{DJR1}	Receiver Data Jitter Tolerance	To next transition	–75	–	75	ns
T_{DJR2}	Receiver Data Jitter Tolerance	To pair transition	–45	–	45	ns
T_{DEOP}	Differential to EOP Transition Skew		–40	–	100	ns
T_{EOPR1}	EOP Width at Receiver	Rejects as EOP	–	–	330	ns
T_{EOPR2}	EOP Width at Receiver	Accept as EOP	675	–	–	ns
T_{EOPT}	Source EOP Width		1.25	–	1.5	µs
T_{UDJ1}	Differential Driver Jitter	To next transition	–95	–	95	ns
T_{UDJ2}	Differential Driver Jitter	To pair transition	–95	–	95	ns
T_{LST}	Width of SE0 during Diff. Transition		–	–	210	ns
Non-USB Mode Driver Characteristics						
T_{FPS2}	SDATA/SCK Transition Fall Time		50	–	300	ns
SPI Timing						
T_{SMCK}	SPI Master Clock Rate	F_{CPUCLK}/6	–	–	2	MHz
T_{SSCK}	SPI Slave Clock Rate		–	–	2.2	MHz
T_{SCKH}	SPI Clock High Time	High for CPOL = 0, Low for CPOL = 1	125	–	–	ns
T_{SCKL}	SPI Clock Low Time	Low for CPOL = 0, High for CPOL = 1	125	–	–	ns
T_{MDO}	Master Data Output Time [14]	SCK to data valid	–25	–	50	ns
T_{MDO1}	Master Data Output Time, First bit with CPHA = 0	Time before leading SCK edge	100	–	–	ns

Note
14. In Master mode first bit is available 0.5 SPICLK cycle before Master clock edge available on the SCLK pin.

AC Electrical Characteristics (continued)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
T_{MSU}	Master Input Data Setup time		50	–	–	ns
T_{MHD}	Master Input Data Hold time		50	–	–	ns
T_{SSU}	Slave Input Data Setup Time		50	–	–	ns
T_{SHD}	Slave Input Data Hold Time		50	–	–	ns
T_{SDO}	Slave Data Output Time	SCK to data valid	–	–	100	ns
T_{SDO1}	Slave Data Output Time, First bit with CPHA = 0	Time after $\overline{SS}$ LOW to data valid	–	–	100	ns
T_{SSS}	Slave Select Setup Time	Before first SCK edge	150	–	–	ns
T_{SSH}	Slave Select Hold Time	After last SCK edge	150	–	–	ns

Figure 20. Clock Timing

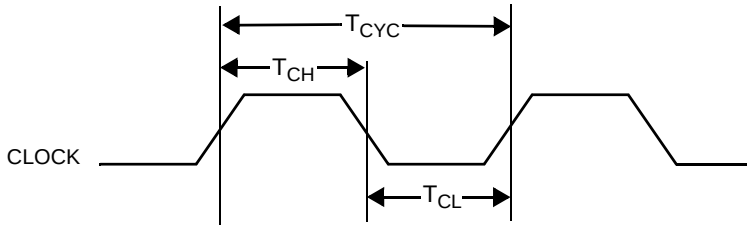


Figure 21. USB Data Signal Timing

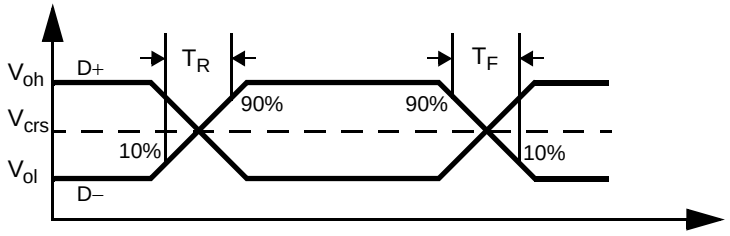


Figure 22. Clock Timing

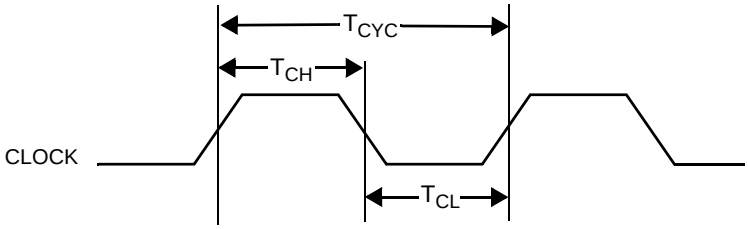


Figure 23. USB Data Signal Timing

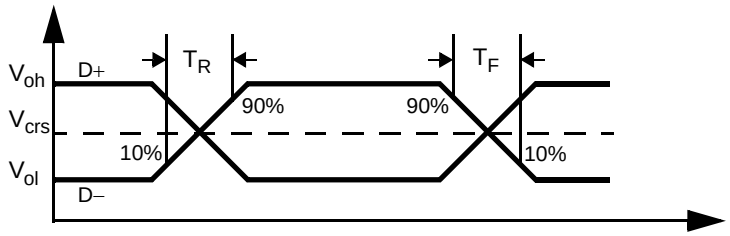


Figure 24. Receiver Jitter Tolerance

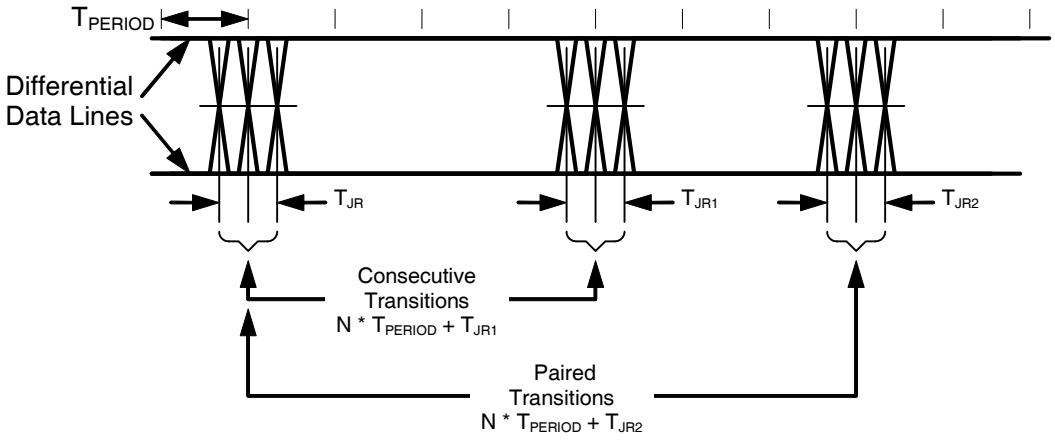


Figure 25. Differential to EOP Transition Skew and EOP Width

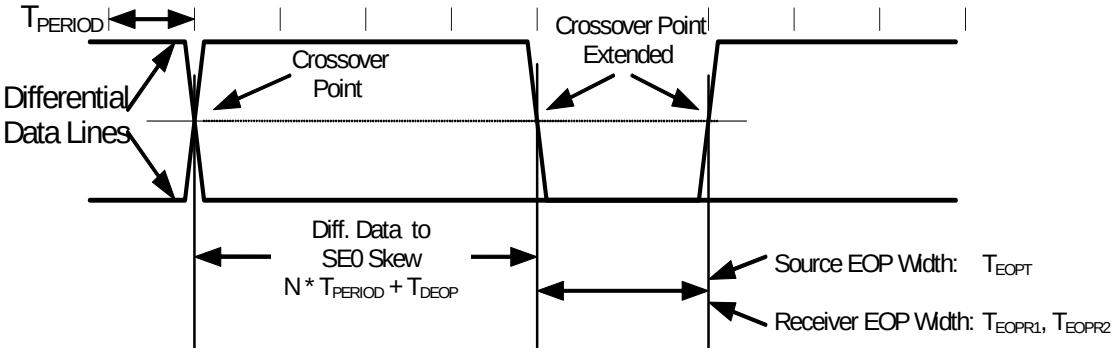


Figure 26. Differential Data Jitter

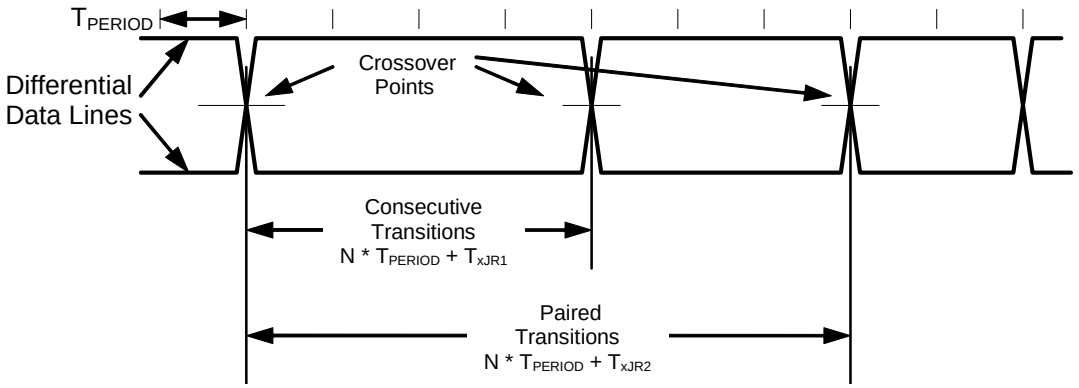


Figure 27. SPI Master Timing, CPHA = 1

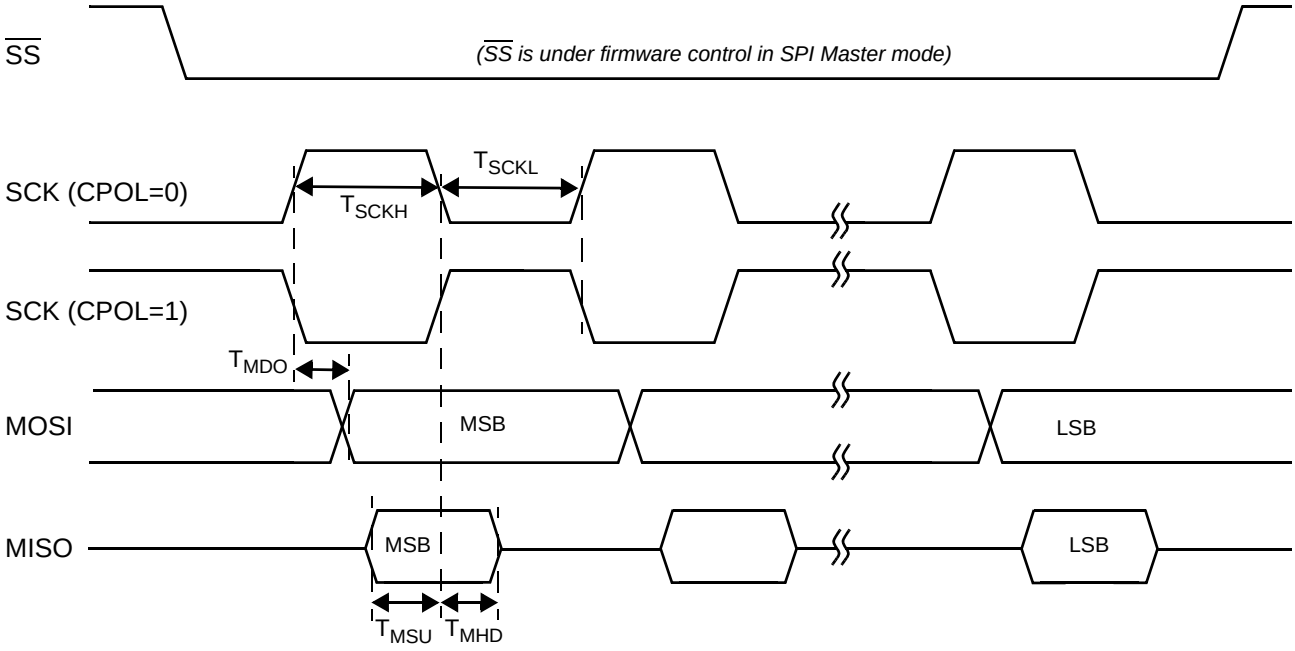


Figure 28. SPI Slave Timing, CPHA = 1

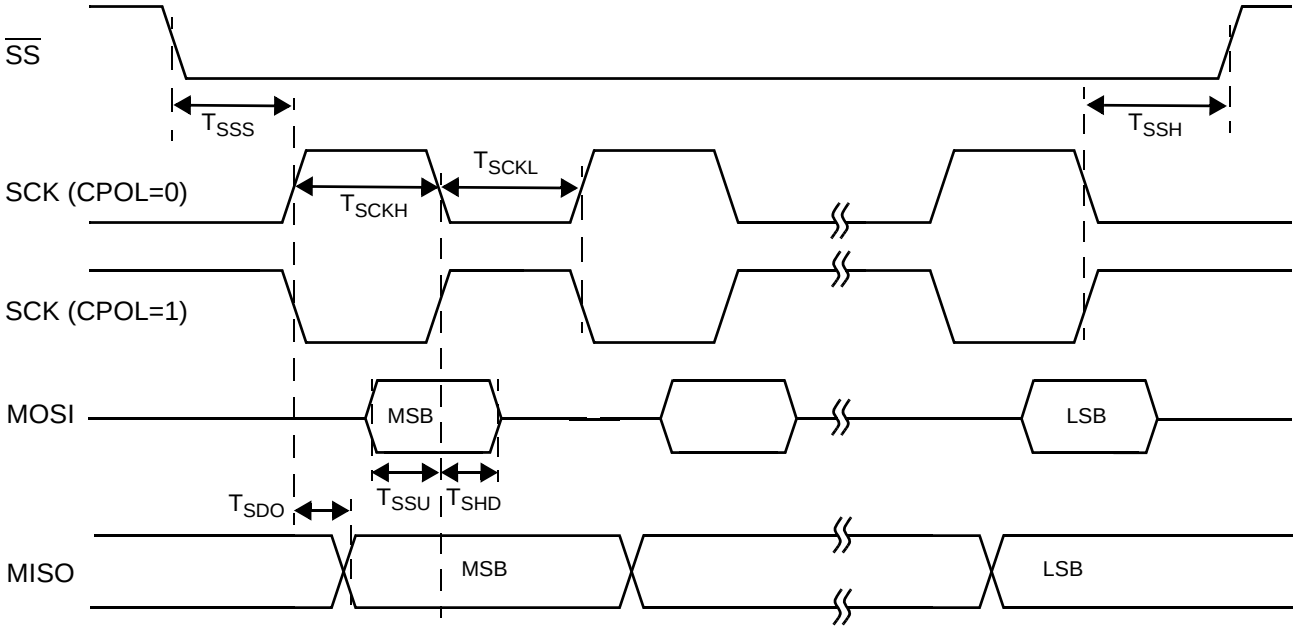


Figure 29. SPI Master Timing, CPHA = 0

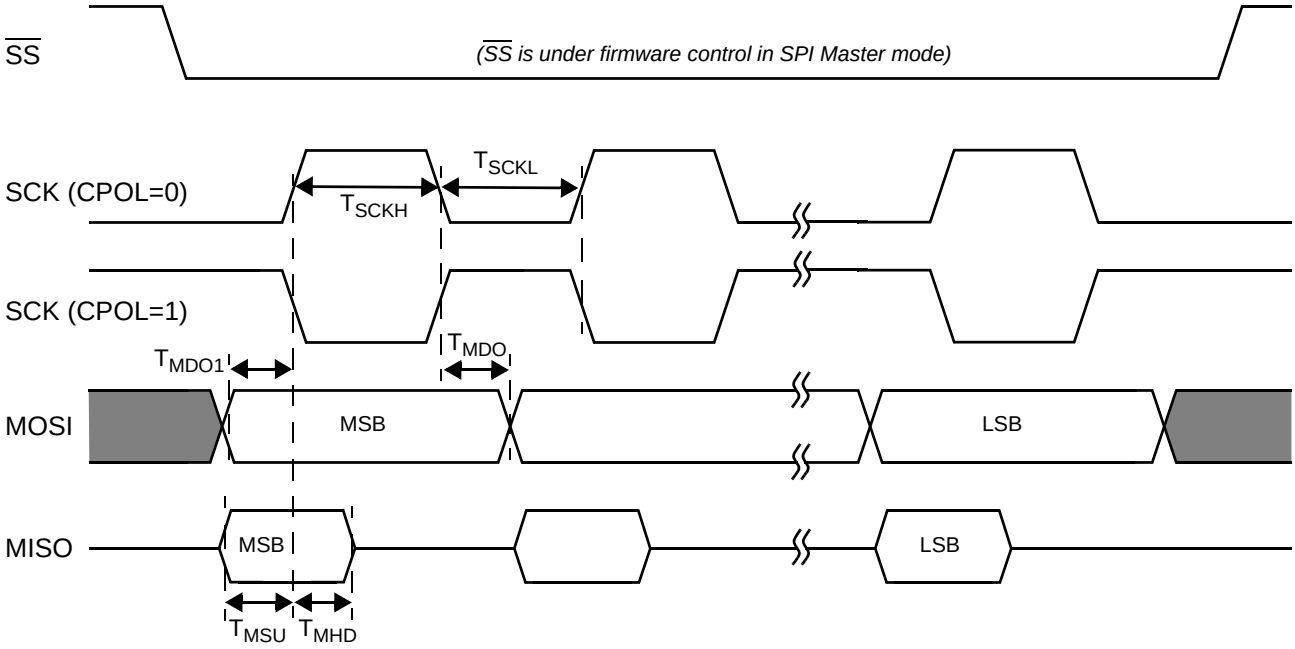
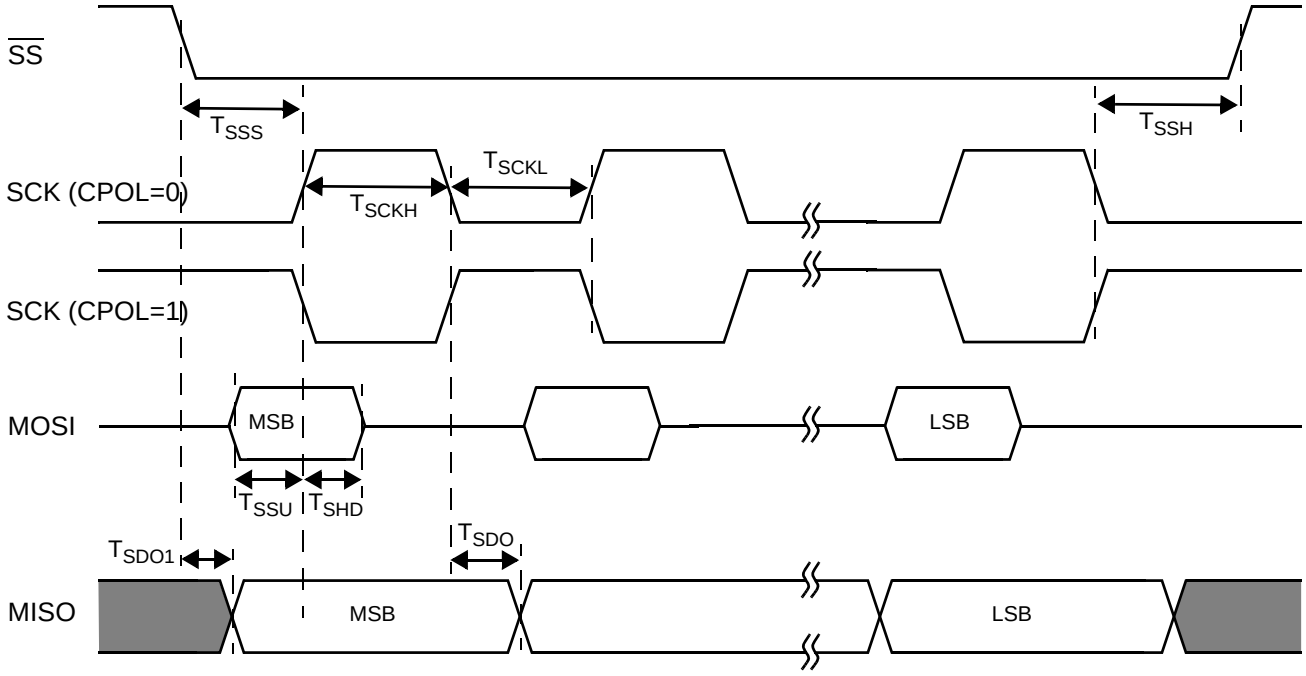


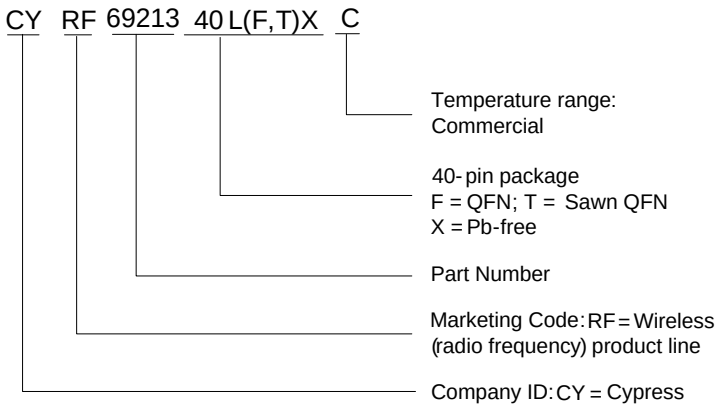
Figure 30. SPI Slave Timing, CPHA = 0



Ordering Information

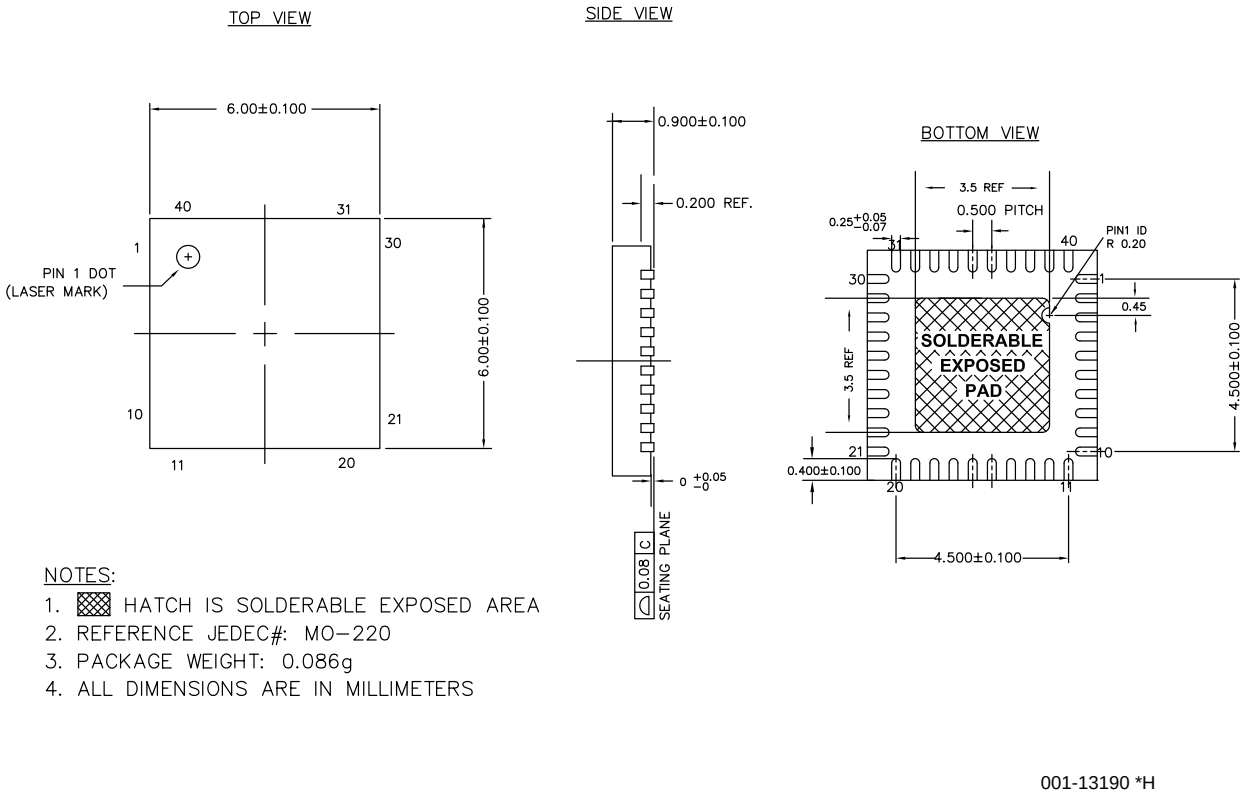
Package	Ordering Part Number	Status
40-pin Pb-free QFN 6 × 6 mm (Sawn)	CYRF69213-40LTXC	In Production
40-pin Pb-free QFN 6 × 6 mm (Punch)	CYRF69213-40LFXC	NRND

Ordering Code Definitions



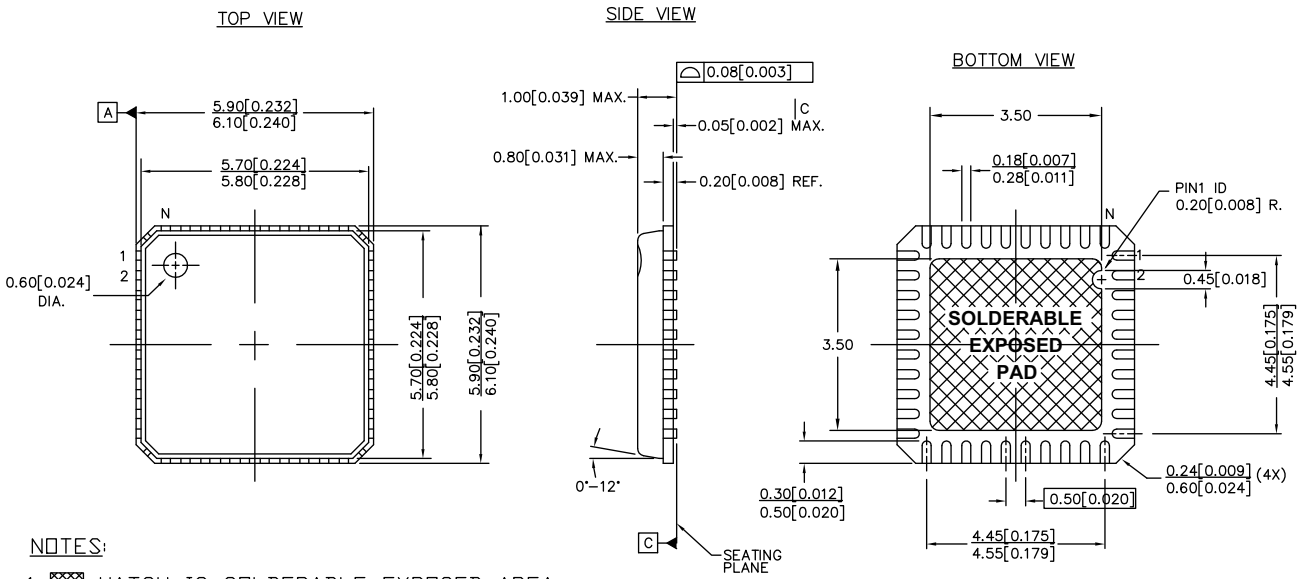
Package Diagram

Figure 31. 40-pin QFN (6 × 6 × 1.0 mm) LT40B (3.5 × 3.5 mm) E-Pad (Sawn) Package Outline, 001-13190



001-13190 *H

Figure 32. 40-pin QFN (6 × 6 × 1.0 mm) LF40A/LY40A (3.50 × 3.50 mm) E-Pad (Punch) Package Outline, 001-12917 [15]



NOTES:

1. HATCH IS SOLDERABLE EXPOSED AREA
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.086g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LF40A	STANDARD
LY40A	PB-FREE

001-12917 *C

Note
15. Not Recommended for New Design.

Document History Page

Document Title: CYRF69213, Programmable Radio on Chip Low Power Document #: 001-07552				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	436355	OYR	See ECN	New advance data sheet.
*A	501280	OYR	See ECN	Preliminary data sheet.
*B	631538	BOO	See ECN	Final datasheet. Updated DC Characteristics table with characterization data. Minor text changes Removed all residual references to external crystal oscillator and GPIO4 Voltage regulator line/load regulation documented GPIO capacitance and timing diagram included Sleep and Wake up sequence documented. EP1MODE/EP2MODE register issue discussed Updated radio function register descriptions Changed L/D pin description Changed RST Capacitor from 0.1uF to 0.47uF
*C	2447906	VNY / VGT / AESA	See ECN	Modified figure 1: Vbat changed to Vbat 0,1,2 for pins 36,6 and 9 Drive level changed to 100uW Figures 1and 3 have a 1 ohm resistor added between Vreg and Vcc Radio register map summary has PFET disable added to bit 4 of PWR_CTRL_ADR Modified register map notes summary for the radio. Modified P02CR to P03CR Added a table to include properties of P01CR Modified the enCoRe II register summary table to include properties of P01CR Modified section on low power in Sleep mode Updated Template
*D	2661527	TGE / PYRS	18/02/09	Changed package spec to 001-12917 Removed Backward Compatibility section Changed "PFET disable" bit in register 0x0B to "RSVD". Added text “For RF activity, Vcc=Vbat=3.0 V-3.6 V” to Radio Function Operating Voltage
*E	2899829	KKU	03/26/2010	Updated the following sections: Pinouts, Clock Block Diagram, Clock Architecture Description, CPU Clock During Sleep Mode, Reset, Sleep Mode, and Register Summary
*F	3550855	ANTG	03/15/2012	Added new ordering part number for Sawn type package Added new package diagram for Sawn type package. Added a section “Receive Spurious Response” Added note# 16 and provided reference to it in Table 88 Added ordering code definition Updated the package diagram for Punch type package
*G	3717153	ANKC	08/18/2012	Updated Ordering Information (No change in part numbers, included a column “Status”). Updated Package Diagram (spec 001-13190 (Changed revision from *G to *H), added Note 15 and referred the same note in Figure 32). Updated in new template.

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