12V MOSFET Drivers with Output Disable for Single Phase Synchronous-Rectified Buck Converter

General Description

The uP1962 is a dual, high voltage MOSFET driver optimized for driving two N-channel MOSFETs in a synchronous-rectified buck converter. Each driver is capable of driving a 5000pF capacitive load with 30ns transition time. This device combined with uPI multi-phase buck PWM controller forms a complete core voltage regulator for advanced micro-processors.

The uP1962 features anti-shoot-through protection that prevents cross-conduction of the external MOSFET while maintains minimum deadtime for optimized efficiency.

This part has integrated bootstrap switch to help minimize the external component count. Both gate drives are turned off by pulling low EN pin or high-impedance at PWM pin, preventing rapid output capacitor discharge during system shutdown.

This device also supports supply input under voltage lockout. The uP1962 is available in thermally enhanced WDFN2x2-8L and WDFN3x3-8L and PSOP-8L packages.

Ordering Information

Order Number	Package	Top Marking
uP1962PDN8	WDFN2x2 - 8L	FH
uP1962QDN8		FG
uP1962SDD8	WDFN3x3 - 8L	uP1962S
uP1962XSU8	PSOP-8L	uP1962X

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/ JEDEC J-STD-020 requirements. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

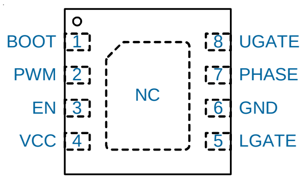
Features

- **All-In-One Synchronous Buck Drivers**
- **Integrated Bootstrap Switch**
- **Anti-Shoot-Through Protection Circuitry**
- **1 PWM Signal Generates both Drivers**
- **Tri-State Input for Bridge Shutdown**
- **Output Disable Control Turns Off both MOSFETs**
- **Under Voltage Lockout for Supply Input**
- **High-Side MOSFET Short Power on Protection**
- **Allow PWM Pin as Multi-Function Setting Application**
- **WDFN2x2-8L and WDFN3x3-8L, PSOP-8L Packages**
- **RoHS Compliant and Halogen Free**

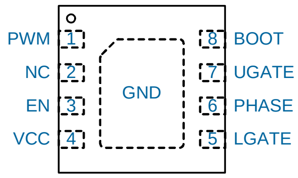
Applications

- **Desktop CPU Core Voltage Regulators**
- **High Frequency Low Profile DC/DC Converter**
- **High Current Low Voltage DC/DC Converter**

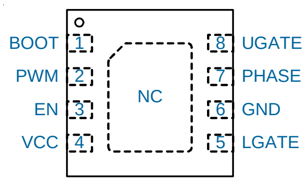
Pin Configuration



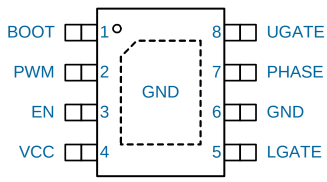
uP1962P



uP1962Q

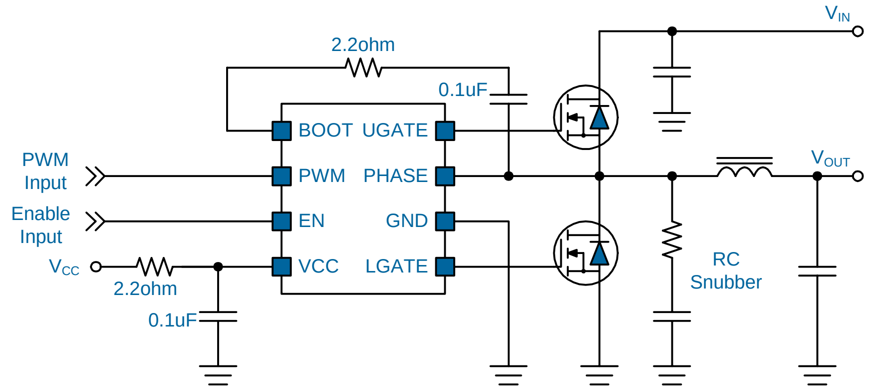


uP1962S

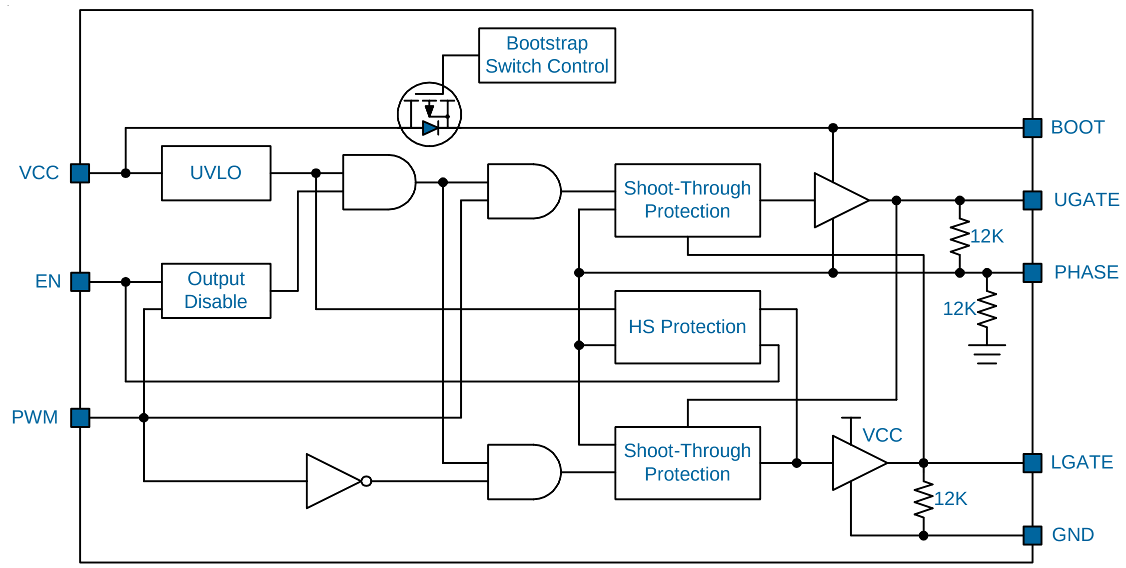


uP1962X

Typical Application Circuit



Functional Block Diagram



Functional Pin Description

Pin No.			Pin Name	Pin Function
PDN8 / SDD8	QDN8	XSU8		
1	8	1	BOOT	**Bootstrap Supply.** For the floating upper gate driver. Connect the bootstrap capacitor C_{BOOT} between BOOT pin and the PHASE pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Make sure that C_{BOOT} is placed near the IC.
2	1	2	PWM	**PWM Input.** This pin receives logic level input and controls the driver outputs. The PWM pin is in high input impedance state if EN input is low. When EN input is high, the PWM pin voltage will be pulled to tri-state by internal circuit. The resistor connected from PWM pin to GND for PWM controller function setting must be greater than 15kΩ.
3	3	3	EN	**Enable Control.** This pin disables normal operation and forces both UGATE and LGATE off when it is pulled low. This pin also controls the state of PWM pin. When the EN pin is pulled low, the PWM pin is in high-input impedance state. There is no internal pull-up or pull-low mechanism to this pin.
4	4	4	VCC	**Supply Voltage for the IC.** This pin provides bias voltage for the IC. Connect this pin to 12V voltage source and bypass it with an R/C filter.
5	5	5	LGATE	**Lower Gate Driver Output.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the shoot-through protection circuitry to determine when the lower MOSFET has been turned off.
7	6	7	PHASE	**PHASE Switch Node.** Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the return path for the UGATE driver. This pin is also monitored by the shoot-through protection circuitry to determine when the upper MOSFET has been turned off.
8	7	8	UGATE	**Upper Gate Driver Output.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the shoot-through protection circuitry to determine when the upper MOSFET has been turned off.
6	Exposed Pad	6, Exposed Pad	GND	**Ground for the IC.** All voltage levels are measured with respect to this pin.
Exposed Pad	2	--	NC	**Not Internally Connected.** Although the exposed pad of uP1962P is not electrically connected to GND. It is still highly recommended to connect the exposed pad to GND plane for maximum heat dissipation.

Enable Control

The EN pin controls PWM pin state and the MOSFET gate driver output state. Logic input low to EN pin disables the gate drivers. Both UGATE and LGATE will be kept low, and PWM pin will be in high input impedance state. Logic input high to EN pin enables the gate drivers after a delay time T_{PDHDEN} as shown in Figure 1. During this time period the PWM pin stays at high input impedance state, both UGATE and LGATE outputs are kept low, and the internal control circuit does not respond to the PWM input voltage. After T_{PDHDEN} expires, both UGATE and LGATE begin to respond to the PWM input. This mechanism is specifically designed for uPI's PWM controller, which uses its PWM pin as a multi-functional pin.

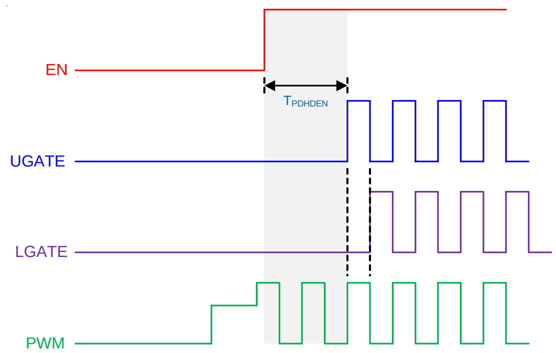


Figure 1. Enable Control, EN

PWM Input

The PWM pin is a tri-state input. Logic high turns on the high-side gate driver and turns off the low-side gate driver once the POR of VCC is granted and EN is kept high. Logic low turns off the high-side gate driver and turns on the low-side gate driver. High impedance input at PWM pin will keep both high-side and low-side gate drivers low and turns off both MOSFETs. The PWM pin voltage is kept around 1.6V by internal bias circuit when floating.

Refer to Figure 1, during T_{PDHDEN}, both UGATE and LGATE are kept low, the PWM pin is in high-input impedance state, and the PWM input will be ignored. For the PWM controller uses its PWM pin as a multi-functional pin, a resistor will be connected from PWM pin to GND to set parameter. Note that this resistor must be greater than 15kΩ. Lower resistor value will cause incorrect PWM voltage level at the PWM pin when the PWM controller output is in tri-state (high-impedance state).

Low-Side Driver

The low-side driver is designed to drive a ground referenced N-channel MOSFET. The bias to the low-side driver is internally connected to VCC supply and GND. The low-side driver output is out of phase with the PWM input when it is enabled. The low side driver is held low if the EN pin is pulled low or high-impedance at PWM pin.

High-Side Driver

The high-side driver is designed to drive a floating N-channel MOSFET. The bias voltage to the high-side driver is internally connected to BOOT and PHASE pins. An integrated bootstrap switch that is connected between BOOT and VCC pins provides the bias current for the high side gate driver.

The bootstrap capacitor C_{BOOT} is charged to V_{CC} when PHASE pin is grounded by turning on the low-side MOSFET. The PHASE rises to V_{IN} when the high-side MOSFET is turned on, forcing the BOOT pin voltage to $V_{IN} + V_{CC}$ that provides voltage to hold the high-side MOSFET on.

The high-side gate driver output is in phase with the PWM input when it is enabled. The high-side driver is held low if the EN pin is pulled low or high-impedance at PWM pin.

Shoot Through Protection

The shoot-through circuit prevents the high-side and low-side MOSFETs from being turned on simultaneously and conducting destructive large current. It is done by turning on one MOSFET only after the other MOSFET is off already with adequate delay time.

At the high-side off edge, UGATE and PHASE voltages are monitored for anti-shoot-through protection. The low-side driver will not begin to output high until both ($V_{UGATE} - V_{PHASE}$) and V_{PHASE} are lower than 1.2V, making sure the high-side MOSFET is turned off completely.

At the low-side off edge, LGATE voltage is monitored for anti-shoot-through protection. The high-side driver will not begin to output high until V_{LGATE} is lower than 1.2V, making sure the low-side MOSFET is turned off completely.

HSFET Short Circuit Power on Protection

The uP1962 provides a protection function to protect the load device of the converter when the converter is powered on with a damaged high-side MOSFET (its drain and source are shorted together). When VCC rises from 0V and across 4.3V, uP1962 starts to detect PHASE voltage. This detection ends when VCC rises above POR 8V (typical value). During this VCC voltage interval, if the PHASE voltage is greater than 2.2V (typical value), LGATE will go high to turn on the low-side MOSFET to pull down the PHASE voltage to protect the load device. The EN pin will be internally pulled low simultaneously to disable the other MOSFET drivers and the PWM controller. This high-side MOSFET short protection is a latch-off function and can only be reset by VCC re-POR.

Figure 2 illustrates the implementation of supply input to VCC if high-side MOSFET short circuit protection function is used. 5VSB and 12V are connected to VCC through a diode. Thus the VCC is supplied by 5VSB before system power on (before 12V is on) and the high-side MOSFET short circuit protection is activated.

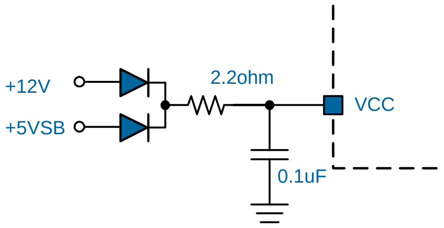


Figure 2. Supply Input to VCC

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, VCC ---------- -0.3V to +15V

BOOT to PHASE ---------- -0.3V to +15V

PHASE to GND

- DC ---------- -0.7V to +15V
- < 200ns ---------- -8V to +30V

BOOT to GND

- DC ---------- -0.3V to (VCC +15V)
- < 200ns ---------- -0.3V to +42V

UGATE to PHASE

- DC ---------- -0.3V to (BOOT - PHASE +0.3V)
- < 200ns ---------- -5V to (BOOT - PHASE +0.3V)

LGATE to GND

- DC ---------- -0.3V to (VCC +0.3V)
- < 200ns ---------- -5V to (VCC +0.3V)

PWM ---------- -0.3V to +6V

EN ---------- -0.3V to (VCC +0.3V)

Storage Temperature Range ---------- -65^{O}C to +150^{O}C

Junction Temperature ---------- 150^{O}C

Lead Temperature (Soldering, 10 sec) ---------- 260^{O}C

ESD Rating (Note 2)

- HBM (Human Body Mode) ---------- 2kV
- MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)

- WDFN2x2 - 8L θ_{JA} ---------- 155^{O}C/W
- WDFN2x2 - 8L θ_{JC} ---------- 20^{O}C/W
- WDFN3x3 - 8L θ_{JA} ---------- 68^{O}C/W
- WDFN3x3 - 8L θ_{JC} ---------- 6^{O}C/W

Power Dissipation, P_D @ T_A = 25^{O}C

- WDFN2x2 - 8L ---------- 0.65W
- WDFN3x3 - 8L ---------- 1.47W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40^{O}C to +125^{O}C

Operating Ambient Temperature Range ---------- -40^{O}C to +85^{O}C

Supply Input Voltage, V_{CC} ---------- 10.8V to 13.2V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25^{O}C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

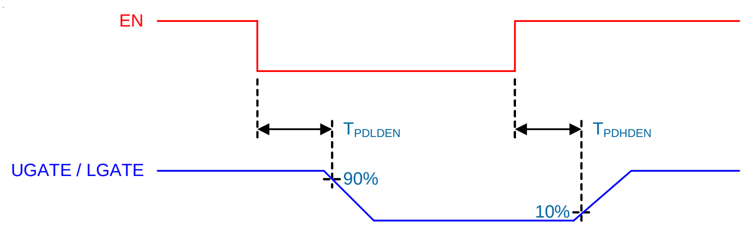
Electrical Characteristics

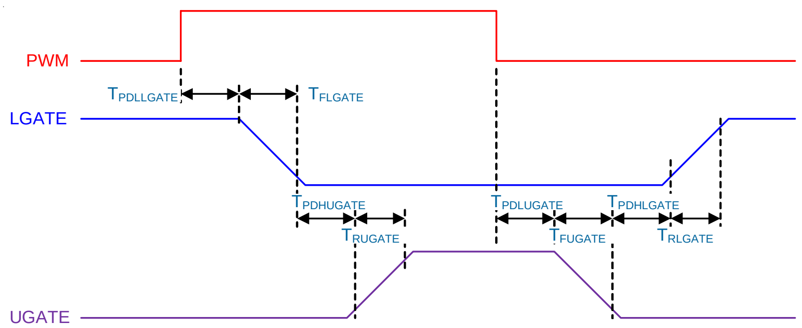
(VCC = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Current	I_{CC}	EN = 0V	--	1	3	mA
VCC POR Rising Threshold	V_{CCRTH}	V_{CC} Rising	7	8	9	V
VCC POR Falling Threshold	V_{CCHYS}	V_{CC} Falling	--	--	4.3	V
PWM Input						
Input High Level	PWM_H		2.9	--	--	V
Input Low Level	PWM_L		--	--	0.4	V
PWM Floating Voltage	PWM_{FLT}		--	1.6	--	V
PWM Input Current	I_{PWM}	PWM = 0V	-520	-280	-200	uA
		PWM = 3.3V	0.5	1	1.6	mA
		PWM = 5V	1	2	2.6	mA
Enable Control						
Input High	EN_H		2	--	--	V
Input Low	EN_L		--	--	0.6	V
Propagation Delay Time	T_{PDHDEN}		1	2	3	us
	T_{PDLDEN}		60	80	100	ns
Bootstrap Switch						
On Resistance	$R_{DS(ON)}$	Forward bias current = 1mA	--	40	--	Ω
High Side Driver						
Output Resistance, Sourcing	R_{H_SRC}	V_{BOOT} - V_{PHASE} = 12V, I_{UGATE} = 80mA	--	2	4	Ω
Output Resistance, Sinking	R_{H_SNK}	V_{BOOT} - V_{PHASE} = 12V, I_{UGATE} = -80mA	--	1	2	Ω
Output Rising Time	T_{RUGATE}	V_{BOOT} - V_{PHASE} = 12V, C_{LOAD} = 3nF	--	35	45	ns
Output Falling Time	T_{FUGATE}	V_{BOOT} - V_{PHASE} = 12V, C_{LOAD} = 3nF	--	20	30	ns
Propagation Delay Time	T_{PDHUG}	V_{BOOT} - V_{PHASE} = 12V	--	40	65	ns
	T_{PDLUG}	V_{BOOT} - V_{PHASE} = 12V	--	20	35	ns

Electrical Characteristics

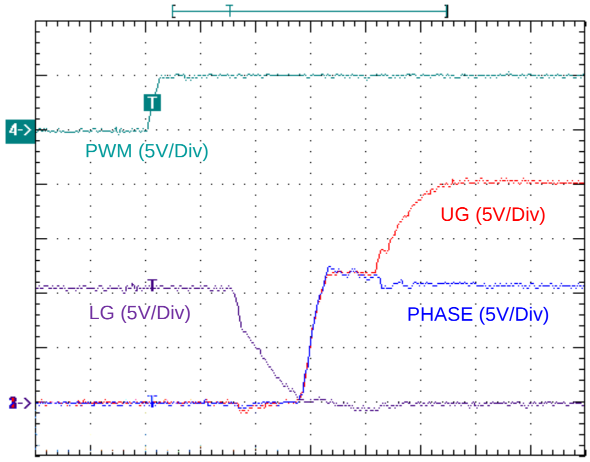
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Low Side Driver						
Output Resistance, Sourcing	R_{L_SRC}	V_{CC} = 12V, I_{LGATE} = 80mA	--	2	4	Ω
Output Resistance, Sinking	R_{L_SNK}	V_{CC} = 12V, I_{LGATE} = -80mA	--	0.8	1.6	Ω
Output Rising Time	T_{RLGATE}	V_{CC} = 12V, C_{LOAD} = 3nF	--	35	45	ns
Output Falling Time	T_{FLGATE}	V_{CC} = 12V, C_{LOAD} = 3nF	--	20	30	ns
Propagation Delay Time	T_{PDHLG}	V_{CC} = 12V	--	40	65	ns
	T_{PDLLG}	V_{CC} = 12V	--	20	35	ns
High Side MOSFET Short Protection						
Trigger Level	V_{HSPT}	V_{CC} = 6V, measure PHASE voltage	2	2.2	2.4	V





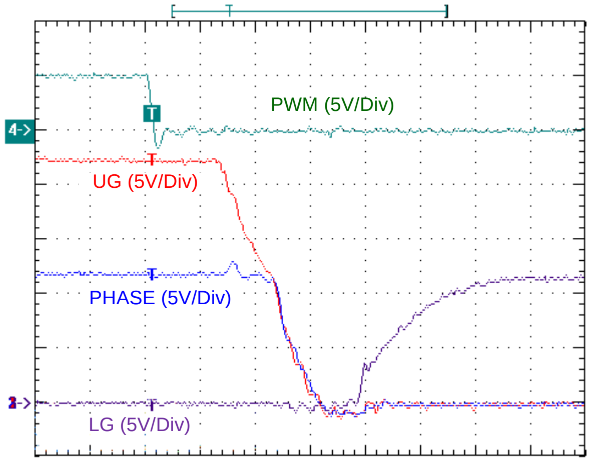
Typical Operation Characteristics

LG Falling to UG Rising Dead Time



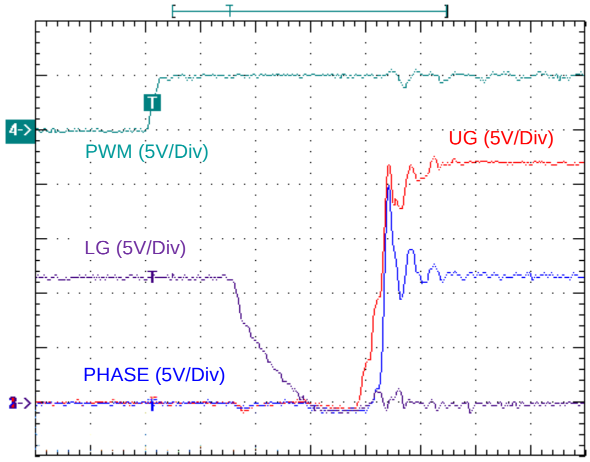
Time : 20ns/Div
V_{IN}=12V,V_{CC}=12 V, Converter Load = 0A,HSFET = QM3004*2,LSFET=QM3006*2, RC Snubber R=2.2Ω, C = 3.3nF

UG Falling to LG Rising Dead Time



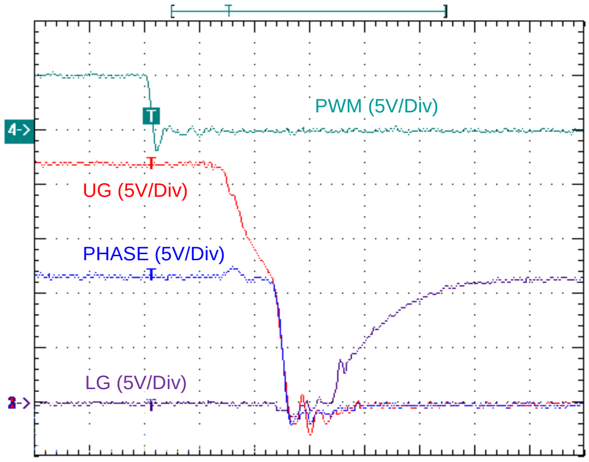
Time : 20ns/Div
V_{IN}=12V,V_{CC}=12 V, Converter Load = 0A, HSFET = QM3004*2,LSFET=QM3006*2, RC Snubber R=2.2Ω, C = 3.3nF

LG Falling to UG Rising Dead Time



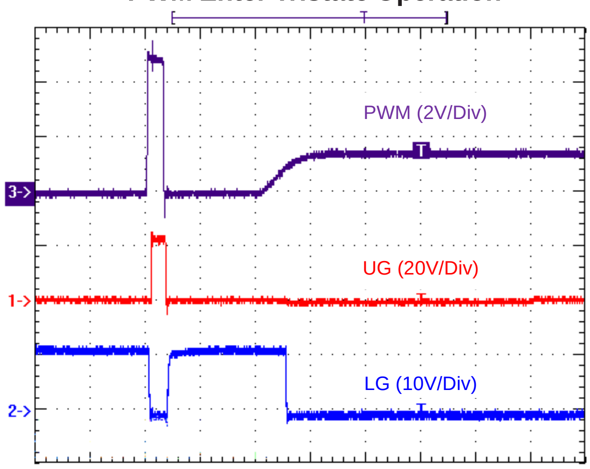
Time : 20ns/Div
V_{IN}=12V,V_{CC}=12 V, Converter Load = 20A, HSFET = QM3004*2,LSFET=QM3006*2, RC Snubber R=2.2Ω, C = 3.3nF

UG Falling to LG Rising Dead Time



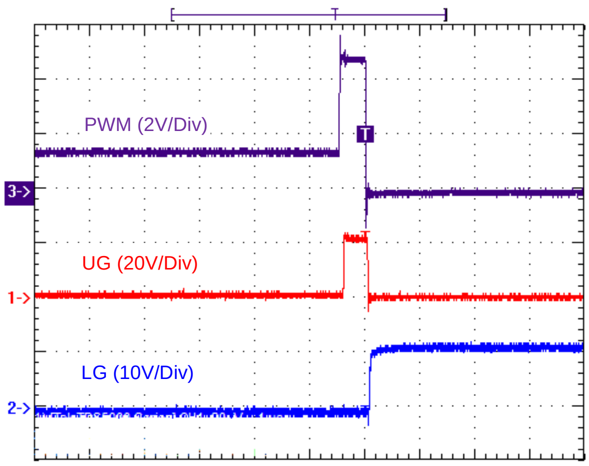
Time : 20ns/Div
V_{IN}=12V,V_{CC}=12 V, Converter Load = 20A, HSFET = QM3004*2,LSFET=QM3006*2, RC Snubber R=2.2Ω, C = 3.3nF

PWM Enter Tristate Operation



Time : 1us/Div
V_{IN}=12V,V_{CC}=12 V, Converter Load = 0A, HSFET = QM3004*2,LSFET=QM3006*2

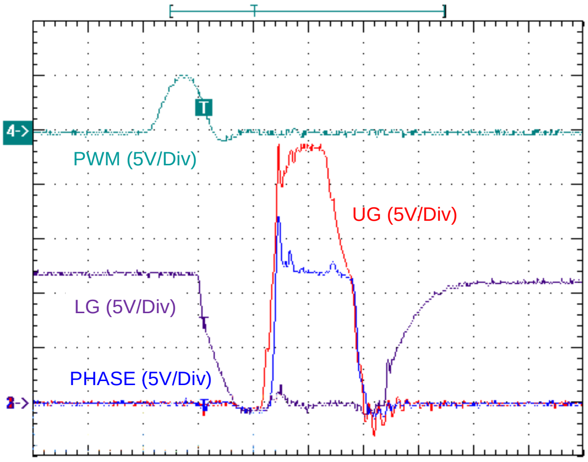
PWM Exit Tristate Operation



Time : 1us/Div
V_{IN}=12V,V_{CC}=12 V, Converter Load = 0A, HSFET = QM3004*2,LSFET=QM3006*2

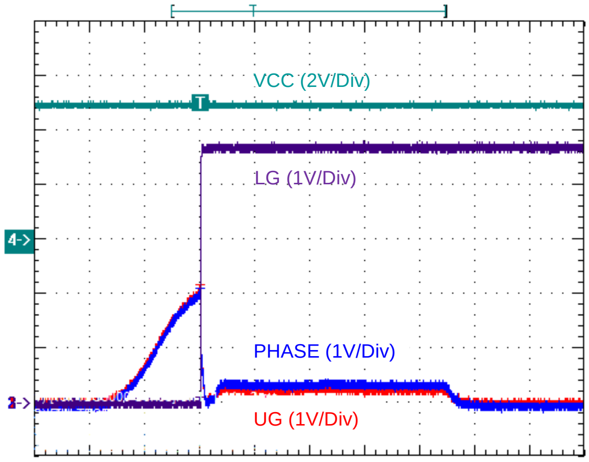
Typical Operation Characteristics

Short Pulse



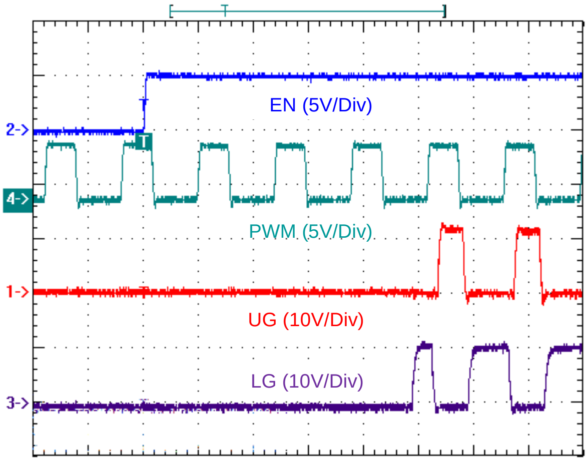
Time : 40ns/Div
V_{IN}=12V,V_{CC}=12 V, PWM=30ns,Converter Load = 5A,
HSFET = QM3004*2,LSFET=QM3006*2

High-side MOSFET Short Protection



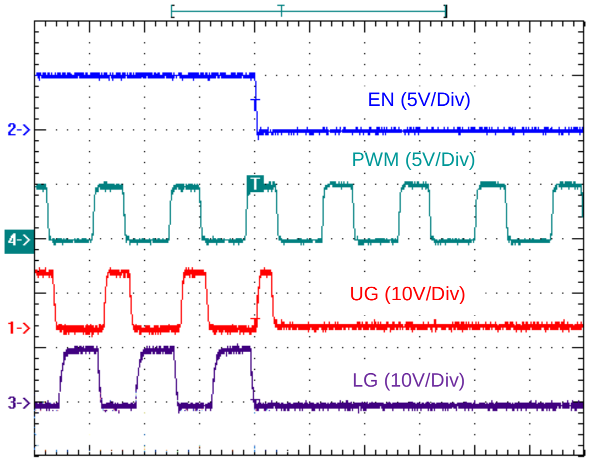
Time : 2ms/Div
Use ATX power, V_{IN}=12V,V_{CC}=12 V

EN go High Delay



Time : 400ns/Div
V_{CC} = 12V, PWM = 1.8MHz, D=40%,
HSFET = QM3004*2,LSFET=QM3006*2

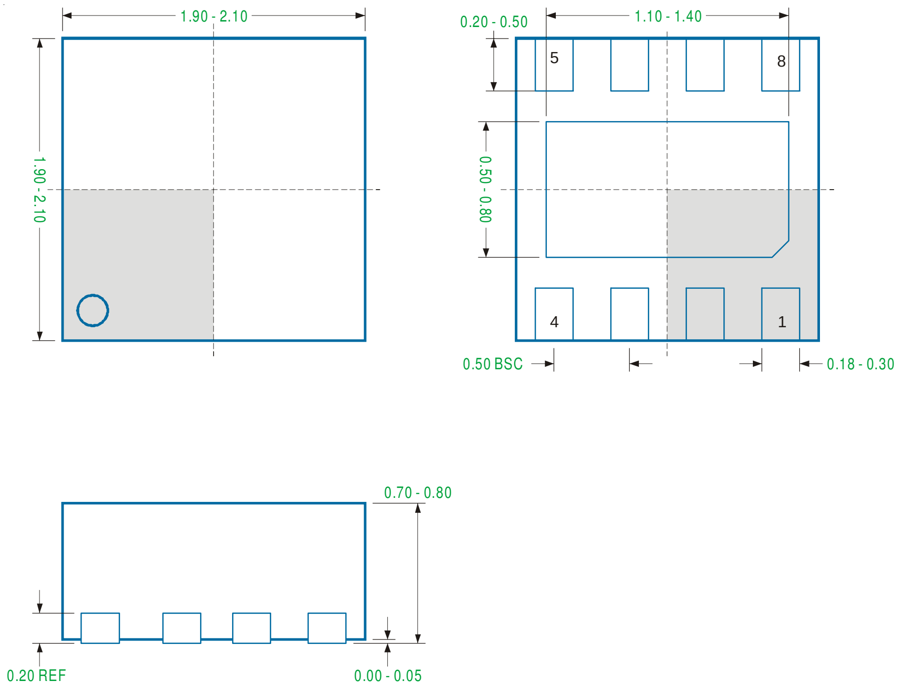
EN go Low Delay



Time : 400ns/Div
V_{CC} = 12V, PWM = 1.8MHz, D = 40%
HSFET = QM3004*2,LSFET=QM3006*2

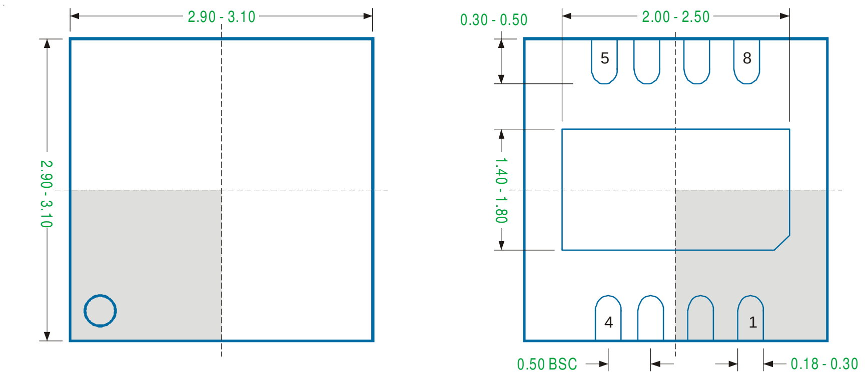
Package Information

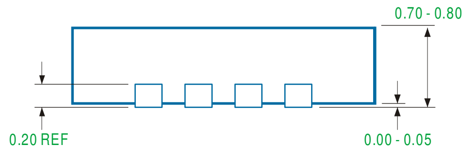
WDFN2x2 - 8L



Note
1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

WDFN3x3 - 8L





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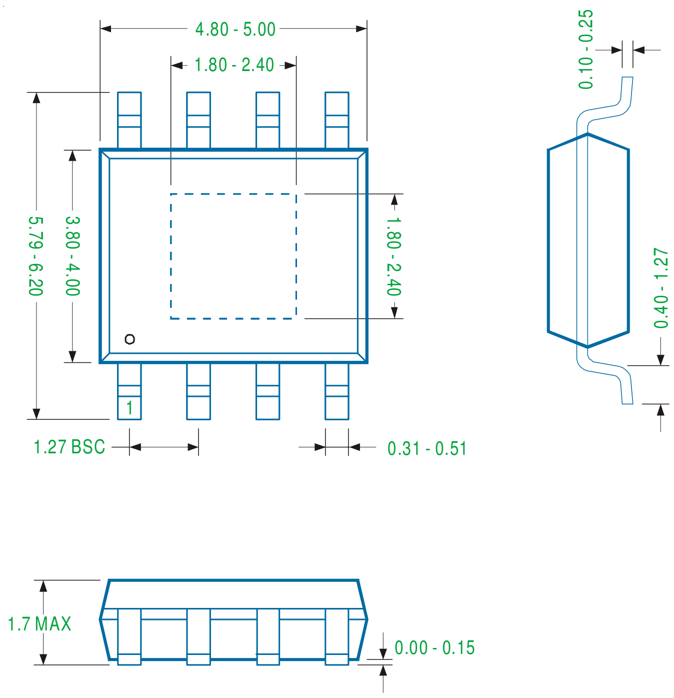
PSOP - 8L



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