LXT350/351 Integrated T1/E1 S/H Transceivers

With Crystal-less Jitter Attenuation

General Description

The LXT350 and LXT351 are full-featured, fully-integrated transceivers for T1 and E1 short-haul applications. They are software switchable between T1 and E1 operation, and offer pulse equalization settings for all short-haul T1 and E1 line interface (LIU) applications.

The LXT350 and LXT351 are identical except for their control interface. The LXT350 provides both a serial I/O port for microprocessor control and a hardware control mode for stand alone operation. The LXT351 offers an Intel- or Motorola-bus compatible parallel I/O port for microprocessor control. Both incorporate advanced crystal-less digital jitter attenuation in either the transmit or receive data path starting at 3 Hz. B8ZS/HDB3 encoding/decoding and unipolar or bipolar data I/O are available. Both LIUs provide loss of signal monitoring and a variety of diagnostic loopback modes.

The LXT350/351 design uses an advanced double-poly, double-metal fabrication process and requires only a single 5-volt power supply.

Applications

- T1/E1 Asynchronous Multiplexers
- Digital Loop Carrier - Subscriber Carrier Systems
- SDH/SONET Multiplexers
- T1/E1 LAN/WAN interfaces for Bridges
- Digital Cross Connects

Features

- Fully integrated transceiver for short-haul T1 or E1 interfaces
- Crystal-less digital jitter attenuation
  - –Selectable either transmit or receive path
  - –No crystal or high-speed external clock required
- Meet or exceed specifications in ANSI T1.403 and T1.408; ITU G.703, G.736, G.775 and G.823; ITU-T I.431; ETSI 300-166 and 300-233; and AT&T Pub 62411
- Support 75 Ω (E1 coax), 100 Ω (T1 twisted-pair) and 120 Ω (E1 twisted-pair) applications
- Fully restores the received signal after transmission through a cable with attenuation of 18dB, at 1024 kHz
- Five Pulse Equalization Settings for T1 short-haul applications
- Transmit/receive performance monitors with Driver Fail Monitor Open (DFM) and Loss of Signal (LOS) outputs
- Selectable unipolar or bipolar data I/O and B8ZS/HDB3 encoding/decoding
- QRSS generator/detector for testing or monitoring
- Output short circuit current limit protection
- Local, remote and analog loopback capability
- Multiple-register serial- or parallel-control interface
- Compatible with Level One's LXT360/361 T1/E1 Long Haul/Short Haul Transceiver (Universal LIU)

LXT350 Transceiver Block Diagram

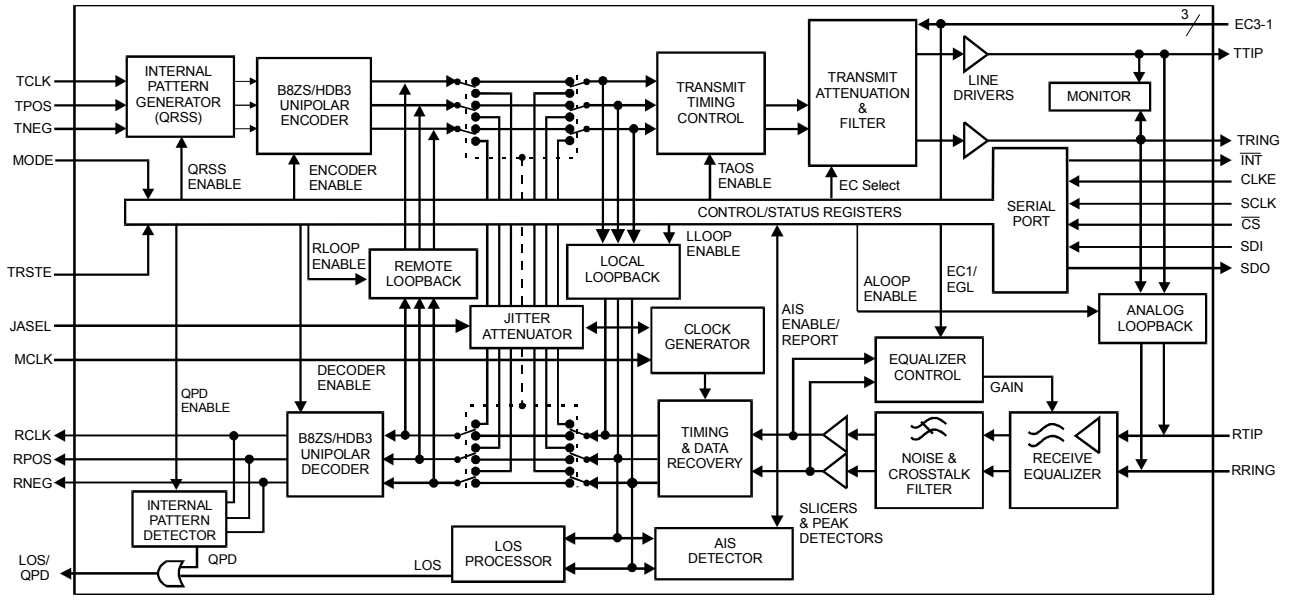


Figure 1: LXT350 Hardware Controlled Bipolar Mode Pin Assignments

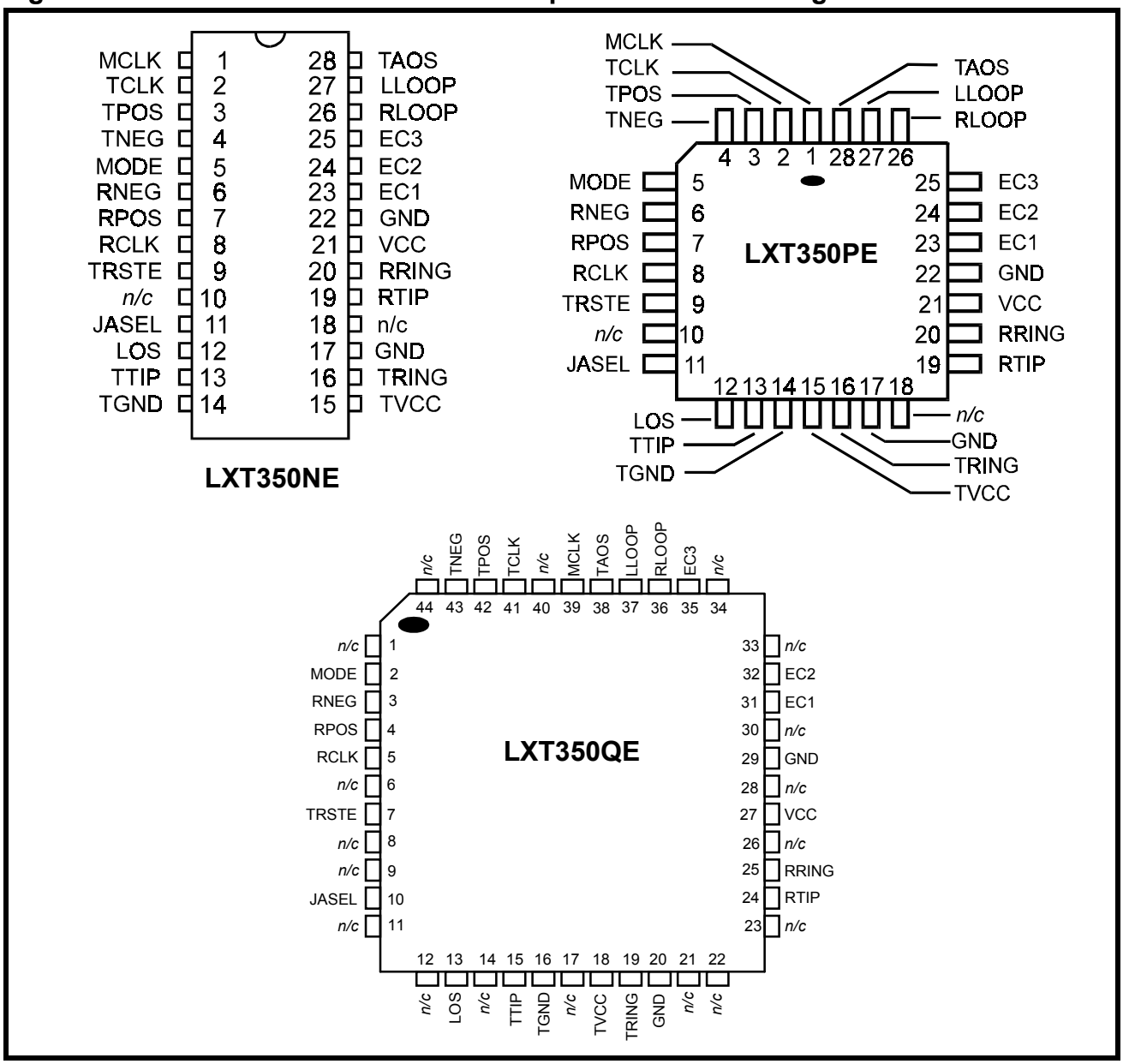


Table 1: LXT350 Clock and Data Pin Assignments by Mode[1]

Pin # NE/ PE	Pin # QE	External Data Modes		QRSS Modes	
		Bipolar Mode	Unipolar Mode	Bipolar Mode	Unipolar Mode
1	39	MCLK			
2	41	TCLK			
3	42	TPOS	TDATA	INSLER	

1. Data pins change based on whether external data or internal QRSS mode is active. Clock pins remain the same in both Hardware and Host Modes

Table 1: LXT350 Clock and Data Pin Assignments by Mode[1]

Pin # NE/ PE	Pin # QE	External Data Modes		QRSS Modes	
		Bipolar Mode	Unipolar Mode	Bipolar Mode	Unipolar Mode
4	43	TNEG	INSBPV	INSBPV	
6	3	RNEG	BPV	RNEG	BPV
7	4	RPOS	RDATA	RPOS	RDATA
8	5	RCLK			
13	15	TTIP			
14	16	TGND			
15	18	TVCC			
16	19	TRING			
19	24	RTIP			
20	25	RRING			
21	27	VCC			
22	29	GND			

1. Data pins change based on whether external data or internal QRSS mode is active. Clock pins remain the same in both Hardware and Host Modes

Table 2: LXT350 Control Pins by Mode

Pin NE/ PE	Pin QE	Hardware Modes		Host Modes		Pin NE/ PE	Pin QE	Hardware Modes		Host Modes	
		Unipolar/ Bipolar	QRSS	Unipolar/ Bipolar	QRSS			Unipolar/ Bipolar	QRSS	Unipolar/ Bipolar	QRSS
5	2	MODE		MODE		24	32	EC2		SDI	
9	7	TRSTE		TRSTE		25	35	EC3		SDO	
11	10	JASEL		*Low*		26	36	RLOOP		$\overline{CS}$	
12	13	LOS	LOS/ QPD	LOS	LOS/ QPD	27	37	LLOOP		SCLK	
23	31	EC1		$\overline{INT}$		28	38	TAOS	QRSS	CLKE	

Table 3: LXT350 Hardware Controlled Bipolar Mode Signal Descriptions

Pin NE/ PE	Pin QE[1]	Symbol	I/O[2]	Description
1	39	MCLK	DI	**Master Clock**. Connect to 1.544 MHz for T1 operation; to 2.048 MHz for E1. MCLK requires an external, independent input to generate internal clocks. Required accuracy is better than **± 32 ppm** with a typical duty cycle of 50%. Upon Loss of Signal (LOS), RCLK is derived from MCLK.
2	41	TCLK	DI	**Transmit Clock**. 1.544 MHz or 2.048 MHz clock input. Transceiver samples TPOS and TNEG on the falling edge of TCLK
3 4	42 43	TPOS TNEG	DI	**Transmit Data – Positive and Negative**. In the Bipolar I/O mode, these pins are the positive and negative sides of a bipolar input pair. Data to be transmitted onto the line is input at these pins. Table 4 describes Unipolar Mode functions.
5	2	MODE	DI	**Mode Select**. Connecting MODE Low puts the LXT350 in Hardware Mode. In Hardware Mode, the serial interface is disabled and hardwired pins are used to control configuration and report status. Leaving MODE open activates Hardware Mode and enables the B8ZS/HDB3 encoder/ decoder and Unipolar Mode. Connecting MODE High puts the LXT350 in Host Mode. In Host Mode, the serial interface controls the LXT350 and displays its status.
6 7	3 4	RNEG RPOS	DO	**Receive Data – Negative and Positive**. In the Bipolar I/O mode, these pins are the positive and negative sides of a bipolar output pair. Data recovered from the line interface is output on these pins. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP/ RRING. RNEG/RPOS outputs are Non-Return-to-Zero. Both outputs are stable and valid on the rising edge of RCLK. Refer to Table 4 for Unipolar mode function descriptions.
8	5	RCLK	DO	**Recovered Clock**. The clock recovered from the line input signal is output on this pin. Under LOS conditions there is a smooth transition from RCLK to MCLK output.
9	7	TRSTE	DI	**Tristate**. Connecting TRSTE High forces all output pins to a high-impedance state. Connecting TRSTE Low sets the LXT350 to the Hardware Bipolar Mode. Leaving TRSTE open enables the Unipolar Mode. (See Table 4 for Unipolar function descriptions.)

1. Pins 1, 6, 8, 11, 12, 14, 17, 20, 22, 23, 26, 28, 33, 34, 40 and 44 are not connected (*n/c*). Pins 9 and 21 must be left floating.
2. I/O column entries: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output.

Table 3: LXT350 Hardware Controlled Bipolar Mode Signal Descriptions – continued

Pin NE/ PE	Pin QE[1]	Symbol	I/O[2]	Description
10	–	*n/c*	DO	*No connection. Leave this pin floating.*
11	10	JASEL	DI	**Jitter Attenuation Select**. Selects jitter attenuation location. Connecting JASEL High activates the jitter attenuator in the receive path. Connecting JASEL Low activates the jitter attenuator in the transmit path. Leaving JASEL open disables JA.
12	13	LOS	DO	**Loss of Signal Indicator**. In T1 mode, LOS goes High on receipt of 175 consecutive spaces and returns Low when the received signal reaches a mark density of 12.5% (determined by receipt of 16 marks within a sliding window of 128 bits with fewer than 100 consecutive zeros). In E1 modes, LOS goes High on receipt of 32 consecutive spaces, and returns Low when the receiver detects 12.5% mark density (determined by receipt of 4 marks within a sliding window of 32 bits with fewer than 16 consecutive zeros). The transceiver outputs receives marks on RPOS and RNEG even when LOS is High.
13 16	15 19	TTIP TRING	AO	**Transmit Tip and Ring**. Differential Driver Outputs. These outputs are designed to drive a 50 - 200 Ω load. The transformer and line matching resistors should be selected to give the desired pulse height and return loss performance.
14	16	TGND	–	**Ground.** Ground return for the transmit driver power supply TVCC.
15	18	TVCC	DI	**+5 VDC Power Supply** input for the transmit drivers. TVCC must not vary from VCC by more than ± 0.3 V.
17	29	GND	–	**Ground**. Tie this pin to ground.
18	–	*n/c*	–	*Leave this pin open.*
19 20	24 25	RTIP RRING	AI	**Receive Tip and Ring**. The AMI signal received from the line is applied at these pins. A 1:1 transformer is required. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
21	27	VCC	–	**+5 VDC Power Supply** for all circuits except the transmit drivers. (Transmit drivers are supplied by TVCC.)
22	29	GND	–	**Ground.** Ground return for power supply VCC.
23 24 25	31 32 35	EC1 EC2 EC3	DI	**Equalization Control 3-1**. These pins define the **Pulse Equalization** settings. See Table 12 for additional details.
26	36	RLOOP	DI	**Remote Loopback.** When held High, the clock and data inputs from the framer (TPOS/TNEG or TDATA) are ignored and the data received from the line is transmitted back onto the line at the RCLK frequency. During remote loopback, the device ignores the in-line encoders/decoders. See Figure 8.
27	37	LLOOP	DI	**Local Loopback**. When held High, the data on TPOS and TNEG loops back digitally to RPOS and RNEG outputs (through JA if enabled). Leaving this pin open enables Analog Loopback (TTIP and TRING looped back to RTIP and RRING). See Figures 5, 6, and 7.
28	38	TAOS	DI	**Transmit All Ones**. When held High the transmit data inputs are ignored and the LXT350 transmits a stream of 1s at the TCLK frequency. (If TCLK is not supplied, MCLK is the transmit clock reference.) TAOS is inhibited during Remote Loopback. Leaving this pin open enables QRSS pattern generation and detection. See Figures 5, 10, and 11.

1. Pins 1, 6, 8, 11, 12, 14, 17, 20, 22, 23, 26, 28, 33, 34, 40 and 44 are not connected (*n/c*). Pins 9 and 21 must be left floating.
2. I/O column entries: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output.

Table 4: LXT350 Hardware Controlled Unipolar Mode Signal Assignments

Pin NE/ PE	Pin QE	Symbol	I/O[1]	Description
3	42	TDATA	DI	**Transmit Data**. Unipolar input for data to be transmitted onto the line.
4	43	INSBPV	DI	**Insert Bipolar Violation**. This pin is sampled on the falling edge of TCLK to control Bipolar Violation Insertions in the transmit data stream. A Low-to-High transition is required to insert subsequent BPVs.
6	3	BPV	DO	**Bipolar Violation.** BPV goes High to report receipt of a bipolar violation from the line. This is an NRZ output, valid on the rising edge of RCLK.
7	4	RDATA	DO	**Receive Data**. RDATA is a unipolar NRZ output of data recovered from the line interface. In Hardware Mode RDATA is stable and valid on the rising edge of RCLK.

1. I/O Column entries: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output.

Table 5: LXT350 Hardware Controlled QRSS Unipolar Mode Signal Assignments

Pin NE/ PE	Pin QE	Symbol	I/O[1]	Description
3	42	INSLER	DI	**Insert Logic Error**. When this pin goes from Low to High, the transceiver inserts a logic error into the transmitted QRSS data pattern. The error follows the data flow in whatever loopback mode is in effect. The LXT350 samples this pin on the falling edge of TCLK (or MCLK, if TCLK is not present).
4	43	INSBPV	DI	**Insert Bipolar Violation**. When this pin goes from Low to High, the transceiver inserts a bipolar violation error into the transmitted QRSS data pattern. A subsequent insertion requires another Low to High transition. The LXT350 samples this pin on the falling edge of TCLK (or MCLK, if TCLK is not present).
6	3	BPV[2]	DO	**Bipolar Violation**. BPV goes High to report receipt of a bipolar violation from the line. This is an NRZ output, valid on the rising edge of RCLK.
7	4	RDATA[2]	AO	**Received Data**. RDATA is a unipolar NRZ output of data recovered from the line interface. In hardware Mode, RDATA is stable and valid on the rising edge of RCLK.
12	13	LOS/QPD	DO	**Loss of Signal/QRSS Pattern Detect**. This pin acts as a QPD indicator as well as LOS indicator. The QRSS Pattern synchronization criterion is fewer than four errors in 128 bits. In this mode, as long as the transceiver does not detect a QRSS pattern QPD stays High. As soon as the device does detect a QRSS pattern, the pin goes Low; any bit errors cause QPD to go High for half a clock cycle. This output can trigger an external error counter. An LOS condition also makes this pin go High. See Figure 11.
28	38	QRSS	DI	**QRSS**. Leaving this pin open, enables QRSS pattern generation and detection. The transceiver transmits the QRSS pattern at the TCLK rate (or MCLK, if TCLK is not present).

1. I/O Column entries: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output.
2. In QRSS Bipolar Mode, pins 6 and 7 (or pins 3 and 4 on the QFP package) act as RNEG and RPOS output, respectively.

Table 6: LXT350 Host Controlled Bipolar Mode Signal Assignments [1,2]

Pin NE/ PE	Pin QE	Symbol	I/O[3]	Description
6 7	3 4	RNEG RPOS	DO	**Received Data–Negative and Positive**. In the Bipolar I/O Mode, these pins are the negative and positive sides of a bipolar output pair. The transceiver outputs the data recovered from the line interface on these pins. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. A signal on RPOS corresponds to receipt of a positive signal on RTIP/RRING. RNEG/RPOS outputs are Non-Return-to-Zero (NRZ). CLKE determine the clock edge at which these outputs are stable and valid. See Figure 19.
9	7	TRSTE	DI	**Tristate**. Connecting TRSTE High forces all output pins to high-impedance state. Connect this pin Low for normal operation.
10	–	*n/c*	–	*Not connected.*
11	10	GND	–	*Tie this pin to ground.*
17	29	GND	–	*Tie this pin to ground*
23	31	$\overline{\text{INT}}$	DO	**Interrupt** (Active Low–Maskable). $\overline{\text{INT}}$ goes Low to flag the host when any of LOS, AIS, QRSS or DFMO changes state or when there is an Elastic Store overflow or underflow. $\overline{\text{INT}}$ is an open drain output which requires a connection to power supply VCC through a resistor. Reset $\overline{\text{INT}}$ by writing a one to the respective bit in the Interrupt Clear Register.
24	32	SDI	DI	**Serial Data Input**. Input port for the 16-bit serial address/command and data word. LXT350 samples SDI on the rising edge of SCLK. See Figure 20.
25	35	SDO	DO	**Serial Data Output**. If CLKE is High, SDO is valid on the rising edge of SCLK. If CLKE is Low, SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to or when $\overline{\text{CS}}$ is High. See Figure 21.
26	36	$\overline{\text{CS}}$	DI	**Chip Select** (Active Low). This input is used to access the serial interface. For each read or write operation, $\overline{\text{CS}}$ must transition from High to Low, and remain Low.
27	37	SCLK	DI	**Serial Clock**. This clock is used to write data to or read data from the serial interface registers. The clock frequency can be any rate up to 2.048 MHz.
28	38	CLKE	DI	**Clock Edge**. Setting CLKE High causes RPOS and RNEG to be valid on the falling edge of RCLK, with SDO valid on the rising edge of SCLK. Setting CLKE Low makes RPOS and RNEG valid on the rising edge of RCLK and SDO valid on the falling edge of SCLK.

1. For pins not described in this table, see Table 3. Pin out for data pins in Unipolar and QRSS Modes remains the same as in Tables 4 and 5. In Host Mode, the control pins (23-28 for NE/PE or 31-38 for QE) change as shown in Table 6.
2. In QRSS Bipolar Mode, pins 6 and 7 (or pins 3 and 4 on the QFP package) seven act as RNEG and RPOS, respectively.
3. I/O Column entries: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output.

Figure 2: LXT351 Bipolar Mode Pin Assignments

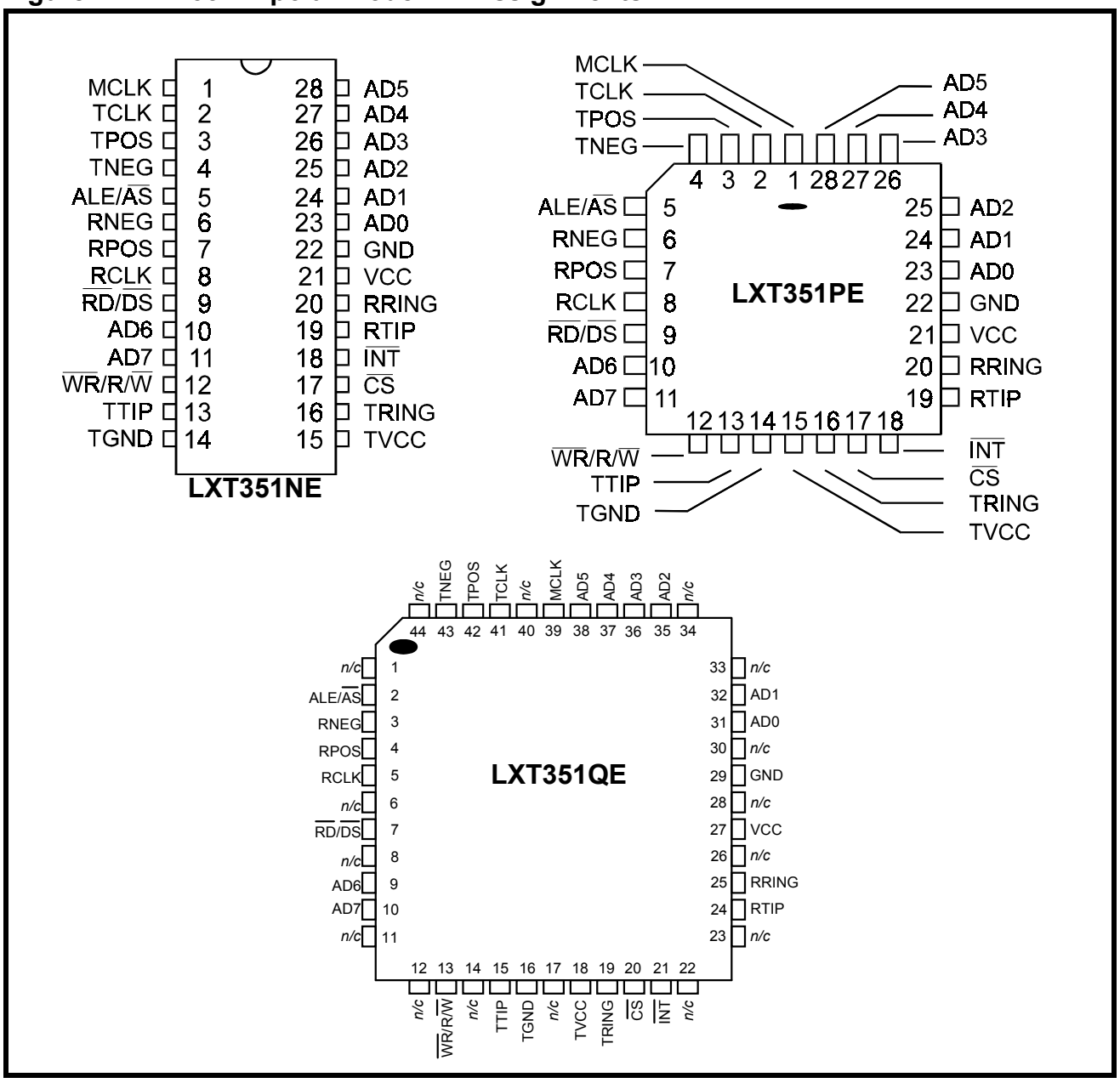


Table 7: LXT351 Clock and Data Pin Assignments by Mode[1]

Pin NE/ PE	Pin QE	External Data Modes		QRSS Modes	
		Bipolar Mode	Unipolar Mode	Bipolar Mode	Unipolar Mode
1	39	MCLK			
2	41	TCLK			
3	42	TPOS	TDATA	INSLER	

1. Data pins change based on whether external data or internal QRSS mode is active. These pins remain the same in both Hardware and Host Modes.

Table 7: LXT351 Clock and Data Pin Assignments by Mode[1]

Pin NE/ PE	Pin QE	External Data Modes		QRSS Modes	
		Bipolar Mode	Unipolar Mode	Bipolar Mode	Unipolar Mode
4	43	TNEG	INSBPV	INSBPV	
6	3	RNEG	BPV	RNEG	BPV
7	4	RPOS	RDATA	RPOS	RDATA
8	5	RCLK			
13	15	TTIP			
14	16	TGND			
15	18	TVCC			
16	19	TRING			
19	24	RTIP			
20	25	RRING			
21	27	VCC			
22	29	GND			

1. Data pins change based on whether external data or internal QRSS mode is active. These pins remain the same in both Hardware and Host Modes.

Table 8: LXT351 Processor Interface Pins

Pin NE/ PE	Pin QE	Address/Data Bus Type		Pin NE/ PE	Pin QE	Address/Data Bus Type	
		Intel	Motorola			Intel	Motorola
5	2	ALE	$\overline{AS}$	25	35	AD2	
9	7	$\overline{RD}$	DS	26	36	AD3	
12	13	$\overline{WR}$	R/$\overline{W}$	27	37	AD4	
17	20	$\overline{CS}$		28	38	AD5	
18	21	$\overline{INT}$		10	9	AD6	
23	31	AD0		11	10	AD7	
24	32	AD1					

Table 9: LXT351 Bipolar Mode Signal Assignments

Pin NE/ PE	Pin QE[2]	Symbol	I/O[1]	Description
1	39	MCLK	DI	**Master Clock**. Connect to 1.544 MHz for T1 operation; to 2.048 MHz for E1. MCLK requires an external, independent input to generate internal clocks. Required accuracy is better than ± 32 ppm with a typical duty cycle of 50%. Upon Loss of Signal (LOS), the transceiver derives RCLK from MCLK.
2	41	TCLK	DI	**Transmit Clock**. 1.544 MHz or 2.048 MHz bit rate clock input. The transceiver samples TPOS and TNEG on the falling edge of TCLK
3 4	42 43	TPOS TNEG	DI	**Transmit Data – Positive and Negative**. In the Bipolar I/O Mode, these pins are the positive and negative sides of a bipolar input pair. Data for transmission onto the line is input at these pins.
5	2	ALE $\overline{AS}$	DI	**Address Latch Enable/Address Strobe** (Active Low). Connects to Intel (ALE) or Motorola ($\overline{AS}$) signal. On Motorola bus, this signal is Active Low. **Leaving this pin floating forces all output pins into a high impedance state.**
6 7	3 4	RNEG RPOS	DO	**Receive Data – Negative and Positive**. In the Bipolar I/O mode, these pins are the positive and negative sides of a bipolar output pair. Data recovered from the line interface is output on these pins. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP/RRING. RNEG/RPOS outputs are Non-Return-to Zero. Both outputs are stable and valid on the rising edge of RCLK. Refer to Table 10 for Unipolar mode function descriptions.
8	5	RCLK	DO	**Recovered Clock**. The output on this pin is the clock recovered from the line input signal. Under LOS conditions there is a smooth transition from RCLK to MCLK output.
9	7	$\overline{RD}$ $\overline{DS}$	DI	**Read** (Active Low)**/Data Strobe** (Active Low). On an Intel bus, this signal, Read, goes Low to command a read operation. On a Motorola bus, this signal, Data Strobe, goes Low when data is being driven on the address/data bus. Data is valid on the rising edge of $\overline{DS}$.
10	9	AD6	DI/ O	**Address/Data bus lines 6 and 7**. Used with pins 24-28 as the address/data bus.
11	10	AD7	DI/ O	
12	13	$\overline{WR}$ R/$\overline{W}$	DI	**Write** (Active Low) or **Write/Read**. On an Intel bus, driving this signal (Write) Low enables a write operation on the Address/Data bus. On a Motorola bus, driving this signal (Read/Write) High commands a read operation, driving it Low commands a write operation.
13 16	15 19	TTIP TRING	AO	**Transmit Tip and Ring**. Differential Driver Outputs. The design load for these outputs is 50 - 200 Ω. Select the transformer and line matching resistors to give the desired pulse height.
14	16	TGND	–	**Ground.** Ground return for the transmit drivers power supply TVCC.

1. I/O column entries DI = Digital Input; DO = Digital Output, DI/O = Digital Input and Output; AI = Analog Input , AO = Analog Output.
2. Pins 1, 6, 8, 11, 12, 17, 22, 23, 26, 28, 30, 33, 34, 40 and 44 are not connected (*n/c).*

Table 9: LXT351 Bipolar Mode Signal Assignments – continued

Pin NE/ PE	Pin QE[2]	Symbol	I/O[1]	Description
15	18	TVCC		**+5 VDC Power Supply** input for the transmit drivers. TVCC must not vary from VCC by more than ± 0.3 V.
17	20	$\overline{CS}$	DI	**Chip Select** (Active Low). For each read or write on the Address/Data bus, this pin must go Low during the operation. See Figures 22 and 23 for timing requirements. In the case of a single processor controlling several chips, this is the line it uses to command a specific transceiver.
18	21	$\overline{INT}$	DO	**Interrupt** (Active Low). This pin goes Low to signal an interrupt on the chip. To identify the specific interrupt, read the Performance Status Register. To clear or mask an interrupt, write a one to the appropriate bit in the Clear Interrupt Register.
19 20	24 25	RTIP RRING	AI	**Receive Tip and Ring**. The AMI signal received from the line is applied at these pins. A 1:1 transformer is required. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
21	27	VCC		**+5 VDC Power Supply** for all circuits except the transmit drivers. (Transmit drivers are supplied by TVCC.)
22	29	GND		**Ground** return for power supply VCC.
23 24 25 26 27 28	31 32 35 36 37 38	AD0 AD1 AD2 AD3 AD4 AD5	DI/ O	**Address/Data Lines 0-5**. (Also pins 10, 11–AD6 and 7) Conform to Intel and Motorola Address/Data bus specifications.

1. I/O column entries DI = Digital Input; DO = Digital Output, DI/O = Digital Input and Output; AI = Analog Input , AO = Analog Output.
2. Pins 1, 6, 8, 11, 12, 17, 22, 23, 26, 28, 30, 33, 34, 40 and 44 are not connected (*n/c).*

Table 10: LXT351 Unipolar Mode Signal Assignments[1]

Pin NE/ PE	Pin QE	Symbol	I/O[2]	Description
3	42	TDATA	DI	**Transmit Data**. Unipolar data for transmission onto the line.
4	43	INSBPV	DI	**Insert Bipolar Violation**. Controls bipolar violation insertions, requires Low-to-High transition to insert each violation, the LXT351 samples the signal on the falling edge of TCLK.
6	3	BPV	DO	**Bipolar Violation**. BPV goes High on receipt of a bipolar violation from the line. This is an NRZ output, valid on the rising edge of RCLK.
7	4	RDATA	DO	**Received Data**. RDATA is an NRZ output of the data recovered from the line interface. RDATA is valid on the rising edge of RCLK.

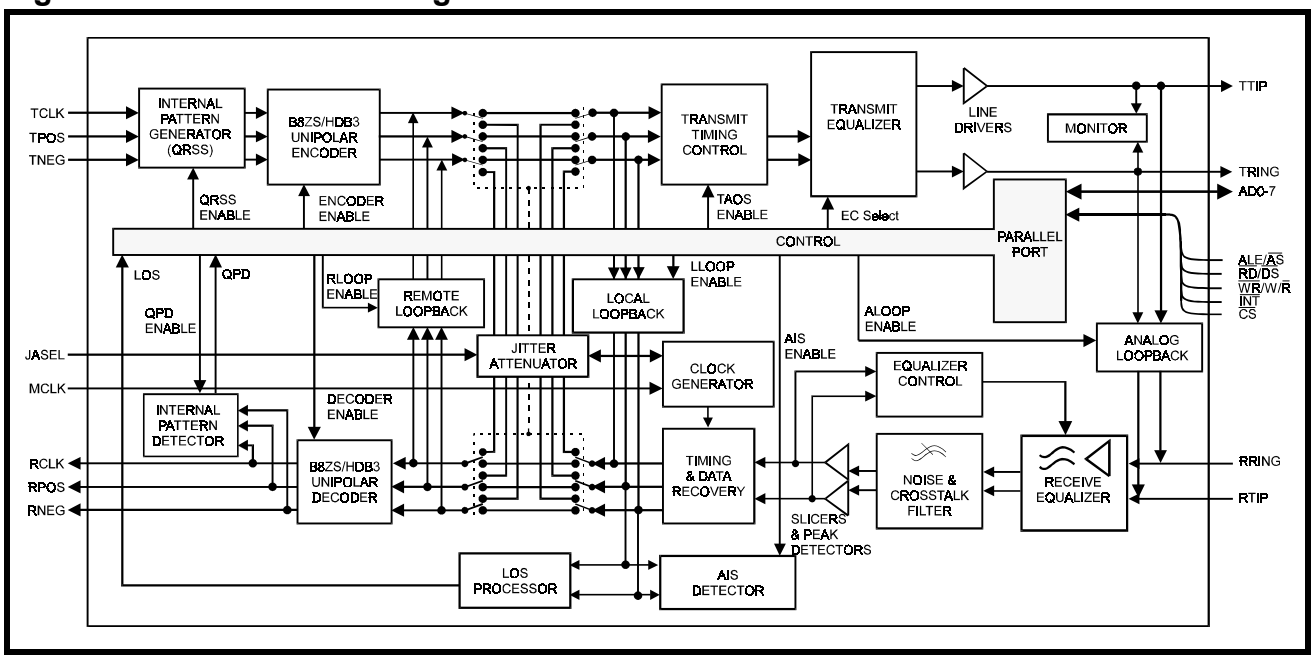
1. For the descriptions of pins not identified in this table, see Table 9: LXT351 Bipolar Mode Signal Assignments.
2. I/O column entries DI = Digital Input; DO = Digital Output, DI/O = Digital Input and Output; AI = Analog Input , AO = Analog Output.

Table 11: LXT351 QRSS Unipolar Mode Signal Assignments[1,2]

Pin NE/ PE	Pin QE	Symbol	I/O[3]	Description
3	42	INSLER	DI	**Insert Logic Error**. When this pin goes from Low to High, the transceiver inserts a logic error into the transmitted QRSS data pattern. The error follows the data flow in whatever loopback mode is in effect. The LXT351 samples this pin on the falling edge of TCLK (or MCLK, if TCLK is not present).
4	43	INSBPV	DI	**Insert Bipolar Violation**. When this pin goes from Low to High, the transceiver inserts a bipolar violation error into the transmitted QRSS data pattern. A subsequent insertion requires another Low to High transition. The LXT351 samples this pin on the falling edge of TCLK (or MCLK, if TCLK is not present).
6	3	BPV	DO	**Bipolar Violation**. BPV goes High on receipt of a bipolar violation from the line. This is an NRZ output, valid on the rising edge of SCLK.
7	4	RDATA	DO	**Received Data**. RDATA is an NRZ output of the data recovered from the line interface. RDATA is valid on the rising edge of RCLK.

1. For the descriptions of pins not identified in this table, see Table 9: LXT351 Bipolar Mode Signal Assignments.
2. In QRSS Bipolar Mode, pins 6 and 7of the NE/PE packages or pins 3 and 4 of the QE package act as RNEG and RPOS, respectively.
3. I/O column entries DI = Digital Input; DO = Digital Output, DI/O = Digital Input and Output; AI = Analog Input, AO = Analog Output.

Figure 3: LXT351 Block Diagram



FUNCTIONAL DESCRIPTION

The LXT350 and LXT351 are fully-integrated, PCM transceivers for or short-haul, 1.544 Mbps (T1) or 2.048 Mbps (E1) applications allowing full-duplex transmission of digital data over existing twisted-pair installations. They interface with two lines (one pair each for transmit and receive) through standard pulse transformers and appropriate resistors.

The figure on the front of this Data Sheet shows a block diagram of the LXT350. In Host Mode the device is controlled through a serial microprocessor. In Hardware Mode it is controlled via individual pins. Figure 3 is a block diagram of the LXT351. The LXT351 has a parallel port for microprocessor control. Both transceivers provide a high-precision, crystal-less jitter attenuator. The user may place it in the transmit or receive path, or bypass it completely. The transceivers meet or exceed ANSI, ITU and E1 requirements.

INITIALIZATION

During power up, the transceiver remains static until the power supply reaches approximately 3 V. On crossing this threshold, the device begins a 32 ms reset cycle to calibrate the Phase Locked Loops. The transceiver uses a reference clock to calibrate the PLL–the transmitter reference is TCLK, and the receiver reference clock is MCLK. MCLK is mandatory for chip operation.

Reset Operation

Reset clears and sets all registers to 0 and resets the status and state machines for the LOS, AIS and QRSS blocks. In Hardware Mode, holding pins RLOOP, LLOOP and TAOS High for at least one clock cycle resets the device. Writing a 1 to the bit CR2.RESET commands reset in Host Mode. Allow 32 ms for the device to settle after removing all reset conditions.

TRANSMITTER

Digital Data Interface

Input data for transmission onto the line is clocked serially into the device at the TCLK rate. TPOS and TNEG are the bipolar data inputs. TDATA accepts unipolar data. (Leaving TRSTE open enables Hardware Unipolar Mode.)

Input data may pass through either the Jitter Attenuator or B8ZS/HDB3 encoder or both. Bit CR1.ENCENB = 1 enables B8ZS/HDB3 encoding in Host Mode. In Hardware Mode, leaving the MODE pin open selects zero suppression coding. With zero suppression enabled, the EC*x* inputs (see Table 12) determine the coding scheme (B8ZS for T1 or HDB3 for E1 mode). For the HDB3 scheme, set EC3-1 to 000 or 001. Other EC*x* settings select the B8ZS option. The transmit clock (TCLK) supplies input synchronization. The Test Specifications section defines the transmit timing requirements for TCLK and the Master Clock (MCLK).

Short Circuit Current Limit

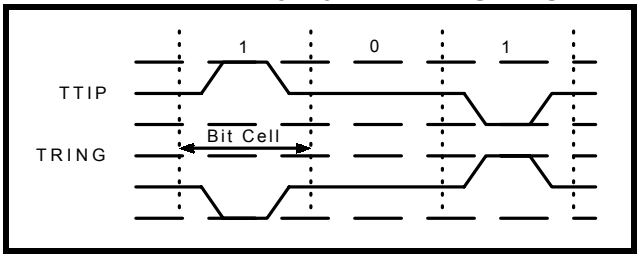
The transmitter includes a short-circuit limiter. This limits the current sourced into a low-impedance load. It automatically resets when the load current drops below the limit. The current is determined by the interface circuitry (total resistance on transmit side).

In Host Mode, the Performance Status Register flags open circuits in bit PSR.DFMO. A transition on DFMO will provide an interrupt and the transition sets bit TSR.DFMO = 1. Writing a 1 in bit ICR.CDFMO clears the interrupt; leaving a 1 in the bit masks that interrupt.

Output Drivers

The transceivers transmit data as a 50% line code as shown in Figure 4. Activating the line driver only during a mark reduces power consumption. The output driver is disabled during transmission of a space. Biasing of the transmit DC level is on-chip.

Figure 4: 50% Duty Cycle Coding Diagram



Idle Mode

Transmit Idle Mode is a normal operational mode (as opposed to modes) which allows multiple transceivers to be connected to a single line for redundant applications. TTIP and TRING remain in a high impedance state when TCLK is not present. Remote or Dual Loopback, TAOS or any internal transmit patterns temporarily disable the high impedance state.

Pulse Shape

The Equalizer Control inputs (EC3 through EC1) determine the transmitted pulse shape. In Host Mode, the I/O port controls the EC*x* values. For the LXT350 in Hardware Mode, three individual pins provide the EC*x* inputs.

Shaped pulses meeting the T1 DSX-1 and E1 specifications are applied to the AMI line driver for transmission onto the line at TTIP and TRING. Refer to the Test Specifications section for pulse mask specifications.

RECEIVER

A 1:1 transformer provides the interface to the line. Recovered data is output at RPOS/RNEG (RDATA in Unipolar mode), and the recovered clock is output at RCLK. The Test Specifications section shows receiver timing.

The transceiver filters the equalized signal and applies it to the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. The data slicers are set at 50% of the peak value to ensure optimum signal-to-noise performance for T1 or E1 operation.

After processing through the data slicers, the received signal goes to the data and timing recovery section, then to the B8ZS/HDB3 decoder (if selected) and to the receive monitor. The data and timing recovery circuits provide input jitter tolerance significantly better than required by AT&T Pub 62411 and ITU G.823. See the Test Specifications section.

Table 12: Equalizer Control Input Settings

EC3	EC2	EC1	Function	Pulse	Cable	Coding[1]
0	0	0	E1	ITU Rec G.703	75 Ω Coax/120 Ω TP	HDB3
0	1	1	T1	0-133 ft / 0.6 dB	100 Ω TP	B8ZS
1	0	0	T1	133-266 ft / 1.2 dB	100 Ω TP	B8ZS
1	0	1	T1	266-399 ft / 1.8 dB	100 Ω TP	B8ZS
1	1	0	T1	399-533 ft / 2.4 dB	100 Ω TP	B8ZS
1	1	1	T1	533-655 ft / 3.0 dB	100 Ω TP	B8ZS

1. When enabled.

Digital Data Interface

In either Host or Hardware Control Mode the recovered data goes to the Loss of Signal (LOS) Monitor. In Host Control Mode, it also goes through the Alarm Indication Signal (AIS, Blue Alarm) Monitor. The jitter attenuator circuit may be enabled or disabled in the receive data path or the transmit path. Received data may go through either the B8ZS or HDB3 decoder or neither. Finally, the device may send the digital data to the framer as either unipolar or bipolar data.

When transmitting unipolar data to the framer, the device reports receiving bipolar violations by driving the BPV pin High. During E1 operation in Host Control Mode, the device can report HDB3 code violations and Zero Substitution Violations on the BPV pin. The diagnostics section explains these options in more detail.

JITTER ATTENUATION

A Jitter Attenuation Loop (JAL) with an Elastic Store (ES) provides jitter attenuation as shown in the Test Specifications section. The JAL requires no special circuitry, such as an external quartz crystal or high-frequency clock (higher than the line rate). Its timing reference is the master clock, MCLK.

In Hardware Control Mode the ES is a 32 x 2-bit register. Setting the JASEL pin High places the JA circuitry in the received data path; setting JASEL Low places the JA in the transmit data path; leaving it open disables the JA.

In Host Mode, bit CR1.JASEL0 enables or disables the JA circuit. With bit CR1.JASEL0 = 1, bit CR1.JASEL1 controls the JA circuit placement (see Table 17). The ES can be either a 32 x 2-bit or 64 x 2-bit register depending on the value of bit CR3.ES64 (see Table 19.)

The device clocks data into the ES using either TCLK or RCLK depending on whether the JA circuitry is in the transmit or receive data path, respectively. Data is shifted out of the elastic store using the dejittered clock from the JAL. When the FIFO is within two bits of overflowing or underflowing, the ES adjusts the output clock by $^1/_8$ of a bit period. The ES produces an average delay of 16 bits (or 32 bits, with the 64-bit ES option selected in Host Control Mode) in the associated data path. When the Jitter Attenuator is in the receive path, the output RCLK transitions smoothly to MCLK in the event of an LOS condition.

The Transition Status Register bits TSR.ESOVR and TSR.ESUNF indicate an overflow or underflow, respectively in the ES. These are sticky bits: Once set to 1, they remain set until the host reads the register. The ES can also provide a maskable interrupt on either overflow or underflow.

DIAGNOSTIC MODE OPERATION

LXT350/351 offers multiple diagnostic modes as shown in Table 13. In Hardware Mode, the diagnostic modes are selected by a combination of pin settings. In Host Mode, the diagnostic modes are selected by writing appropriate bits in the Diagnostic Control Register.

Table 13: Diagnostic Mode Availability

Diagnostic Mode	Availability[1]		Host Mode[2] Maskable
	H/W	Host	
Loopback Modes			
Local Loopback (LLOOP)	Yes	Yes	No
Analog Loopback (ALOOP)	Yes	Yes	No
Remote Loopback (RLOOP)	Yes	Yes	No
Dual Loopback (DLOOP)	Yes	Yes	No
Internal Data Pattern Generation and Detection			
Transmit All Ones (TAOS)	Yes	Yes	No
Quasi-Random Signal Source (QRSS)	Yes	Yes	Yes
Error Insertion and Detection			
Bipolar Violation Insertion (INSBPV)	Yes	Yes	No
Logic Error Insertion (INSLER)	Yes	Yes	No
Bipolar Violation Detection (BPV)	Yes	Yes	No
Logic Error Detection, QRSS (QPD)	Yes	Yes	No
HDB3 Code Violation Detection (CODEV)	No	Yes	No
HDB3 Zero violation Detection (ZEROV)	No	Yes	No
Alarm Condition Monitoring			
Receive Loss of Signal (LOS) Monitoring	Yes	Yes	Yes
Receive Alarm Indication Signal (AIS) Monitoring	No	Yes	Yes
Transmit Driver Failure Monitoring—Open (DFMO)	No	Yes	Yes
Elastic Store Overflow and Underflow Monitoring	No	Yes	Yes
Built-In Self Test (BIST)	No	Yes	Yes

1. In Hardware Control Mode, a combination of pin settings selects the Diagnostic Modes; in Host Control Mode, writing appropriate bits into the Control Registers selects the Diagnostic Modes.
2. Host Control Mode allows interrupt masking by writing a "1" to the corresponding bit in the Interrupt Clear Register. Hardware Control Mode has no interrupt masking feature.

LOOPBACK MODES

NOTE
Hardware Mode pins discussed in this section refer to the LXT350 only.

Local Loopback

See Figures 5 and 6. In Hardware Mode, Local Loopback (LLOOP) is selected by tying LLOOP High; in Host Mode, by setting CR2.ELLOOP to 1. LLOOP inhibits the receiver circuits. The transmit clock and data inputs (TCLK and TPOS/TNEG or TDATA) loop back through the jitter attenuator (if enabled) and show up at RCLK and RPOS/RNEG or RDATA. (During LLOOP, the JASEL input is strictly an Enable/Disable control; it does not affect the placement of the JAL. If JA is enabled, it is active in the loopback circuit. If JA is bypassed, it is not active in the loopback circuit.)

The transmitter circuits are unaffected by LLOOP. LXT350/351 transmits the TPOS/TNEG or TDATA inputs (or a stream of 1s if TAOS is asserted) normally. When used in this mode, the transceiver can function as a stand-alone jitter attenuator.

Figure 5: TAOS with LLOOP (JA Selected)

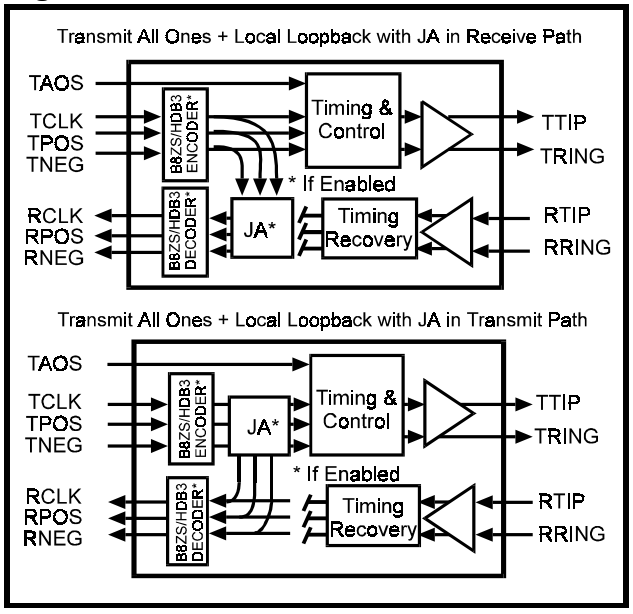
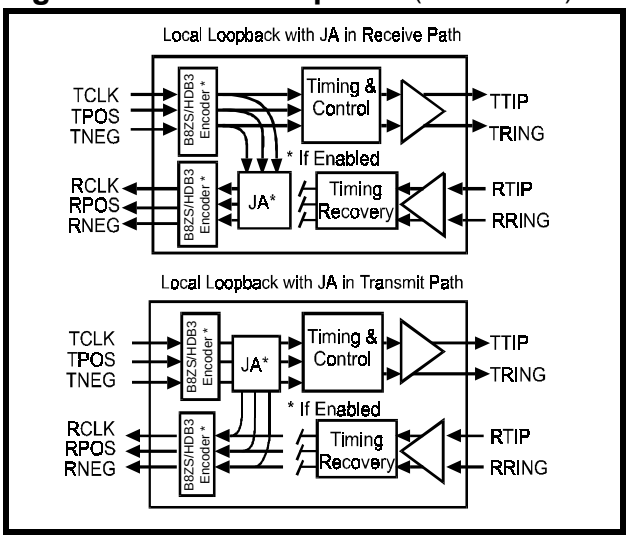


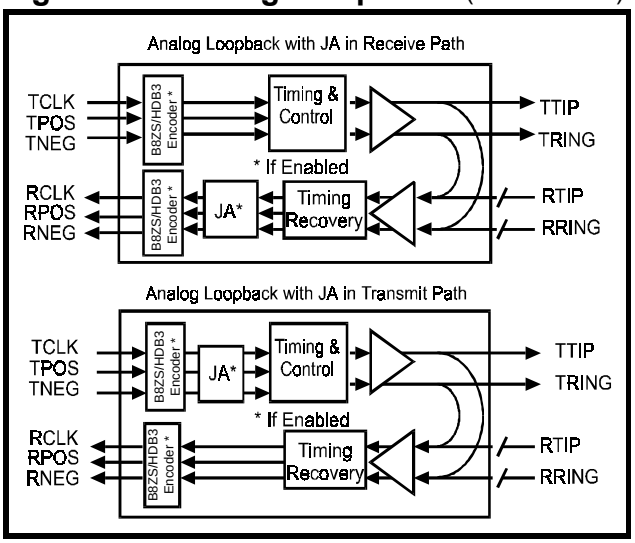
Figure 6: Local Loopback (JA Selected)



Analog Loopback

See Figure 7. Analog Loopback (ALOOP) exercises the maximum number of functional blocks. ALOOP operation disconnects the RTIP/RRING inputs from the line and routes the transmit outputs back into the receive inputs. This tests the encoders/decoders, jitter attenuator, transmitter, receiver and timing recovery sections. In Hardware Mode, leaving pin 27 open commands Analog Loopback; in Host Mode, writing a 1 to bit CR2.EALOOP enables the function. The ALOOP function overrides all other loopback modes.

Figure 7: Analog Loopback (JA Selected)



Remote Loopback

See Figure 8. In Remote Loopback (RLOOP) mode, the device ignores the transmit data and clock inputs (TCLK and TPOS/TNEG or TDATA), and bypasses the in-line encoders/decoders. The RPOS/RNEG or RDATA outputs loop back through the transmit circuits to TTIP and TRING at the RCLK frequency. The RLOOP command does not affect the receiver circuits which continue to output the RCLK and RPOS/RNEG or RDATA signals received from the twisted-pair line. In Host Mode, command RLOOP by writing a 1 to bit CR2.ERLOOP. In Hardware Mode, RLOOP is commanded by setting pin 26 High.

Dual Loopback

See Figure 9. To select Dual Loopback (DLOOP), set both RLOOP and LLOOP High in Hardware Mode or set bits CR2.ERLOOP and CR2.ELLOOP to 1 in Host Mode. In DLOOP mode, the transmit clock and data inputs (TCLK and TPOS/TNEG or TDATA) loop back through the Jitter Attenuator (unless disabled) to RCLK and RPOS/RNEG or RDATA. The data and clock recovered from the line loop back through the transmit circuits to TTIP and TRING without jitter attenuation.

Figure 8: Remote Loopback (JA Selected)

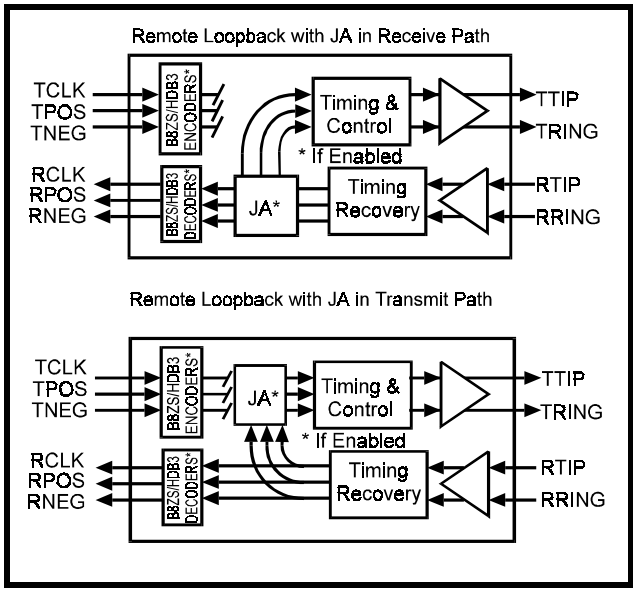
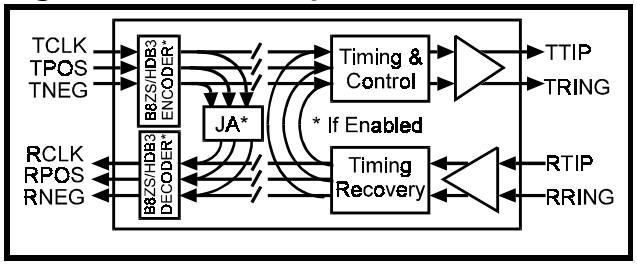


Figure 9: Dual Loopback

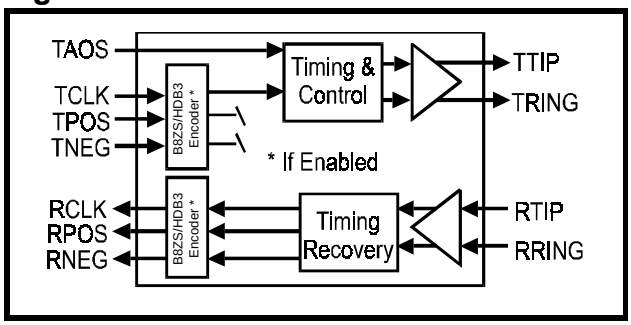


INTERNAL PATTERN GENERATION AND DETECTION

Transmit All Ones

See Figure 10. In Transmit All Ones (TAOS) Mode the transceiver ignores the TPOS and TNEG inputs and transmits a continuous stream of 1s at the TCLK frequency. (With no TCLK, the TAOS output clock is MCLK.) This can be used as the Alarm Indication Signal (AIS–also called the Blue Alarm). In Host Mode, TAOS is commanded by writing a 1 to bit CR2.ETAOS. In Hardware Mode setting pin 28 High does so. Both TAOS and Local Loopback can occur simultaneously as shown in Figure 5, but Remote Loopback inhibits TAOS. When both TAOS and LLOOP are active, TCLK and TPOS/TNEG loop back to RCLK and RPOS/RNEG through the jitter attenuator (if enabled), and an all ones pattern goes to TTIP/TRING.

Figure 10: TAOS Data Path



Quasi-Random Signal Source (QRSS)

For T1 operation the Quasi-Random Signal Source (QRSS) is a 2^{20}-1 pseudo-random bit sequence (PRBS) with no more than 14 consecutive zeros. For E1 operation, QRSS is 2^{15}-1 PRBS with inverted output.

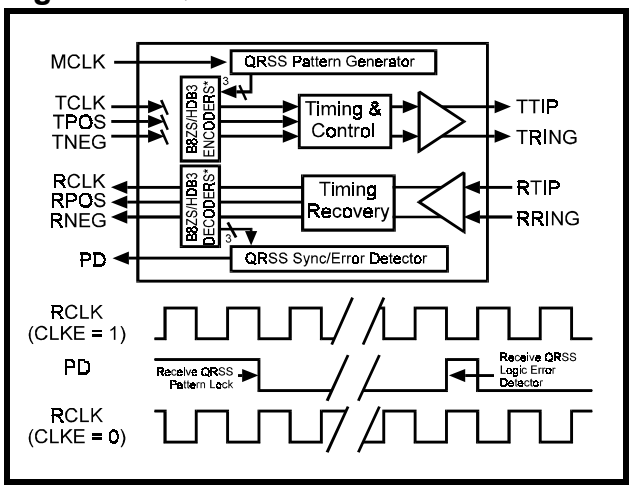
Both Hardware and Host Modes allow QRSS Mode. The QRSS pattern is normally locked to TCLK; but if there is no TCLK, MCLK is the clock source. Bellcore Pub 62411 defines the T1 QRSS transmit format and ITU G.703 defines the E1 format.

Leaving TAOS (pin 28) open enables QRSS transmission in Hardware Mode. In Host Mode, setting bits CR2.EPAT0 = 0 and CR2.EPAT1=1enables this function.

With QRSS transmission enabled, it is possible to insert a logic error into the transmit data stream by causing a Low-to-High transition on INSLER (pin 3). However, if no logic or bit errors are to be inserted into the QRSS pattern, INSLER must remain Low. Logic Error insertion waits until the next bit if the current bit is “jammed”. (When there are more than 14 consecutive 0s, the output is jammed to a 1.)

Furthermore a bipolar violation in the QRSS pattern is possible by causing a Low-to-High transition on INSBPV (pin 4) without regard to whether the device is in bipolar or unipolar operating mode.

Figure 11: QRSS Mode



Choosing QRSS Mode also enables the QRSS Pattern Detection (QPD) in the receive path. The QRSS pattern is synchronized when there are fewer than four errors in 128 bits. After achieving synchronization the device drives QPD (pin 12) Low (QPD output is available on LXT350 only). The LXT351 does not support bit error detection in QRSS Mode. In the LXT350 QRSS Mode, any subsequent bit error in the QRSS pattern causes QPD to go High for half an RCLK clock cycle (the precise relationship to RCLK depends on the value of CLKE–when CLKE is Low, QPD goes High while RCLK is High; if CLKE is High, QPD goes High while RCLK is Low). This signal edge can serve as a trigger for an external bit-error counter. An LOS condition or a loss of QRSS synchronization will cause this output to go High continuously. In this case, and with either Unipolar Mode or the encoders/decoders enabled, the BPV pin indicates BPVs, CODEVs or ZEROVs as chosen.

Host Mode offers an additional interrupt to indicate that QRSS detection and sychronization have occurred, or that synchronization is lost. This interrupt is available when bit ICR.CQRSS = 0. If the QPD signal triggers a bit error counter, the interrupt could start or reset the counter.

Also in Host Mode, the PSR.QRSS bit provides an indication of the QRSS pattern synchronization. This bit goes Low with no QRSS pattern detected (*i.e.*, when there are more than four errors in 128 bits). The TQRSS bit in the Transition Status Register indicates that QRSS status has changed since the last QRSS Interrupt Clear command.

ERROR INSERTION AND DETECTION

Bipolar Violation Insertion (INSBPV)

In Unipolar Mode, both Hardware and Host Modes provide for Bipolar Violation Insertion (INSBPV). Choosing Unipolar Mode configures pin 4 as INSBPV. Bipolar violation insertion requires a Low-to-High transition on INSBPV. Sampling occurs on the falling edge of TCLK. When INSBPV goes High a BPV is inserted on the next available mark except in the three following situations:

- Zero suppression (HDB3 or B8ZS) is not violated
- If LLOOP and TAOS are both active, the BPV is looped back to RNEG/BPV indicator and the line driver transmits all ones with no violation.
- BPV insertion is disabled with RLOOP (remote loopback) active.

With the LXT350/351 configured to transmit internally generated QRSS data patterns a BPV can be inserted on the transmit pattern independent of whether the device is in the unipolar or bipolar mode of operation.

Logic Error Insertion (INSLER)

When configured to transmit internally generated QRSS data patterns, the device can insert a logic error on the transmit data pattern when there is a Low-to-High transition on INSLER. The transceiver treats data patterns the same way it treats data applied to TPOS/TNEG, so the inserted logic error will follow the data flow path as defined by the loopback mode in effect.

Logic Error Detection (QPD) (LXT350 Only)

After receiving pattern synchronization when configured in the QRSS Mode, LXT350 reports logic errors on QPD (pin 12). To indicate a logic error, this pin goes High for half an RCLK cycle (during the High period of RCLK if CLKE is Low but during the Low RCLK period if CLKE is High). To monitor logic errors, connect an error counter to QPD. A continuous High level on this pin indicates loss of either the QRSS pattern lock or LOS condition. The QRSS section has additional details on QRSS pattern lock criteria.

Bipolar Violation Detection (BPV)

With the internal encoders/decoders enabled or when configured in Unipolar Mode, the LXT350/351 reports received Bipolar Violations at BPV (pin 6). The pin goes High for a full clock cycle to indicate receipt of a BPV. However, if the encoders/decoders are enabled, LXT350/351 does not report bipolar violations due to the line coding scheme.

HDB3 Code Violation Detection (CODEV)

LXT350/351 can detect HDB3 code violations in Host Mode with HDB3 encoders enabled. This requires CR1.ENCENB = 1 and CR1.EC3-1 = 000, 001 or 010, which establishes E1 operation. To enable CODEV, set bit CR4.CODEV = 1.

An HDB3 code violation (CODEV) occurs when the device receives two consecutive bipolar violations of the same polarity (refer to ITU O.161). With CODEV detection enabled, LXT350/351 reports a violation on the BPV pin along with received BPVs and ZEROVs (if these options are enabled). LXT350/351 forces the BPV pin High for a full RCLK cycle to report a CODEV.

HDB3 Zero Substitution Violation Detection (ZEROV)

With encoders/decoders enabled, the LXT350/351 can detect HDB3 zero substitution violations (ZEROV) in Host Mode. This requires CR1.ENCENB = 1 and CR1.EC3-1 = 000, 001, or 1010, which establish E1 operation, and CR4.ZEROV = 1.

LXT350/351 forces the BPV pin High for a full RCLK cycle to report a ZEROV. An HDB3 ZEROV is the receipt of four or more consecutive zeros. This does not occur with correctly encoded HDB3 data unless there are transmission errors. With ZEROV detection enabled, the device reports a violation on the BPV pin along with received BPVs and CODEVs (if these options are enabled).

ALARM CONDITION MONITORING

Loss of Signal (LOS)

The LXT350/351 Loss of Signal (LOS) monitor function is compatible with ITU G.775 and ETSI 300233. They use a combination analog and digital detection scheme. The receiver LOS monitor loads a digital counter at the RCLK frequency. The counter increments with each received 0 and it resets to 0 on receipt of a 1. Any signal that remains 25 dB typical below the nominal 0dB signal for n consecutive pulse generates an internal LOS condition. For T1 operations, n = 175; for E1 operations, n = 32. In Host Mode, either number can be changed to 2048 by setting bit CR4.LOS2048 to 1. MCLK replaces the recovered clock at the RCLK output in a smooth transition.

For T1 operation, when the received signal has 12.5% 1s density (16 marks in a sliding 128-bit period, with fewer than 100 consecutive 0s), the LOS flag returns Low and the recovered clock replaces MCLK at the RCLK output in another smooth transition.

For E1 operation, the LOS condition is cleared when the received signal rises above 25 dBtypical below the minimum 0 dB level and has 12.5% 1s density (four 1s in a sliding 32-bit window with fewer than 16 consecutive 0s). In Host Mode E1 operation, the out-of-LOS criterion can be modified from 12.5% marks density to 32 consecutive marks by setting bit CR4.COL32CM = 1.

During LOS, the device sends received data to the RPOS/RNEG pins (or RDATA in Unipolar Mode). LXT350 reports an LOS condition on the LOS pin in Hardware Mode. In Host Mode, the LOS bit in the Performance Status Register goes High to indicate an LOS condition and will interrupt the host controller if so programmed.

Alarm Indication Signal Detection (AIS)

The Alarm Indication Signal (AIS) is available only in Host Mode. The receiver detects an AIS pattern when it receives fewer than three 0s in any string of 2048 bits. The device clears the AIS condition when it receives three or more 0s in a string of 2048 bits.

The AIS bit in the Performance Status Register indicates AIS detection. When the AIS status changes, the TAIS bit in the Transition Status Register goes High. The change of status interrupts the host controller by pulling $\overline{\text{INT}}$ Low, unless the interrupt is masked. Writing a 1 to the ICR.CAIS bit masks the interrupt until the bit returns to 0.

Driver Failure Mode Open (DFMO)

In Host Mode a DFM Open (DFMO) bit is available in the Performance Status Register to indicate an open condition on the lines. DFMO can generate an $\overline{\text{INT}}$ to the host controller. The Transition Status Register bit DFMO indicates a transition in the status of the bit. Writing a 1 to ICR.CDFMO will clear or mask the interrupt.

Elastic Store Overflow/Underflow (ESOVR/ESUNF)

When the bit count in the Elastic Store (ES) is within two bits of overflowing or underflowing the ES adjusts the output clock by $^1/_8$ of a bit period. In Host Mode, the ES provides an indication of overflow and underflow in the TRS.ESOVR and TSR.ESUNF. These are sticky bits and will stay set to 1 until the host controller reads the register. These interrupts can be cleared or masked by writing a 1 to the bits ICR.CESO and ICR.CESU, respectively.

OTHER DIAGNOSTIC MODES

Built-In Self Test (BIST)

LXT350/351 provides a Built-In Self Test (BIST) capability in Host Mode. The BIST exercises the internal circuits

by providing an internal QRSS pattern, running it through the encoders and the transmit drivers then looping it back through the receive equalizer, Jitter Attenuator and decoders to the QRSS pattern detection circuitry. If all the blocks in this data path work correctly, the receive pattern detector locks onto the pattern. It then pulls $\overline{INT}$ Low and sets the following bits High:

- TSR.TQRSS
- PSR.QRSS
- PSR.BIST

The QPD pin (pin 12) also indicates completion status of the test. Starting the test forces this pin High. During the test, it remains High until the test finishes successfully at which time it goes Low.

OPERATING MODES

The LXT350/351 share many features. However, their control modes are very different.

- The LXT350 operates in either Hardware or (Serial Port) Host Mode
- The LXT351 operates in (Parallel Port) Host Mode only.

In the Hardware Mode (LXT350 only) individual pins control the transceiver.

The logic level at the MODE pin sets the LXT350 mode of operation. In Host Mode (LXT350/351), a microprocessor controls the device through a data interface. The LXT350 has a serial interface and the LXT351 uses a parallel interface.

Hardware Mode Operation (LXT350 Only)

The LXT350 operates in Hardware Mode when MODE is left open or set Low. In Hardware Mode individual pins access and control the transceiver. The outputs (RPOS/RNEG or RDATA) are valid on the rising edge of RCLK.

There are some advanced functions provided only in Host Mode. Interrupt ($\overline{INT}$), AIS detection indicator, DFM open indicator and CLKE functions are some of the features available in Host Mode.

Table 14: Control and Operational Mode Selection for LXT350 Transceiver

Input to Pin[1]		Mode of Operation						
Mode	**TRSTE**	**Hardware**	**Software**	**Unipolar**	**Bipolar**	**AMI Enc/Dec**	**B8ZS/HDB3 Encoder/Decoder**	**All Outputs Tristated**
Low	Low	On	Off	Off	On	Off[3]	Off	No
Low	High	On	Off	Off	On	Off[3]	Off	Yes
Low	Open	On	Off	On	Off	On	Off	No
High[2]	Low	Off	On	x	x	x	x	No
High[2]	High	Off	On	x	x	x	x	Yes
High[2]	Open	Off	On	x	x	x	x	No
Open	Low	On	Off	On	Off	Off	On	No
Open	High	On	Off	On	Off	Off	On	Yes
Open	Open	On	Off	On	Off	Off	On	No

1. Open is either a midrange voltage or the pin is floating
2. In Software Mode, the contents of register CR1 determine the operation mode.
3. Encoding is done externally.

Host Mode Operation

The LXT350 operates in Host Mode when MODE is set High. In Host Mode a microprocessor accesses and controls the transceiver through a data port using the internal registers. The outputs (RPOS/RNEG or RDATA) are valid on the rising edge of RCLK

In Host Mode there are eight control and status registers–five read/write and three read-only registers. The LXT350 accesses them through its serial interface (SIO). The LXT351 provides this access using an 8-bit parallel interface (PIO).

The host processor/controller can completely configure the device as well as get a full diagnostic/status report

through the SIO or PIO. Only the clocks and data for Bipolar Mode and BPV/Logic Error insertions for Unipolar or QRSS Mode need to be provided directly to the input pins. Similarly, the recovered clock, data, and BPV/Logic Error occurrences are available only at output pins. All other mode settings and diagnostic information are available through the data port.

Table 15 shows the address used by the SIO or PIO to access each register on the LXT350 or LXT351, respectively. Table 16 summarizes the control and status registers and labels each bit they contain. Tables 17 through 23 identify the bits in each register.

Table 15: Serial (LXT350) and Parallel (LXT351) Port Register Addresses

Register		Address[1]	
Name	Abbr	Serial Port (A7-A1)	Parallel Port (A7-A0)
Control #1	CR1	x010000	x010000x
Control #2	CR2	x010001	x010001x
Control #3	CR3	x010010	x010010x
Interrupt Clear	ICR	x010011	x010011x
Transition Status	TSR	x010100	x010100x
Performance Status	PSR	x010101	x010101x
Control #4	CR4	x010111	x010111x

1. x = “don’t care”.

Table 16: Register Addresses and Bit Names

Register		Type	Bit							
Name	Sym		7	6	5	4	3	2	1	0
Control #1	CR1	R/W	JASLE1	JASEL0	ENCEB	UNIENB	*reserved*[2]	EC3	EC2	EC1
Control #2	CR2	R/W	RESET	EPAT1	EPAT0	ETAOS	*reserved*[2]	EALOOP	ELLOOP	ERLOOP
Control #3	CR3	R/W	JA6HZ	PCLKE[1]	SBIST	*reserved*[2]	*reserved*[2]	ES64	ESCEN	ESJAM
Interrupt Clear	ICR	R/W	CESU	CESO	CDFMO	*reserved*[3]	CQRSS	CAIS	*reserved*[3]	CLOS
Transition Status	TSR	R	ESUNF	ESOVR	TDFMO	*reserved*[2]	TQRSS	TAIS	*reserved*[2]	TLOS
Performance Status	PSR	R	*reserved*[2]	BIST	DFMO	*reserved*[2]	QRSS	AIS	*reserved*[2]	LOS
Control #4	CR4	R/W	*reserved*[2]	*reserved*[2]	*reserved*[2]	*reserved*[2]	COL32CM	LOS2048	ZEROV	CODEV

1. Bit CR3.PCLKE is available only in the LXT351; for the LXT350, set this bit to zero.
2. In write registers, bits labeled reserved should be set to 0 (except as in note 3 below) for normal operation and ignored in read only registers.
3. Write a 1 into this bit for normal operation.

Table 17: Control Register #1 Read/Write, Address (A7-A1) = x010000

Bit	Name	Function	Jitter Attenuation		
			JASEL0	JASEL1	Position
0	EC1	Set the Equalizer Control codes (see Table 12).	1	0	Transmit
1	EC2		1	1	Receive
2	EC3		0	X	disabled
3	—	*reserved, set this bit to 0, ignore when reading.*			
4	UNIENB	Enables Unipolar I/O Mode and insertion/detection of BPVs.			
5	ENCENB	Enables B8ZS/HDB3 encoders/decoders; device enters Unipolar Mode and pins 3, 4, 6 and 7 change to their unipolar functions.			
6	JASEL0	Jitter Attenuation Mode, selects jitter attenuation circuitry position in data path or disables it. See right hand section of table for values. ↗			
7	JASEL1				

Table 18: Control Register #2 Read/Write, Address (A7-A1) = x010001

Bit	Name	Function	Pattern		
			EPAT0	EPAT1	Selected
0	ERLOOP[1]	Enables Remote Loopback (RLOOP)	0	0	Transmit TPOS/TNEG
1	ELLOOP[1]	Enables Local Loopback (LLOOP)	0	1	Detect and transmit QRSS
2	EALOOP	Enables Analog Loopback (ALOOP)			
3	—	*reserved, set this bit to 0, ignore when reading.*			
4	ETAOS	Enables Transmit All Ones (TAOS)			
5	EPAT0	Enables internal data pattern transmission. See right hand section of table for values.			
6	EPAT1				
7	RESET	RESET = 1 resets device state and all registers.			

1. To enable Dual Loopback (DLOOP), set both ERLOOP = 1, ELLOOP = 1.

Table 19: Control Register #3 Read/Write, Address (A7-A1) = x010010

Bit	Name	Description
0	ESJAM	Disables Jamming of Elastic Store Read Out Clock ($^1/_8$ bit-time adjustment for over/underflow).
1	ESCEN	Centers ES pointer for a difference of 16 or 32 (depending on depth-clears automatically).
2	ES64	Increases ES depth from 32 to 64 bits.
3	—	*reserved–set to 0 for normal operation.*
4	—	*reserved–set to 0 for normal operation.*
5	SBIST	Starts Built-In Self Test.
6	PLCKE	This bit is meaningful only in the LXT351– *for LXT350, set this bit to 0.* PCLKE = 0 sets RPOS/RNEG valid on the rising edge of RCLK. PCLKE = 1 sets RPOS/RNEG valid on the falling edge of RCLK .
7	JA6HZ	When JA6HZ = 1, changes bandwidth of Jitter Attenuation Loop from 3 Hz (default) to 6 Hz.

Table 20: Interrupt Clear Register Read/Write, Address (A7-A1) = x010011

Bit	Name	Function[1]
0	CLOS	Clears/Masks LOS Interrupt.
1	—	*reserved, set this bit to 1* for normal operation.
2	CAIS	Clears/Masks AIS Interrupt.
3	CQRSS	Clears/Masks QRSS Interrupt.
4	—	*reserved–set this bit to 1 for normal operation.*
5	CDFMO	Clears/Masks DFMO.
6	CESO	Clears/Masks ES Overflow Interrupt.
7	CESU	Clears/Masks ES Underflow Interrupt.

1. Leaving a one in any of these bits masks the associated interrupt.

Table 21: Transition Status Register Read Only, Address (A7-A1) = x010100

Bit	Name	Function
0	TLOS	Loss of Signal (LOS) has changed since last clear LOS interrupt occurred.
1	—	*reserved-ignore.*
2	TAIS	AIS has changed since last clear AIS interrupt occurred.
3	TQRSS	QRSS has changed since last clear QRSS interrupt occurred[1].
4	—	*reserved-ignore.*
5	TDFMO	DFMO has changed since last clear DFMS interrupt occurred.
6	ESOVR	ES overflow status sticky bit[2].
7	ESUNF	ES underflow status sticky bit[2].

1. A QRSS transition indicates receive QRSS pattern sync or loss. A simple error in QRSS pattern is not reported as a transition.
2. Tripping the overflow or underflow indicator in the ES sets the ESOVR/ESUNF status bit(s). Reading the Transition Status Register clears these bits. Setting CESO and CESU in the Interrupt Clear Register masks these interrupts.

Table 22: Performance Status Register Read Only, Address (A7-A1) = x010101

Bit	Name	Function
0	LOS	Loss of Signal (LOS) Status.
1	—	*reserved-ignore.*
2	AIS	Alarm Indicator (AIS) Status.
3	QRSS	QRSS Pattern Detect Status.
4	—	*reserved–ignore.*
5	DFMO	Driver Open Indication.
6	BIST	Built-In Self Test Status.
7	—	*reserved–ignore*

Table 23: Control Register #4 Read/Write, Address (A7-A1) = x010111

Bit	Name	Function
0	CODEV	Enables detection of HDB3 code violation on the BPV pin along with bipolar violations and ZEROVs (as enabled).
1	ZEROV	Enables detection of four consecutive zeros (an HDB3 coding violation) on the BPV pin along with bipolar violation and ZEROVs (as enabled).
2	LOS2048	Changes LOS detection threshold from 32 consecutive zeros (for E1 operation) or 175 consecutive zeros (T1 operation) to 2048 consecutive zeros in either environment.
3	COL32CM	In E1 Mode, changes "clear LOS condition" criterion from 12.5% marks density (default) to receipt of 32 consecutive marks.
4	—	*reserved–set to 0 for normal operation; ignore when reading.*
5	—	*reserved–set to 0 for normal operation; ignore when reading.*
6	—	*reserved–set to 0 for normal operation; ignore when reading.*
7	—	*reserved–set to 0 for normal operation; ignore when reading.*

Serial Port Operation (LXT350 Only)

The LXT350 operates in Host Mode when the MODE pin is set High. Figure 12 shows the SIO data structure. The registers are accessible through a 16-bit word: an 8-bit Command/Address byte (bits R/$\overline{W}$ and A1-A7) and a subsequent 8-bit data byte (bits D0-7). Bit R/$\overline{W}$ determines whether a read or a write operation occurs. Bits A6-1 in the Command/Address byte address specific registers (the address decoder ignores bit A7). The data byte depends on both the value of bit R/$\overline{W}$ and the address of the register as set in the Command/Address byte.

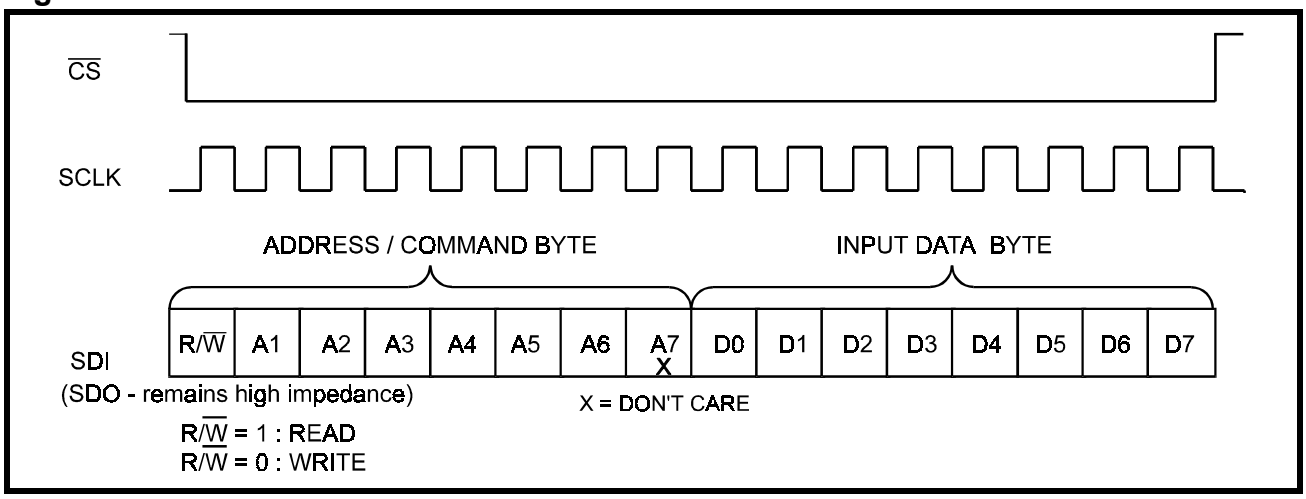
Host Mode provides a latched interrupt output ($\overline{INT}$). A change in the state of any of the following bits in the Performance Status Register will drive $\overline{INT}$ Low: LOS, AIS, QRSS, or DFMO. An interrupt will also occur when there is an elastic store overflow or underflow. When the interrupt has occurred, the $\overline{INT}$ output pin is pulled Low. The output stage of each $\overline{INT}$ pin consists only of a pull-down device, so each one requires an external pull-up resistor. The interrupt is cleared when the interrupt condition no longer exists, and the host processor writes a 1to the respective interrupt causing bit(s) in the Interrupt Register. Leaving a 1 in any of these interrupt status bits masks that interrupt.

Host Mode also allows control of the serial data and receive data output timing. The clock edge (CLKE) signal determines when the outputs are valid, relative to the Serial Clock (SCLK) or RCLK as shown in Table 24.

Table 24: CLKE Settings

CLKE	Output	Clock	Valid Edge
Low	RPOS	RCLK	Rising
	RNEG	RCLK	Rising
	SDO	SCLK	Falling
High	RPOS	RCLK	Falling
	RNEG	RCLK	Falling
	SDO	SCLK	Rising

Figure 12: LXT350 Serial Interface Data Structure



Parallel Port Operation (LXT351 Only)

The LXT351 address/control bus pins and control pins are compatible with both the Intel and Motorola address/data buses. See Figures 22 and 23 for the I/O timing diagram for each bus. The device automatically detects bus timing based on the Intel and Motorola microprocessor bus specifications. The maximum recommended processor speed for an Intel device is 20 MHz; for a Motorola device, 16.78 MHz. Table 17 summarizes the control and status registers for the LXT351. Tables 17 through 23 identify and explain the bits in the control registers.

The LXT351 provides a latched interrupt output ($\overline{INT}$). A change in the state of any of the following bits in the Performance Status Register will drive $\overline{INT}$ Low: LOS, AIS, QRSS, DFMO. When the interrupt has occurred, the $\overline{INT}$ output pin is pulled Low. The output stage of $\overline{INT}$ pin consists only of a pull-down device, so each pin requires an external pull-up resistor. The interrupt is cleared when the interrupt condition no longer exists, and the host processor writes a 1 to the respective interrupt causing bit(s) in the Interrupt Register. Leaving a 1 in any of these interrupt status bits masks that interrupt.

The received data output is valid on the rising edge of RCLK, when bit CR3.PCLKE = 0. The data output is valid on the falling edge of RCLK when CR3.PCLKE =1.

There are five read/write and three read-only registers. Only bits A6-1 in the address byte are valid. (The address decoder ignores bits A7 and A0.) Tables 17 through 23 show the register address bits A7-1, without regard to bit A0.

APPLICATION INFORMATION

NOTE

This application information is for design aid only.

Table 25 shows the specification for transmit return loss in E1 applications. (The G.703/CH PTT specification is a Swiss Telecommunications Ministry specification.)

Table 26 shows the transmit return loss values for T1 applications. Table 34 shows the receive return loss values.

Table 25: E1 Transmit Return Loss Requirements

Frequency Band	Return Loss	
	ETS 300 166	G.703/CH PTT
51-102 kHz	6 dB	8 dB
102-2048 kHz	8 dB	14 dB
2048 - 3072 kHz	8 dB	10 dB

Table 26: Transmit Return Loss (2.048 Mbps)

EC3-1	Xfrmr/ Rt	Rload (Ω)	Cl (pF)	Return Loss (dB)
000	1:2/ 9.1 Ω	75	0	14
			470	16
		120	0	12
			470	13
	1:2.3/ 9.1 Ω	120	0	13
			470	16

Table 27: Transmit Return Loss (1.544 Mbps)

EC3-1	Xfrmr/ Rt	Rload (Ω)	Cl (pF)	Return Loss (dB)
011[2]	1:2/ 9.1 Ω	100	0	16
			470	17
	1:1.15[1]/ 0.0 Ω	100	0	2
			470	2

1. A 1:1.15 transmit transformer keeps the total transceiver power dissipation at a low level, a 0.47 µF DC blocking capacitor must be placed on TTIP or TRING.
2. Refer to Table 12.

Table 28: Transformer Specifications for LXT350/LXT351

Tx/ Rx	Frequency MHz	Turns Ratio	Primary Inductance µH (minimum)	Leakage Inductance µH (max)	Interwinding Capacitance pF (max)	DCR Ω (maximum)	Dielectric[1] Breakdown V (minimum)
Tx	1.544	1:1.15	600	0.80	60	0.90 pri 1.70 sec	1500 V_{RMS}
	2.048	1:2.3	600	0.80	60	0.70 pri 1.20 sec	1500 V_{RMS}[2] (3000 V_{RMS})
	1.544/2.048	1:2	600	0.80	60	1.0 pri 1.70 sec	1500 V_{RMS}[2] (3000 V_{RMS})
Rx	1.544/2.048	1:1	600	1.10	60	1.10 pri 1.10 sec	1500 V_{RMS}[2] (3000 V_{RMS})

1. Some ETSI applications may require a 2.3 kV dielectric breakdown voltage.
2. Some applications require transformers to guarantee performance in extended temperature range (-40° to +85° C) ETSI applications require a dielectric breakdown voltage of 3000 V_{RMS}.

Table 29: Recommended Transformers for LXT350/LXT351

Tx/Rx	Turns Ratio	Part Number	Manufacturer
Tx	1:1.15	PE-65388	Pulse Engineering
		PE-65770	
		16Z5952	Vitec
	1:2	PE-65351	Pulse Engineering
		PE-65771	
		0553-5006-IC	Bell-Fuse
		66Z-1308	Fil-Mag
		671-5832	Midcom
		67127370	Schott Corp
		67130850	
		TD61-1205D	HALO (combination Tx/Rx set)
		TG26-1205NI	HALO (surface mount dual transformer 1CT:2CT & 1CT:2CT)
		TG48-1205NI	HALO (surface mount dual transformer 1CT:2CT & 1:1)
		16Z5946	Vitec
	1:2.3	PE-65558	Pulse Engineering
Rx	1:1	FE 8006-155	Fil-Mag
		671-5792	Midcom
		PE-64936	Pulse Engineering
		PE-65778	
		67130840	Schott Corp
		67109510	
		TD61-1205D	HALO (combination Tx/Rx set)

Figure 13 shows a typical LXT350 application in either or T1 or E1 environment. See Tables 26 through 31 to select the transformers (T1 and T2), resistors (Rt and Rl) and capacitors (Cl) needed for this application.

NOTE

If the application includes surge protection, such as a varistor or sidactor on the TTIP/TRING lines, it may also require reducing the value of the capacitor CL or eliminating it completely. Excessive capacitance at CL will distort the transmitted signals.

Figure 13: Typical T1/E1 LXT350 Hardware Mode Application

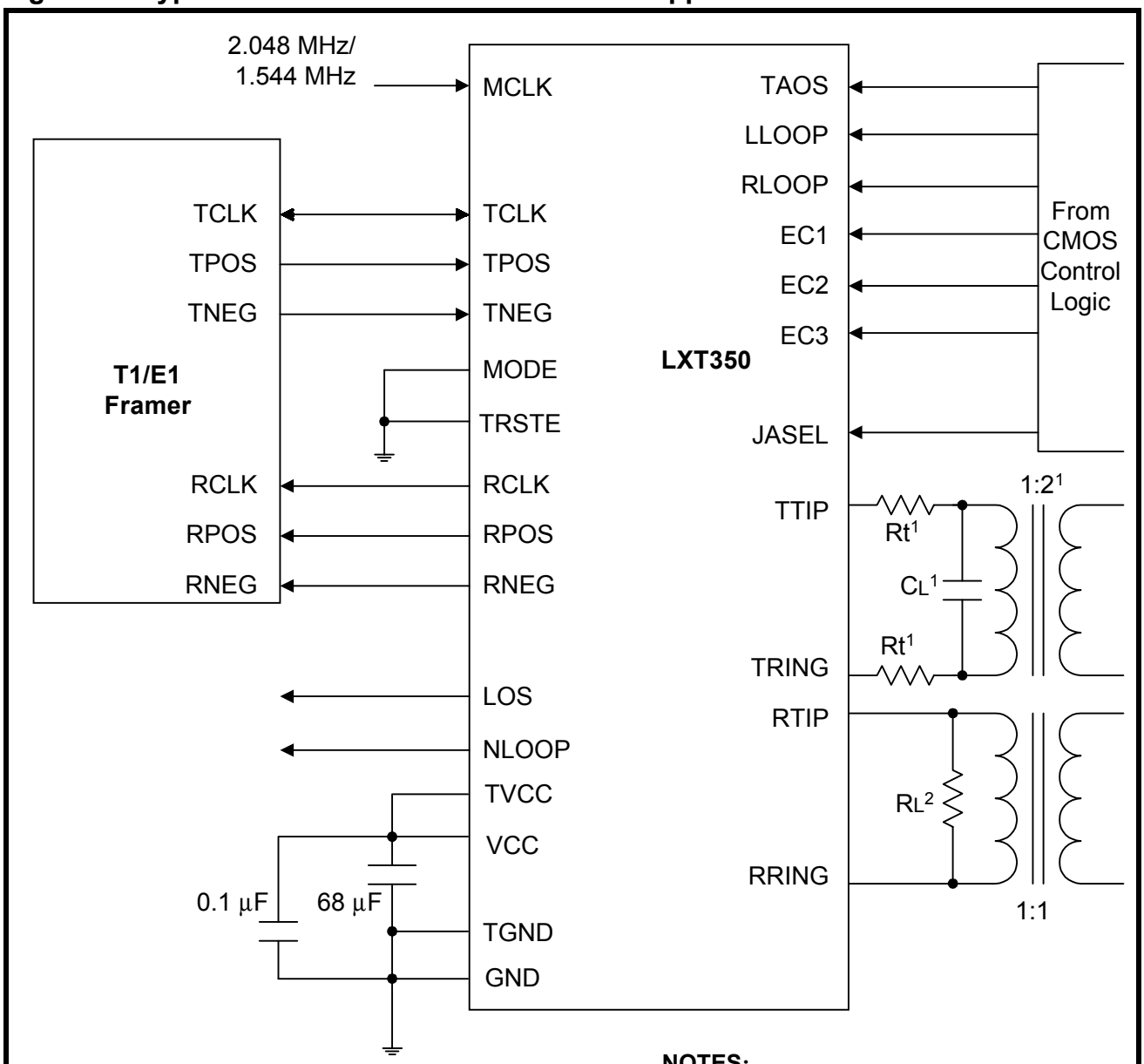
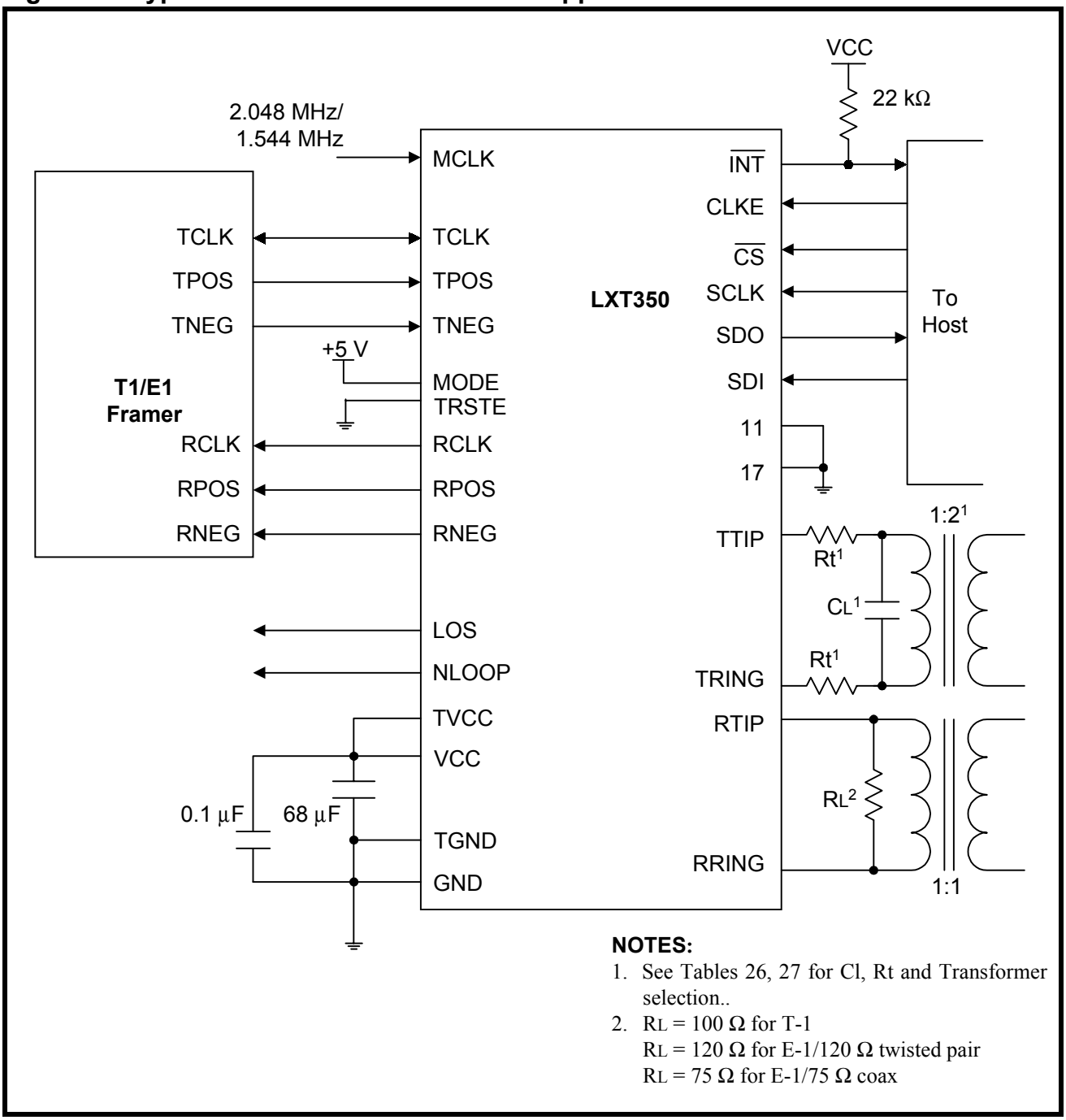


Figure 14 shows an application using the LXT350 in its Host Controlled Mode. See Tables 26 through 27 to select the transformers (T1 and T2), resistors (Rt and Rl) and capacitors (Cl) needed for this application.

NOTE

If the application includes surge protection, such as a varistor or sidactor on the TTIP/TRING lines, it may also require reducing the value of the capacitor CL or eliminating it completely. Excessive capacitance at CL will distort the transmitted signals.

Figure 14: Typical T1/E1 LXT350 Host Mode Application



NOTES:

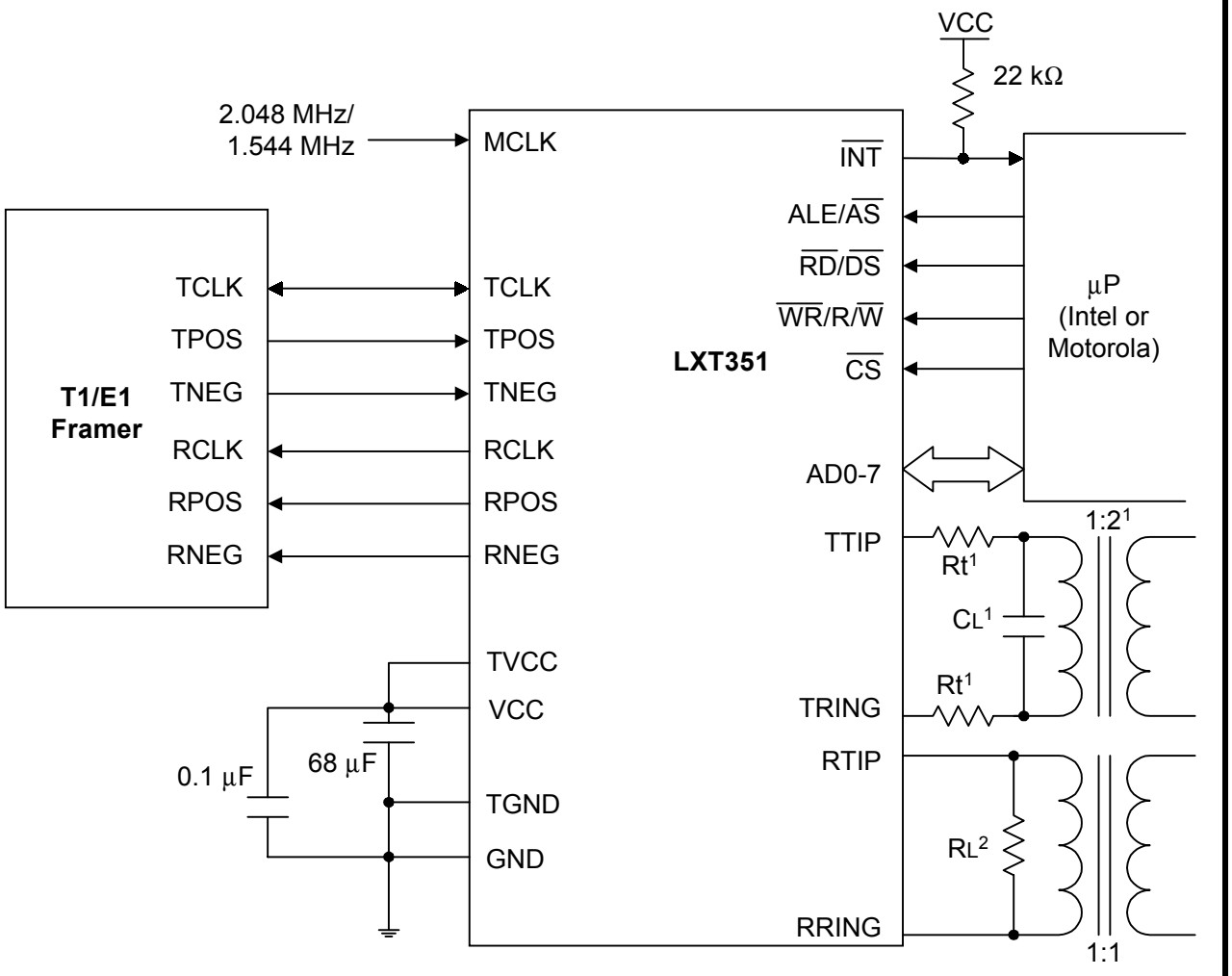
1. See Tables 26, 27 for Cl, Rt and Transformer selection..
2. RL = 100 Ω for T-1
   RL = 120 Ω for E-1/120 Ω twisted pair
   RL = 75 Ω for E-1/75 Ω coax

Figure 15 shows an application using the LXT351. See Tables 26 through 27 to select the transformers (T1 and T2), resistors (Rt and Rl) and capacitors (Cl) needed for this application.

NOTE

If the application includes surge protection, such as a varistor or sidactor on the TTIP/TRING lines, it may also require reducing the value of the capacitor C_L or eliminating it completely.

Figure 15: Typical T1/E1 LXT351 Application



NOTES:

1. See Tables 26, 27 for Cl, Rt and Transformer selection..
2. R_L = 100 Ω for T-1
   R_L = 120 Ω for E-1/120 Ω twisted pair
   R_L = 75 Ω for E-1/75 Ω coax

TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 30 to 42 and Figures 16 through 26 represent the performance spcifications of the LXT350 and LXT351 and are guaranteed by test, except where noted by design.

Table 30: Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
DC supply (reference to GND)	V_{CC},TV_{CC}	–	6.0	V
Input voltage, any pin [1]	V_{IN}	GND -0.3 V	V_{CC} + 0.3 V	V
Input current, any pin [2]	I_{IN}	- 10	10	mA
Storage Temperature	T_{STG}	-65	150	°C

CAUTION

Operation at these limits may permanently damage the device.
Normal operation at these extremes not guaranteed.

1. TVCC and VCC must not differ by more than 0.3 V during operation. TGND and GND must not differ by more than 0.3 V during operation.
2. Transient currents of up to 100 mA will not cause SCR latch-up. TTIP, TRING, TVCC, and TGND can withstand continuous currents of up to 100 mA.

Table 31: Recommended Operating Conditions

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
DC Supply [2]		V_{CC},TV_{CC}	4.75	5.0	5.25	V	
Ambient Operating Temperature		T_A	- 40	25	85	° C	
Total Power Dissipation[3]	T1	P_D	–	310	380	mW	100% mark density
		P_D	–	225	295	mW	50% mark density
	E1	P_D	–	275	330	mW	100% mark density
		P_D	–	215	270	mW	50% mark density

1. Typical figures are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. TVCC and VCC must not differ by more than 0.3 V.
3. Power dissipation while driving 75 Ω load over operating range for T1 operation or 60 Ω load for E1 operation. Includes power dissipation on device and load. Digital levels are within 10% of the supply rails and digital outputs driving a 50 pF capacitive load.

Table 32: LXT350 DC Electrical Characteristics (over recommended operating range)

Parameter	Sym	Min	Typ	Max	Units	Test Conditions
Digital I/O Pins						
High level input voltage [1,2] (pins 1-4, 23-25)[4]	V_{IH}	2.0	–	–	V	
Low level input voltage [1,2] (pins 1-4, 23-25)[4]	V_{IL}	–	–	0.8	V	
High level output voltage [1,2] (pins 6-8, 12, 23, 25)[4]	V_{OH}	2.4	–	–	V	I_{OUT} = -400 µA
Low level output voltage [1,2] (pins 6-8, 12, 23, 25)[4]	V_{OL}	–	–	0.4	V	I_{OUT} = 1.6 mA
Tri-state leakage current [1] (all outputs)	I_{3L}	0	–	±10	µA	
Mode Input Pins						
High level input voltage [3] (pins 5, 9, 11, 26-28)[4]	V_{IH}	3.5	–	–	V	
Midrange output voltage [3] (pins 5, 9, 11, 26-28)[4]	V_{OM}	2.3	–	2.7	V	
Low level input voltage [3] (pins 5, 9, 11, 26-28)[4] Host Mode	V_{IL}	–	–	0.8	V	
Low level input voltage [3] (pins 5, 9, 11, 26-28)[4] H/W Mode	V_{IL}	–	–	1.5	V	
Input leakage current (pins 5, 9, 11, 26-28)[4]	I_{LL}	0	–	±50	µA	
Tri-state Leakage current[1] (all outputs)	I3L	0	–	±10	µA	
TTIP/TRING Leakage current	I_{TR}	–	–	1.2	mA	In power down and tristate

1. Functionality of pin 23 and 25 depends on mode. See Host Mode and Hardware Mode description
2. Output drivers will output CMOS logic levels into CMOS loads.
3. As an alternative to supplying 2.3 - 2.7 V to these pins, they may be left open.
4. Listed pins are for 28-pin DIP and PLCC packages. Refer to I/O description for 44-pin QFP package.

Table 33: LXT351 DC Electrical Characteristics (over recommended operating range)

Parameter	Sym	Min	Typ	Max	Units	Test Conditions
Digital I/O Pins						
High level input voltage [1,2] (pins 1-5, 9-12, 17, 23-28)[3]	V_{IH}	2.0	–	–	V	
Low level input voltage [1,2] (pins 1-5, 9-12, 17, 23-28)[3]	V_{IL}	–	–	0.8	V	
High level output voltage [1,2] (pins 6-8, 10, 11,23, 28)[3]	V_{OH}	2.4	–	–	V	I_{OUT} = -400 µA
Low level output voltage [1,2] (pins 6-8, 10, 11,23, 28)[3]	V_{OL}	–	–	0.4	V	I_{OUT} = 1.6 mA
Input leakage current	I_{LL}	–	–	±10	µA	

1. Functionality of pins 23 and 25 depends on mode. See Host Mode description.
2. Output drivers will output CMOS logic levels into CMOS loads.
3. Listed pins are for 28-pin DIP and PLCC packages. Refer to I/O description for 44-pin QFP package.

Table 34: Analog Characteristics (over recommended operating range)

Parameter		Min	Typ[1]	Max	Units	Test Conditions
Recommended output load on TTIP/TRING		50	–	200	Ω	
AMI Output Pulse Amplitudes	T1	2.4	3.0	3.6	V	R_L = 100 Ω
	E1	2.7	3.0	3.3	V	R_L = 120 Ω
Jitter added by the transmitter[2]	10 Hz - 8 kHz [3]	–	–	0.02	UI	
	8 kHz - 40 kHz [3]	–	–	0.025	UI	
	10 Hz - 40 kHz[3]	–	–	0.025	UI	
	Broad Band	–	–	0.05	UI	
Receiver Sensitivity		0	–	18	dB	@ 1024 kHz 1.431
Allowable consecutive zeros before LOS (T1)		160	175	190	–	
Allowable consecutive zeros before LOS (E1)		–	32	–	–	
Input jitter tolerance (T1)	10 kHz - 100 kHz	0.4	–	–	UI	0 dB line AT&T Pub 62411
	1 Hz[3]	138	–	–	UI	
Input jitter tolerance (E1)	10 kHz - 100 kHz	0.2	–	–	UI	0 dB line ITU (G.823)
	1 Hz[3]	37	–	–	UI	
Jitter attenuation curve corner frequency [4]		–	3	–	Hz	selectable in data port
Driver Output Impedance		–	3	–	Ω	
Receiver Input Impedance		–	40	–	kΩ	RTIP to RRING
Receive Return Loss (E1)	51 kHz - 102 kHz[3]	20	22	–	dB	
	102 kHz - 2.048 MHz[3]	20	28	–	dB	
	2.048 MHz - 3.072 MHz[3]	25	30	–	dB	

1. Typical figures are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. Input signal to TCLK is jitter-free. The Jitter Attenuator is in the receive path or disabled.
3. Guaranteed by characterization; not subject to production testing.
4. Circuit attenuates jitter at 20 dB/decade above the corner frequency.

Figure 16: 2.048 Mbps E1 Pulse (See Table 35)

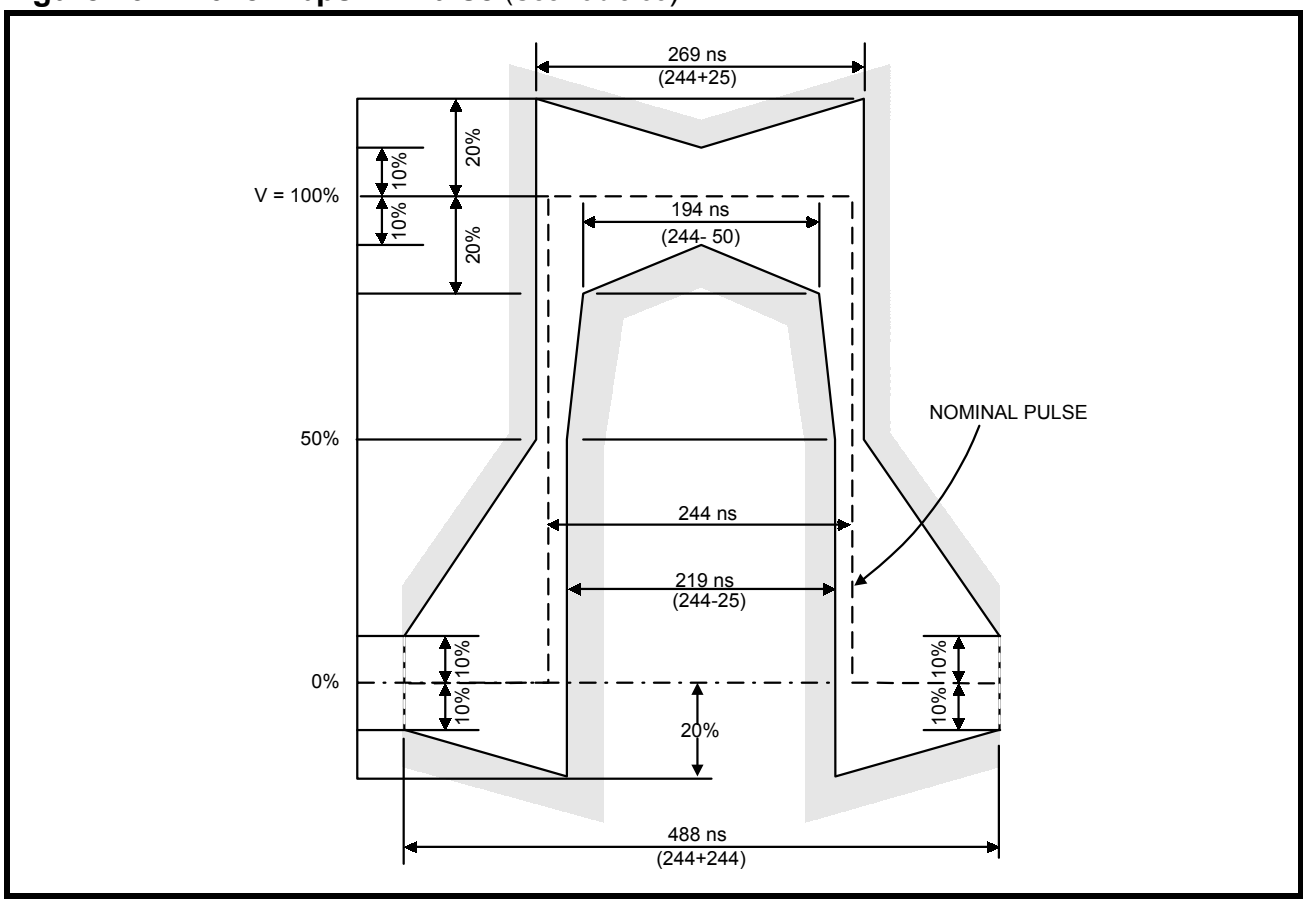


Table 35: 2.048 Mbps E1 Pulse Mask Specifications

Parameter	TPW	Coax	Unit
Test load impedance	120	75	Ω
Nominal peak mark voltage	3.0	2.37	V
Nominal peak space voltage	0 ±0.30	0 ±0.237	V
Nominal pulse width	244	244	ns
Ratio of positive and negative pulse amplitudes at center of pulse	95-105	95-105	%
Ratio of positive and negative pulse amplitudes at nominal half amplitude	95-105	95-105	%

Figure 17: 1.544 Mbps T1 Pulse (DSX-1) (See Table 36)

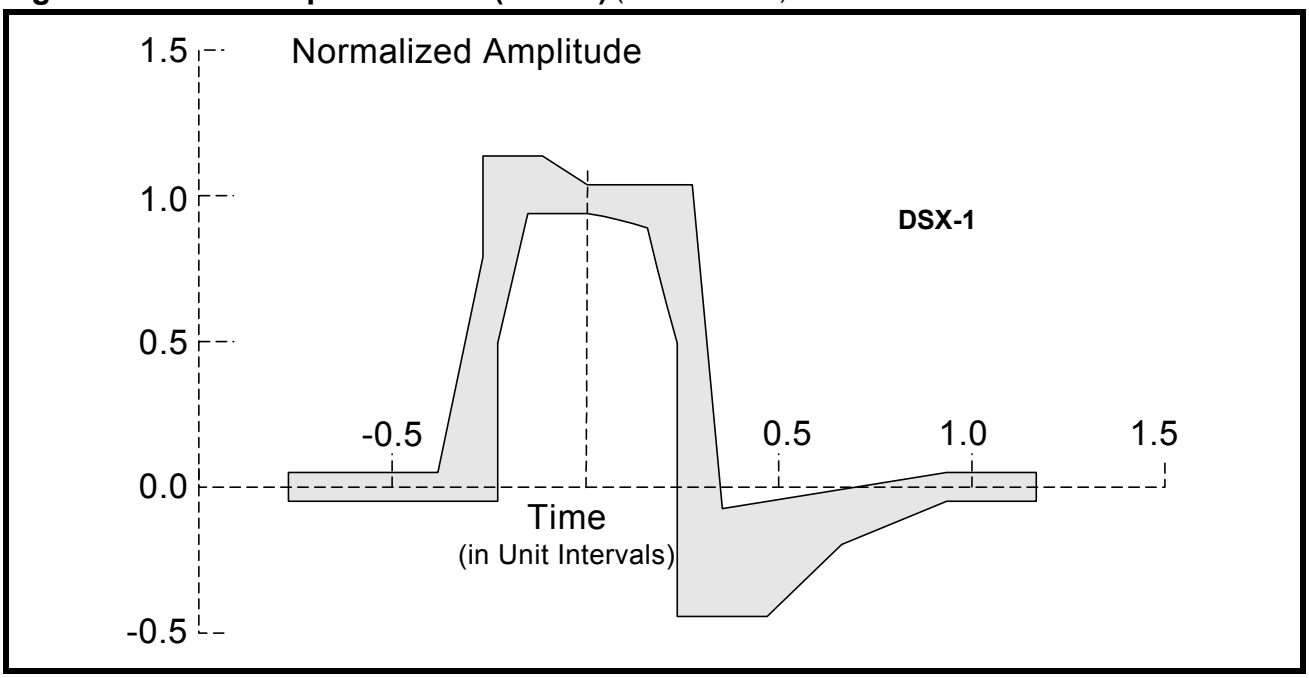


Table 36: 1.544 Mbps T1 (DSX-1) Pulse Mask Corner Point Specifications

DSX-1 Template *(per ANSI T1. 102-1993)*			
Minimum Curve		**Maximum Curve**	
Time *(UI)*	**Amplitude**	**Time** *(UI)*	**Amplitude**
-0.77	-0.05	-0.77	0.05
-0.23	-0.05	-0.39	0.05
-0.23	0.50	-0.27	0.80
-0.15	0.95	-0.27	1.15
0.0	0.95	-0.12	1.15
0.15	0.90	0.0	1.05
0.23	0.50	0.27	1.05
0.23	-0.45	0.35	-0.07
0.46	-0.45	0.93	0.05
0.66	-0.20	1.16	0.05
0.93	-0.05		
1.16	-0.05		

Table 37: Master and Transmit Clock Timing Characteristics for T1 Operation

(over recommended operating range) (see Figure 18)

Parameter	Sym	Min	Typ[1]	Max	Units	Notes
Master clock frequency	MCLK	–	1.544	–	MHz	must be supplied
Master clock tolerance	MCLKt	–	±32	–	ppm	
Master clock duty cycle	MCLKd	40	–	60	%	
Transmit clock frequency	TCLK	–	1.544	–	MHz	
Transmit clock tolerance	TCLKt	–	–	±100	ppm	
Transmit clock duty cycle	TCLKd	10	–	90	%	
TPOS/TNEG to TCLK setup time	t_{SUT}	50	–	–	ns	
TCLK to TPOS/TNEG hold time	t_{HT}	50	–	–	ns	

1. Typical figures are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Table 38: Master and Transmit Clock Timing Characteristics for E1 Operation

(see Figure 18)

Parameter	Sym	Min	Typ[1]	Max	Units	Notes
Master clock frequency	MCLK	–	2.048	–	MHz	must be supplied
Master clock tolerance	MCLKt	–	±32	–	ppm	
Master clock duty cycle	MCLKd	40	–	60	%	
Transmit clock frequency	TCLK	–	2.048	–	MHz	
Transmit clock tolerance	TCLKt	–	–	±100	ppm	
Transmit clock duty cycle	TCLKd	10	–	90	%	
TPOS/TNEG to TCLK setup time	t_{SUT}	50	–	–	ns	
TCLK to TPOS/TNEG hold time	t_{HT}	50	–	–	ns	

1. Typical figures are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Figure 18: Transmit Clock Timing

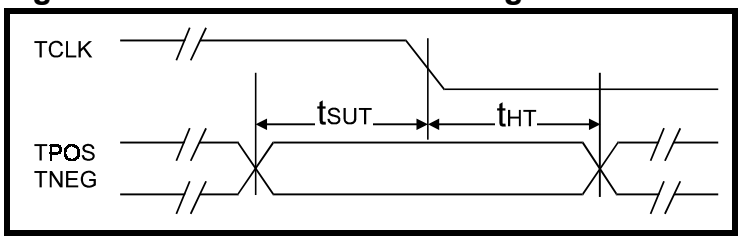


Table 39: Receive Timing Characteristics for T1 Operation (See Figure 19)

Parameter	Sym	Min	Typ[1]	Max	Units
Receive clock duty cycle [2, 3]	RLCKd	40	50	60	%
Receive clock pulse width [2, 3]	tPW	–	648	–	ns
Receive clock pulse width high	tPWH	–	324	–	ns
Receive clock pulse width low[1,3]	tPWL	260	324	388	ns
RPOS/RNEG to RCLK rising time	tSUR	–	274	–	ns
RCLK rising to RPOS/RNEG hold time	tHR	–	274	–	ns

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. RCLK duty cycle widths will vary according to extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions.
3. Worst case conditions guaranteed by design only.

Table 40: Receive Timing Characteristics for E1 Operation (See Figure 19)

Parameter	Sym	Min	Typ[1]	Max	Units
Receive clock duty cycle [2, 3]	RLCKd	40	50	60	%
Receive clock pulse width [2, 3]	tPW	–	488	–	ns
Receive clock pulse width high	tPWH	–	244	–	ns
Receive clock pulse width low[1,3]	tPWL	195	244	293	ns
RPOS/RNEG to RCLK rising time	tSUR	–	194	–	ns
RCLK rising to RPOS/RNEG hold time	tHR	–	194	–	ns

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. RCLK duty cycle widths will vary according to extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions (0.4 UI clock displacement for 1.544 MHz.)
3. Worst case conditions guaranteed by design only.

Figure 19: Receive Clock Timing

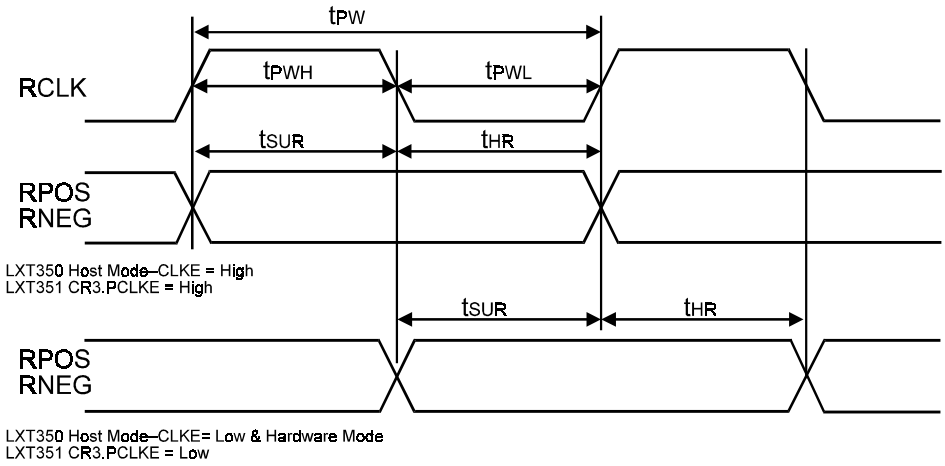


Table 41: LXT350 Serial I/O Timing Characteristics (See Figures 20 and 21)

Parameter	Sym	Min	Typ[1]	Max	Units	Parameter
Rise/fall time—any digital output	t_{RF}	–	–	100	ns	Load 1.6 mA, 50 pF
SDI to SCLK setup time	t_{DC}	50	–	–	ns	
SCLK to SDI hold time	t_{CDH}	50	–	–	ns	
SCLK low time	t_{CL}	240	–	–	ns	
SCLK high time	t_{CH}	240	–	–	ns	
SCLK rise and fall time	t_R, t_F	–	–	50	ns	
$\overline{CS}$ falling edge to SCLK rising edge	t_{CC}	50	–	–	ns	
Last SCLK edge to $\overline{CS}$ rising edge	t_{CCH}	50	–	–	ns	
$\overline{CS}$ inactive time	t_{CWH}	250	–	–	ns	
SCLK to SDO valid time	t_{CDV}	–	–	200	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO high-Z	t_{CDZ}	–	100	–	ns	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 20: LXT350 Serial Data Input Timing Diagram

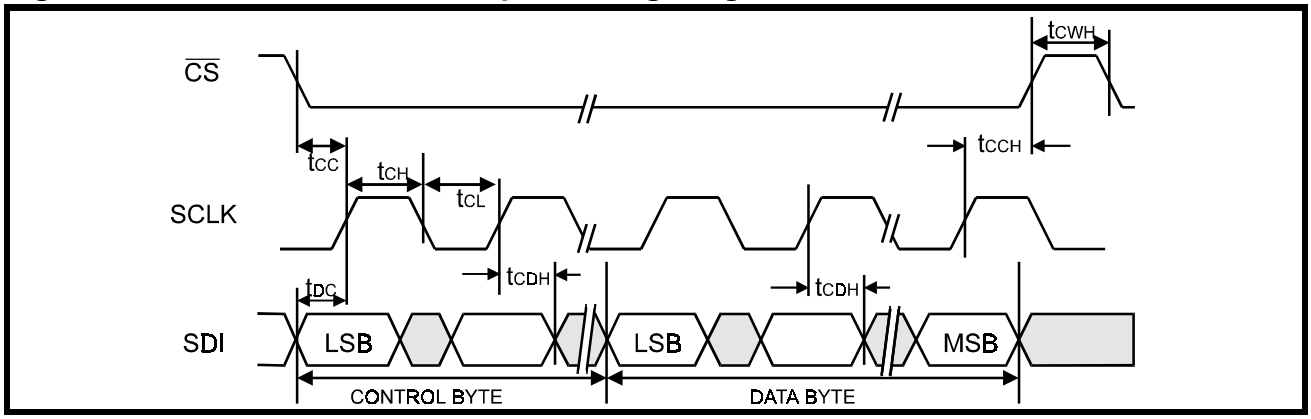


Figure 21: Serial Data Output Timing Diagram

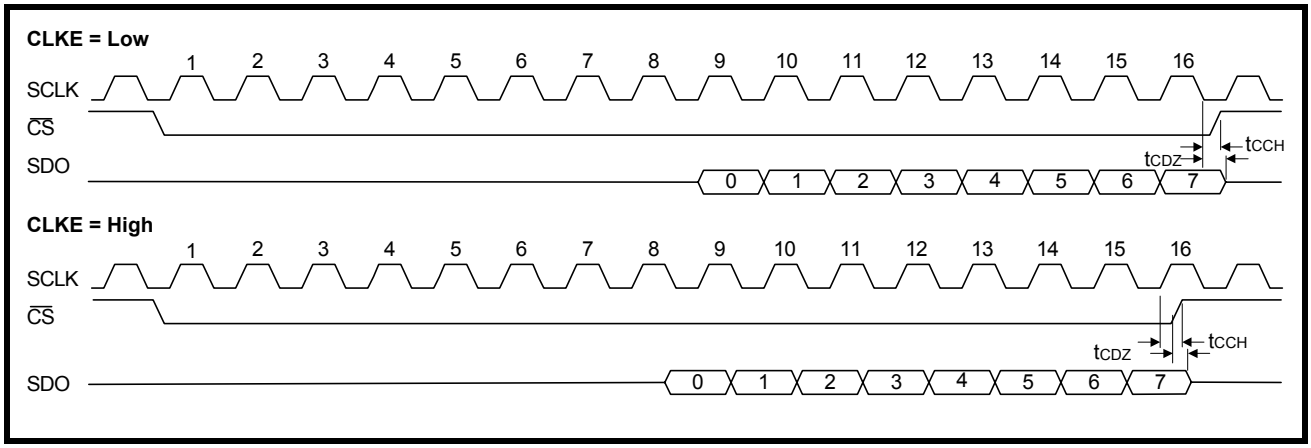


Table 42: LXT351 20 MHz Intel Bus Parallel I/O Timing Characteristics (See Figure 22)

Parameter	Sym	Min	Max	Units	Test Conditions
ALE pulse width	TLHLL	35	–	ns	
Address valid to ALE falling edge	TAVLL	10	–	ns	
ALE falling edge to address hold time	TLLAX	10	–	ns	
ALE falling edge to $\overline{RD}$ falling edge	TLLRL	10	–	ns	
ALE falling edge to $\overline{WR}$ falling edge	TLLWL	10	–	ns	
$\overline{CS}$ falling edge to $\overline{RD}$ falling edge	TCLRL	10	–	ns	
$\overline{CS}$ falling edge to $\overline{WR}$ falling edge	TCLWL	10	–	ns	
$\overline{RD}$ low pulse width	TRLRH	95	–	ns	
$\overline{RD}$ falling edge to data valid	TRLDV	10	55	ns	
Data hold time after $\overline{RD}$ rising edge	TRHDX	5	35	ns	
$\overline{RD}$ rising edge to ALE rising edge	TRHLH	15	–	ns	
$\overline{RD}$ rising edge to address valid	TRHAV	35	–	ns	
$\overline{CS}$ low hold time after $\overline{RD}$ rising edge	TRHCH	0	–	ns	
$\overline{WR}$ low pulse width	TWLWH	95	–	ns	
Data setup time before $\overline{WR}$ rising edge	TDVWH	40	–	ns	
Data hold time after $\overline{WR}$ rising edge	TWHDX	30	–	ns	
$\overline{WR}$ rising edge to ALE rising edge	TWHLH	15	–	ns	
$\overline{CS}$ low hold time after $\overline{WR}$ rising edge	TWHCH	15	–	ns	

Figure 22: LXT351 I/O Timing Diagram for Intel Address/Data Bus

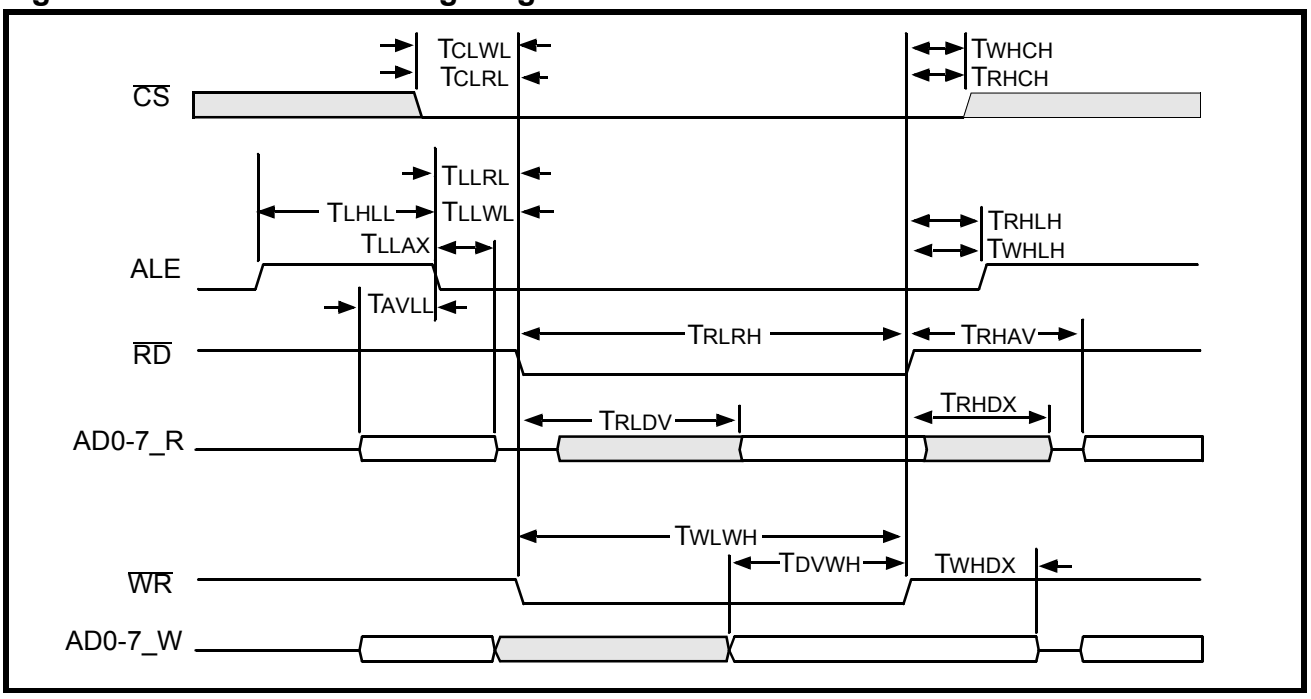


Table 43: LXT351 16.78 MHz Motorola Bus Parallel I/O Timing Characteristics

(See Figure 23)

Parameter	Sym	Min	Max	Units	Test Conditions
$\overline{DS}$ rising edge to $\overline{AS}$ rising edge	TDSHASH	15	–	ns	
$\overline{AS}$ high pulse width	TASHASL	35	–	ns	
Address valid setup time at $\overline{AS}$ falling edge	TAVASL	10	–	ns	
$\overline{AS}$ falling edge to Address valid hold time	TASLAX	10	–	ns	
$\overline{AS}$ falling edge to $\overline{DS}$ falling edge	TASLDSL	20	–	ns	
$\overline{CS}$ falling edge to $\overline{DS}$ falling edge	TCSLDSL	10	–	ns	
$\overline{DS}$ low pulse width	TDSLDSH	95	–	ns	
$\overline{DS}$ falling edge to data valid	TDSLDV	10	55	ns	
Data hold time after $\overline{DS}$ rising edge	TDSHDX	5	35	ns	
R/$\overline{W}$ falling edge to $\overline{DS}$ falling edge	TRWLDSL	10	–	ns	
Data setup time before $\overline{DS}$ rising edge	TDVDSH	40	–	ns	
Data hold time after DS rising edge	TDXDSH	30	–	ns	
R/$\overline{W}$ low hold time after $\overline{DS}$ rising edge	TDSHRWH	15	–	ns	
$\overline{CS}$ low hold time after $\overline{DS}$ rising edge	TDSHCSH	15	–	ns	

Figure 23: LXT351 I/O Timing Diagram for Motorola Address/Data Bus

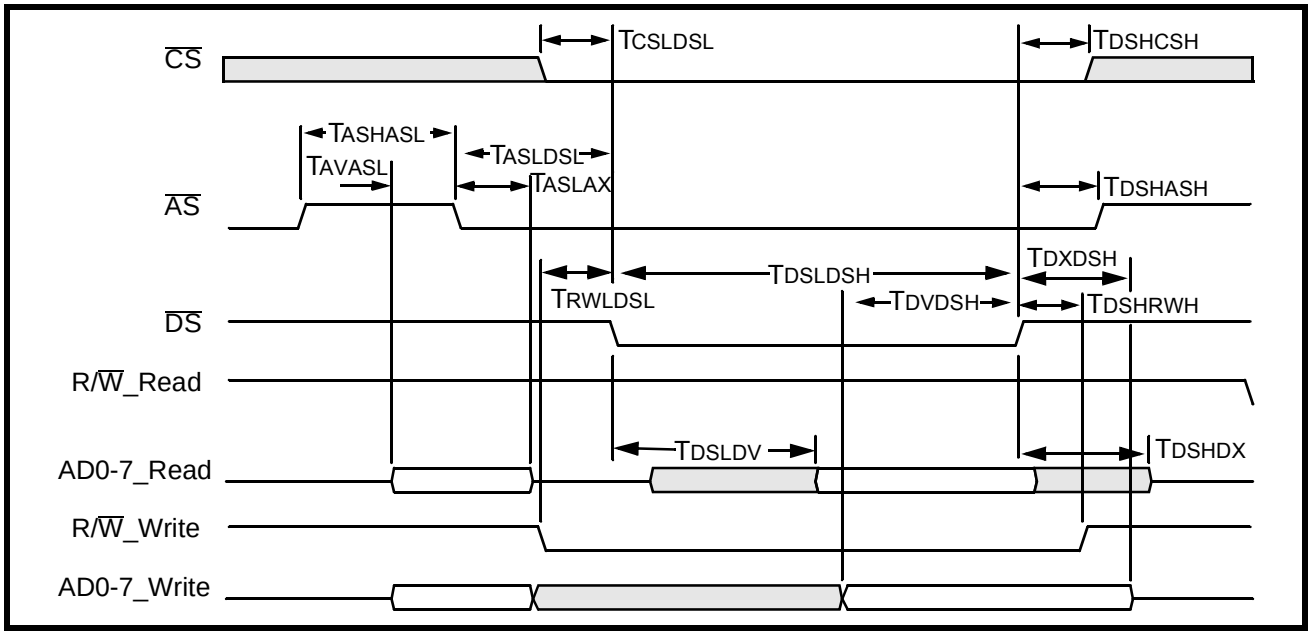
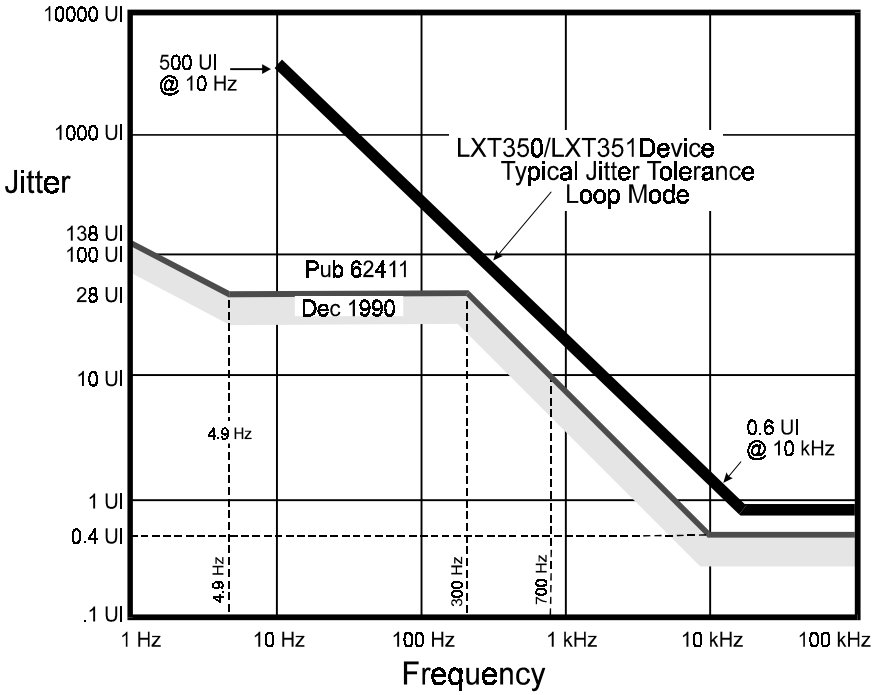


Figure 24: Input Jitter Tolerance (Typical)

Typical T1 Input Jitter Tolerance



Typical E1 Input Jitter Tolerance

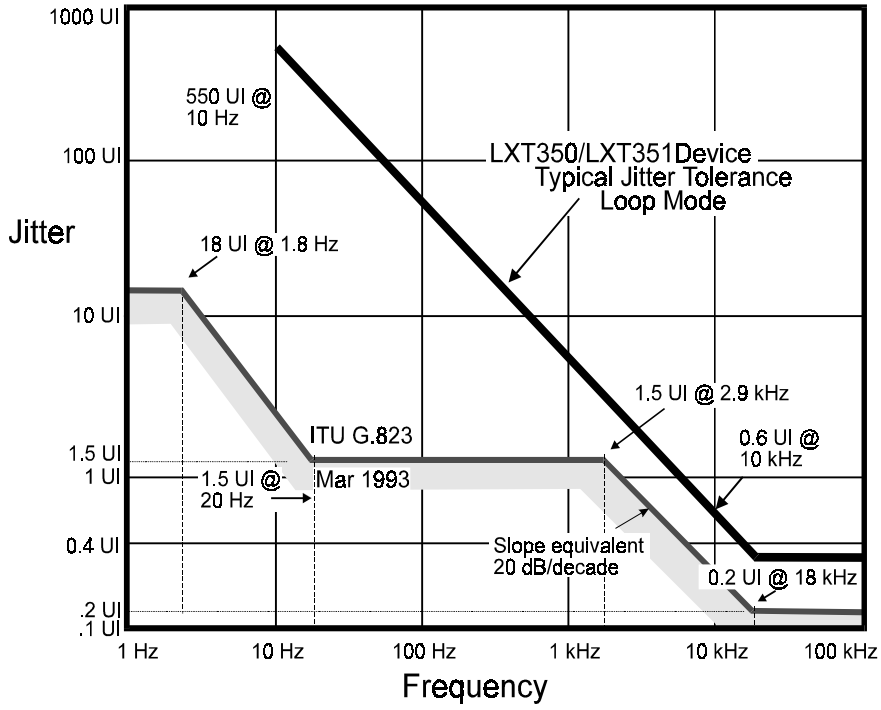


Figure 25: E1 Jitter Transfer Performance (Typical)

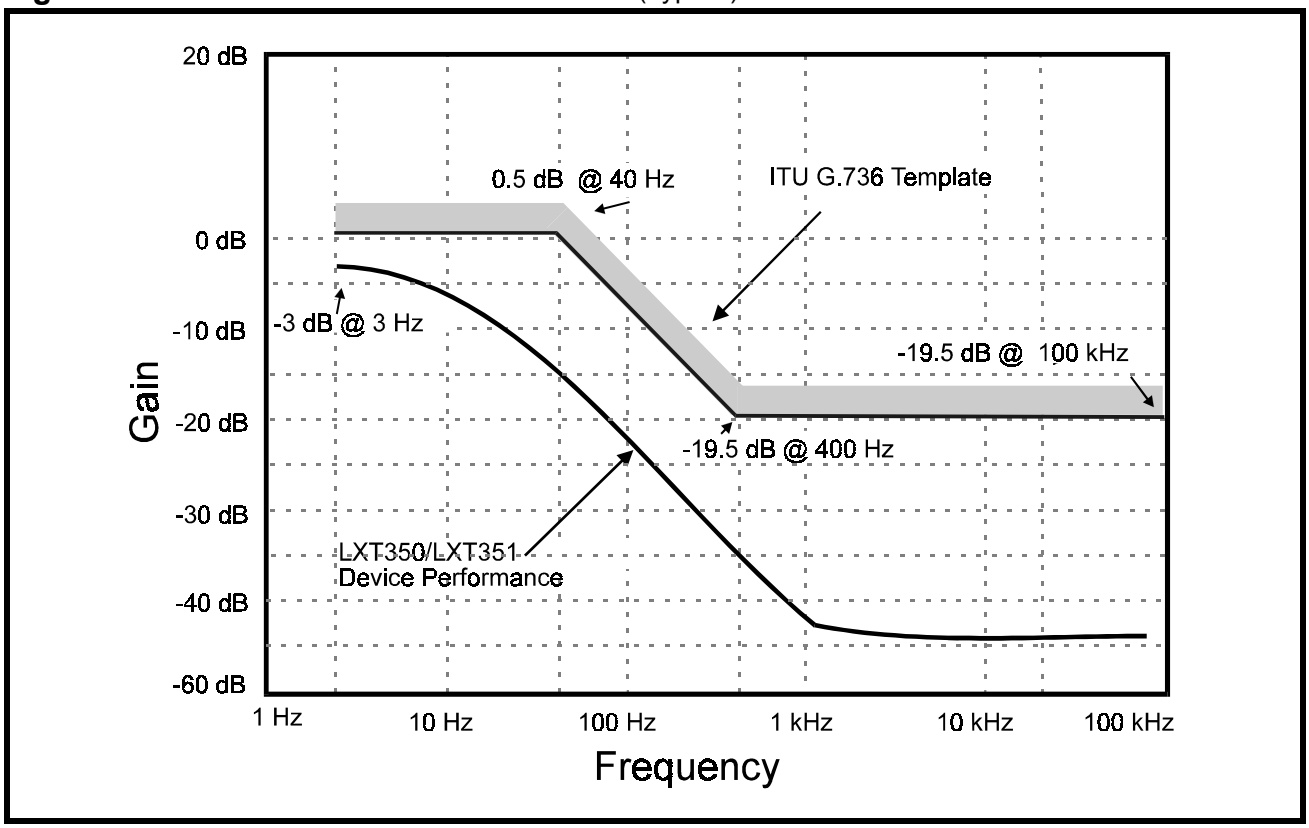


Figure 26: T1 Jitter Transfer Performance (Typical)

