Rev 0; 4/08

EVALUATION KIT AVAILABLE

Multiprotocol Dual Smart Card Interface

DS8007A

General Description

The DS8007A multiprotocol dual smart card interface is an automotive grade, low-cost, dual smart card reader interface supporting all ISO 7816, EMV™, and GSM11-11 requirements. Through its 8-bit parallel bus and dedicated address selects (AD3–AD0), the DS8007A can easily and directly connect to the nonmultiplexed byte-wide bus of a Maxim secure microcontroller. Optionally, the parallel bus can be multiplexed to allow direct access to the multiplexed bus of an 80C51-compatible microcontroller through MOVX memory addressing.

One integrated UART is multiplexed among the interfaces to allow high-speed automatic smart card processing with each card-possessing, independent, variable, baud-rate capability. The card interface is controlled by internal sequencers that support automatic activation and deactivation sequencing, handling all actions required for T = 0, T = 1, and synchronous protocols. Emergency deactivation is also supported in case of supply dropout. A third card is supported through the auxiliary I/O. The same set of I/O can optionally be used as additional serial interface for the UART.

The DS8007A provides all electrical signals necessary to interface with two smart cards. The integrated voltage converter ensures full cross-compatibility between 1.8V/3V/5V cards and a 1.8V/3V/5V environment, and allows operation within a 2.7V to 6V supply voltage range. The standard DS8007 revision is available for nonautomotive applications.

Applications

Banking Applications (Point-of-Sale Terminals, Debit/Credit Payment Terminals, PIN Pads, Automated Teller Machines)

Telecommunications

Pay Television

Access Control

Ordering Information

PART	TEMP RANGE	SMART CARDS SUPPORTED	PIN-PACKAGE
DS8007A-EAG+	-40°C to +125°C	2 + auxiliary	48 LQFP

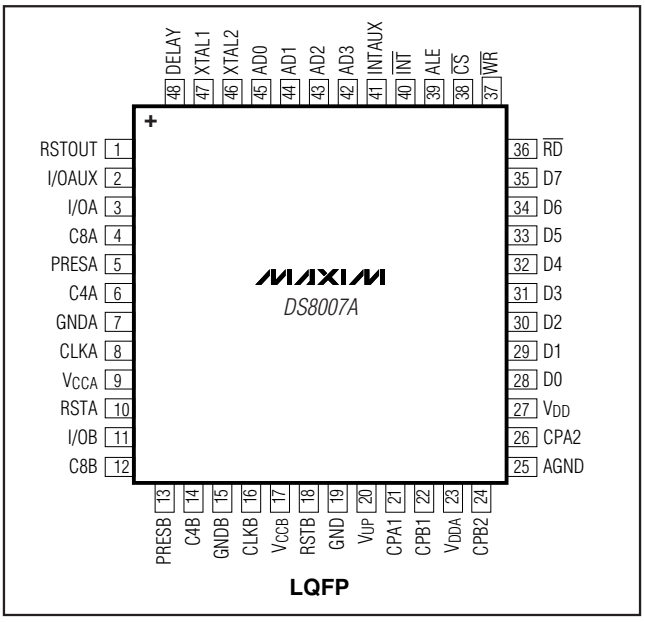
+Denotes a lead(Pb)-free/RoHS-compliant device.

EMV is a trademark owned by EMVCo LLC.

Features

- **Complete Interface/Control for Two Separate Smart Card Devices**
- **8kV (min) ESD Protection on Card Interfaces**
- **Internal IC Card Supply Voltage Generation**
  - **5.0V ±5%, 65mA (max)**
  - **3.0V ±8%, 50mA (max)**
  - **1.8V ±10%, 30mA (max)**
- **Automatic Card Activation, Deactivation, and Data Communication Controlled by Dedicated Internal Sequencer**
- **Host Interface Through an 8-Bit Parallel Bus (User-Selectable Multiplexed or Nonmultiplexed Modes)**
- **Chip Select and Three-State Bus Allow Multiple Devices (Card Readers and Memories) on Bus**
- **8-Character Receive FIFO with Optional Programmable Depth/Threshold**
- **I/O Interface Pin to External ISO 7816 UART**
- **Separate Card Clock Generation (Up to 10MHz) with 2x Frequency Doubling**
- **Selectable Card Clock Stop High, Stop Low, or Internally Generated 1.25MHz (for Card Power-Down)**
- **EMV-Certified Reference Design and Evaluation Kit Available (DS8007-KIT)**

Pin Configuration



Typical Operating Circuit appears at end of data sheet.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to: **www.maxim-ic.com/errata**.*

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Multiprotocol Dual Smart Card Interface

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{DD} Relative to Ground .....-0.5V to +6.5V
Voltage Range on V_{DDA} Relative to Ground .....-0.5V to +6.5V
Voltage Range on Any Pin Relative to Ground
Pins CPA1, CPA2, CPB1, CPB2, and V_{UP} .....-0.5V to +7.5V
All Other Pins.....-0.5V to (V_{DD} + 0.5V)

Maximum Junction Temperature .....+150°C
Maximum Power Dissipation (T_A = -25°C).....900mW
Storage Temperature Range .....-55°C to +150°C
Soldering Temperature.....Refer to the IPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +3.3V, V_{DDA} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Supply Voltage		V_{DD}		2.7		6.0	V
Step-Up Converter Supply Voltage		V_{DDA}		V_{DD}		6.0	V
Power-Down V_{DD} Current	Cards Inactive	I_{PD}	f_{XTAL} = 0MHz			0.9	mA
	Cards Active		f_{XTAL} = 0MHz, f_{CLK} = 0MHz, V_{CCx} = 5V			2.2	
Sleep Mode V_{DD} Current (Cards Active)		I_{STOP}	f_{CLK} = 0MHz, V_{CC} = 5V			24	mA
Active V_{DD} Current 5V Cards		I_{DD}	3x V_{DD} step-up: I_{CCA} + I_{CCB} = 80mA, V_{DD} = 2.7V, f_{XTAL} = 20MHz, f_{CLK} = 10MHz			325	mA
Active V_{DD} Current 3V Cards		I_{DD}	2x V_{DD} step-up: I_{CC1} + I_{CC2} = 80mA, f_{XTAL} = 20MHz, f_{CLK} = 10MHz, V_{DD} = 2.7V			225	mA
			No step-up: I_{CC1} + I_{CC2} = 80mA, f_{XTAL} = 20MHz, f_{CLK} = 10MHz, V_{DD} = 5V			120	
Power-Fail Reset Voltage		V_{RST}	Threshold voltage (falling)	2.1		2.5	V
		V_{HYS}	Hysteresis	50		170	mV
Delay Pin	Reset Threshold	V_{DRST}			1.25		V
	Output Voltage	V_{DO}				V_{DD} + 0.3	
	Output Current	I_{DO}	V_{DELAY} = 0V		-2		µA
			V_{DELAY} = V_{DD}		+2		mA
	Output Capacitance	C_{DO}		1			nF
RSTOUT PIN							
Output High Voltage		V_{OHRSTO}	I_{OH} = -1mA	0.8 x V_{DD}		V_{DD} + 0.3	V
Output Low Voltage		V_{OLRSTO}	I_{OL} = 2mA	-0.3		+0.4	V
Leakage Current		I_L	V_{OL} = 0V, V_{OH} = 5V	-10		+10	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3.3V, V_{DDA} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER			SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Alarm Pulse Width			t_W	C_{DELAY} = 22nF		10		ms
External Clock Frequency			f_{XTAL}	External crystal	4		20	MHz
				External oscillator	0		20	
Internal Oscillator			f_{INT}		1.6	2.5	3.7	MHz
Voltage on V_{UP} Pin			V_{UP}	3x step-up		5.7		V
				2x step-up		4.1		
Voltage Detection of V_{DDA} for 2x, 3x Step-Up			V_{DET}		3.25	3.50	3.60	V
Shutdown Temperature			T_{SD}			+150		°C
RSTx Pins	Card Inactive Mode	Output Low Voltage	V_{OLRST}	I_{OLRST} = 1mA	0		0.3	V
		Output Current	I_{OLRST}	V_{OLRST} = 0V	0		-1	mA
	Card Active Mode	Output Low Voltage	V_{OLRSTL}	I_{OLRST} = +200µA	0		0.3	V
		Output High Voltage	V_{OHRSTH}	I_{OHRST} = -200µA	V_{CC} – 0.5		V_{CC}	
		Rise Time	t_{RRST}	C_L = 30pF			0.1	µs
		Fall Time	t_{FRST}	C_L = 30pF			0.1	
		Shutdown Current	$I_{RST(SD)}$			-25		mA
		Current Limitation	$I_{RST(LIMIT)}$		-30		+30	
CLKx Pins	Card Inactive Mode	Output Low Voltage	V_{OLCLK}	I_{OLCLK} = 1mA	0		0.3	V
		Output Current	I_{OLCLK}	V_{OLCLK} = 0V	0		-1	mA
	Card Active Mode	Output Low Voltage	V_{OLCLK}	I_{OLCLK} = +200µA	0		0.3	V
		Output High Voltage	V_{OHCLK}	I_{OHCLK} = -200µA	V_{CC} – 0.5		V_{CC}	
		Rise Time	t_{RCLK}	C_L = 30pF (Note 2)			8	ns
		Fall Time	t_{FCLK}	C_L = 30pF (Note 2)			8	
		Current Limitation	$I_{CLK(LIMIT)}$		-90		+90	mA
	Clock Frequency		f_{CLK}	Idle configuration (1MHz)	1		1.85	MHz
				Operational	0		10	
	Duty Factor		δ	C_L = 30pF	45		55	%

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3.3V, V_{DDA} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER			SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CCx} Pins	Card Inactive Mode	Output Low Voltage	V_{CC}	I_{CC} = 1mA	0		0.3	V
		Output Current	I_{CC}	V_{CC} = 0V	0		-1	mA
	Card Active Mode	Output Low Voltage	V_{CC}	$I_{CC(5V)}$ < 65mA	4.72	5.00	5.25	V
				$I_{CC(3V)}$ < 50mA	2.75	3.00	3.22	
				$I_{CC(1.8V)}$ < 30mA	1.62	1.80	1.95	
				5V card, current pulses of 40nC with I < 200mA, t < 400ns, f < 20MHz	4.6		5.4	
				3V card, current pulses of 24nC with I < 200mA, t < 400ns, f < 20MHz	2.75		3.25	
				1.8V card, current pulses of 12nC with I < 200mA, t < 400ns, f < 20MHz	1.62		1.98	
		Output Current	I_{CC}	$V_{CC(5V)}$ = 0 to 5V			-65	mA
				$V_{CC(3V)}$ = 0 to 3V			-50	
				$V_{CC(1.8V)}$ = 0 to 1.8V			-30	
		Total Current (Two Cards)	$I_{CC(A+B)}$				-80	
		Shutdown Current	$I_{CC(SD)}$			-100		
		Slew Rate	V_{CCSR}	Up/down, C < 300nF (Note 3)	0.05	0.16	0.5	V/µs
I/Ox Pins	Card Inactive Mode	Output Low Voltage	V_{OLIO}	I_{OLIO} = 1mA	0		0.3	V
		Output Current	I_{OLIO}	V_{OLIO} = 0V	0		-1	mA
		Internal Pullup Resistor	R_{PULLUP}	To V_{CCx}	9	14	19	kΩ
	Card Active Mode	Output Low Voltage	V_{OLIO}	I_{OLIO} = 1mA	0		0.3	V
		Output High Voltage	V_{OHIO}	$I_{OHIO} \leq$ -20µA	0.8 x V_{CC}		V_{CC}	
				$I_{OHIO} \leq$ -40µA (3V/5V)	0.75 x V_{CC}		V_{CC}	
		Output Rise/Fall Time	t_{OT}	C_L = 30pF			0.1	µs
		Input Low Voltage	V_{ILIO}		-0.3		+0.8	V
		Input High Voltage	V_{IHIO}		1.5		V_{CC}	
		Input Low Current	I_{ILIO}	V_{ILIO} = 0V			700	µA
		Input High Current	I_{IHIO}	V_{IHIO} = V_{CC}			20	
		Input Rise/Fall Time	t_{IT}	C_L = 30pF			1.2	µs
		Current Limitation	$I_{IO(LIMIT)}$		-25		+25	mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3.3V, V_{DDA} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER			SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
C4x, C8x Pins	Card Inactive Mode	Output Low Voltage	V_{OLC48}	I_{OLC48} = 1mA	0		0.3	V
		Output Current	I_{OLC48}	V_{OLC48} = 0V	0		-1	mA
		Internal Pullup Resistor	R_{PULLUP}	Between C4 or C8 and V_{CCx}	6	10	14	kΩ
	Card Active Mode	Output Low Voltage	V_{OLC48}	I_{OLC48} = 1mA	0		0.35	V
		Output High Voltage	V_{OHC48}	I_{OHC48} -20µA	0.8 x V_{CC}		V_{CC}	V
				I_{OHC48} -40µA (3V/5V)	0.75 x V_{CC}		V_{CC}	V
		Output Rise/Fall Time	t_{OT}	C_L = 30pF			0.1	µs
		Input Low Voltage	V_{ILC48}		-0.3		+0.8	V
		Input High Voltage	V_{IHC48}		1.5		V_{CC}	V
		Input Low Current	I_{ILC48}	V_{ILIO} = 0V			850	µA
		Input High Current	I_{IHC48}	V_{IHIO} = V_{CC}			20	µA
		Input Rise/Fall Time	t_{IT}	C_L = 30pF			1.2	µs
		Pullup Pulse Width	t_{WPU}	Active pullup		200		ns
		Operating Frequency	f_{MAX}	On card contact pins			1	MHz
TIMING								
Activation Sequence Duration			t_{ACT}	See Figure 9			130	µs
Deactivation Sequence Duration			t_{DE}	See Figure 9			150	µs
PRESA/PRESB PINS								
Input Low Voltage			V_{ILPRES}				0.25 x V_{DD}	V
Input High Voltage			V_{IHPRES}		0.7 x V_{DD}			V
Input Low Current			I_{ILPRES}	V_{ILPRES} = 0V			40	µA
Input High Current			I_{IHPRES}	V_{IHPRES} = V_{DD}			40	µA
I/OAUX PIN								
Internal Pullup Resistor			R_{PULLUP}	Between I/OAUX and V_{DD}	9	14	19	kΩ
Output Low Voltage			V_{OLAUX}	I_{OLAUX} = 1mA			0.3	V
Output High Voltage			V_{OHAUX}	I_{OHAUX} = 40µA (3V/5V)	0.75 x V_{DD}		V_{DD}	V
Output Rise/Fall Time			t_{OT}	C_L = 30pF			0.1	µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3.3V, V_{DDA} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{ILAUX}		-0.3		0.3 x V_{DD}	V
Input High Voltage	V_{IHAUX}		0.7 x V_{DD}		V_{DD}	V
Input Low Current	I_{ILAUX}	V_{ILAUX} = 0V			700	µA
Input High Current	I_{IHAUX}	V_{IHIO} = V_{DD}	-20		+20	µA
Input Rise/Fall Time	t_{IT}	C_L = 30pF			1.2	µs
INTERRUPT PIN						
Output Low Voltage	V_{OLINT}	I_{OH} = 2mA			0.3	V
Input High Leakage Current	I_{LIHINT}				10	µA
D7 TO D0, ALL OTHER LOGIC PINS						
Output Low Voltage	V_{OLD}	I_{OLD} = +5mA			0.2 x V_{DD}	V
Output High Voltage	V_{OD}	I_{OHD} = -5mA	0.8 x V_{DD}		V_{DD}	V
Output Rise/Fall Time	t_{OT}	C_L = 50pF			25	ns
Input Low Voltage	V_{ILD}				0.3 x V_{DD}	V
Input High Voltage	V_{IHD}		0.7 x V_{DD}			V
Input Low Current	I_{ILD}		-20		+20	µA
Input High Current	I_{IHD}		-20		+20	µA
Load Capacitance	C_{LD}				10	pF

Note 1: Operation guaranteed at -40°C but not tested.

Note 2: Parameters are guaranteed to meet all ISO 7816, GSM11-11, and EMV 2000 requirements. For the 1.8V card, the maximum rise and fall time is 10ns.

Note 3: Parameter is guaranteed to meet all ISO 7816, GSM11-11, and EMV 2000 requirements. For the 1.8V card, the minimum slew rate is 0.05V/µs and the maximum slew rate is 0.5V/µs.

AC ELECTRICAL SPECIFICATIONS—TIMING PARAMETERS FOR MULTIPLEXED PARALLEL BUS

(V_{DD} = 3.3V, V_{DDA} = 3.3V, T_A = +25°C, unless otherwise noted.) (Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
XTAL 1 Cycle Time	$t_{CY(XTAL1)}$		50			ns
ALE Pulse Width	$t_{W(ALE)}$		20			ns
Address Valid to ALE Low	t_{AVLL}		10			ns
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	$t_{(AL-RWL)}$		10			ns
$\overline{RD}$ Pulse Width	$t_{W(RD)}$	Register URR	2 x $t_{CY(XTAL1)}$			ns
		Other registers	10			
$\overline{RD}$ Low to Data Read Valid	$t_{(RL-DV)}$				50	ns
$\overline{WR}$/$\overline{RD}$ High to ALE High	$t_{(RWH-AH)}$		10			ns
$\overline{WR}$ Pulse Width	$t_{W(WR)}$		10			ns
Data Write Valid to $\overline{WR}$ Low	$t_{(DV-WL)}$		10			ns

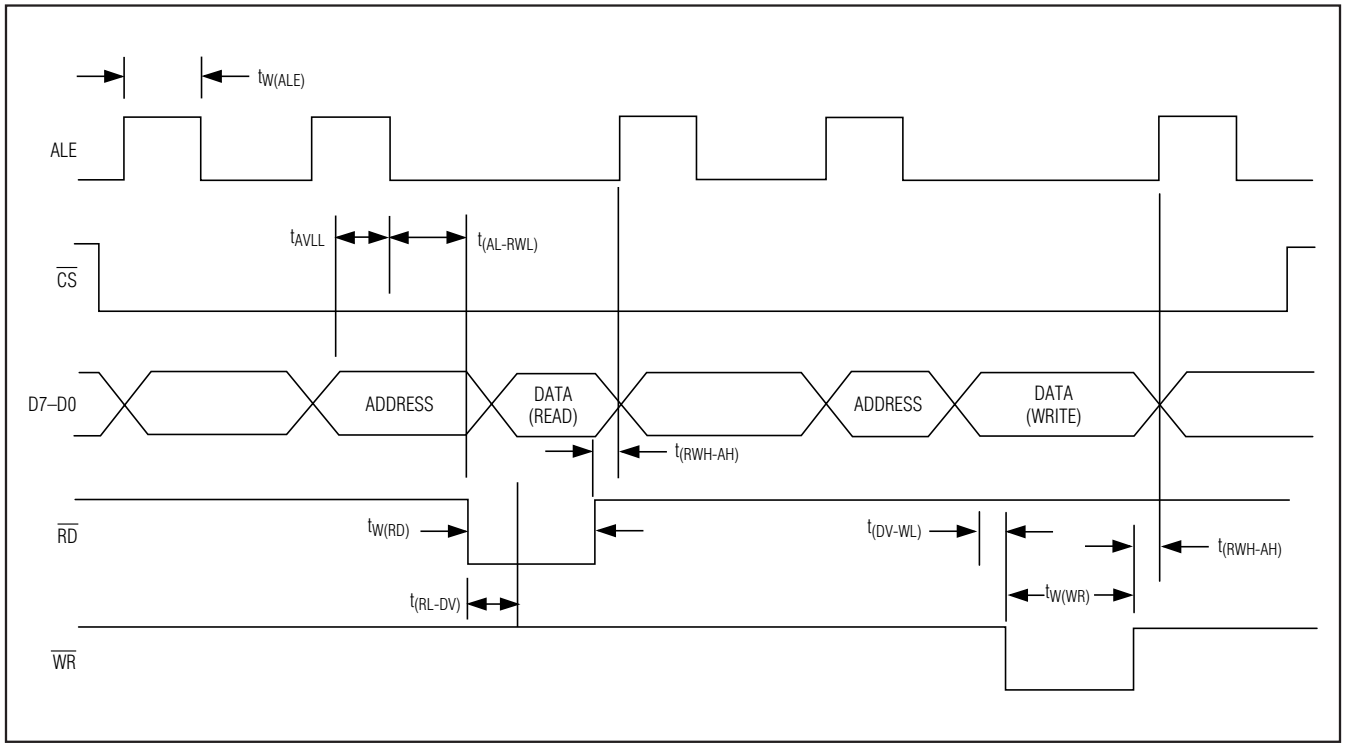


Figure 1. Multiplexed Parallel Bus Timing

Multiprotocol Dual Smart Card Interface

AC ELECTRICAL SPECIFICATIONS—TIMING PARAMETERS FOR NONMULTIPLEXED PARALLEL BUS (READ AND WRITE)

(V_{DD} = 3.3V, V_{DDA} = 3.3V, T_A = +25°C, unless otherwise noted.) (See Figure 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{RD}$ High to $\overline{CS}$ Low	t_1		10			ns
Access Time $\overline{CS}$ Low to Data Out Valid	t_2				50	ns
$\overline{CS}$ High to Data Out High Impedance	t_3				10	ns
Data Valid to End of Write	t_4		10			ns
Data Hold Time	t_5		10			ns
$\overline{RD}$ Low to $\overline{CS}$ or $\overline{WR}$ Low	t_6		10			ns
Address Stable to $\overline{CS}$ or $\overline{WR}$ High	t_7		10			ns
Address to $\overline{CS}$ Low	t_8		10			ns

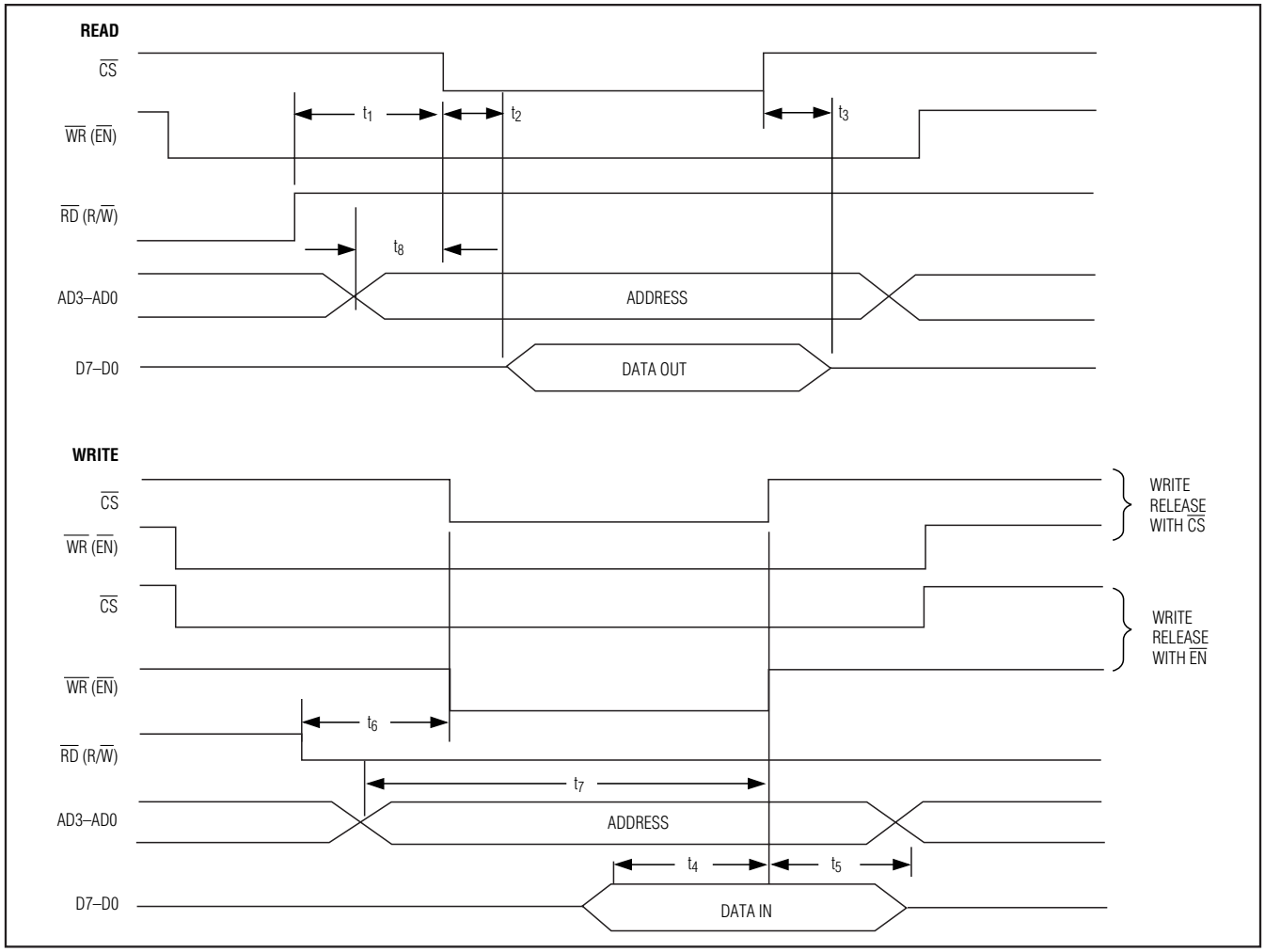


Figure 2. Nonmultiplexed Parallel Bus Timing (Read and Write)

AC ELECTRICAL SPECIFICATIONS—TIMING PARAMETERS FOR CONSECUTIVE READ/WRITE TO URR/UTR/TOC

(V_{DD} = 3.3V, V_{DDA} = 3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SEE FIGURE 3						
$\overline{RD}$ Pulse Width	$t_{W(RD)}$		10			ns
$\overline{RD}$ Low to Bit CRED = 1	$t_{RD(URR)}$		$t_{W(RD)}$ + $2t_{CY(CLK)}$		$t_{W(RD)}$ + $3t_{CY(CLK)}$	ns
Set Time Bit FE	$t_{SB(FE)}$		10.5			ETU
Set Time Bit RBF	$t_{SB(RBF)}$		10.5			ETU
SEE FIGURE 4						
$\overline{WR}/\overline{CS}$ Pulse Width	$t_{W(WR)}$	(Note 4)	10			ns
$\overline{WR}/\overline{CS}$ Low to I/O Low	$t_{WR(UTR)}$		$t_{W(WR)}$ + $2t_{CY(CLK)}$		$t_{W(WR)}$ + $3t_{CY(CLK)}$	ns
SEE FIGURE 5						
$\overline{WR}/\overline{CS}$ Pulse Width	$t_{W(WR)}$		10			ns
$\overline{WR}/\overline{CS}$ High to Bit CRED = 1	$t_{W(TOC)}$	(Notes 4 and 5)	1 / PSC		2 / PSC	ETU

Note 4: Depends on the leading edge of $\overline{WR}$ or $\overline{CS}$ (whichever is deasserted first). Reference this specification to the rising edge of $\overline{CS}/\overline{WR}$ instead of the falling edge.

Note 5: PSC is the programmed prescaler value (31 or 32).

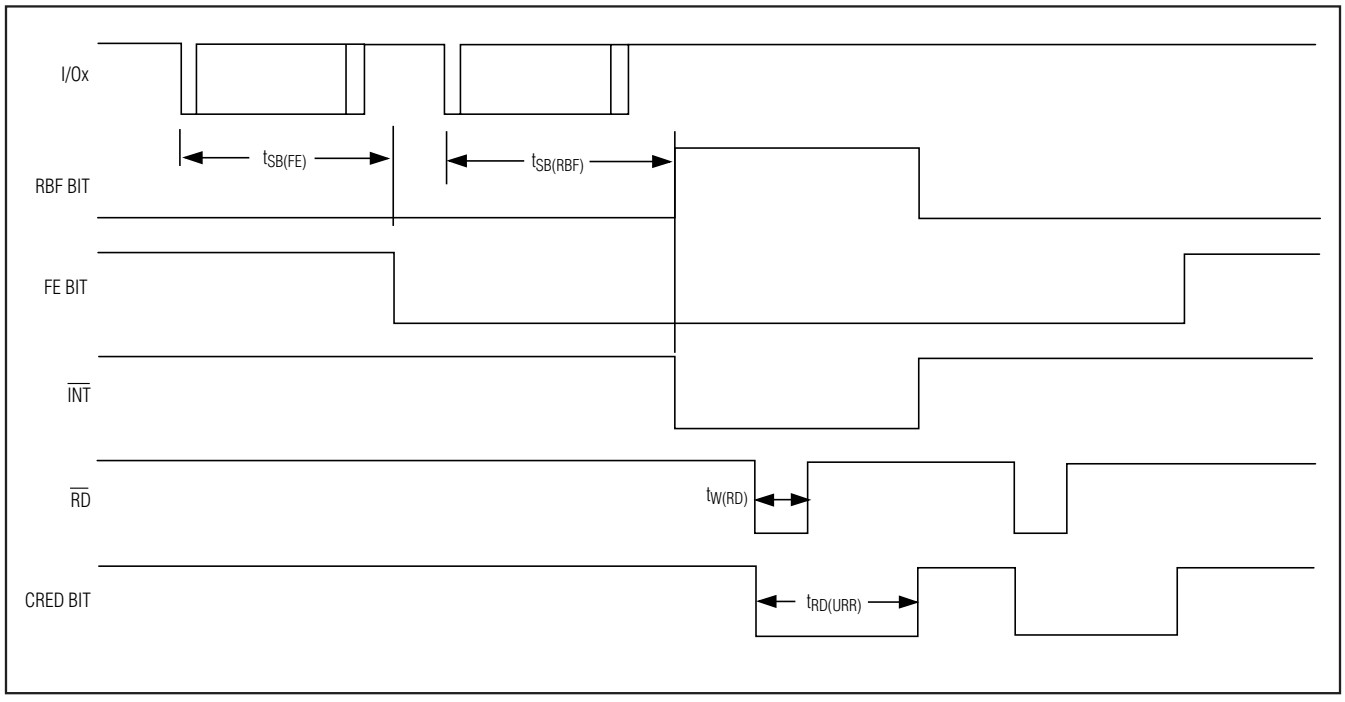


Figure 3. Timing Between Two Read Operations in Register URR

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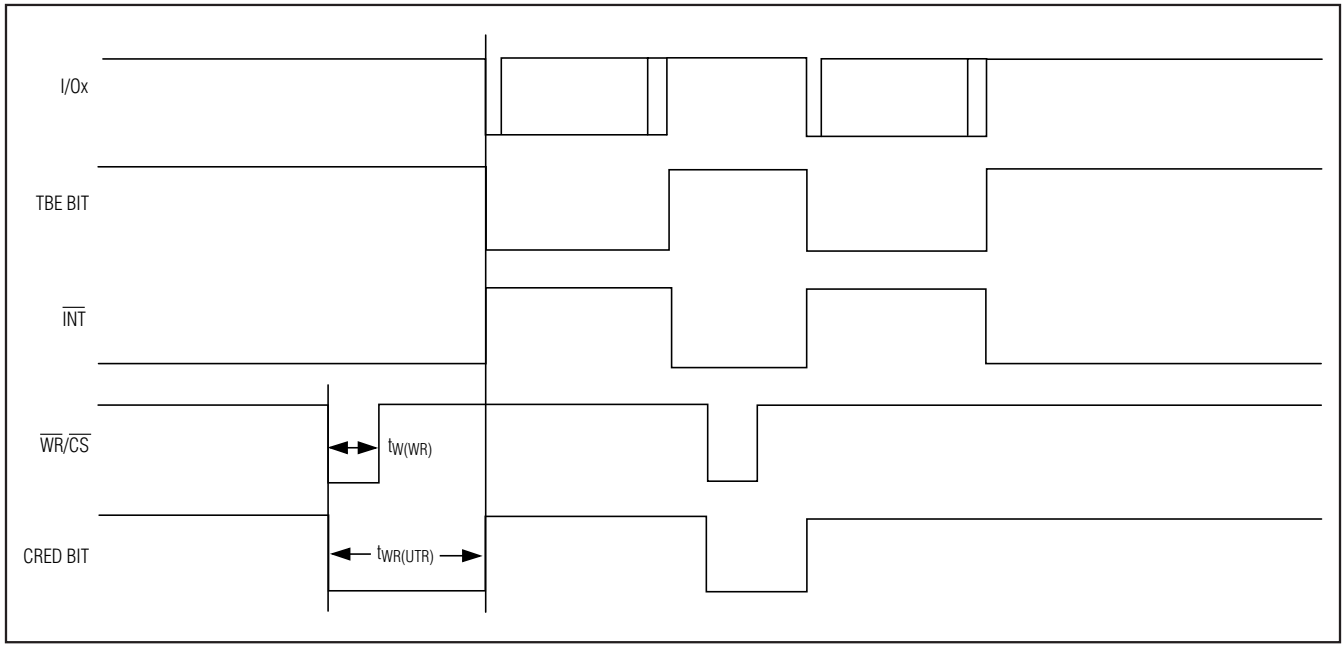


Figure 4. Timing Between Two Write Operations in Register UTR

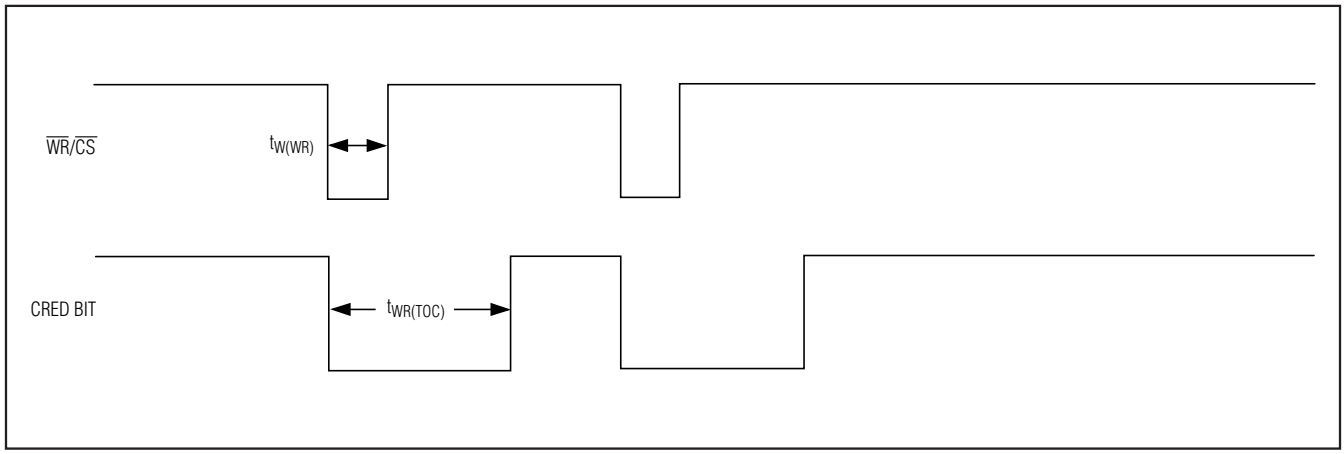


Figure 5. Timing Between Two Write Operations in Register TOC

Pin Description

PIN	NAME	FUNCTION
1	RSTOUT	Reset Output. This active-high output is provided for resetting external devices. The RSTOUT pin is driven high until the DELAY pin reaches V_{DRST}. Once the DELAY pin reaches V_{DRST}, the RSTOUT pin is tri-stated so it can externally be pulled down. The SUPL bit is set for each RSTOUT pulse.
2	I/OAUX	Auxiliary I/O. This I/O pin allows connection to an auxiliary smart card interface.
3	I/OA	Smart Card A I/O Data Line. This is the I/O data line associated with smart card A. This is also referred to as the ISO C7 contact.
4	C8A	Smart Card A Auxiliary I/O. This is an auxiliary I/O associated with smart card A. This is also referred to as the ISO C8 contact. This can be associated with synchronous cards.
5	PRESA	Smart Card A Presence Contact. This is the active-high presence contact associated with smart card A.
6	C4A	Smart Card A Auxiliary I/O. This is an auxiliary I/O associated with smart card A. This is also referred to as the ISO C4 contact. This can be associated with synchronous cards.
7	GNDA	Smart Card A Ground. This must be connected to GND.
8	CLKA	Smart Card A Clock Output. This is the clock output associated with smart card A. This is also referred to as the ISO C3 contact.
9	V_{CCA}	Smart Card A Supply Voltage. This is the supply voltage output associated with smart card A. This is also referred to as the ISO C1 contact.
10	RSTA	Smart Card A Reset. This is the reset output associated with smart card A. This is also referred to as the ISO C2 contact.
11	I/OB	Smart Card B I/O Data Line. This is the I/O data line associated with smart card B. This is also referred to as the ISO C7 contact.
12	C8B	Smart Card B Auxiliary I/O. This is an auxiliary I/O associated with smart card B. This is also referred to as the ISO C8 contact. This can be associated with synchronous cards.
13	PRESB	Smart Card B Presence Contact. This is the active-high presence contact associated with smart card B.
14	C4B	Smart Card B Auxiliary I/O. This is an auxiliary I/O associated with smart card B. This is also referred to as the ISO C4 contact. This can be associated with synchronous cards.
15	GNDB	Smart Card B Ground. This must be connected to GND.
16	CLKB	Smart Card B Clock Output. This is the clock output associated with smart card B. This is also referred to as the ISO C3 contact.
17	V_{CCB}	Smart Card B Supply Voltage. This is the supply voltage output associated with smart card B. This is also referred to as the ISO C1 contact.
18	RSTB	Smart Card B Reset. This is the reset output associated with smart card B. This is also referred to as the ISO C2 contact.
19	GND	Ground
20	V_{UP}	Step-Up Converter Connection. Connect a low-ESR capacitor of 220nF between this pin and ground.

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Pin Description (continued)

PIN	NAME	FUNCTION
21	CPA1	Step-Up Converter Contact 1. Connect a low-ESR capacitor of 220nF between CPA1 and CPA2.
22	CPB1	Step-Up Converter Contact 3. Connect a low-ESR capacitor of 220nF between CPB1 and CPB2.
23	V_{DDA}	Analog Supply Voltage. Positive analog-supply voltage for the step-up converter; can be higher but not lower than V_{DD}. This pin should be decoupled to AGND with a good quality capacitor.
24	CPB2	Step-Up Converter Contact 4. Connect a low-ESR capacitor of 220nF between CPB1 and CPB2.
25	AGND	Analog Ground
26	CPA2	Step-Up Converter Contact 2. Connect a low-ESR capacitor of 220nF between CPA1 and CPA2.
27	V_{DD}	Digital Supply Voltage. This pin should be decoupled to GND with a good quality capacitor.
28–35	D0–D7	8-Bit Digital I/O. This port functions as the data or address/data communication lines between the host controller and the DS8007A for the nonmultiplexed and multiplexed operating modes, respectively.
36	$\overline{RD}$	Active-Low Parallel Bus Read Strobe Input. In multiplexed mode, this input indicates when the host processor is reading information from the DS8007A. In nonmultiplexed mode, this pin signals the current operation is a read ($\overline{RD}$ = 1) or a write ($\overline{RD}$ = 0) when $\overline{CS}$ and $\overline{WR}$ are low.
37	$\overline{WR}$	Active-Low Parallel Bus Write Strobe Input. In multiplexed mode, this input indicates when the host processor is writing information to the DS8007A. In nonmultiplexed mode, a low on this pin signals the bus is engaged in a read or write operation.
38	$\overline{CS}$	Active-Low Chip-Select Input. This input indicates when the DS8007A is active on the parallel bus.
39	ALE	Address Latch Enable Input. This signal monitors the ALE signal when the host processor bus is operating in multiplexed mode. Connect this signal to V_{DD} when operating in nonmultiplexed mode.
40	$\overline{INT}$	Active-Low Interrupt. This output indicates an interrupt is active.
41	INTAUX	Auxiliary Interrupt Input. This pin serves as an auxiliary interrupt.
42–45	AD3–AD0	Register Selection Address Inputs. These pins function as the address input lines for the nonmultiplexed configuration and should be connected to ground or V_{DD} in the multiplexed configuration.
46, 47	XTAL2, XTAL1	Crystal Oscillators. Place a crystal with appropriate load capacitors between these pins if that is the desired clock source. XTAL1 also acts as an input if there is an external clock source in place of a crystal.
48	DELAY	External Delay Capacitor Connection. Connect a capacitor from this pin to ground to set the power-on reset delay.

Detailed Description

The following describes the major functional features of the device. Use of this document requires the reader have a basic understanding of ISO 7816 terminology.

Parallel Bus Interface

The device interfaces to a host computer/processor through a multiplexed or demultiplexed, parallel, 8-bit data bus (D0–D7). The parallel bus interface monitors the ALE signal and automatically detects whether a multiplexed or nonmultiplexed external bus interface is intended. The nonmultiplexed external bus interface is the default configuration and is maintained so long as no edge (activity) is detected on the ALE pin. Once a rising edge is detected on the ALE pin, the DS8007A is placed into the multiplexed mode of operation. Once in the multiplexed mode of operation, a reset/power cycle or the deassertion of $\overline{CS}$ forces the device to the nonmultiplexed mode. Connecting the ALE pin to V_{DD} or ground forces the device into nonmultiplexed parallel bus mode. Figure 7 shows that the bus recognition dictates whether the external address lines (AD3–AD0) can be used directly or whether the external data lines (D7–D0) must be latched according to the ALE input signal. In the multiplexed mode of operation, a new address is latched irrespective of the state of $\overline{CS}$.

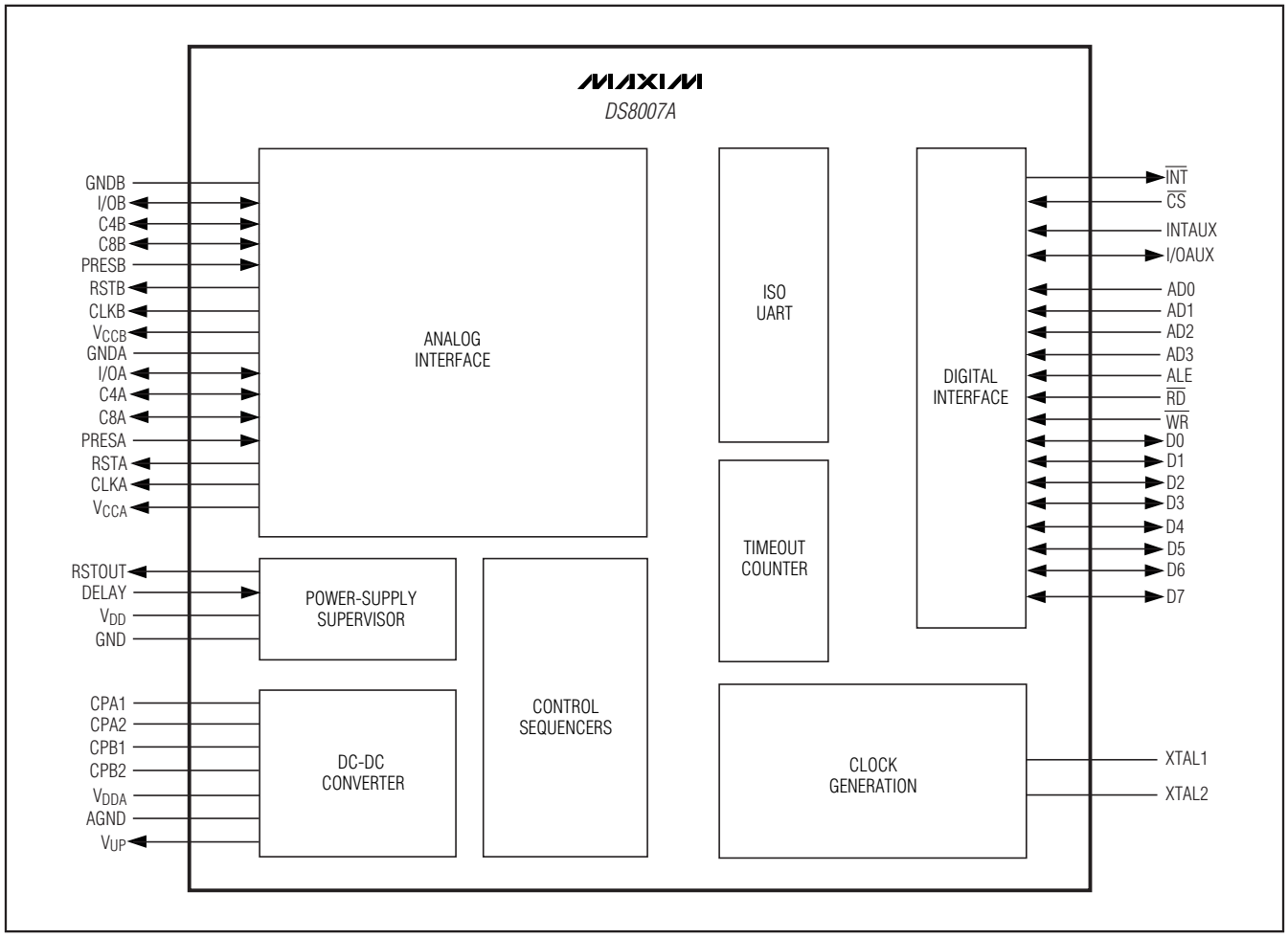


Figure 6. Block Diagram

Multiprotocol Dual Smart Card Interface

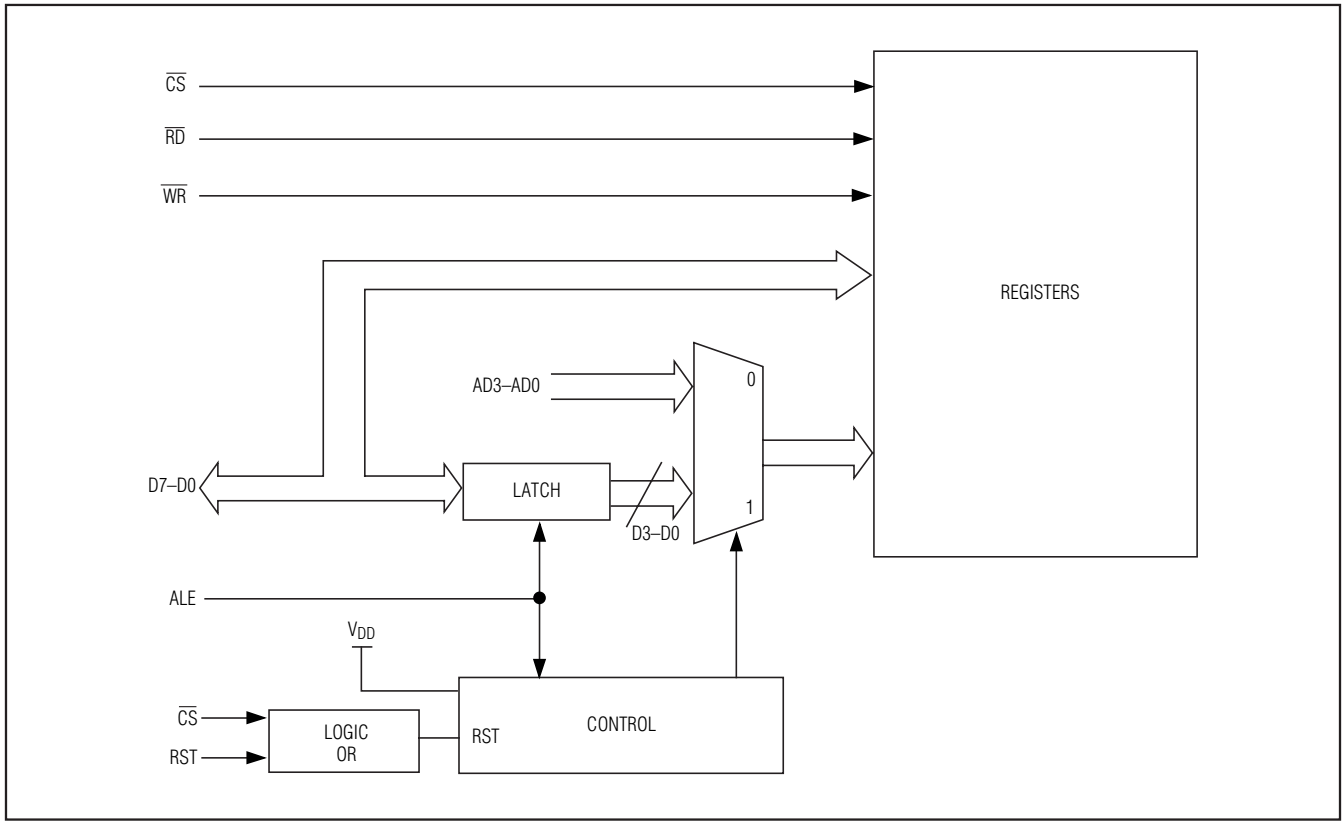


Figure 7. Parallel Bus Interface

Multiplexed Mode

In the multiplexed mode of operation, the D7–D0 signals are multiplexed between address and data. The falling edge of the address latch enable (ALE) signal from the host microcontroller latches the address (D3–D0), and the $\overline{RD}$ and $\overline{WR}$ strobe input signals are used to enable a read or write operation, respectively, if the DS8007A is selected (i.e., $\overline{CS}$ = 0). See the AC timing for the multiplexed parallel bus mode found earlier in this data sheet.

Nomultiplexed Mode

In the nonmultiplexed mode of operation, the address is always provided on the AD3–AD0 signals, and the data is always transacted on the D7–D0 signals. The $\overline{RD}$ input signal is used as a read/write (R/W) operation select. The $\overline{WR}$ and $\overline{CS}$ input signals serve as active-low enables, and must be asserted for the read or write operation to take place. See the AC timing for the nonmultiplexed parallel bus mode found earlier in this data sheet.

Control Registers

Special control registers that the host computer/microcontroller accesses through the parallel bus manage most DS8007A features. Many of the registers, although only mentioned once in the listing, are duplicated for each card interface. The PDR, GTR, UCR1, UCR2, and CCR registers exist separately for each of the three card interfaces. The PCR register is provided only for card interface A and card interface B.

The specific register to be accessed is controlled by the current setting of the SC3–SC1 bits in the Card Select Register. For example, there are three instances of the UART Control Register 1 (UCR1) at address 06h. If the SC3–SC1 bits are configured so that card A is selected, then all reads and writes to address 06h only affect card A. If SC3–SC1 are changed to select card B, then all reads and writes to address 06h only affect card B, etc.

In addition, some registers have different functions based on whether the register is being read from or written to. An example of this are the UART Receive (URR)/UART Transmit (UTR) registers located at address 0Dh. Although they share the same address, during read operations the receive register is read, and write operations go to a separate transmit register. This selection requires no extra configuration by the software.

Table 1. Special Function Register Map

ADDRESS (HEX)	REGISTER NAME	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET	$\overline{RIU}$ = 0*
00	CSR	R/W	CSR7	CSR6	CSR5	CSR4	$\overline{RIU}$	SC3	SC2	SC1	0011 0000	0011 0uuu
01	CCR	R/W	—	—	SHL	CST	SC	AC2	AC1	AC0	0000 0000	00uu uuuu
02	PDR	R/W	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	0000 0000	uuuu uuuu
03	UCR2	R/W	—	DISTBE/ RBF	DISAUX	PDWN	SAN	$\overline{AUTOC}$	CKU	PSC	0000 0000	uuuu uuuu
05	GTR	R/W	GTR.7	GTR.6	GTR.5	GTR.4	GTR.3	GTR.2	GTR.1	GTR.0	0000 0000	uuuu uuuu
06	UCR1	R/W	FTE0	FIP	—	PROT	T/R	LCT	SS	CONV	0000 0000	0uuu 00uu
07	PCR	R/W	—	—	C8	C4	1V8	RSTIN	3V/5V	START	0011 0000	0011 uuuu
08	TOC	R/W	TOC7	TOC6	TOC5	TOC4	TOC3	TOC2	TOC1	TOC0	0000 0000	0000 0000
09	TOR1	W	TOL7	TOL6	TOL5	TOL4	TOL3	TOL2	TOL1	TOL0	0000 0000	uuuu uuuu
0A	TOR2	W	TOL15	TOL14	TOL13	TOL12	TOL11	TOL10	TOL9	TOL8	0000 0000	uuuu uuuu
0B	TOR3	W	TOL23	TOL22	TOL21	TOL20	TOL19	TOL18	TOL17	TOL16	0000 0000	uuuu uuuu
0C	MSR	R	CLKSW	FER	BGT	CRED	PRB	PRA	INTAUX	TBE/ RBF	0101 0000	u1u1 uuu0
0C	FCR	W	—	PEC2	PEC1	PEC0	FTE1	FL2	FL1	FL0	0000 0000	0uuu 0uuu
0D	URR	R	UR7	UR6	UR5	UR4	UR3	UR2	UR1	UR0	0000 0000	0000 0000
0D	UTR	W	UT7	UT6	UT5	UT4	UT3	UT2	UT1	UT0	0000 0000	0000 0000
0E	USR	R	TO3	TO2	TO1	EA	PE	OVR	FER	TBE/ RBF	0000 0000	0000 0000
0F	HSR	R	—	PRTLB	PRTLA	SUPL	PRLB	PRLA	INTAUX	PTL	0001 0000	0uuu xxxu

** u = unchanged, x = always reflects state of external device pin, even when RIU = 0.*

Note: *Writes to unimplemented bits have no effect. Reads of unimplemented bits return 0.*

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Card Select Register (CSR)

	7	6	5	4	3	2	1	0
Address 00h	CSR7	CSR6	CSR5	CSR4	$\overline{RIU}$	SC3	SC2	SC1
	R-0	R-0	R-1	R-1	RW-0	RW-0	RW-0	RW-0

R = unrestricted read, W = unrestricted write, -n = value after reset. This register is reset to 00110uuub on $\overline{RIU}$ = 0.

Bits 7 to 4: Identification Bits (CSR7 to CSR4). These bits provide a method for software to identify the device as follows:

0011 = DS8007A revision Ax

Bit 3: Reset ISO UART ($\overline{RIU}$). When this bit is cleared (0), most of the ISO UART registers are reset to their initial values. This bit must be cleared for at least 10ns prior to initiating an activation sequence. This bit must be set (1) by software before any action on the UART can take place.

Bits 2 to 0: Select Card Bits (SC3 to SC1). These bits determine which IC card interface is active as shown below. Only one bit should be active at any time, and no card is selected after reset (i.e., SC3–SC1 = 000b). Other combinations are invalid.

000 = No card is selected.

001 = Card A is selected.

010 = Card B is selected.

100 = AUX card interface is selected.

Clock Configuration Register (CCR)

	7	6	5	4	3	2	1	0
Address 01h	—	—	SHL	CST	SC	AC2	AC1	AC0
	R-0	R-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R = unrestricted read, W = unrestricted write, -n = value after reset. This register is reset to 00uuuuuub on $\overline{RIU}$ = 0.

Bits 7 and 6: Reserved.

Bit 5: Stop High or Low (SHL). This bit determines if the card clock stops in the low or high state when the CST bit is active. It forces the clock to stop in a low state when SHL = 0 or in a high state when SHL = 1.

Bit 4: Clock Stop (CST). For an asynchronous card, this bit allows the clock to the selected card to be stopped. When this bit is set (1), the card clock is stopped in the state determined by the SHL bit. When this bit is cleared (0), the card clock operation is defined by CCR bits AC2–AC0.

Bit 3: Synchronous Clock (SC). For a synchronous card, the card clock is controlled by software manipulation of this SC, and the contact CLK is the copy of the value in this bit. In synchronous transmit mode, a write to the UTR results in the least significant bit (LSb) of the data written to the UTR being driven out on the I/Ox pin. In synchronous receive mode, the state of the I/Ox pin can be read from the LSb of the URR.

Bits 2 to 0: Alternating Clock Select (AC2 to AC0). These bits select the frequency of the clock provided to the active card interface and to the UART for the elementary time unit (ETU) generation as shown below. All frequency changes are synchronous so that there are no spikes or unwanted pulse widths during transitions. f_{INT} is the frequency of the internal oscillator.

AC2–AC0

000 = f_{XTAL}

001 = f_{XTAL} / 2

010 = f_{XTAL} / 4

011 = f_{XTAL} / 8

1xx = f_{INT} / 2

Programmable Divider Register (PDR)

	7	6	5	4	3	2	1	0
Address 02h	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R = unrestricted read, W = unrestricted write, -n = value after reset; all bits unaffected by $\overline{RIU}$ = 0.

Bits 7 to 0: Programmable ETU Divider Register Bits 7 to 0 (PD7 to PD0). These bits, in conjunction with the defined UART input clock (based upon CKU, AC2–AC0) and the prescaler selection (PSC bit), are used to define the ETU for the UART when interfaced to the associated card interface. The output of the prescaler block is further divided according to the PD7–PD0 bits as follows:

- ETU = Prescaler output / (PD7–PD0), when PD7–PD0 = 02h–FFh
- ETU = Prescaler output / 1, when PD7–PD0 = 00h–01h
- Prescaler output / 256 is not supported

UART Control Register 2 (UCR2)

	7	6	5	4	3	2	1	0
Address 03h	—	DISTBE/RBF	DISAUX	PDWN	SAN	$\overline{AUTOC}$	CKU	PSC
	R-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R = unrestricted read, W = unrestricted write, -n = value after reset; all bits unaffected by $\overline{RIU}$ = 0.

Bit 7: Reserved.

Bit 6: Disable TBE/RBF Interrupt (DISTBE/RBF). This bit controls whether the TBE/RBF flag can generate an interrupt on the $\overline{INT}$ pin. When this bit is cleared to 0, an interrupt is signaled on the $\overline{INT}$ pin in response to the TBE/RBF flag getting set. When DISTBE/RBF is set to 1, interrupts are not generated in response to the TBE/RBF flag. Disabling the TBE/RBF interrupt can allow faster communication speed with the card, but requires that a copy of TBE/RBF in register MSR be polled to not lose priority interrupts that can occur in register USR.

Bit 5: Disable Auxiliary Interrupt (DISAUX). This bit controls whether the external INTAUX pin can generate an interrupt on the $\overline{INT}$ output pin. When this bit is cleared to 0, a change on the INTAUX input pin results in assertion of the $\overline{INT}$ output pin. When DISAUX is set to 1, a change on INTAUX does not result in assertion of the $\overline{INT}$ output pin. The INTAUXL bit is set by a change on the INTAUX pin independent of the DISAUX bit state. Since the INTAUX bit is set independent of the DISAUX bit, it is advisable to read HSR (thus clearing INTAUX) prior to clearing DISAUX to avoid an interrupt on the $\overline{INT}$ pin. To avoid an interrupt when selecting a different card, the DISAUX bit should be set to 1 in all UCR2 registers.

Bit 4: Power-Down Mode Enable (PDWN). This bit controls entry into the power-down mode. Power-down mode can only be entered if the SUPL bit has been cleared. When PDWN is set to 1, the XTAL1 and XTAL2 crystal oscillator is stopped, and basic functions such as the sequencers are supported by the internal ring oscillator. The UART is put in a suspended state, and the clocks to the UART, the ETU unit, and the timeout counter are gated off. During the power-down mode, it is not possible to select a card other than the one currently selected (advisory to the programmer, selecting another card during power-down mode is not recommended). There are five ways of exiting the power-down mode:

- Insertion of card A or card B (detected by PRLA or PRLB).
- Withdrawal of card A or card B (detected by PRLA or PRLB).
- Reassertion of the $\overline{CS}$ pin to select the DS8007A ($\overline{CS}$ must be deasserted after setting PDWN = 1 for this event to exit from power-down).
- INTAUXL bit is set due to change in INTAUX (INTAUXL bit must be cleared first).
- Clearing of PDWN bit by software (if $\overline{CS}$ pin is always tied to 0).

Except in the case of a read operation of register HSR, the $\overline{INT}$ pin remains asserted in the active-low state. The host device can read the status registers after the oscillator warmup time, and the $\overline{INT}$ signal returns to the high state.

Bit 3: Synchronous/Asynchronous Card Select (SAN). This bit selects whether a synchronous or asynchronous card interface is enabled. When this bit is cleared to 0, an asynchronous card interface is expected. When this bit is set to 1, a synchronous interface is expected. In synchronous mode, the UART is bypassed; the SC bit controls the CLK, and I/O is transacted in the LSb of UTR/URR. Card interface AUX cannot operate in the true synchronous mode since it does not have a CLK signal to accompany I/OAUX. However, the SAN bit invokes the same control of I/OAUX through UTR/URR as is given for card interfaces A and B.

Bit 2: Auto Convention Disable ($\overline{AUTOC}$). This active-low bit controls whether the decoding convention should automatically be detected during the first received character in answer-to-reset (ATR). If $\overline{AUTOC}$ = 0, the character decoding convention is automatically detected (while SS = 1) and the UCR1.CONV bit is written accordingly by hardware. If $\overline{AUTOC}$ = 1, the UCR1.CONV bit must be set by software to assign the character decoding convention. The $\overline{AUTOC}$ bit must not be changed during a card session.

Bit 1: Clock UART Doubler Enable (CKU). This bit enables the effective ETU defined for the UART to last half the number of clock cycles defined by the AC2–AC0 and PD7–PD0 configuration (except in the case when AC2–AC0 = 000b, where $f_{CLK} = f_{XTAL}$). When CKU is cleared to 0, the AC2–AC0 defined f_{CLK} is used for ETU timing generation. When CKU is set to 1, a clock frequency of 2 x f_{CLK} is used for ETU generation.

Bit 0: Prescaler Select (PSC). When PSC = 0, the prescaler value is 31. When PSC = 1, the prescaler value is 32.

Guard Time Register (GTR)

	7	6	5	4	3	2	1	0
Address 05h	GTR.7	GTR.6	GTR.5	GTR.4	GTR.3	GTR.2	GTR.1	GTR.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R = unrestricted read, W = unrestricted write, -n = value after reset; all bits unaffected by $\overline{RIU}$ = 0.

Bits 7 to 0: Guard Time Register Bits 7 to 0 (GTR.7 to GTR.0). These bits are used for storing the number of guard time units (ETU) requested during ATR. When transmitting, the DS8007A UART delays these numbers of extra guard time ETU before transmitting a character written to UTR.

UART Control Register 1 (UCR1)

	7	6	5	4	3	2	1	0
Address 06h	FTE0	FIP	—	PROT	T/R	LCT	SS	CONV
	R-0	RW-0	R-0	RW-0	RW-0	RW-0	RW-0	RW-0

R = unrestricted read, W = unrestricted write, -n = value after reset. This register is reset to 0uuu00uub on $\overline{RIU}$ = 0.

Bit 7: FIFO Threshold Enable 0 (FTE0). When this bit and the FTE1 (FCR.3) bit are set, the programmable FIFO threshold feature is enabled. This bit always reads 0 for compatibility.

Bit 6: Force Inverse Parity (FIP). When this bit is configured to 0, the correct parity is transmitted with each character, and receive characters are checked for the correct parity. When FIP = 1, an inverse parity bit is transmitted with each character and correctly received characters are NAK'd.

Bit 5: Reserved. This bit must be left 0. Setting this bit to 1 causes improper device operation.

Bit 4: Protocol Select (PROT). This bit is set to 1 by software to select the asynchronous T = 1 protocol and is cleared to 0 to select the T = 0 protocol.

Bit 3: Transmit/Receive (T/R). This bit should be set by software to operate the UART in transmit mode. When this bit is changed from 0 to 1 (UART changed from receive to transmit mode), hardware sets the USR.RBF/TBE bit, indicating an empty transmit buffer. The T/R bit is automatically cleared to 0 following successful transmission if UCR1.LCT is configured to 1 prior to the transmission. This bit cannot be written to when $\overline{RIU}$ = 0 (holding in reset).

Bit 2: Last Character to Transmit (LCT). This bit is optionally set by software prior to writing the last character to be transmitted to the UART transmit register (UTR). If LCT is set to 1 prior to writing to UTR, hardware resets the LCT, T/R, and TBE/RBF bits following a successful transmission. Setting this bit to 1 allows automatic change to the reception mode after the last character is sent. This bit can be set during and before the transmission. This bit cannot be written to when $\overline{RIU}$ = 0 (holding in reset).

Bit 1: Software Convention Setting (SS). This bit should be set by software prior to ATR to allow automatic convention detection. Hardware automatically resets the SS bit at 10.5 ETU after the detection of the start bit of the first character of the ATR.

Bit 0: Convention (CONV). This bit defines the character decoding convention of the ISO UART. If CONV = 1, the convention is direct. If CONV = 0, the convention is inverted. If automatic convention detection is enabled ($\overline{AUTOC}$ = 0), hardware detects the character convention and configures the CONV bit appropriately at 10.5 ETU. Otherwise ($\overline{AUTOC}$ = 1), software must configure the CONV bit.

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Power Control Register (PCR)

	7	6	5	4	3	2	1	0
Address 07h	—	—	C8	C4	1V8	RSTIN	3V/5V	START
	R-0	R-0	RW-1	RW-1	RW-0	RW-0	RW-0	RW-0

R = unrestricted read, W = unrestricted write, -n = value after reset. This register is reset to 0011uuuub on $\overline{RIU}$ = 0.

Note: *The AUX card interface does not have register PCR. C4 and C8 are external ports that are internally pulled up (10kΩ to V_{CCx}), writing a 1 to C4, C8 configures the weak pullup. Reads are made of the pin state to a different physical bit. Writing a 0 to C4, C8 configures the pulldown. C4 and C8 bits can be written irrespective of the state of the T/R bit.*

Bits 7 and 6: Reserved.

Bit 5: Contact 8 (C8). Writes to this register bit are output on the C8 pin of the card interface. Reads of this register bit reflect the value on the C8 pin.

Bit 4: Contact 4 (C4). Writes to this register bit are output on the C4 pin of the card interface. Reads of this register bit reflect the value on the C4 pin.

Bit 3: 1.8V Card Select (1V8). If this bit is set to 1, the V_{CCx} supplied to the card interface is 1.8V. This bit overrides the 3V/5V bit.

Bit 2: Reset Bit (RSTIN). When a card interface is activated, the RSTx pin is driven according to the value contained in this register bit.

Bit 1: 3V/5V Card Select (3V/5V). This bit determines the V_{CCx} level for the card interface. When this bit is set to 1, V_{CCx} is defined as 3V. When this bit is cleared to 0, V_{CCx} is defined as 5V. When the 1V8 and 3V/5V bits are set to 1, priority is given to 1V8.

Bit 0: Start (START). This bit controls software activation/deactivation of the card interface. When this bit is written to 1, the activation sequence for the selected card is performed. When this bit is written to 0, the deactivation sequence for the selected card is performed. Hardware automatically resets the START bit for the associated card interface when emergency deactivation occurs. This bit can be written regardless of the state of the $\overline{RIU}$ bit.

Timeout Configuration Register (TOC)

	7	6	5	4	3	2	1	0
Address 08h	TOC7	TOC6	TOC5	TOC4	TOC3	TOC2	TOC1	TOC0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R = unrestricted read, W = unrestricted write, -n = value after reset. This register is reset to 00000000b on $\overline{RIU}$ = 0.

Bits 7 to 0: Timeout Counter Configuration Register Bits (TOC7 to TOC0). These register bits determine the counting configuration for the three timeout counter registers. The available configurations are detailed in the *Timeout Counter Operation* section. These registers can be written when $\overline{RIU}$ = 1 before activation and cannot be written to when $\overline{RIU}$ = 0.

Timeout Counter Register 1 (TOR1)

	7	6	5	4	3	2	1	0
Address 09h	TOL7	TOL6	TOL5	TOL4	TOL3	TOL2	TOL1	TOL0
	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

R = unrestricted read, W = unrestricted write, -n = value after reset. This register is unchanged on $\overline{RIU}$ = 0.

Bits 7 to 0: Timeout Counter Register 1 Bits (TOL7 to TOL0). This register can be configured to operate as an 8-bit counter or as the lowest 8 bits of a 24-bit counter. TOR1, TOR2, and TOR3 are concatenated to form a 24-bit ETU counter or a pair of independent 16- and 8-bit counters. These counters are only used when a card is supplied an active clock. See the *Timeout Counter Operation* section for details on configurable modes.

Timeout Counter Register 2 (TOR2)

	7	6	5	4	3	2	1	0
Address 0Ah	TOL15	TOL14	TOL13	TOL12	TOL11	TOL10	TOL9	TOL8
	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

R = unrestricted read, W = unrestricted write, -n = value after reset. This register is unchanged on $\overline{RIU}$ = 0.

Bits 7 to 0: Timeout Counter Register 2 Bits (TOL15 to TOL8). This register can be configured to operate as the lower 8 bits of a 16-bit counter or as the middle 8 bits of a 24-bit counter. See the *Timeout Counter Operation* section for details on configurable modes.

Timeout Counter Register 3 (TOR3)

	7	6	5	4	3	2	1	0
Address 0Bh	TOL23	TOL22	TOL21	TOL20	TOL19	TOL18	TOL17	TOL16
	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

R = unrestricted read, W = unrestricted write, -n = value after reset. This register is unchanged on $\overline{RIU}$ = 0.

Bits 7 to 0: Timeout Counter Register 3 Bits (TOL23 to TOL16). This register can be configured to operate as the high 8 bits of a 16-bit counter or as the high 8 bits of a 24-bit counter. See the *Timeout Counter Operation* section for details on configurable modes.

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Mixed Status Register (MSR)

	7	6	5	4	3	2	1	0
Address 0Ch	CLKSW	FE	BGT	CRED	PRB	PRA	INTAUX	TBE/RBF
	R-0	R-1	R-0	R-1	R-0	R-0	R-0	R-0

R = unrestricted read, W = unrestricted write, -n = value after reset. This register is reset to u1u1uuu0b on $\overline{RIU}$ = 0.

Bit 7: Clock Switch (CLKSW). This status bit indicates the clock (f_{XTAL} / n or f_{INT} / 2) being sourced by the selected card interface and thus may be used to determine when a requested clock switch has occurred properly. When CLKSW is set 1, the clock has switched from f_{XTAL} / n to f_{INT} / 2; when CLKSW is cleared to 0, the clock has switched from f_{INT} / 2 to f_{XTAL} / n.

Bit 6: FIFO Empty Status Bit (FE). This bit is set to 1 when the receive FIFO is empty. This bit is cleared to 0 when at least one character remains in the receive FIFO.

Bit 5: Block Guard Time Status Bit (BGT). This status bit is linked to an ETU counter for the currently selected card interface, and is intended for use in verifying that the block guard time is always being met. The counter restarts on every start bit and stops only if the terminal count is reached. The terminal count is dependent upon the selected protocol (16 ETU for T = 0 and 22 ETU for T = 1). This bit is cleared to 0 on every start bit.

Bit 4: Control Ready (CRED). This bit signals the host device that the DS8007A is ready to handle the next write operation to UTR or TOC or the next read operation of URR. When CRED = 0, the DS8007A is still working on the previous operation and cannot correctly process the new read/write request. When CRED = 1, the DS8007A is ready for the next read/write request. This "busy" bit allows the DS8007A to meet the timing constraints of high-speed host devices. The CRED bit remains low:

- 3 clock cycles after the rising edge of $\overline{RD}$ before reading URR.
- 3 clock cycles after the rising edge of $\overline{WR}$ (or $\overline{CS}$) before writing to UTR.
- 1/PSC (min) ETU and 2/PSC (max) ETU after the rising edge of $\overline{WR}$ (or $\overline{CS}$) before writing to TOC

The CRED bit timing applies to asynchronous mode only; this bit is forced to 1 in synchronous mode.

Bit 3: Presence Card B (PRB). This bit is set to 1 when card B presence is detected and is cleared to 0 when card B is not present.

Bit 2: Presence Card A (PRA). This bit is set to 1 when card A presence is detected and is cleared to 0 when card A is not present.

Bit 1: INTAUX Bit (INTAUX). This bit reflects the state of the INTAUX pin. This bit is set when the INTAUX pin is high and is cleared when the INTAUX pin is low.

Bit 0: Transmit Buffer Empty/Receive Buffer Full (TBE/RBF). This bit signals special conditions relating to the ISO UART and associated hardware. This bit is not set when the last character is transmitted by the UART when LCT = 1.

This bit is set to 1 when:

- UCR1.T/R is changed from 0 (receive mode) to 1 (transmit mode).
- A character is transmitted by the UART.
- The receive FIFO becomes full.

This bit is cleared to 0 when:

- The ISO UART is reset by $\overline{RIU}$ = 0.
- A character is written to the UART transmit register (UTR) in transmit mode.
- A character is read from the receive FIFO in receive mode.
- UCR1.T/R is changed from 1 (transmit mode) to 0 (receive mode).

FIFO Control Register (FCR)

	7	6	5	4	3	2	1	0
Address 0Ch	—	PEC2	PEC1	PEC0	FTE1	FL2	FL1	FL0
	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

R = unrestricted read, W = unrestricted write, -n = value after reset. This register is reset to 0uuu0uuub on $\overline{RIU}$ = 0.

Bit 7: Reserved.

Bits 6 to 4: Parity Error Count (PEC2 to PEC0). These bits are used only for the T = 0 protocol to determine the number of retransmission attempts that can occur in transmit mode and the number of parity errors that can occur before the PE bit is set to 1 to indicate that the parity error limit has been reached. In transmit mode, the DS8007A attempts to retransmit a character up to (PEC2–PEC0) times (when NAK'd by the card) before the PE bit is set. Retransmission attempts are automatically made at 15 ETU from the previous start bit. If PEC2–PEC0 = 000b, no retransmission attempt is made, however, the host device can manually rewrite the character to UTR (in which case, it is re-sent as early as 13.5 ETU from the previous start bit of the error character.

In receive mode, if (PEC2–PEC0 + 1) parity errors have been detected, the USR.PE bit is set to 1. For example, if PEC2–PEC0 = 000b, only one parity error needs to be detected for the PE bit to be set; if PEC2–PEC0 = 111b, 8 parity errors must be detected, etc. If a character is correctly received before the allowed parity error count is reached, the parity counter is reset. For the T = 1 protocol, the parity counter is not used. The PE bit is set whenever a parity error is detected for a received character.

Bit 3: FIFO Threshold Enable 1 (FTE1). When this bit and the FTE0 (UCR1.7) bit are set, the programmable FIFO threshold feature is enabled. This bit always reads 0 for compatibility.

Bits 2 to 0: FIFO Length (FL2 to FL0). These bits determine the depth of the receive FIFO. The receive FIFO has depth equal to (FL2–FL0) + 1 (e.g., FIFO depth = 2 if FL2–FL0 = 001b).

UART Receive Register (URR)/UART Transmit Register (UTR)

	7	6	5	4	3	2	1	0
Address 0Dh	UR7/UT7	UR6/UT6	UR5/UT5	UR4/UT4	UR3/UT3	UR2/UT2	UR1/UT1	UR0/UT0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R = unrestricted read, W = unrestricted write, -n = value after reset. This register is reset to 00000000b on $\overline{RIU}$ = 0.

Bits 7 to 0: UART Receive Register (Read Operations)/UART Transmit Register (Write Operations) (UR7/UT7 to UR0/UT0). This register is used both as the UART transmit and receive buffer by the host microcontroller. Received characters are always read by the host microcontroller in direct convention, meaning that if the CONV bit is 0, then characters received using inverse convention are automatically translated by the hardware. When the receive FIFO is enabled, reads of URR always access the oldest available received data. For the synchronous mode of operation, the LSb (URR.0) reflects the state of the selected card I/Ox line.

Writes by the host microcontroller to this register transmit characters to the selected card. The host microcontroller should write data to UTR in direct convention (inverse convention encoding is handled by the hardware). The UTR register cannot be loaded during transmission. The transmission:

- Starts at the end of the write operation (rising edge of $\overline{WR}$) if the previous character has been transmitted and the extra guard time has been satisfied.
- Starts at the end of the extra guard time if that guard time has not been satisfied.
- Does not start if the transmission of the previous character is not completed (e.g., during retransmission attempts or if a transmit parity error occurs).

For the synchronous mode of operation, only the LSb (UTR.0) of the loaded data is transferred to the I/Ox pin for the selected card.

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UART Status Register (USR)

	7	6	5	4	3	2	1	0
Address 0Eh	TO3	TO2	TO1	EA	PE	OVR	FER	TBE/RBF
	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

R = unrestricted read, W = unrestricted write, -n = value after reset. All register bits are reset to 00000000b on $\overline{RIU}$ = 0.

Note: *If any of the bits TO3, TO2, TO1, EA, PE, OVR, or FER are set, then a USR read operation clears the bit, causing an interrupt less than 2µs after the rising edge of the $\overline{RD}$ strobe. PE and FER can be set by the same reception.*

Bits 7 to 5: Timeout Counter 3/2/1 Status (TO3 to TO1). These bits are set to 1 whenever their respective timeout counter reaches its terminal count. Any of these bits causes the $\overline{INT}$ pin to be asserted.

Bit 4: Early Answer Detected (EA). This bit is set to 1 if a start bit is detected on the I/O line during the ATR between clock cycles 200–368 when the RSTx pin is low, and during the first 368 clock cycles after the RSTx pin is high. When the EA bit becomes set, $\overline{INT}$ is asserted. If the EA bit is set for a card during ATR, this bit is cleared when switched to another card. During the early answer detection period, a 46-clock-cycles sampling period should be used to detect the start bit; there is an undetected period of 32 clock cycles at the end for both cases (between clock cycles 200–368 when the RSTx pin is low, and the first 368 clock cycles after the RSTx pin is high).

Bit 3: Parity Error (PE). This status bit indicates when the transmit or receive parity error count has been exceeded. For protocol T = 0, the PEC2–PEC0 bits define the allowable number of transmit or receive parity errors. For protocol T = 1, any parity error results in the setting of the PE bit. When the PE bit is set, $\overline{INT}$ is asserted. For protocol T = 0, characters received with the incorrect parity are not stored in the receive FIFO. For protocol T = 1, received characters with parity errors are stored to the receive FIFO regardless of the parity bit. The PE bit is set at 10.5 ETU in reception mode and at 11.5 ETU in transmit mode for T = 0 and T = 1 (PE bit is not applicable for transmit for T = 1).

Bit 2: Overrun FIFO (OVR). This status bit is set to 1 if the UART receives a new character when the receive FIFO is full. When a FIFO overrun condition occurs, the new character received is lost and the previous FIFO content remains undisturbed. When the OVR status bit is set, $\overline{INT}$ is asserted. The OVR bit is set at 10.5 ETU in receive mode for T = 0 and T = 1.

Bit 1: Framing Error (FER). This status bit is set to 1 if the I/O line is not in the high state at time = 10.25 ETU after the start bit. The FER bit is set to 10.5 ETU in receive mode for T = 0 and T = 1.

Bit 0: Transmit Buffer Empty/Receive Buffer Full (TBE/RBF). This is a duplicate of the same status bit contained in the Mixed Status Register (MSR).

Hardware Status Register (HSR)

	7	6	5	4	3	2	1	0
Address 0Fh	—	PRTLB	PRTLA	SUPL	PRLB	PRLA	INTAUXL	PTL
	R-0	R-0	R-0	R-1	R-0	R-0	R-0	R-0

R = unrestricted read, W = unrestricted write, -n = value after reset, x = always reflects state of external device pin. This register is reset to 0uuuxxxub on $\overline{RIU}$ = 0.

***Note:** A minimum of 2µs is needed between successive reads of the HSR to allow for hardware updates. In addition, a minimum of 2µs is needed between reads of the HSR and activation of card A, card B, or the AUX card.*

Bit 7: Reserved.

Bit 6: Protection Card Interface B Status Bit (PRTLB). This bit is set to 1 when a fault has been detected on card reader interface B. A fault is defined as detection of a short-circuit condition on either the RSTB or V_{CCB} pin as given by DC specs $I_{RST(SD)}$ and $I_{CC(SD)}$. The $\overline{INT}$ signal is asserted at logic 0 (active) while this bit is set. This bit returns to 0 after any HSR read, unless the condition persists.

Bit 5: Protection Card Interface A Status Bit (PRTLA). This bit is set to a 1 when a fault has been detected on card reader interface A. A fault is defined as detection of a short-circuit condition on either the RSTA or V_{CCA} pin as given by DC specs $I_{RST(SD)}$ and $I_{CC(SD)}$. The $\overline{INT}$ signal is asserted at logic 0 (active) while this bit is set. This bit returns to 0 after any HSR read, unless the condition persists.

Bit 4: Supervisor Latch (SUPL). This bit is set to 1 when $V_{DD} < V_{RST}$ or when a reset is caused by externally driving the DELAY pin < 1.25V. At this time the $\overline{INT}$ signal is asserted at logic 0 (active). This bit returns to 0 only after an HSR read outside the alarm pulse.

Bit 3: Presence Latch B (PRLB). This bit is set to 1 when a level change has been detected on the PRESB pin of card interface B. The $\overline{INT}$ signal is asserted at logic 0 (active) while this bit is set. This bit returns to 0 after any HSR read.

Bit 2: Presence Latch A (PRLA). This bit is set to 1 when a level change has been detected on the PRESA pin of card interface A. The $\overline{INT}$ signal is asserted at logic 0 (active) while this bit is set. This bit returns to 0 after any HSR read.

Bit 1: INTAUX Latch (INTAUXL). This bit is set to 1 when a 0 → 1 or a 1 → 0 level change has been detected on the INTAUX pin. This bit remains set, regardless of further level changes on the INTAUX pin until cleared to 0 by any HSR read.

Bit 0: Protection Thermal Latch (PTL). This bit is set to 1 when excessive heating (approximately +150°C or greater) is detected. The $\overline{INT}$ signal is asserted at logic 0 (active) while this bit is set. This bit returns to 0 after any HSR read, unless the condition persists.

Multiprotocol Dual Smart Card Interface

Card Interface Voltage Regulation and Step-Up Converter Operation

The V_{DD} and V_{DDA} pins supply power to the DS8007A. Voltage supervisor circuitry detects the input voltage levels and automatically engages a step-up converter if necessary to generate the appropriate voltages to the card interfaces according to the control register settings. The conversion process is transparent to the user and is usually only noticed by changes in the V_{UP} pin voltage, which reflects the operation of the internal charge pump. Table 2 elaborates on the V_{UP} pin.

The V_{DD} and V_{DDA} pins must be decoupled externally, but extra care must be taken to decouple large current spikes that can occur on the V_{DDA} pins because of noise generated by the cards and internal voltage step-up circuitry.

Voltage Supply Supervision

The voltage supervisor circuitry monitors V_{DD} and holds the device in reset until V_{DD} is at a satisfactory level. The DELAY pin is an external indicator of the state of internal power and can also be driven externally to hold the device in a reset state. An external capacitor is usually attached to this pin, defining the time constant of a power-on delay for the DS8007A. When V_{DD} is below the voltage threshold V_{RST}, the charging path that exists between V_{DD} and DELAY is disconnected and a strong pulldown is enabled on the DELAY pin. Once V_{DD} exceeds V_{RST}, the strong pulldown on the DELAY pin is released and the pullup to V_{DD} is enabled, allowing the external DELAY capacitor to be charged.

The RSTOUT alarm pin is released (allowing it to be pulled up externally) whenever the DELAY pin voltage is less than V_{DRST}, whether caused by $V_{DD} < V_{RST}$ or as a result of external hardware pulling the DELAY pin low. The minimum duration of the RSTOUT pulse (t_W specification) is defined by the capacitor connected to the DELAY pin and is typically 1ms per 2nF. The RSTOUT pin is driven strongly low once the DELAY pin exceeds the V_{DRST} voltage threshold.

The SUPL bit is set on initial power-up and is reset again when the RSTOUT alarm pulse occurs. The SUPL bit may only be cleared by a read of the HSR register. Figure 8 illustrates the sequencing of the various signals involved.

Short-circuit and thermal-protection circuitry prevent damages done by accidentally shorting the V_{CCx} pins or when the ambient temperature is exceeding the maximum operating temperature. When the internal temperature is approximately +150°C, the voltage V_{CCx} and the drivers to the CLKx, RSTx, I/Ox, C4x, and C8x signals to both card interfaces are turned off. The PTL bit in the HSR is set and an interrupt is generated.

When a short is detected on the RSTx pin, the device initiates a normal deactivation sequence. A short on I/Ox, C4x, and C8x does not cause deactivation.

Table 2. Step-Up Converter Operation

VOLTAGE (V)		
V_{DDA}	SMART CARD	V_{UP}
< 2.4	X	V_{DDA}
2.4–3.5	5	5.7
3.5–5.5	5	5.7
5.5–6.0	5	V_{DDA}
2.4–3.5	3.0	4.1
> 3.5	3.0	V_{DDA}
2.4–6.0	1.8	V_{DDA}

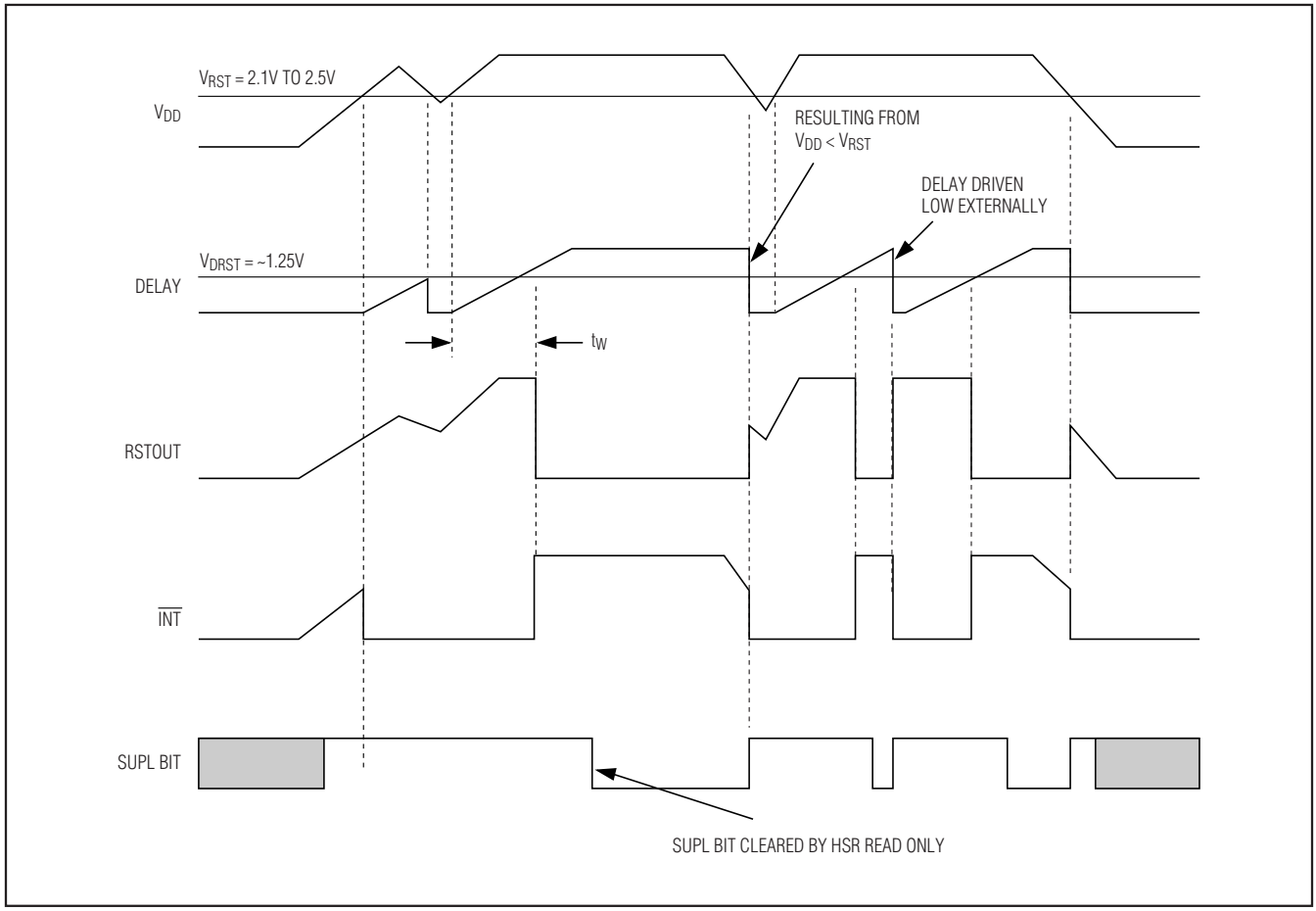


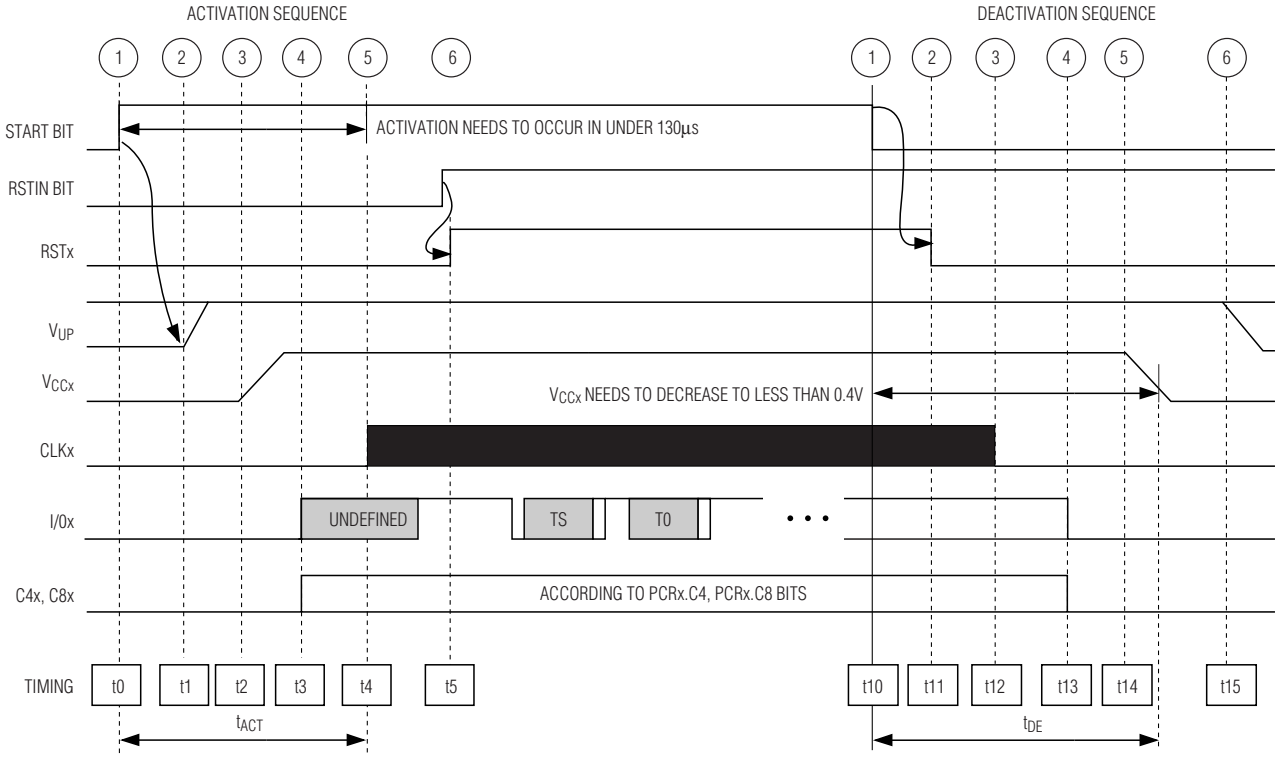
Figure 8. Voltage Supervisor

Multiprotocol Dual Smart Card Interface

Activation Sequencing

An activation sequence can only be requested by a host device through the parallel bus interface. The host can request an activation sequence for a specific card (card A or card B) by setting the START bit of the PCRx register (where x = A or B as determined by the card select SCx bits of the CSR). The host software can activate both cards at the same time, but only one card can be selected to transmit/receive at a given time. The activation sequence can only occur given satisfactory operating conditions (e.g., the card is present and the supply voltage is correct). These conditions can be ascertained through the HSR, MSR, and CSR bits.

If the microcontroller attempts to write the PCRx.START bit to 1 without having satisfied the necessary conditions, the card is not activated and the bit does not change. The activation time (from the assertion of the START bit until the clock output is enabled) is less than 130µs. The activation sequence is detailed in Figure 9.



ACTIVATION SEQUENCE
1. PCRx.START BIT IS SET BY SOFTWARE.
   CONDITIONS NEEDED (IN HARDWARE) ARE:
   MSR.PRx = 1 (CARD x PRESENT)
   HSR.PRTLx, SUPL, PRLx, PTL = 0
2. STEP-UP CONVERTER ACTIVATED (MAY ALREADY BE ON IF ANOTHER CARD WAS ACTIVE).
3. V_{CCx} ENABLED TO 1.8V, 3V, OR 5V AS SELECTED BY PCRx.1V8 AND PCR.3V/5V BITS.
   V_{CCx} RISES FROM 0V TO 1.8V, 3V, OR 5V WITH A CONTROLLED RISE TIME OF 0.17V/µs TYPICAL.
4. I/Ox IS PULLED HIGH. C4x, C8x ARE ALSO PULLED HIGH IF PCRx.C4 = 1, PCRx.C8 = 1 (RESPECTIVELY). THESE PINS HAVE INTEGRATED PULLUPS (14kΩ FOR I/Ox AND 10kΩ FOR C4x AND C8x) TO V_{CCx}.
5. CLKx OUTPUT IS ENABLED AND RST OUTPUT IS ENABLED. (PCRx.RSTIN SHOULD BE "0" FOR ACTIVE-LOW RSTx.)
6. PCRx.RSTIN WRITTEN TO "1" BY SOFTWARE AFTER USING TOC TO TIME SUFFICIENT DURATION OF RSTx PIN ASSERTION.

DEACTIVATION SEQUENCE
1. PCRx.START BIT IS CLEARED BY SOFTWARE.
2. THE ACTIVE-LOW RSTx SIGNAL IS ASSERTED BY SOFTWARE.
3. THE CLKx SIGNAL IS STOPPED.
4. I/Ox, C4x, AND C8x FALL TO 0V.
5. V_{CCx} IS DISABLED AND FALLS TO 0V WITH A TYPICAL RATE OF 0.17V/µs.
6. STEP-UP CONVERTER IS DEACTIVATED IF NOT IN USE BY ANOTHER CARD AND PINS CLKx, RSTx, I/Ox, AND V_{CCx} BECOME LOW IMPEDANCE TO GROUND.

Figure 9. Card Activation, Deactivation Sequences

Deactivation Sequencing

The host device can request a deactivation sequence by resetting the START bit to 0 for the desired card interface. The deactivation (from the deassertion of the START bit, step 1 of the deactivation sequence, to V_{CCx} decrease to less than 0.4V) is less than 150µs.

Emergency Deactivation

An emergency deactivation occurs if unsatisfactory operating conditions are detected. An emergency deactivation occurs for all activated cards in response to a supply-voltage brownout condition (as reported by the HSR.SUPL bit) or chip overheating (as reported by HSR.PTL). Emergency deactivation of an individual card can occur if a short-circuit condition is detected on the associated V_{CCx} or RSTx pin (as reported by HSR.PRTLx) or in the case of a card takeoff (as reported by HSR.PRLx). When an emergency deactivation occurs, hardware automatically forces the associated START bit(s) to the 0 state. The response of the device to the emergency deactivation varies according to the source.

If the RSTx pin is shorted or the device overheats, the sequencer executes a fast emergency deactivation sequence, which ramps down V_{CCX} immediately.

If the V_{CCX} pin was shorted, the sequencer executes a deactivation sequence in same way as if the START bit was cleared to 0.

Interrupt Generation

The $\overline{INT}$ output pin signals the host device that an event occurred that may require attention. The assertion of the $\overline{INT}$ pin is a function of the following sources:

- A fault has been detected on card interfaces (A or B).
- V_{DD} has dropped below the acceptable level.
- A reset is caused by externally driving the DELAY pin to less than 1.25V.
- Excessive heating is detected (i.e., PTL = 1).
- A level change has been detected on pin PRESx or INTAUX for the card interfaces (A, B, or AUX).
- The parity and/or frame error is detected.
- The early answer (EA) bit is set during ATR.
- The timeout counter(s) reach their terminal count(s).
- The FIFO full status is reached.
- The FIFO overrun occurs.
- The transmit buffer is empty.

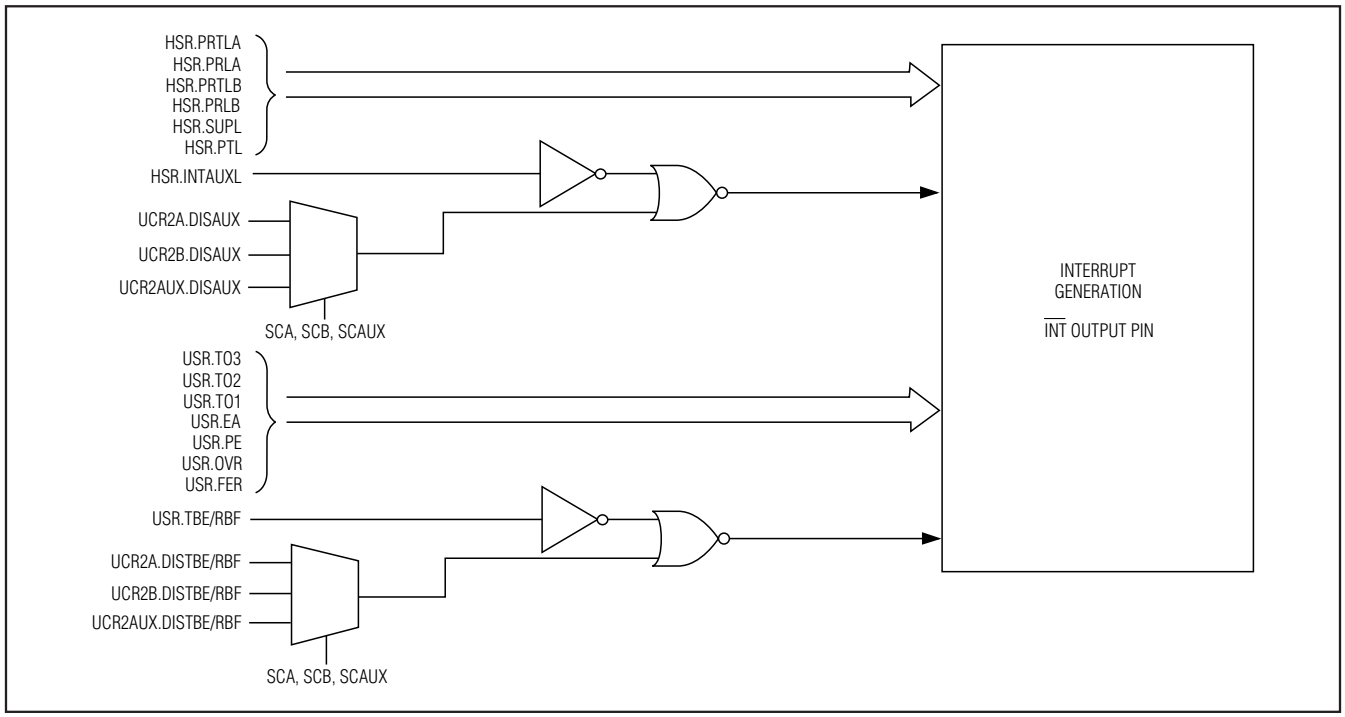


Figure 10. Interrupt Sources

Multiprotocol Dual Smart Card Interface

Timeout Counter Operation

The timeout counter assists the host device in timing real-time events associated with the communication protocols: the Work Wait Time (WWT), Block Waiting Time (BWT), etc. The timeout counter registers count ETUs, so the input clock to the timeout counter is derived from the output of the programmable divided clock (per card PDR register). The timeout counter requires the card be powered and have an active clock.

The timeout counter can operate as a single 24-bit counter (TOR3–TOR1) or as separate 16-bit (TOR3–TOR2) and 8-bit (TOR1) counters. The timeout counters can be operated in either software mode or start bit mode. The software mode is supported for the 16-bit and 24-bit counters. The start-bit mode is supported for all counter widths (8 bit, 16 bit, and 24 bit). See Table 3.

Software Mode

In software mode, software configures the counter to a starting value (while stopped) and starts the down counter by writing the configuration value to the TOC register. When the terminal count is reached (0h), the counter stops, the timeout flag is set, and an interrupt is generated. If the software counter does not reach the terminal count, it must be stopped before loading a new value into the associated TORx counter registers.

It is possible to stop and start the 16-bit software counter while leaving the 8-bit counter enabled (e.g., TOC = 65h ↔ 05h, TOC = E5h ↔ 85h, etc.).

If a compatible software mode command is written to the TOC register before the terminal count is reached (e.g., write 61h to TOC register while the 65h TOC command is running or vice versa), the new command is ignored (still software mode), but the TOC register is updated with the new command, and the counter continues to count until the terminal count is reached, the respective timeout flag(s) is set, and an interrupt is generated.

Start-Bit Mode

When configured to start-bit mode, counting starts (and restarts for the 16-bit and 24-bit counters) when a START bit is detected on the active card interface I/Ox pin. When the terminal count is reached, the 8-bit autoreload counter begins counting from the previously programmed start value, while a 16-bit counter or 24-bit counter stops when terminal count is reached. If the terminal count is reached, the timeout flag is set and an interrupt is generated. The 8-bit autoreload TOR1 register cannot be modified during a count. The 16-bit and 24-bit counter registers can be modified during a count without affecting the current count. The new register data is used on the next START bit detection.

Table 3. Timeout Counter Configurations

TOC VALUE	TOR3	TOR2	TOR1	DESCRIPTION
00h	Stopped			All counters are stopped.
05h	Stopped		Start Bit/Autoreload	Counters 3 and 2 are stopped. Counter 1 continues in start-bit/autoreload mode for both transmission and reception.
61h	Software		Stopped	Counter 1 is stopped. Counters 3 and 2 form a 16-bit counter operating in software mode. The counter is stopped by writing 00h to the TOC register, and must be stopped before reloading new values in TOR3 and TOR2 registers.
65h	Software		Start Bit/Autoreload	Counters 3 and 2 form a 16-bit counter operating in software mode. Writing 05h to the TOC register before reloading new values in TOR2/TOR3 stops the counters. Counter 1 is operated in start-bit/autoreload mode. The TOR1 register may not change during the count. The 16-bit counters are stopped by setting TOC = 05h. Both counters are stopped by setting TOC = 00h.
68h	Software			Counters 1, 2, and 3 form a 24-bit counter operating in software mode. The counter starts after the command is written to the TOC register, and is stopped by setting TOC = 00h. TOR3, TOR2, TOR1 cannot be changed without stopping the counter first.

Table 3. Timeout Counter Configurations (continued)

TOC VALUE	TOR3	TOR2	TOR1	DESCRIPTION
71h	Start Bit		Stopped	Counter 1 is stopped. Counters 3 and 2 form a 16-bit counter operating in start bit mode for both transmission and reception. TOR3 and TOR2 registers can be changed during the count, the current count is not affected, and the values are taken into account at the next START bit detected on the I/Ox pin. Setting TOC = 00h stops the counters.
75h	Start Bit		Start Bit/Autoreload	Counter 1 is an 8-bit counter in start-bit/autoreload mode for both transmission and reception; counters 3 and 2 form a 16-bit counter operating in start-bit mode for both transmission and reception. The TOR1 register is not allowed to change during the count. TOR3, TOR2 registers can be changed during the count, the current count is not affected, and the values are taken into account at the next START bit detected on the I/Ox pin. Setting TOC = 00h stops the counters.
7Ch	Start Bit			Counters 1/2/3 form a 24-bit counter operating in start-bit mode in both transmission and reception. TOR3, TOR2 and TOR1 registers can be changed during the count, the current count is not affected, and the value is taken into account at the next START bit detected on the I/Ox pin. Setting TOC = 00h stops the counter.
85h	Stopped		Start Bit/Autostop (RCV); Start Bit/Autoreload (XMT)	Counters 3 and 2 are stopped. Counter 1 is operated in start-bit/autostop mode in reception and is stopped at the end of the 12th ETU following the first received START bit detected on the I/Ox pin unless the terminal count is reached first. Counter 1 operates in start-bit/autoreload mode in transmission.
E5h	Software		Start Bit/Autostop (RCV); Start Bit/Autoreload (XMT)	Counters 3 and 2 form a 16-bit counter operating in software mode. The counters are stopped by setting TOC = 05h before reloading new values in TOR3 and TOR2 registers. Counter 1 is operated in autostop mode in reception and is stopped at the end of the 12th ETU following the first received START bit detected on the I/Ox pin unless the terminal count is reached first. Counter 1 is operated in start-bit/autoreload mode in transmission.
F1h	Start Bit/Autostop (RCV); Start Bit (XMT)		Stopped	Counter 1 is stopped. Counters 3 and 2 form a 16-bit counter. The 16-bit counter is operated in start-bit/auto-stop mode in reception and is stopped at the end of the 12th ETU following the first received START bit detected on the I/Ox pin unless the terminal count is reached first; and the 16-bit counter is operated in start-bit mode in transmission.
F5h	Start Bit/Autostop (RCV); Start Bit (XMT)		Start Bit/Autostop (RCV); Start Bit/Autoreload (XMT)	Counter 1 is an 8-bit counter operating in start-bit/autostop mode in reception and is stopped at the end of the 12th ETU following the first received START bit detected on the I/Ox pin unless the terminal count is reached first; and the 8-bit counter is operated in start-bit/autoreload mode in transmission. Counters 3 and 2 form a 16-bit counter operating in start-bit mode for transmission but operate in start-bit/autostop mode in reception. Counters 3 and 2 are stopped at the end of the 12th ETU following the first received START bit detected on the I/Ox pin unless the terminal count is reached first; the counters are stopped by setting TOC = 00h.

Multiprotocol Dual Smart Card Interface

ISO UART Implementation

Reset Operation

The HSR.RIU control bit resets the ISO UART. The HSR.RIU must be reset prior to any activation. HSR.RIU must be returned to 1 by software before any UART action can take place.

Synchronous Mode

The synchronous mode of operation is invoked by setting the synchronous/asynchronous card select bit (for a given card interface) to logic 1. In the synchronous mode of operation, the associated I/Ox card interface data is transferred by the LSb of the UART transmit/receive registers (UTR and URR). In this mode, the host device using the CCRx.SC register bit manually controls the CLKx pin for the selected card interface.

Switching to the synchronous mode or vice versa is allowed at any time when the card is active. However, it is the responsibility of the host software/firmware to ensure that the current transmission is concluded before switching. If software configures an active card for synchronous mode, and then activates another card, the I/O pin on the previously active card goes to a high-impedance state with a weak pullup (high). The newly selected interface (if configured to synchronous mode) takes on UTR.0.

The AUX card interface does not have an associated CLK signal, so the CCRAUX.SC bit does not control an output signal when the synchronous mode of operation is in effect. The handshake between the host and the auxiliary smart card interface is accomplished through the auxiliary interrupt input (INTAUX) and the $\overline{INT}$ pins. The MSR.INTAUX bit reflects the state of the INTAUX pin. If the UCR2.DISAUX bit is cleared to 0, a change on the INTAUX input pin results in the assertion of $\overline{INT}$ output pin. The host software/firmware establishes the communication protocol and controls when to transmit/receive data in response to the interrupt. If the UCR2.DISAUX bit is set to 1, the $\overline{INT}$ pin is not asserted, and the host software/firmware must examine the INTAUX bit in the MSR register and responds accordingly.

Asynchronous Mode

The asynchronous mode of operation is the reset default mode for all card interfaces and is selected when the synchronous/asynchronous card select bit (for a given card interface) is configured to logic 0. The I/Ox card interface signal is used for asynchronous half-duplex data communication between the host-controlled ISO UART and the external smart card. The host device can optionally stop the CLKx signal in the high or low state while the card is active using the CCRx.CST and CCRx.SHL register bits.

ETU Generation and Timing

The basic unit of time for asynchronous mode communication on the I/Ox signal is the elementary time unit (ETU). The ETU is defined within the ISO UART as a function of the f_{CLK} frequency that is configured for the card interface (i.e., the same f_{CLK} that can be sourced to the CLKx pin of an associated card interface A or B). In addition to receiving f_{CLK} from the clock generation block, the ISO UART additionally receives a 2 x f_{CLK} frequency if CCRx.AC2–AC0 ≠ 000b. The host device can select whether f_{CLK} or 2 x f_{CLK} is used for ETU generation by using the clock UART (CKU) select bit. When CKU = 0, f_{CLK} is used, while 2 x f_{CLK} is used when CKU = 1. One exception exists when CCRx.AC2–AC0 = 000b, in which case, only f_{CLK} is sourced to the UART and the CKU bit setting has no effect on the duration of an ETU.

The basic clock that is selected for ETU generation by the CKU bit is further prescaled by a factor or 31 or 32. The prescaler select control (PSC) bit makes this prescaler selection. When PSC is configured to logic 0, the prescale setting is 31. When PSC is configured to logic 1, the prescale setting is 32. The output of the clock prescaler drives an 8-bit autoreload down counter. The autoreload value for the downcounter is configured by the host device through the Programmable Divider Register (PDR). The interval provided by this downcounter defines the ETU duration for the selected card. Figure 11 shows a diagram of ETU generation. All the asynchronous character transmit/receive operations are defined in terms of ETU (e.g., 10.5 ETU, 10.25 ETU, etc).

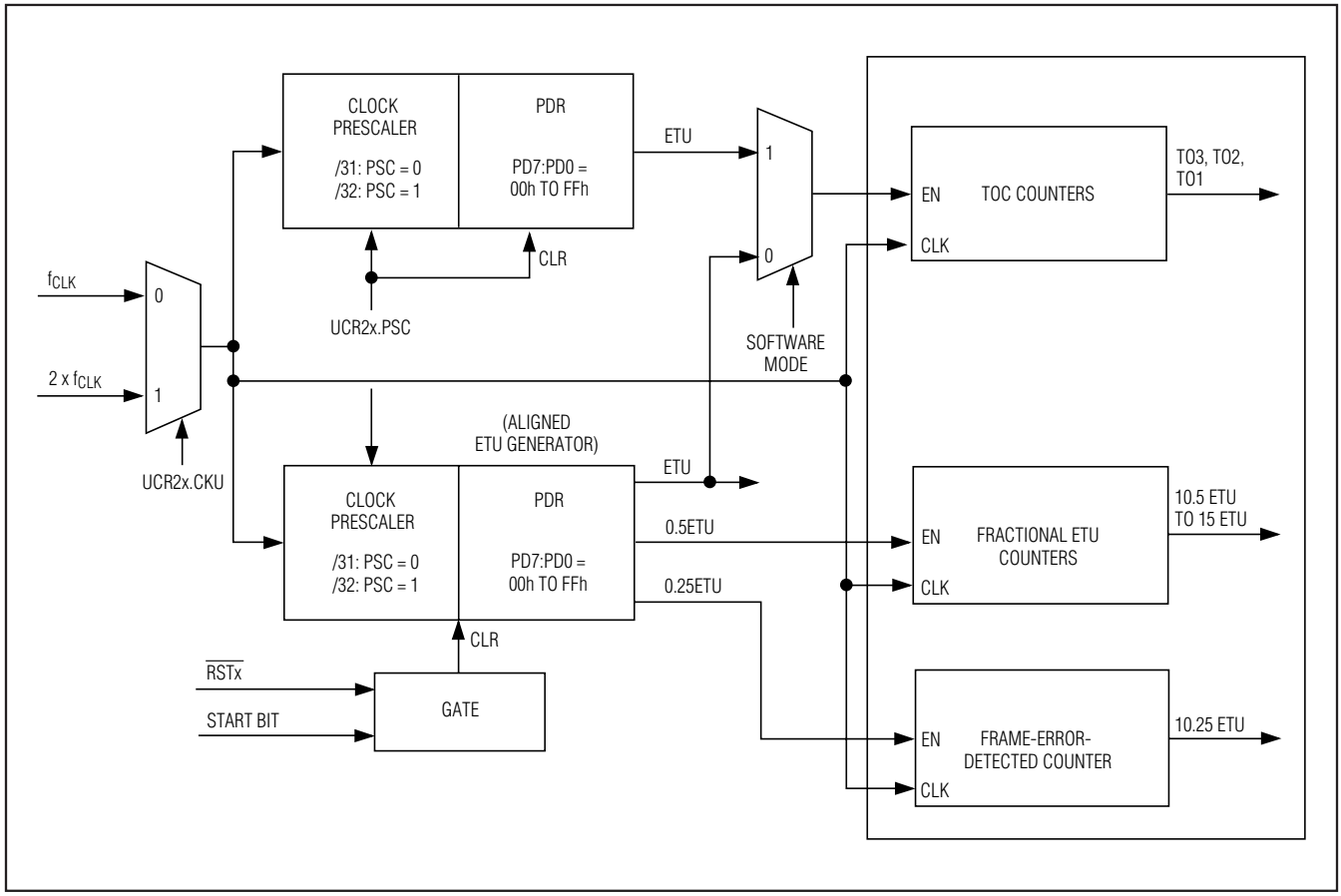


Figure 11. ETU Generation

Standard Clock Frequencies and Baud Rates

The DS8007A supports I/O communication and CLKx frequency generation compliant to the following standards: ISO 7816, EMV2000, and GSM11-11. Each of these standards has an allowable CLKx frequency range and a defined relationship between CLKx frequency and ETU (baud rate) generation that is supported initially and after negotiation.

For ISO 7816, the relationship between ETU (baud rate) timing and CLKx frequency is as follows:

$$ETU = (F / D) \times (1 / f_{CLKX})$$

The minimum CLKx frequency is fixed at 1MHz. The default maximum CLKx frequency is 5MHz, however the maximum CLKx frequency can be increased according to the Fi parameter given by the card during ATR. The ISO 7816-1997(3) specification recommends in Section 4.3.4 that CLKx frequency switches be made a) immediately after ATR or b) immediately after a successful PPS exchange. The transmission parameters F and D are respectively the clock-rate conversion and baud-rate adjustment factors. The notations Fd and Dd are used to represent the 'd'efault values for these parameters, which are Fd = 372 and Dd = 1. The notation Fi and Di are used to represent the values 'i'ndicated by the card within the TA(1) character of ATR. If TA(1) is not present, then Fi,Di are set to the default Fd,Dd values. The notation Fn and Dn represent values 'n'egotiated during a successful PPS exchange, which should be in the range Fd-Fi and Dd-Di, respectively. During ATR, the default Fd, Dd values shall apply. If the card comes up in negotiable mode (i.e., TA(2) is absent from the ATR), then the Fd, Dd parameters con-

tinue to be used until a successful PPS exchange is completed. The negotiated Fn, Dn values are then used after a successful PPS exchange. If the card comes up in specific mode (i.e., TA(2) is present in ATR), then the indicated Fi, Di values apply immediately after successful ATR if bit 5 of the TA(2) character is 0. If bit 5 of TA(2) is 1, implicit values should be used. The TA(1) character of ATR, if present, contains the Fi and Di values indicated by the card.

Table 5 demonstrates how the prescaler (PSC) bit and programmable divider register (PDRx) can be configured to generate the requested F/D ratios. All settings assume that the CKU bit is configured to its reset default logic 0 state.

Table 4. Fi, Di Parameter Possibilities

TA(1).FI	Fi	MAX CLKx (MHz)	Fi =	TA(1).DI	Di
0000	372	4	31 x 12	0000	RFU
0001	372	5	31 x 12	0001	1
0010	558	6	31 x 18	0010	2
0011	744	8	31 x 24	0011	4
0100	1116	12	31 x 36	0100	8
0101	1488	16	31 x 48	0101	16
0110	1860	20	31 x 60	0110	32
0111	RFU	—	—	0111	RFU
1000	RFU	—	—	1000	RFU
1001	512	5	32 x 16	1001	12
1010	768	7.5	32 x 24	1010	20
1011	1024	10	32 x 32	1011	RFU
1100	1536	15	32 x 48	1100	RFU
1101	2048	20	32 x 64	1101	RFU
1110	RFU	RFU	—	1110	RFU
1111	RFU	RFU	—	1111	RFU

RFU = Reserved for future use.

Table 5. PSC, PDR Settings to Support F,D Parameters

TA(1).Fi	PSC 0 = /31 1 = /32	PDR SETTING FOR Di =							
		0001	0010	0011	0100	0101	0110	1000	1001
0000	0	12	6	3	—	—	—	1	—
0001	0	12	6	3	—	—	—	1	—
0010	0	18	9	—	—	—	—	—	—
0011	0	24	12	6	3	—	—	2	—
0100	0	36	18	9	—	—	—	3	—
0101	0	48	24	12	6	3	—	4	—
0110	0	60	30	15	—	—	—	5	3
1001	1	16	8	4	2	1	—	—	—
1010	1	24	12	6	3	—	—	2	—
1011	1	32	16	8	4	2	1	—	—
1100	1	48	24	12	6	3	—	4	—
1101	1	64	32	16	8	4	2	—	—

Character Encoding/ Decoding Convention

The ISO UART is designed to support two possible character encoding/decoding formats: direct and inverted. The direct character coding convention transmits and receives data LSb first and associates a high logic level with a bit 1 and a low logic level with a bit 0. The inverse character coding convention transmits and receives data most significant bit first and associates a high logic level with a bit 0 and a low logic level with a bit 1.

The UCR1.CONV bit defines which character convention (CONV = 0:inverse; CONV = 1:direct) should be used by the ISO UART. The UCR1.CONV bit can be configured by the host device software or be configured by hardware if automatic convention detection has been enabled.

Automatic Convention Detection

The automatic convention detection relies upon recognition of a predefined pattern in the first character received (TS character) in ATR for establishing future character coding convention. To enable automatic convention detection, the UCR1.SS bit must be set to logic 1 and the UCR2.$\overline{\text{AUTOC}}$ bit should be configured to logic 0 prior to ATR. The SS bit is automatically cleared by hardware 10.5 ETU after the character is received. If automatic convention detection is enabled and an unrecognized character is received, the CONV bit is not written. If neither the direct nor inverse character are detected, a parity error occurs along with error signal generation for the T = 0 protocol. The $\overline{\text{AUTOC}}$ bit should not be modified during a card session.

Framing Error Detection

The DS8007A monitors the selected card I/Ox signal at 10.25 ETU following each detected start bit. If the I/Ox signal is not in the high state at this point in time, the USR.FER (framing error) bit is set to 1 at 10.5 ETU. The FER bit is cleared to 0 whenever USR is read.

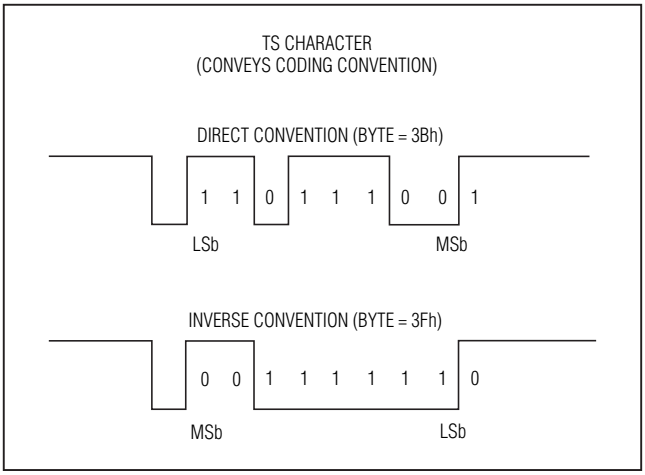


Figure 12. Direct, Inverse Character Coding Conventions

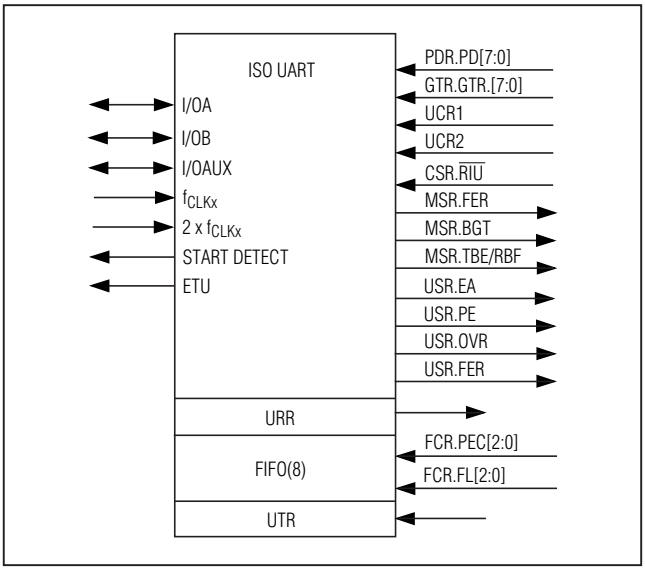


Figure 13. ISO UART Signal Interface

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Block Guard Time

The block guard time for the asynchronous serial communication between the smart card reader (DS8007A) and the ICC is defined as the minimum delay between consecutive start bits sent in the opposite direction. The DS8007A implements an internal ETU counter specifically to help the host device assess that this minimum block guard time is being met. This internal ETU counter is loaded on each start bit with the value 22d or 16d, dependent upon the protocol selected. For T = 0, the counter is loaded with the value 16d and for T = 1, the counter is loaded with the value 22d. If the counter reaches 0, the MSR.BGT status bit is set and the counter stops. If a start bit is detected before the counter reaches 0, the counter is reloaded and the BGT status bit is cleared to 0.

Transmit Mode

The ISO UART transmit mode is invoked by setting the associated UCR1.T/R bit to logic 1. When the ISO UART is placed into transmit mode, the TBE/RBF bit is set to 1 to indicate that the transmit buffer is empty. When a character is written to UTR register, the TBE/RBF bit is cleared to indicate that the transmit buffer is no longer empty. If the transmit serial shift register is available (which is the case unless character retransmission is occurring), the character is translated according to the character coding convention (CONV bit) and moved from the transmit buffer to the serial shift register. The TBE/RBF bit returns high so that another character can be loaded into the UTR register.

Guard Time

Some smart cards require extra time to handle information received from an interface device. To allow this extra time, the DS8007A implements a Guard Time Register (GTR) per card interface. This register is programmed with the number of extra ETU that should be enforced between consecutive start bits transmitted by the DS8007A (discounting retransmissions at the request of the ICC). The GTR register defaults to 00h on reset, indicating that no extra guard time is required (i.e., 12 ETU must be enforced between transmission of consecutive start bits). If the GTR register is programmed to FFh, the delay required between consecutive start bits is dependent upon the protocol selected (per UCR1.PROT).

GTR = FFh

T = 0 protocol: 11.8 ETU

T = 1 protocol: 10.8 ETU

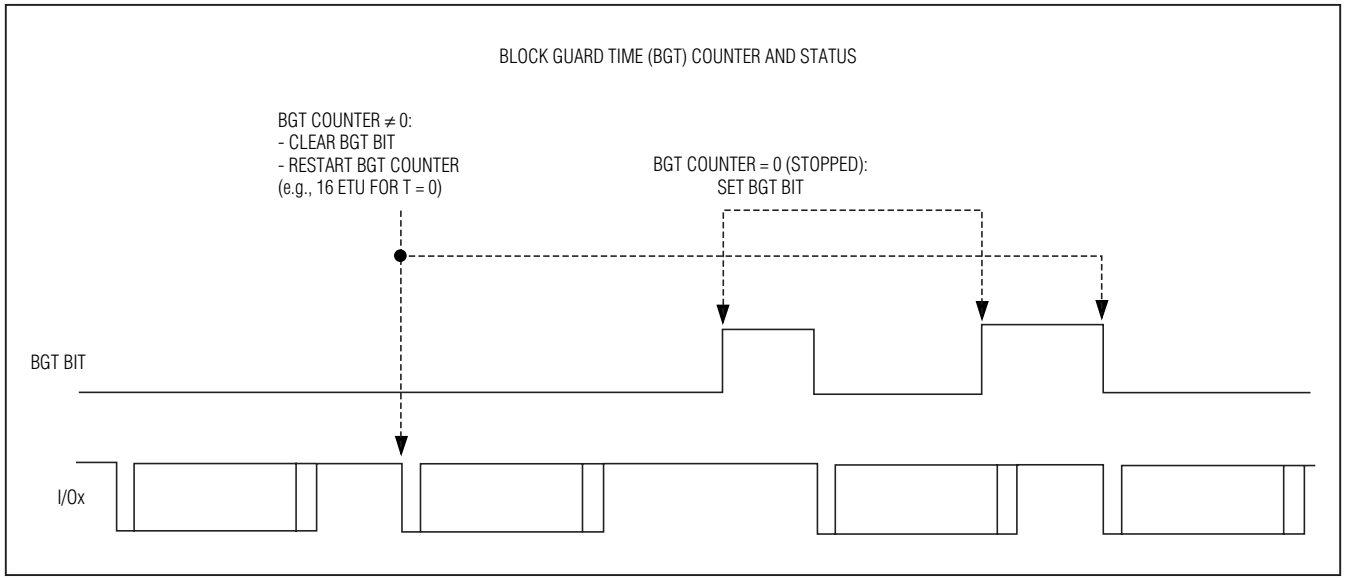


Figure 14. Block Guard Time ETU Counter Operation

Last Character to Transmit

The ISO UART implements a special control input that allows an automatic switch from transmit mode (UCR1.T/R = 1) to receive mode (UCR1.T/R = 0) upon successful character transmission. The last character to transmit (UCR1.LCT) bit must be set to 1 by host software prior to writing the last character for transmission to UTR. Upon successful transmission of the character, the UCR1.T/R bit and the LCT bit are cleared by hardware. When the LCT bit is used, the TBE/RBF bit is not set at the end of the transmission.

Receive Mode

The ISO UART receive mode is in effect if the associated UCR1.T/R bit is 0. When the ISO UART is changed to receive mode, the MSR.FE bit is set to 1 to indicate that the receive FIFO is empty. When at least one unread receive character exists in the FIFO, the FE bit is cleared. When the FIFO, with depth defined by FL2–FL0, is full, the TBE/RBF bit is set to 1 to indicate that the receive buffer is full. Once a character is read from a full FIFO, the RBF/TBE bit is cleared to indicate that the FIFO is no longer full. The controller ready (CRED) bit should be polled to assess data readiness when reading from register URR at high frequencies.

Parity Check

The T = 1 protocol selection checks receive parity. For T = 1, the parity error count bits (PEC2–PEC0) have no function and the USR.PE bit are set on the first parity error.

The T = 0 protocol selection also checks receive parity, but allows setting of the USR.PE parity error bit to be based upon detection of 1–8 parity errors. The PEC2–PEC0 bits define the number of consecutive parity errors that should be detected before setting USR.PE.

The ISO UART implements a special control input that allows testing for inverse parity. If the UCR1.FIP bit is configured to 0 during receive mode, the ISO UART tests for correct parity on each received character. If UCR1.FIP is configured to 1, inverse parity is expected. This control can be useful in testing that the ICC properly detects error signals generated by the DS8007A and retransmits requested characters.

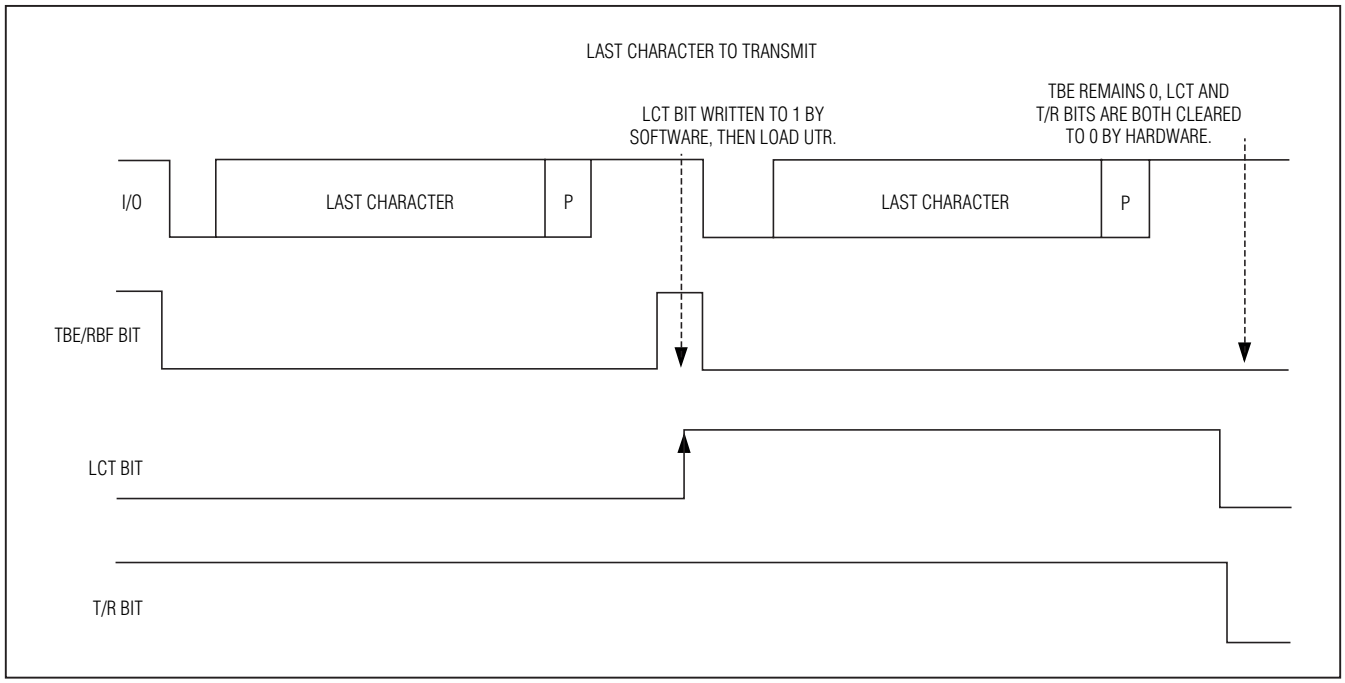


Figure 15. Last Character to Transmit

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Error-Signal Generation

The T=1 protocol does not support error-signal generation. When configured to receive using the T = 0 protocol (UCR1.PROT = 0), the DS8007A supports error-signal generation in response to parity. The parity error count bits (PEC2–PEC0) of the FIFO control register (FCR) determine the number of allowed repetitions in reception, and therefore the number of times that an error signal is generated in response to a received character with incorrect parity before the USR.PE bit becomes set.

When receiving a character, the DS8007A verifies even parity for the combination of the received 8-bit character and parity bit. If incorrect parity is determined and consecutive parity error counter has not reached terminal count (000b), the DS8007A generates an error signal on the I/Ox line starting at 10.5 ETU and lasting for 1.0 ETU. The parity error counter is initialized through the PEC2–PEC0 bits. Configure the PEC2–PEC0 bits to 000b means that no repetition in reception is allowed and that an error signal generation occurs in response to a character received with incorrect parity. Configuring PEC2–PEC0 bits to 001b means one repetition in reception is allowed and that the DS8007A generates an error signal only once per character receive attempt. When the consecutive parity error counter reaches 000b and a character is received with incorrect parity, the USR.PE bit is set to 1. If the parity error counter has not reached terminal count, it is reset to the originally programmed value upon reception of a character having the correct parity. Once the USR.PE bit signals a parity count error, the software must re-establish any nonzero PEC2–PEC0 setting.

Receive FIFO

The DS8007A implements an enhanced receive FIFO. If the FIFO threshold-enable bits FTE0 and FTE1 are set to 0, the FIFO functions as a standard FIFO that is configurable to a depth of 1 to 8 characters. The T = 0 and T = 1 protocols allow the FIFO depth to be determined by the FCR.FL2–FCR.FL0 bits. When configurable, the FIFO depth is equal to (FL2–FL0) + 1 (e.g., FL2–FL0 = 001b configures the FIFO depth to 2). The RBF/TBE and FE status bits report the full and empty FIFO conditions, respectively. If the receive FIFO is full (at a maximum depth of 8), the FIFO Overrun (OVR) bit is set to 1, the new character received is lost, and the previous FIFO contents remain undisturbed.

The received characters are read from the URR. When the receive FIFO is enabled, reads of the URR always access the oldest available received data. The FIFO is initialized every time the receive mode is invoked (i.e., T/R bit is cleared to 0).

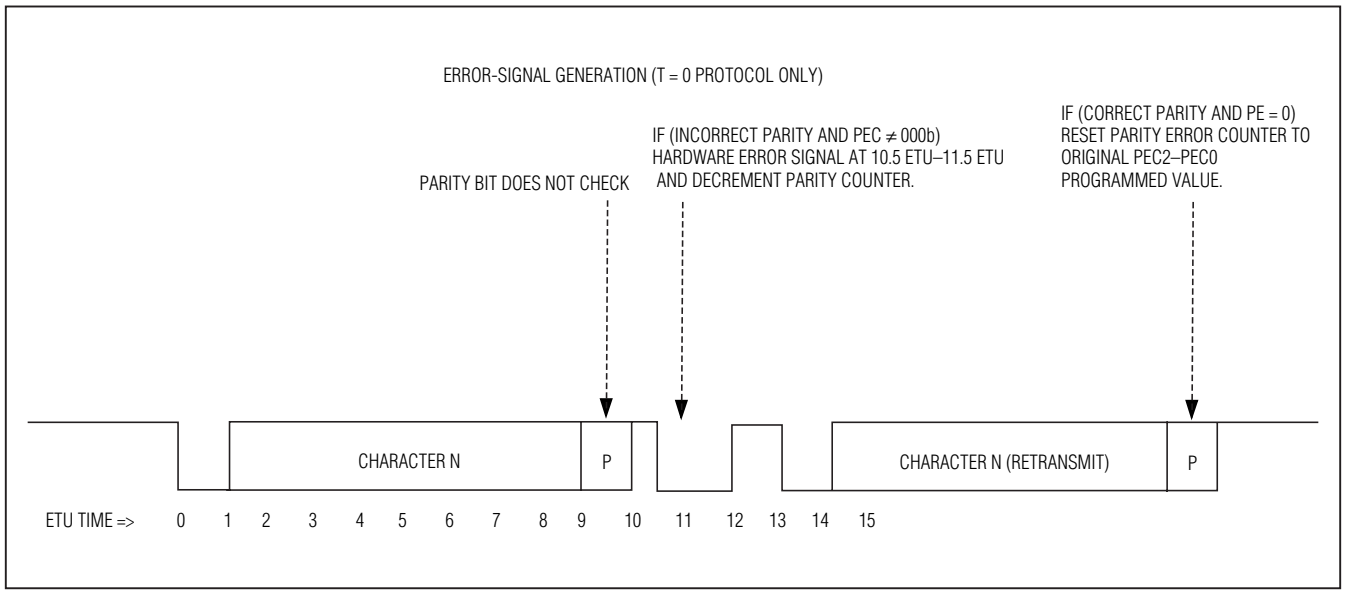


Figure 16. Receive Mode—Error Signal Generation

For the T = 0 protocol, only received characters without parity errors are stored in the receive FIFO. When UCR1.FIP = 1 during T = 0 reception, only those characters with incorrect parity are stored to the receive FIFO since the DS8007A is checking for inverse parity. For the T = 1 protocol, the receive character is stored to the FIFO no matter whether the parity checks correctly or not.

If the FIFO threshold enable bits FTE0 and FTE1 are set to 1, the FIFO implements a programmable threshold for the assertion of the RBF/TBE bits and the interrupt line. In this mode, the internal FIFO length is forced to 8 bytes, and FL[2:0] (the programmable FIFO length bits) determines the threshold value.

Characters are accumulated in the FIFO without setting the RBF/TBE bits until the FIFO depth is greater than the threshold value. As long as the used depth is greater than the FL[2:0] value, the RBF/TBE bits (USR and MSR) are set and the interrupt pin is asserted. Reading the FIFO to a level less than or equal to the threshold value resets the RBF/TBE bit and deasserts the interrupt line.

Writing a zero or eight into the FL bits while the programmable threshold mode is enabled causes the FIFO to behave as it does in nonprogrammable threshold mode.

If the programmable FIFO depth is at its maximum (8 characters) the RBF/TBE bit is set when the eighth character is received and written into the FIFO. If another character is received while the FIFO is full, the overflow (OVR) status is set, and the new character overwrites the previously received character.

If the programmable FIFO depth is set to zero, the receipt of a single character sets RBF/TBE. Receiving another character in this state sets the OVR bit and overwrites the character.

The FIFO empty status bit (FE) operates as before. The programmable threshold feature functions the same in T = 0 and T = 1 modes.

Early Answer (EA)

WHEN START BIT IS ASSERTED	EA BIT STATUS	CHARACTER RECEIVED
Between 0 and 200 clock cycles when RSTx = low	0	No
Between 200 and 368 clock cycles when RSTx = low	1	Yes
Between 368 and 400 clock cycles when RSTx = low	0	Yes
Within the first 368 clock cycles after RSTx = high	1	Yes
Between 368 and 4000 clock cycles after RSTx =	0	Yes

If a start bit is detected on the I/O line during the ATR between clock cycles 200–368 when the RSTx pin is low and during the first 368 clock cycles after the RSTx is high, it is recognized as an early answer (EA), and the EA bit is set in the USR.EA register. When the EA bit is set, $\overline{INT}$ is asserted.

During the early answer detection period, 46 clock cycles sampling periods should be used to detect the start bit and there is an undetected (uncertainty) period of 32 clock cycles at the end for both cases (between clock cycles 200–368 when the RSTx pin is low, and the first 368 clock cycles after RSTx is high). Table 6 summarizes the status of the early answer bit. The answer on the I/O line begins between 400 and 40,000 clock cycles after the rising edge of the RSTx signal.

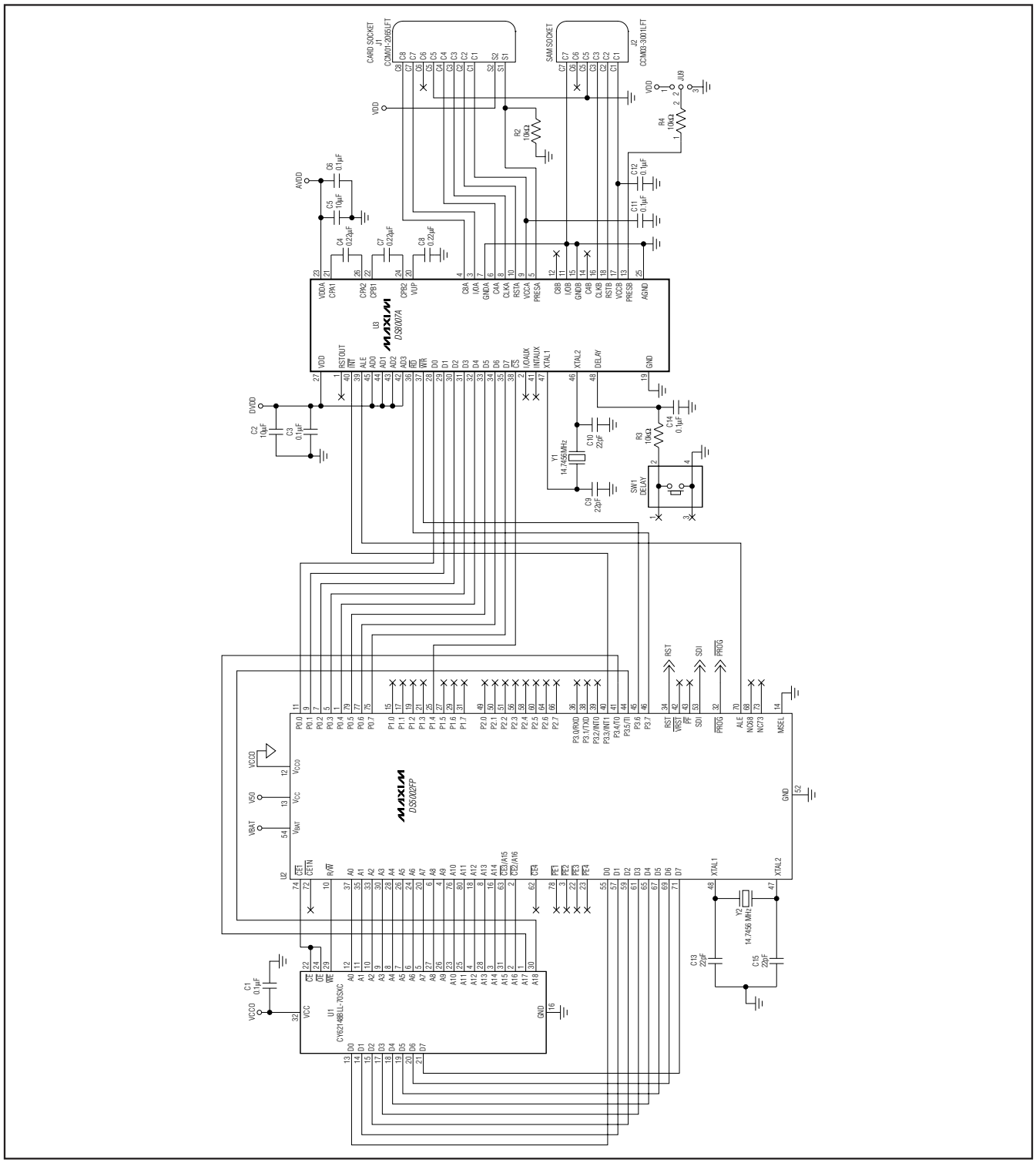
Development and Technical Support

The DS8007 evaluation kit (EV kit) is available to assist in the development of designs using the DS8007/DS8007A multiprotocol smart card interface. The EV kit can be purchased directly from Maxim.

For technical support, go to **https://support.maxim-ic.com/micro**.

Multiprotocol Dual Smart Card Interface

Typical Operating Circuit



MAXIM

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
48 LQFP	C48L+1	**21-0054**

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