MCP6H01/2/4

1.2 MHz, 16V Op Amps

Features:

- Input Offset Voltage: ±0.7 mV (typical)
- Quiescent Current: 135 µA (typical)
- Common Mode Rejection Ratio: 100 dB (typical)
- Power Supply Rejection Ratio: 102 dB (typical)
- Rail-to-Rail Output
- Supply Voltage Range:
  - Single-Supply Operation: 3.5V to 16V
  - Dual-Supply Operation: ±1.75V to ±8V
- Gain Bandwidth Product: 1.2 MHz (typical)
- Slew Rate: 0.8V/µs (typical)
- Unity Gain Stable
- Extended Temperature Range: -40°C to +125°C
- No Phase Reversal

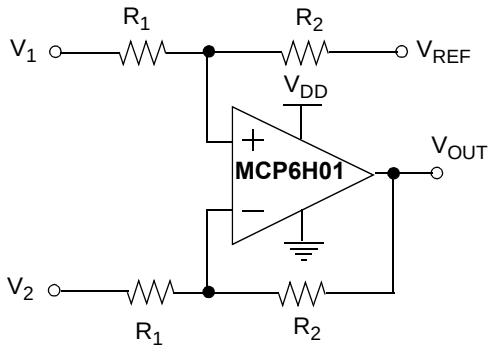
Applications:

- Automotive Power Electronics
- Industrial Control Equipment
- Battery Powered Systems
- Medical Diagnostic Instruments

Design Aids:

- SPICE Macro Models
- FilterLab® Software
- MAPS (Microchip Advanced Part Selector)
- Analog Demonstration and Evaluation Boards
- Application Notes

Typical Application



Difference Amplifier

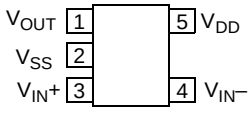
Description:

Microchip's MCP6H01/2/4 family of operational amplifiers (op amps) has a wide supply voltage range of 3.5V to 16V and rail-to-rail output operation. This family is unity gain stable and has a gain bandwidth product of 1.2 MHz (typical). These devices operate with a single-supply voltage as high as 16V, while only drawing 135 µA/amplifier (typical) of quiescent current.

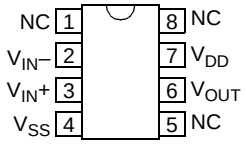
The MCP6H01/2/4 family is offered in single (MCP6H01), dual (MCP6H02) and quad (MCP6H04) configurations. All devices are fully specified in extended temperature range from -40°C to +125°C.

Package Types

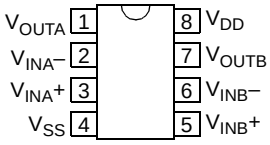
MCP6H01
SC70-5, SOT 23-5



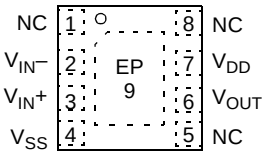
MCP6H01
SOIC



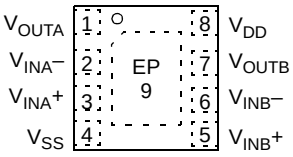
MCP6H02
SOIC



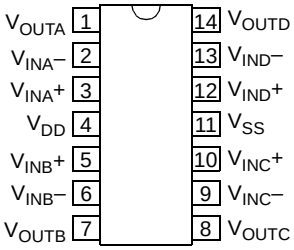
MCP6H01
2x3 TDFN



MCP6H02
2x3 TDFN



MCP6H04
SOIC, TSSOP



* Includes Exposed Thermal Pad (EP); see Table 3-1.

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NOTES:

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1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

$V_{DD} - V_{SS}$.....17V
Current at Input Pins.....±2 mA
Analog Inputs ($V_{IN}+$, $V_{IN}-$)††.....V_{SS} – 1.0V to V_{DD} + 1.0V
All Other Inputs and Outputs .....V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input Voltage.....$V_{DD} - V_{SS}$
Output Short-Circuit Current.....continuous
Current at Output and Supply Pins .....±65 mA
Storage Temperature.....-65°C to +150°C
Maximum Junction Temperature (T_J).....+150°C
ESD protection on all pins (HBM; MM).....≥ 2 kV; 200V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **4.1.2 "Input Voltage Limits".**

DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +3.5V to +16V, V_{SS} = GND, T_A = +25°C, $V_{CM} = V_{DD}/2 - 1.4V$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$ and R_L = 10 kΩ to V_L. (Refer to Figure 1-1).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-3.5	±0.7	+3.5	mV	
Input Offset Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	±2.5	—	µV/°C	T_A = -40°C to +125°C
Power Supply Rejection Ratio	PSRR	87	102	—	dB	
Input Bias Current and Impedance						
Input Bias Current	I_B	—	10	—	pA	
	I_B	—	600	—	pA	T_A = +85°C
	I_B	—	10	25	nA	T_A = +125°C
Input Offset Current	I_{OS}	—	±1	—	pA	
Common Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||6	—	Ω||pF	
Common Mode						
Common Mode Input Voltage Range	V_{CMR}	V_{SS} – 0.3	—	V_{DD} – 2.3	V	
Common Mode Rejection Ratio	CMRR	78	93	—	dB	V_{CM} = -0.3V to 1.2V, V_{DD} = 3.5V
		82	98	—	dB	V_{CM} = -0.3V to 2.7V, V_{DD} = 5V
		84	100	—	dB	V_{CM} = -0.3V to 12.7V, V_{DD} = 15V
Open-Loop Gain						
DC Open-Loop Gain (Large Signal)	A_{OL}	95	115	—	dB	0.2V < V_{OUT} <(V_{DD} – 0.2V)

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DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +3.5V to +16V, V_{SS} = GND, T_A = +25°C, $V_{CM} = V_{DD}/2 – 1.4V$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$ and R_L = 10 kΩ to V_L. (Refer to Figure 1-1).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Output						
High-Level Output Voltage	V_{OH}	3.490	3.495	—	V	V_{DD} = 3.5V 0.5V input overdrive
		4.985	4.993	—	V	V_{DD} = 5V 0.5V input overdrive
		14.970	14.980	—	V	V_{DD} = 15V 0.5V input overdrive
Low-Level Output Voltage	V_{OL}	—	0.005	0.010	V	V_{DD} = 3.5V 0.5 V input overdrive
		—	0.007	0.015	V	V_{DD} = 5V 0.5 V input overdrive
		—	0.020	0.030	V	V_{DD} = 15V 0.5 V input overdrive
Output Short-Circuit Current	I_{SC}	—	±27	—	mA	V_{DD} = 3.5V
		—	±45	—	mA	V_{DD} = 5V
		—	±50	—	mA	V_{DD} = 15V
Power Supply						
Supply Voltage	V_{DD}	3.5	—	16	V	Single-supply operation
		±1.75	—	±8	V	Dual-supply operation
Quiescent Current per Amplifier	I_Q	—	125	175	µA	I_O = 0, V_{DD} = 3.5V $V_{CM} = V_{DD}/4$
		—	130	180	µA	I_O = 0, V_{DD} = 5V $V_{CM} = V_{DD}/4$
		—	135	185	µA	I_O = 0, V_{DD} = 15V $V_{CM} = V_{DD}/4$

AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +3.5V to +16V, V_{SS} = GND, $V_{CM} = V_{DD}/2 - 1.4V$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 10 kΩ to V_L and C_L = 60 pF. (Refer to Figure 1-1).

Parameters	Sym	Min	Typ	Max	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	1.2	—	MHz	
Phase Margin	PM	—	57	—	°C	G = +1V/V
Slew Rate	SR	—	0.8	—	V/µs	
Noise						
Input Noise Voltage	E_{ni}	—	12	—	µVp-p	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	35	—	nV/√Hz	f = 1 kHz
		—	30	—	nV/√Hz	f = 10 kHz
Input Noise Current Density	i_{ni}	—	1.9	—	fA/√Hz	f = 1 kHz

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TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +3.5V to +16V and V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SC70	θ_{JA}	—	331	—	°C/W	
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 8L-2x3 TDFN	θ_{JA}	—	41	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	149.5	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	95.3	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note 1: The internal junction temperature (T_J) must not exceed the absolute maximum specification of +150°C.

1.2 Test Circuits

The circuit used for most DC and AC tests is shown in Figure 1-1. This circuit can independently set V_{CM} and V_{OUT} (refer to Equation 1-1). Note that V_{CM} is not the circuit's common mode voltage ((V_P + V_M)/2), and that V_{OST} includes V_{OS} plus the effects (on the input offset error, V_{OST}) of temperature, CMRR, PSRR and A_{OL}.

EQUATION 1-1:

$$G_{DM} = R_F / R_G$$
$$V_{CM} = (V_P + V_{DD}/2)/2$$
$$V_{OST} = V_{IN-} - V_{IN+}$$
$$V_{OUT} = (V_{DD}/2) + (V_P - V_M) + V_{OST} \cdot (1 + G_{DM})$$

Where:

G_{DM}	=	Differential Mode Gain	(V/V)
V_{CM}	=	Op Amp's Common Mode Input Voltage	(V)
V_{OST}	=	Op Amp's Total Input Offset Voltage	(mV)

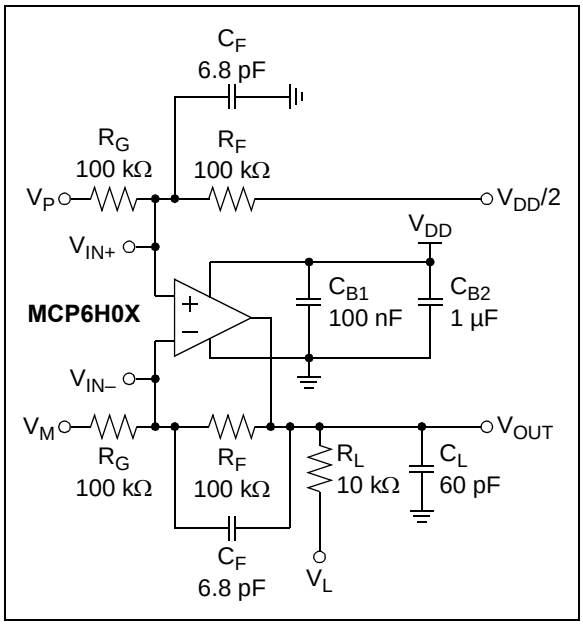


FIGURE 1-1: *AC and DC Test Circuit for Most Specifications.*

NOTES:

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +3.5V to +16V, V_{SS} = GND, V_{CM} = V_{DD}/2 - 1.4V, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 60 pF.

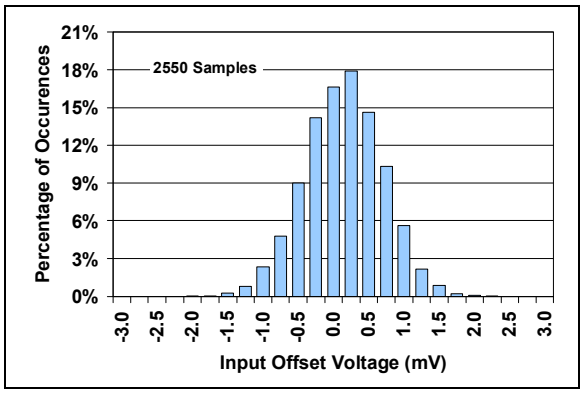


FIGURE 2-1: *Input Offset Voltage.*

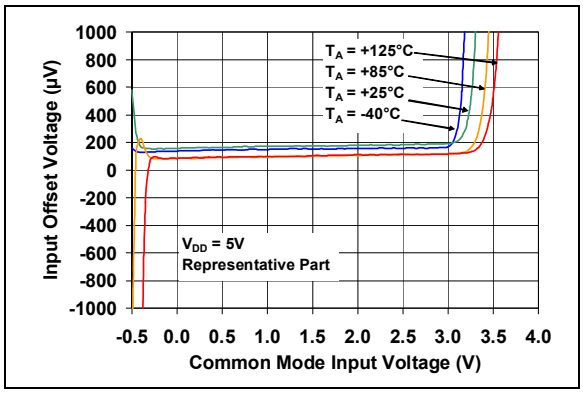


FIGURE 2-4: *Input Offset Voltage vs. Common Mode Input Voltage.*

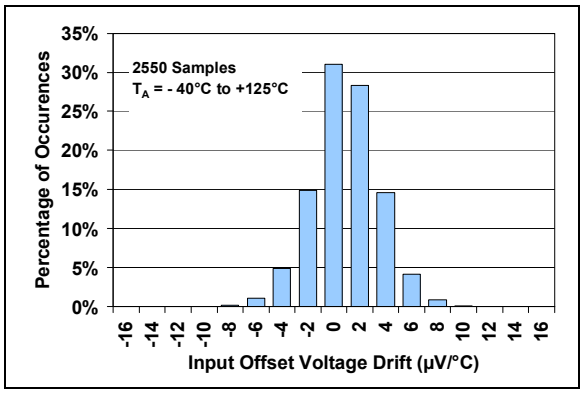


FIGURE 2-2: *Input Offset Voltage Drift.*

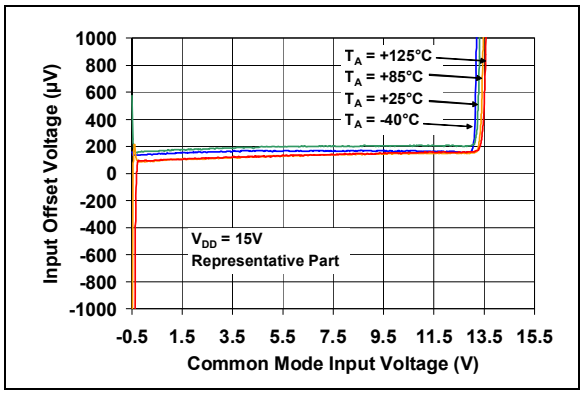


FIGURE 2-5: *Input Offset Voltage vs. Common Mode Input Voltage.*

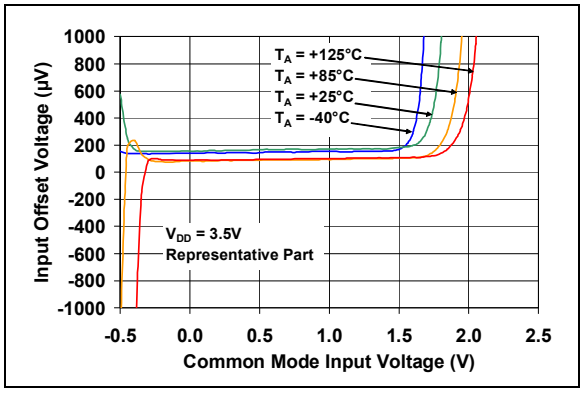


FIGURE 2-3: *Input Offset Voltage vs. Common Mode Input Voltage.*

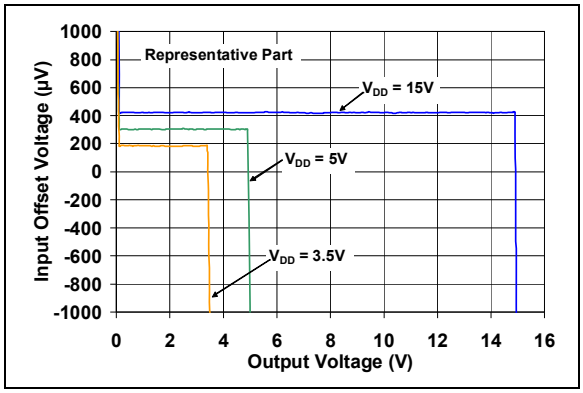


FIGURE 2-6: *Input Offset Voltage vs. Output Voltage.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +3.5V to +16V, V_{SS} = GND, V_{CM} = V_{DD}/2 - 1.4V, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 60 pF.

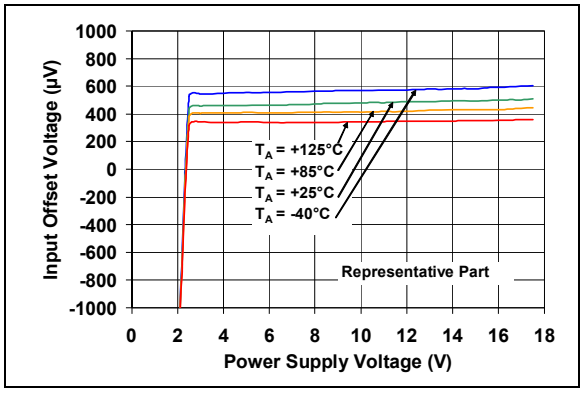


FIGURE 2-7: *Input Offset Voltage vs. Power Supply Voltage.*

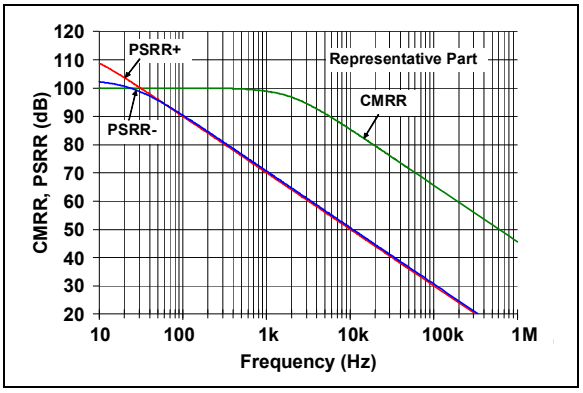


FIGURE 2-10: *CMRR, PSRR vs. Frequency.*

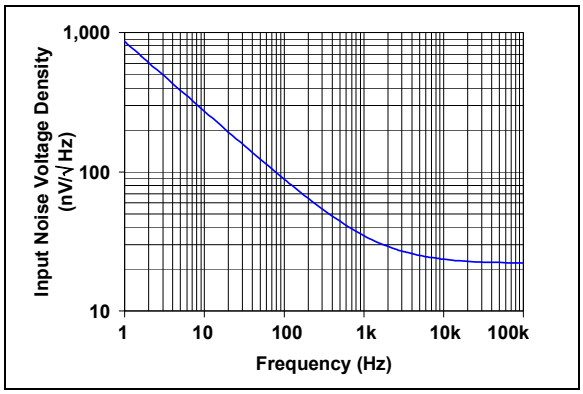


FIGURE 2-8: *Input Noise Voltage Density vs. Frequency.*

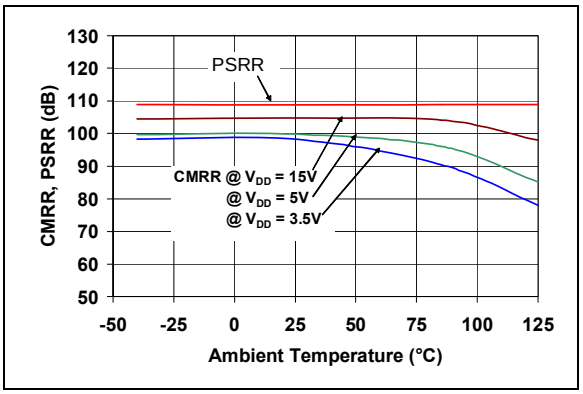


FIGURE 2-11: *CMRR, PSRR vs. Ambient Temperature.*

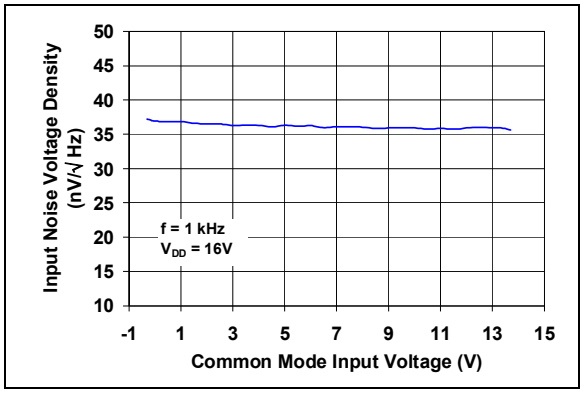


FIGURE 2-9: *Input Noise Voltage Density vs. Common Mode Input Voltage.*

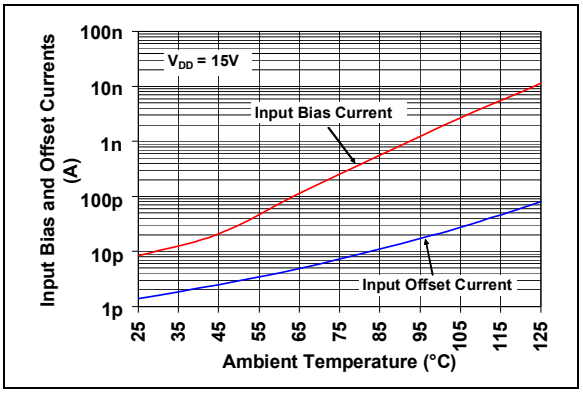


FIGURE 2-12: *Input Bias, Offset Currents vs. Ambient Temperature.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +3.5V to +16V, V_{SS} = GND, V_{CM} = V_{DD}/2 - 1.4V, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 60 pF.

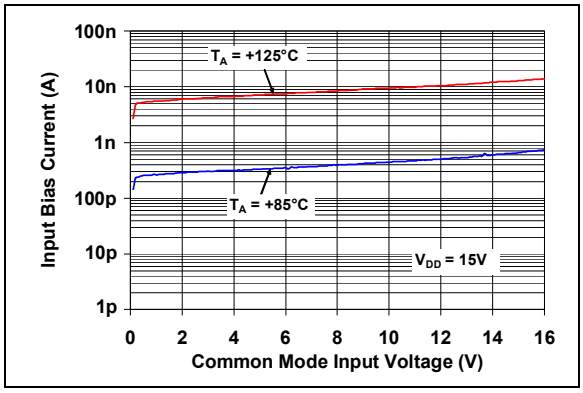


FIGURE 2-13: *Input Bias Current vs. Common Mode Input Voltage.*

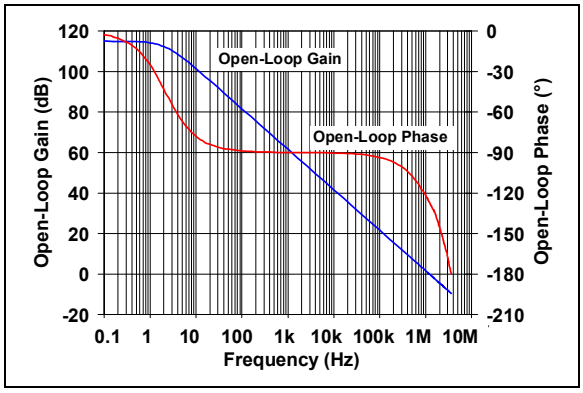


FIGURE 2-16: *Open-Loop Gain, Phase vs. Frequency.*

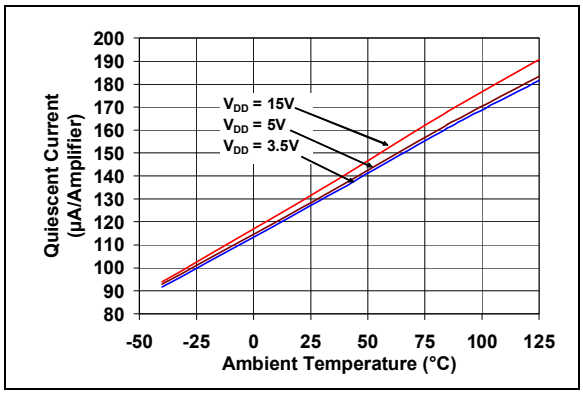


FIGURE 2-14: *Quiescent Current vs. Ambient Temperature.*

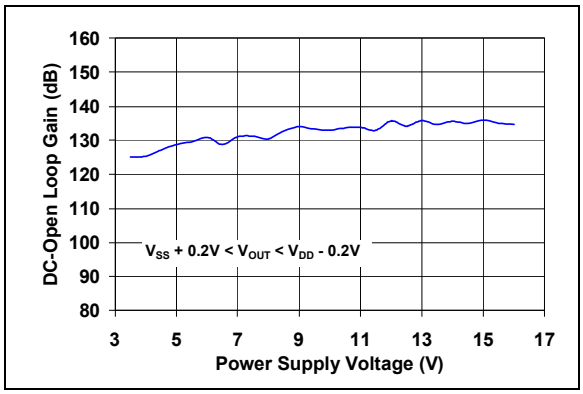


FIGURE 2-17: *DC Open-Loop Gain vs. Power Supply Voltage.*

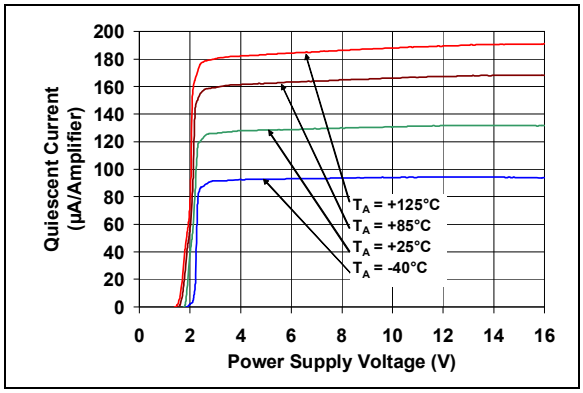


FIGURE 2-15: *Quiescent Current vs. Power Supply Voltage.*

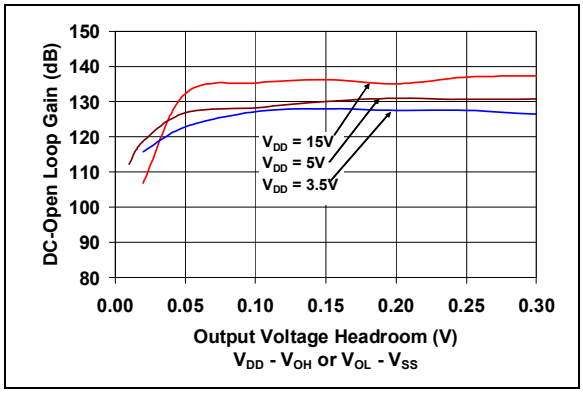


FIGURE 2-18: *DC Open-Loop Gain vs. Output Voltage Headroom.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +3.5V to +16V, V_{SS} = GND, V_{CM} = V_{DD}/2 - 1.4V, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 60 pF.

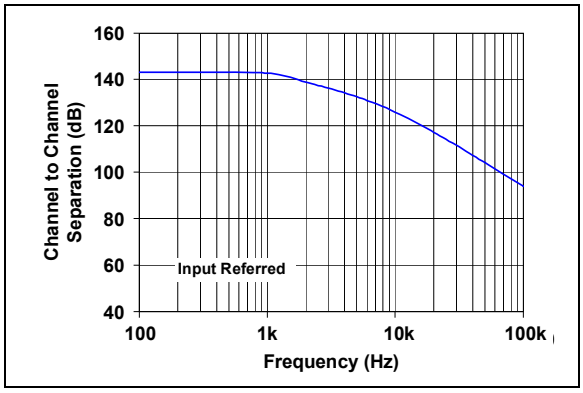


FIGURE 2-19: *Channel-to-Channel Separation vs. Frequency (MCP6H02 only).*

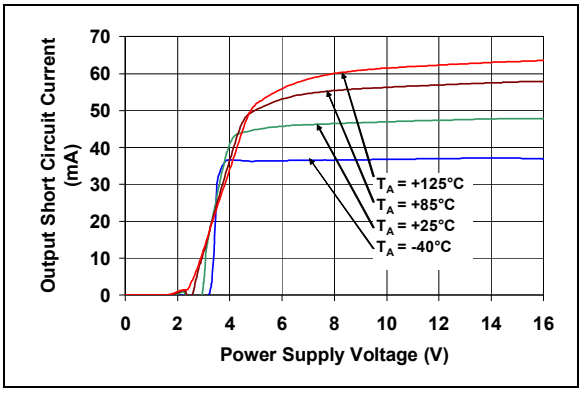


FIGURE 2-22: *Output Short Circuit Current vs. Power Supply Voltage.*

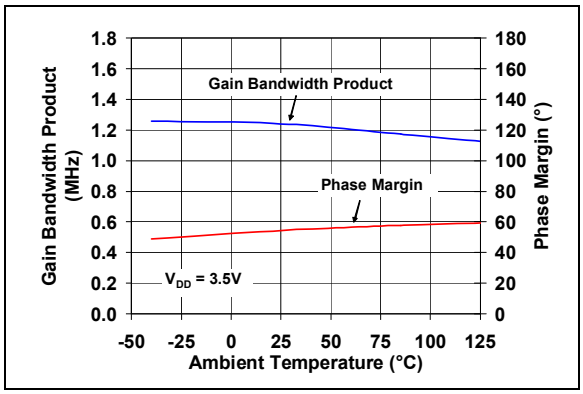


FIGURE 2-20: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.*

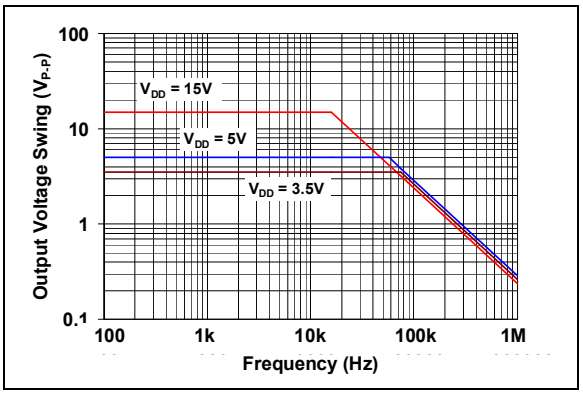


FIGURE 2-23: *Output Voltage Swing vs. Frequency.*

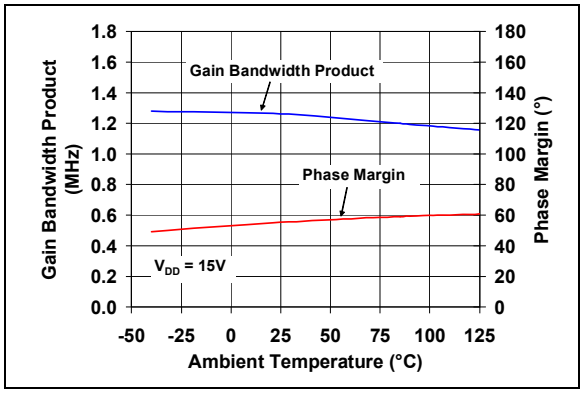


FIGURE 2-21: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.*

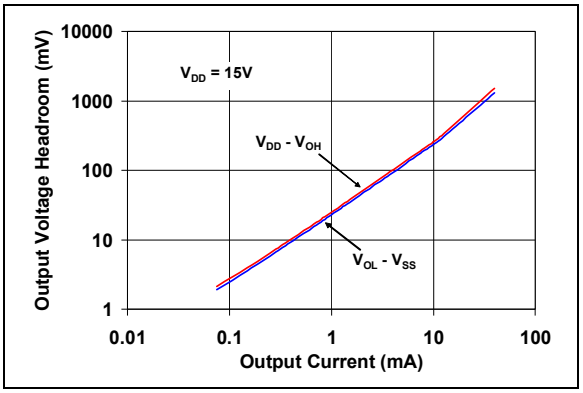


FIGURE 2-24: *Output Voltage Headroom vs. Output Current.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +3.5V to +16V, V_{SS} = GND, V_{CM} = V_{DD}/2 - 1.4V, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 60 pF.

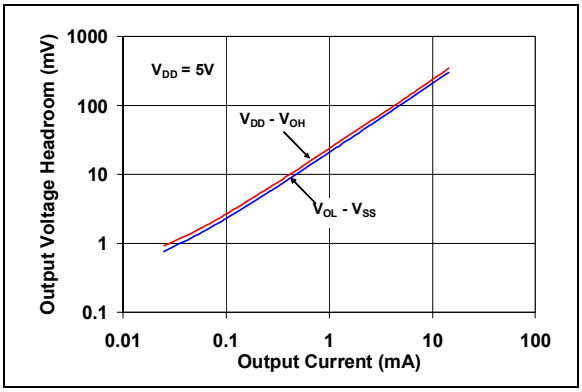


FIGURE 2-25: *Output Voltage Headroom vs. Output Current.*

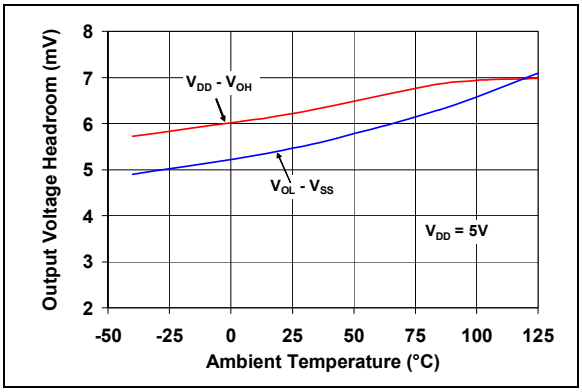


FIGURE 2-28: *Output Voltage Headroom vs. Ambient Temperature.*

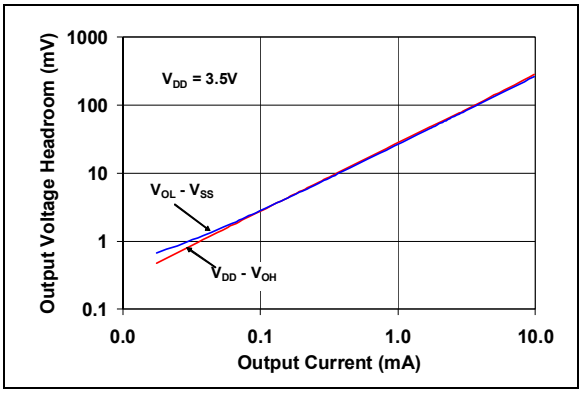


FIGURE 2-26: *Output Voltage Headroom vs. Output Current.*

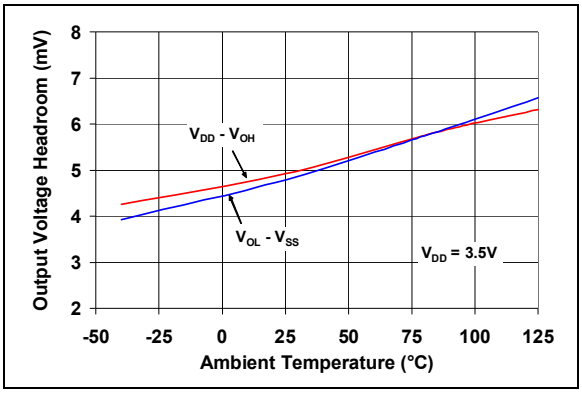


FIGURE 2-29: *Output Voltage Headroom vs. Ambient Temperature.*

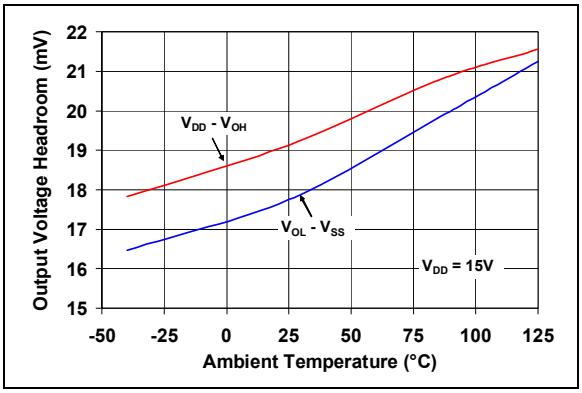


FIGURE 2-27: *Output Voltage Headroom vs. Ambient Temperature.*

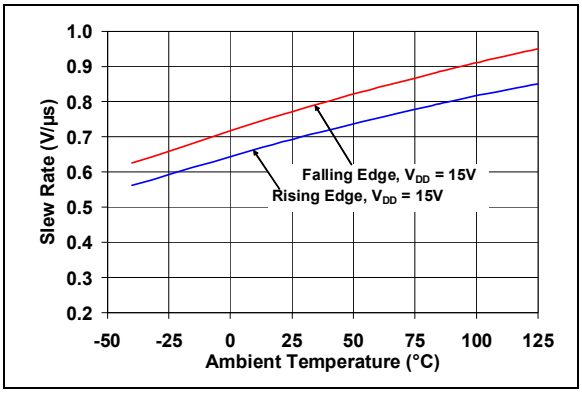


FIGURE 2-30: *Slew Rate vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +3.5 V to +16 V, V_{SS} = GND, V_{CM} = V_{DD}/2 - 1.4V, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 60 pF.

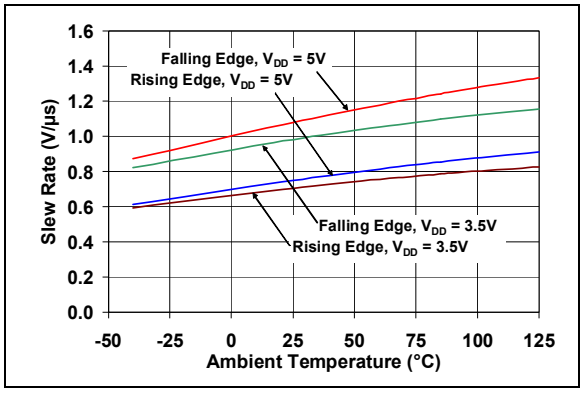


FIGURE 2-31: *Slew Rate vs. Ambient Temperature.*

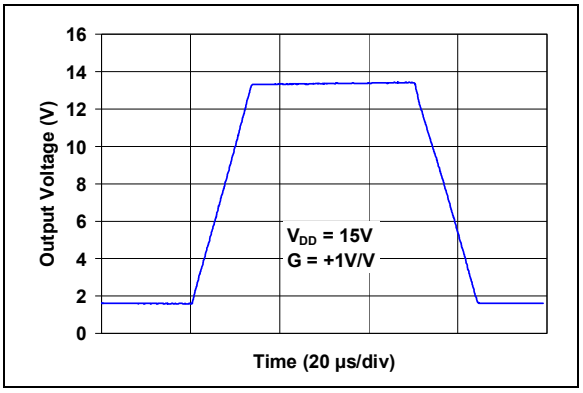


FIGURE 2-34: *Large Signal Non-Inverting Pulse Response.*

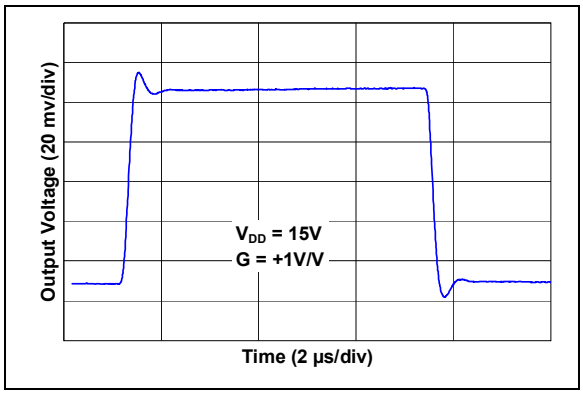


FIGURE 2-32: *Small Signal Non-Inverting Pulse Response.*

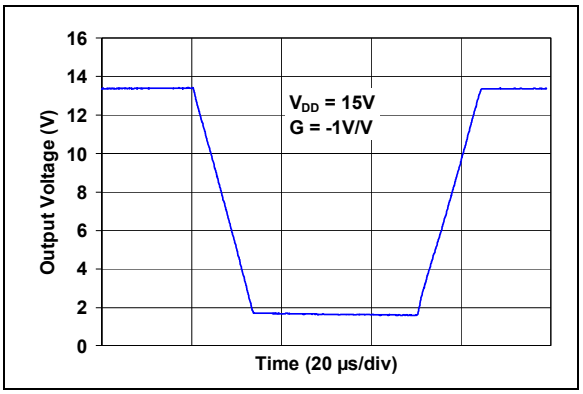


FIGURE 2-35: *Large Signal Inverting Pulse Response.*

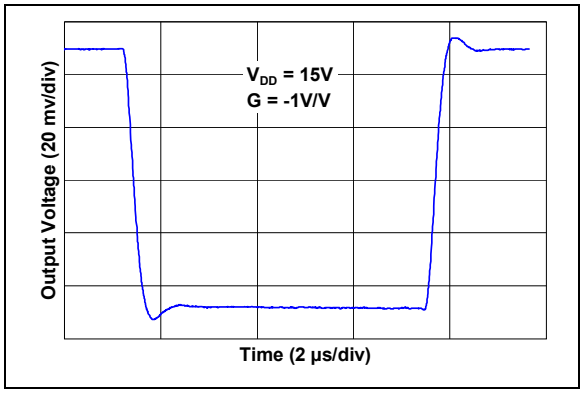


FIGURE 2-33: *Small Signal Inverting Pulse Response.*

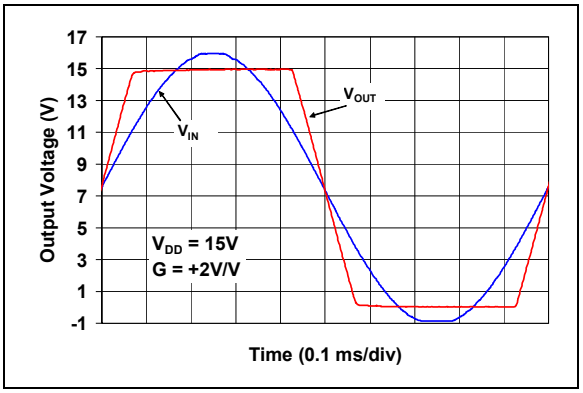


FIGURE 2-36: *The MCP6H01/2/4 Shows No Phase Reversal.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +3.5 V to +16 V, V_{SS} = GND, V_{CM} = V_{DD}/2 - 1.4V, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 60 pF.

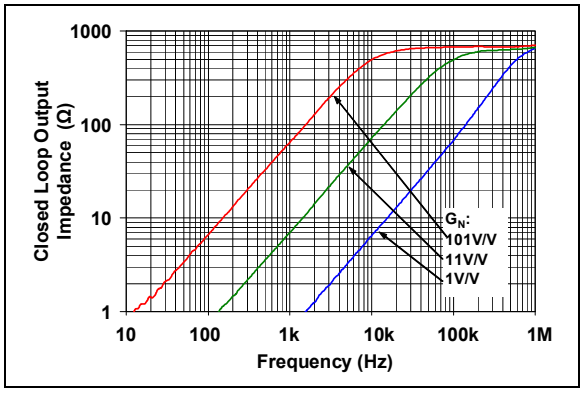


FIGURE 2-37: *Closed Loop Output Impedance vs. Frequency.*

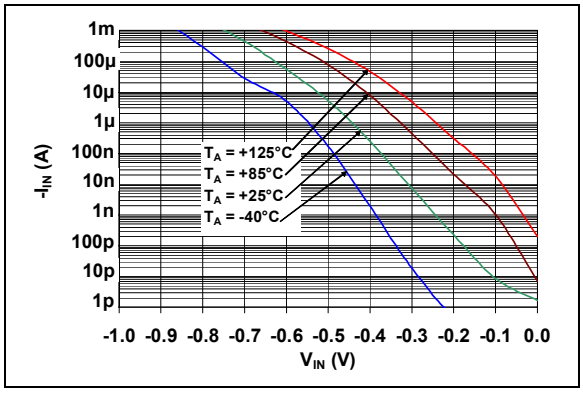


FIGURE 2-38: *Measured Input Current vs. Input Voltage (below V_{SS}).*

NOTES:

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3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP6H01			MCP6H02		MCP6H04	Symbol	Description
SC70-5, SOT-23-5	SOIC	2x3 TDFN	SOIC	2x3 TDFN	SOIC, TSSOP		
1	6	6	1	1	1	V_{OUT}, V_{OUTA}	Analog Output (op amp A)
4	2	2	2	2	2	$V_{IN}-$, $V_{INA}-$	Inverting Input (op amp A)
3	3	3	3	3	3	$V_{IN}+$, $V_{INA}+$	Non-inverting Input (op amp A)
5	7	7	8	8	4	V_{DD}	Positive Power Supply
—	—	—	5	5	5	$V_{INB}+$	Non-inverting Input (op amp B)
—	—	—	6	6	6	$V_{INB}-$	Inverting Input (op amp B)
—	—	—	7	7	7	V_{OUTB}	Analog Output (op amp B)
—	—	—	—	—	8	V_{OUTC}	Analog Output (op amp C)
—	—	—	—	—	9	$V_{INC}-$	Inverting Input (op amp C)
—	—	—	—	—	10	$V_{INC}+$	Non-inverting Input (op amp C)
2	4	4	4	4	11	V_{SS}	Negative Power Supply
—	—	—	—	—	12	$V_{IND}+$	Non-inverting Input (op amp D)
—	—	—	—	—	13	$V_{IND}-$	Inverting Input (op amp D)
—	—	—	—	—	14	V_{OUTD}	Analog Output (op amp D)
—	1, 5, 8	1, 5, 8	—	—	—	NC	No Internal Connection
—	—	9	—	9	—	EP	Exposed Thermal Pad (EP); must be connected to V_{SS}.

3.1 Analog Outputs

The output pins are low-impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply Pins

The positive power supply (V_{DD}) is 3.5V to 16V higher than the negative power supply (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}.

Typically, these parts can be used in single-supply operation or dual-supply operation. Also, V_{DD} will need bypass capacitors.

3.4 Exposed Thermal Pad (EP)

There is an internal electrical connection between the Exposed Thermal Pad (EP) and the V_{SS} pin; they must be connected to the same potential on the Printed Circuit Board (PCB).

NOTES:

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4.0 APPLICATION INFORMATION

The MCP6H01/2/4 family of op amps is manufactured using Microchip's state-of-the-art CMOS process and is specifically designed for low-power, high-precision applications.

4.1 Inputs

4.1.1 PHASE REVERSAL

The MCP6H01/2/4 op amps are designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-36 shows the input voltage exceeding the supply voltage without any phase reversal.

4.1.2 INPUT VOLTAGE LIMITS

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the voltages at the input pins (see **Section 1.1 "Absolute Maximum Ratings †"**).

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors against many (but not all) over-voltage conditions, and to minimize the input bias current (I_B).

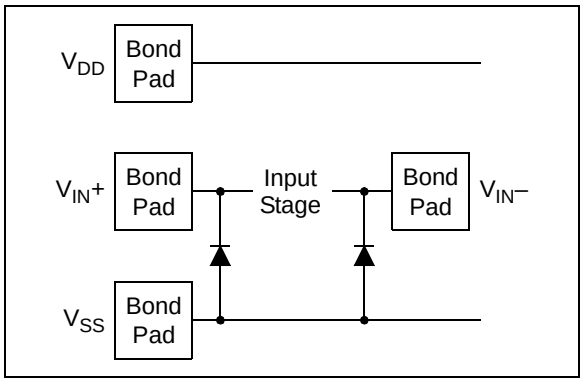


FIGURE 4-1: *Simplified Analog Input ESD Structures.*

The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that go well above V_{DD}. Their breakdown voltage is high enough to allow normal operation, but not low enough to protect against slow overvoltage (beyond V_{DD}) events. Very fast ESD events (that meet the specification) are limited so that damage does not occur.

In some applications, it may be necessary to prevent excessive voltages from reaching the op amp inputs; Figure 4-2 shows one approach to protecting these inputs.

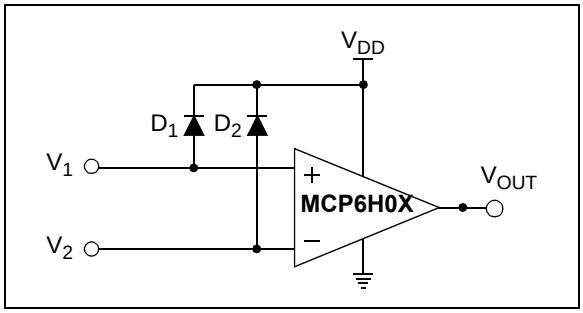


FIGURE 4-2: *Protecting the Analog Inputs.*

A significant amount of current can flow out of the inputs when the common mode voltage (V_{CM}) is below ground (V_{SS}), see Figure 2-38.

4.1.3 INPUT CURRENT LIMITS

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the currents into the input pins (see **Section 1.1 "Absolute Maximum Ratings †"**).

Figure 4-3 shows one approach to protecting these inputs. The resistors R_1 and R_2 limit the possible currents in or out of the input pins (and the ESD diodes, D_1 and D_2). The diode currents will go through either V_{DD} or V_{SS}.

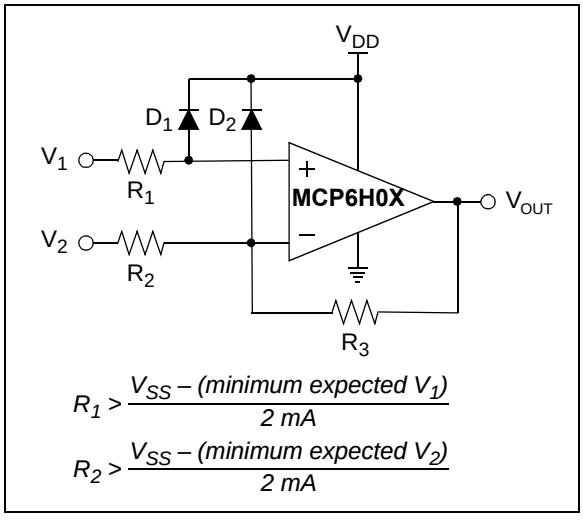


FIGURE 4-3: *Protecting the Analog Inputs.*

4.1.4 NORMAL OPERATION

The inputs of the MCP6H01/2/4 op amps connect to a differential PMOS input stage. It operates at a low common mode input voltage (V_{CM}), including ground. With this topology, the device operates with a V_{CM} up to V_{DD} – 2.3V and 0.3V below V_{SS} (refer to Figure 2-3 through 2-5). The input offset voltage is measured at $V_{CM} = V_{SS} – 0.3V$ and $V_{DD} – 2.3V$ to ensure proper operation.

For a unity gain buffer, V_{IN} must be maintained below V_{DD} – 2.3V for correct operation.

4.2 Rail-to-Rail Output

The output voltage range of the MCP6H01/2/4 op amps is 0.020V (typical) and 14.980V (typical) when R_L = 10 kΩ is connected to $V_{DD}/2$ and V_{DD} = 15V. Refer to Figures 2-24 through 2-29 for more information.

4.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. While a unity-gain buffer (G = +1V/V) is the most sensitive to capacitive loads, all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 100 pF when G = + 1V/V), a small series resistor at the output (R_{ISO} in Figure 4-4) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will generally be lower than the bandwidth with no capacitance load.

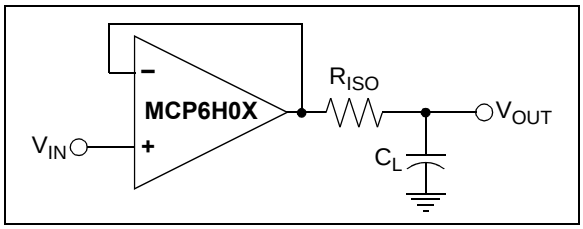


FIGURE 4-4: *Output Resistor, R_{ISO} Stabilizes Large Capacitive Loads.*

Figure 4-5 gives the recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For non-inverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is 1 + |Signal Gain| (e.g., -1V/V gives G_N = +2V/V).

After selecting R_{ISO} for your circuit, double check the resulting frequency response peaking and step response overshoot. Modify R_{ISO}'s value until the response is reasonable. Bench evaluation and simulations with the MCP6H01/2/4 SPICE macro model are helpful.

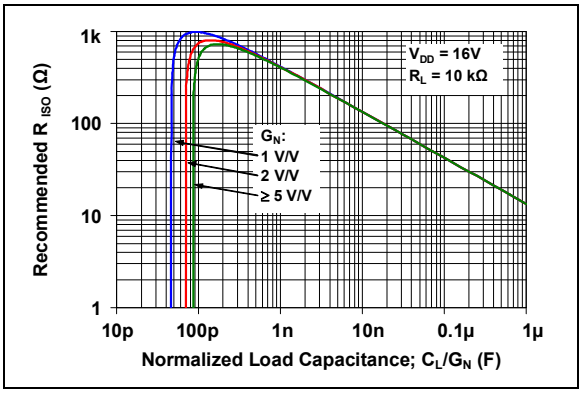


FIGURE 4-5: *Recommended R_{ISO} Values for Capacitive Loads.*

4.4 Supply Bypass

With this family of operational amplifiers, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high-frequency performance. It can use a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

4.5 Unused Op Amps

An unused op amp in a quad package (MCP6H04) should be configured as shown in Figure 4-6. These circuits prevent the output from toggling and causing crosstalk. Circuit A sets the op amp at its minimum noise gain. The resistor divider produces any desired reference voltage within the output voltage range of the op amp, and the op amp buffers that reference voltage. Circuit B uses the minimum number of components and operates as a comparator, but it may draw more current.

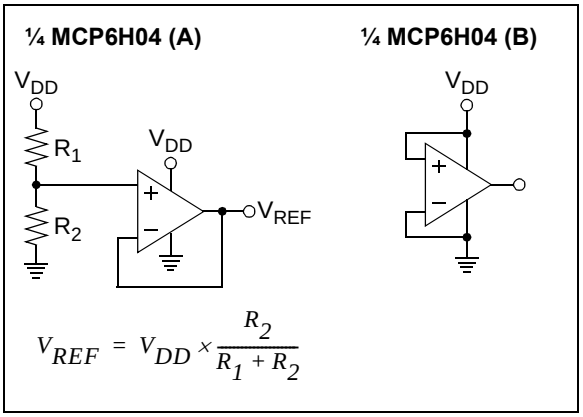


FIGURE 4-6: *Unused Op Amps.*

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4.6 PCB Surface Leakage

In applications where low input bias current is critical, PCB surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low-humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 15V difference would cause 15 pA of current to flow; which is greater than the MCP6H01/2/4 family's bias current at +25°C (10 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-7.

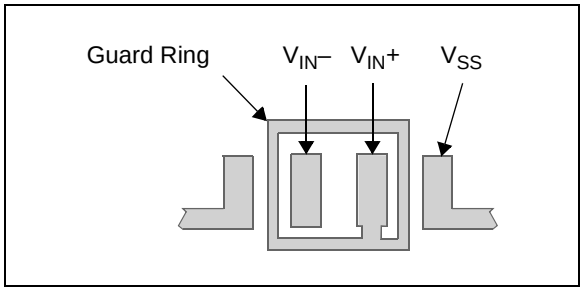


FIGURE 4-7: *Example Guard Ring Layout for Inverting Gain.*

1. Non-inverting Gain and Unity-Gain Buffer:
   a. Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b. Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the common mode input voltage.
2. Inverting Gain and Trans-impedance Gain Amplifiers (convert current to voltage, such as photo detectors):
   a. Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op amp (e.g., V_{DD}/2 or ground).
   b. Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

4.7 Application Circuits

4.7.1 DIFFERENCE AMPLIFIER

The MCP6H01/2/4 op amps can be used in current sensing applications. Figure 4-8 shows a resistor (R_{SEN}) that converts the sensor current (I_{SEN}) to voltage, as well as a difference amplifier that amplifies the voltage across the resistor while rejecting common mode noise. R_1 and R_2 must be well matched to obtain an acceptable Common Mode Rejection Ratio (CMRR). Moreover, R_{SEN} should be much smaller than R_1 and R_2 in order to minimize the resistive loading of the source.

To ensure proper operation, the op amp common mode input voltage must be kept within the allowed range. The reference voltage (V_{REF}) is supplied by a low-impedance source. In single-supply applications, V_{REF} is typically V_{DD}/2.

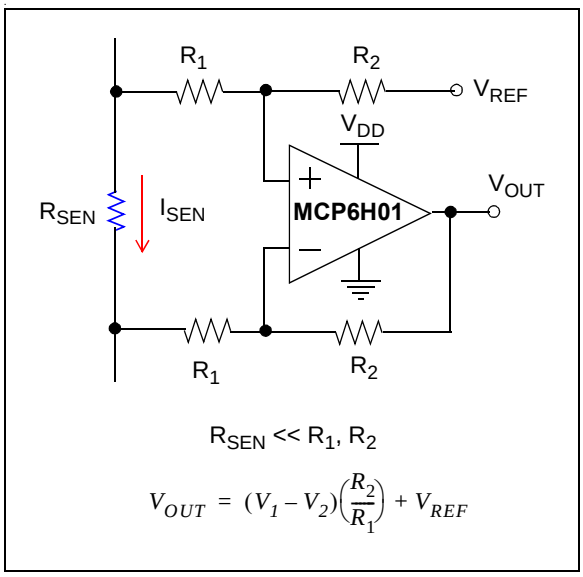


FIGURE 4-8: *High Side Current Sensing Using Difference Amplifier.*

4.7.2 TWO OP AMP INSTRUMENTATION AMPLIFIER

The MCP6H01/2/4 op amps are well suited for conditioning sensor signals in battery-powered applications. Figure 4-9 shows a two op amp instrumentation amplifier using the MCP6H02, which works well for applications requiring rejection of common mode noise at higher gains.

To ensure proper operation, the op amp common mode input voltage must be kept within the allowed range. The reference voltage (V_{REF}) is supplied by a low-impedance source. In single-supply applications, V_{REF} is typically $V_{DD}/2$.

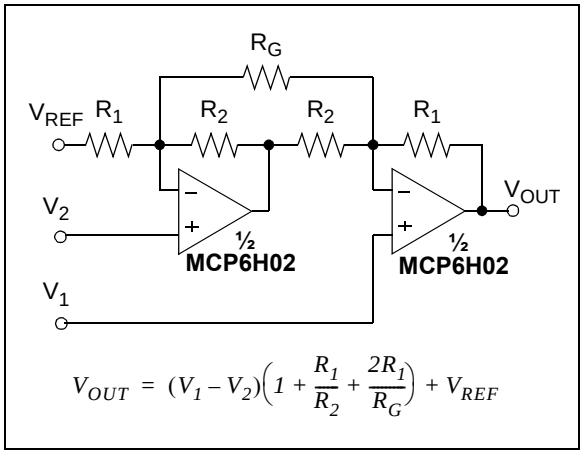


FIGURE 4-9: *Two Op Amp Instrumentation Amplifier.*

To obtain the best CMRR possible, and not limit the performance by the resistor tolerances, set a high gain with the R_G resistor.

4.7.3 PHOTODETECTOR AMPLIFIER

The MCP6H01/2/4 op amps can be used to easily convert the signal from a sensor that produces an output current (such as a photo diode) into voltage (a trans-impedance amplifier). This is implemented with a single resistor (R_2) in the feedback loop of the amplifiers shown in Figure 4-10. The optional capacitor (C_2) sometimes provides stability for these circuits.

A photodiode configured in Photovoltaic mode has a zero voltage potential placed across it. In this mode, the light sensitivity and linearity is maximized, making it best suited for precision applications. The key amplifier specifications for this application are: low input bias current, common mode input voltage range (including ground), and rail-to-rail output.

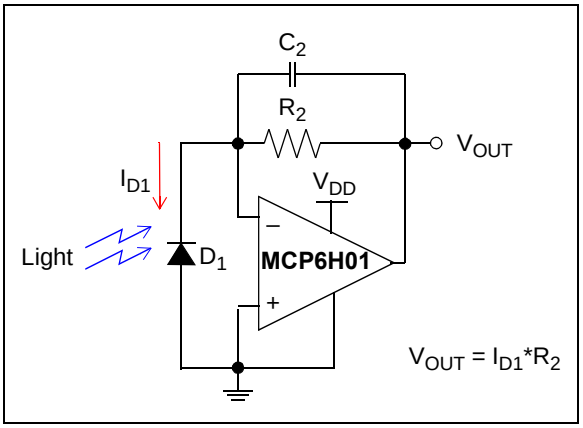


FIGURE 4-10: *Photodetector Amplifier.*

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5.0 DESIGN AIDS

Microchip provides the basic design tools needed for the MCP6H01/2/4 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6H01/2/4 op amp is available on the Microchip web site at www.microchip.com. The model was written and tested in PSPICE owned by Orcad (Cadence). For other simulators, it may require translation.

The model covers a wide aspect of the op amp's electrical specifications. Not only does the model cover voltage, current and resistance of the op amp, but it also covers the temperature and noise effects on the behavior of the op amp. The model has not been verified outside the specification range listed in the op amp data sheet. The model behaviors under these conditions cannot be guaranteed to match the actual op amp performance.

Moreover, the model is intended to be an initial design tool. Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 FilterLab Software

Microchip's FilterLab software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip web site at www.microchip.com/filterlab, the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

5.3 MAPS (Microchip Advanced Part Selector)

MAPS is a software tool that helps semiconductor professionals efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip web site at www.microchip.com/maps, MAPS is an overall selection tool for Microchip's product portfolio that includes analog, memory, MCUs and DSCs. Using this tool, you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for data sheets, purchases and sampling of Microchip parts.

5.4 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site: www.microchip.com/analogtools.

Some boards that are especially useful include:

- MCP6XXX Amplifier Evaluation Board 1
- MCP6XXX Amplifier Evaluation Board 2
- MCP6XXX Amplifier Evaluation Board 3
- MCP6XXX Amplifier Evaluation Board 4
- Active Filter Demo Board Kit
- 5/6-Pin SOT-23 Evaluation Board, P/N VSUPEV2
- 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board, P/N SOIC8EV

5.5 Application Notes

The following Microchip analog design note and application notes are available on the Microchip web site at www.microchip.com/appnotes, and are recommended as supplemental reference resources.

- **ADN003:** *"Select the Right Operational Amplifier for your Filtering Circuits",* DS21821
- **AN722:** *"Operational Amplifier Topologies and DC Specifications",* DS00722
- **AN723:** *"Operational Amplifier AC Specifications and Applications",* DS00723
- **AN884:** *"Driving Capacitive Loads With Op Amps",* DS00884
- **AN990:** *"Analog Sensor Conditioning Circuits – An Overview",* DS00990
- **AN1177:** *"Op Amp Precision Design: DC Errors",* DS01177
- **AN1228:** *"Op Amp Precision Design: Random Noise",* DS01228
- **AN1297:** *"Microchip's Op Amp SPICE Macro Models"* DS01297
- **AN1332:** *"Current Sensing Circuit Concepts and Fundamentals"* DS01332

These application notes and others are listed in:

- *"Signal Chain Design Guide",* DS21825

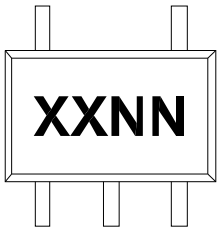
NOTES:

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6.0 PACKAGING INFORMATION

6.1 Package Marking Information

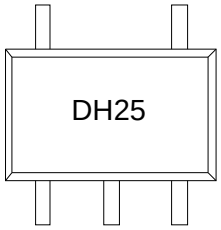
5-Lead SC-70 (MCP6H01)



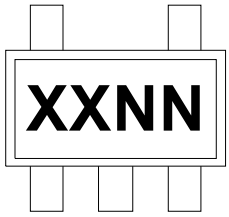
Device	Code
MCP6H01	DHNN

Note: Applies to 5-Lead SC-70.

Example



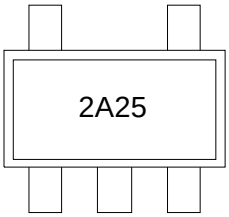
5-Lead SOT-23 (MCP6H01)



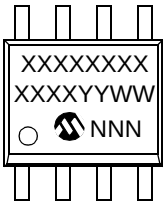
Device	Code
MCP6H01	2ANN

Note: Applies to 5-Lead SOT-23.

Example:



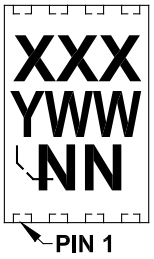
8-Lead SOIC (150 mil) **(MCP6H01, MCP6H02)**



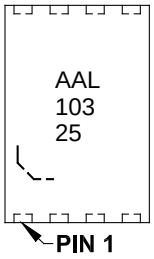
Example:



8-Lead 2x3 TDFN **(MCP6H01, MCP6H02)**



Example:

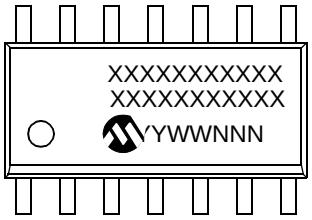


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

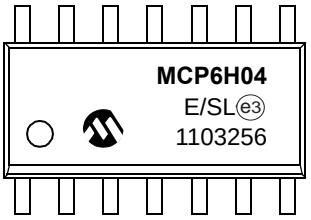
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Package Marking Information

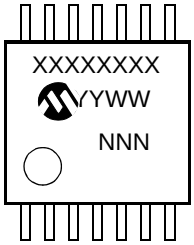
14-Lead SOIC (150 mil) (**MCP6H04**)



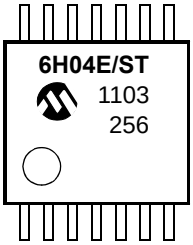
Example:



14-Lead TSSOP (**MCP6H04**)



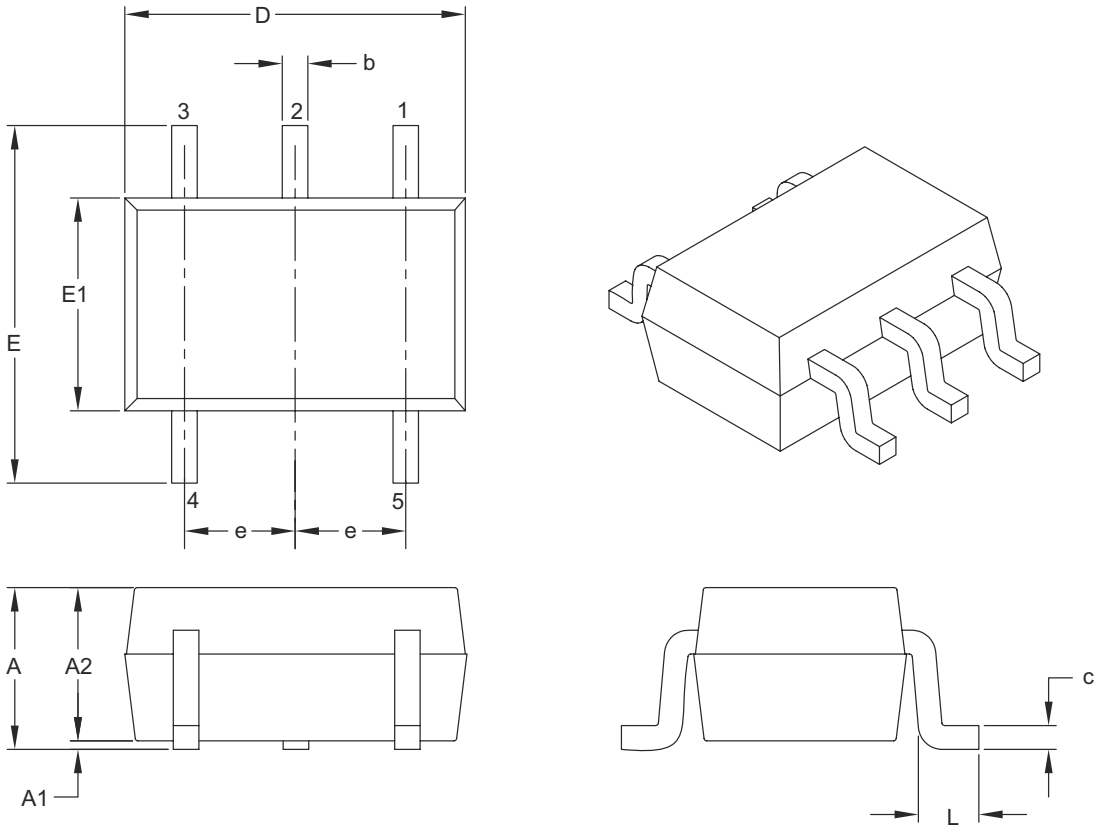
Example:



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5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	–	1.10
Molded Package Thickness	A2	0.80	–	1.00
Standoff	A1	0.00	–	0.10
Overall Width	E	1.80	2.10	2.40
Molded Package Width	E1	1.15	1.25	1.35
Overall Length	D	1.80	2.00	2.25
Foot Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.15	–	0.40

Notes:

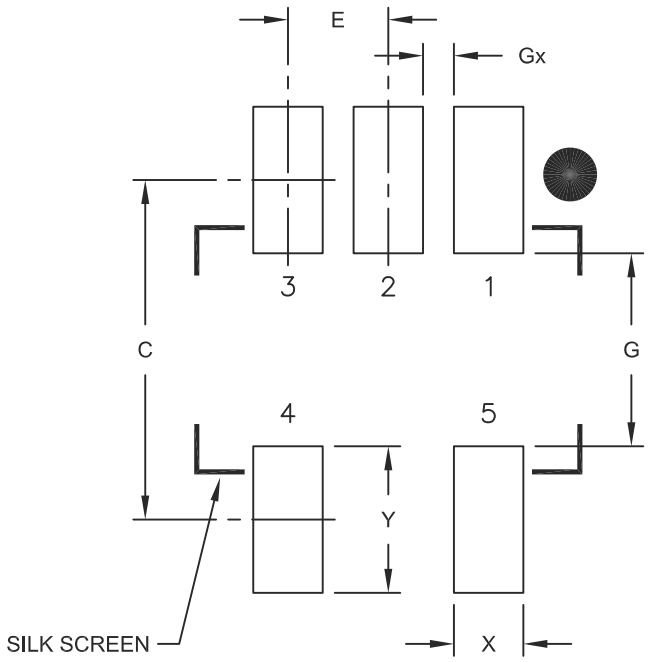
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-061B

5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		2.20	
Contact Pad Width	X			0.45
Contact Pad Length	Y			0.95
Distance Between Pads	G	1.25		
Distance Between Pads	Gx	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

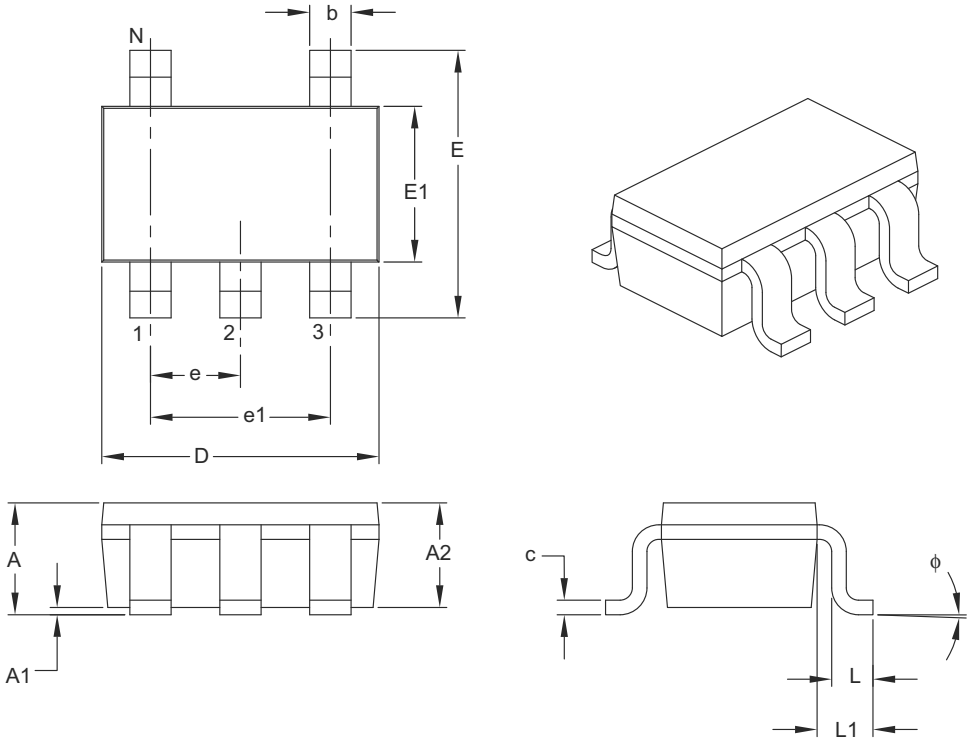
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2061A

© 2010-2011 Microchip Technology Inc.

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

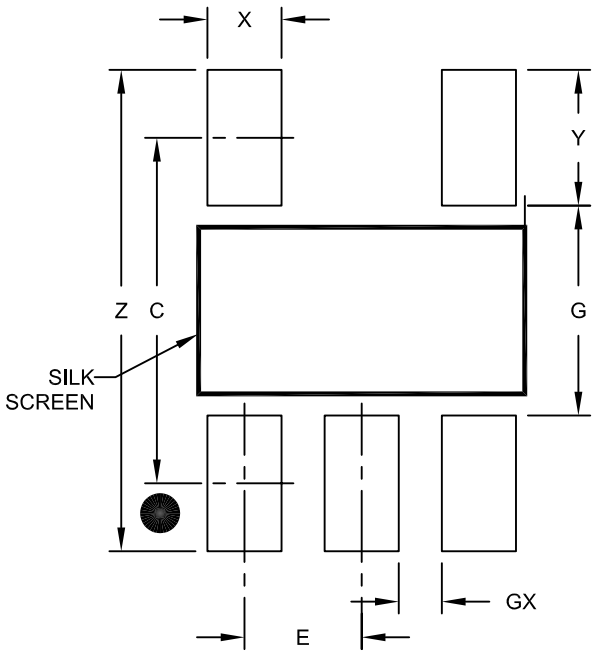
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

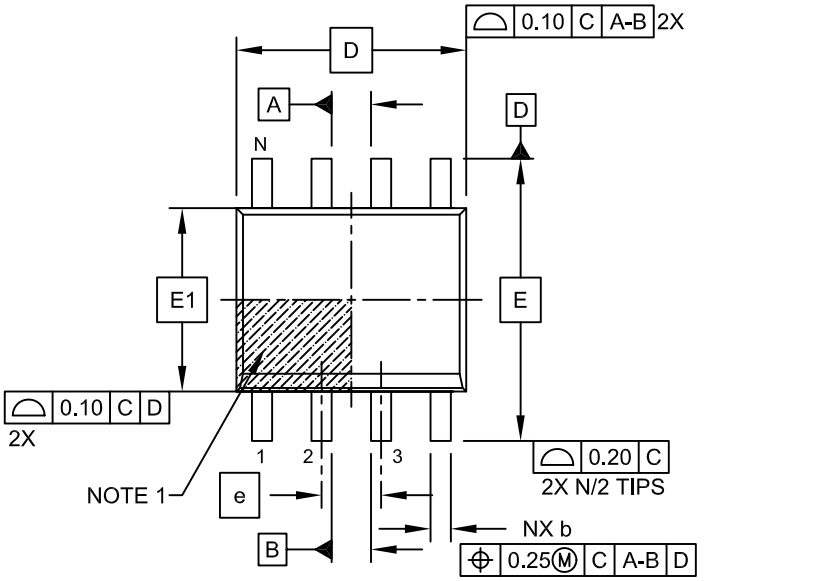
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091A

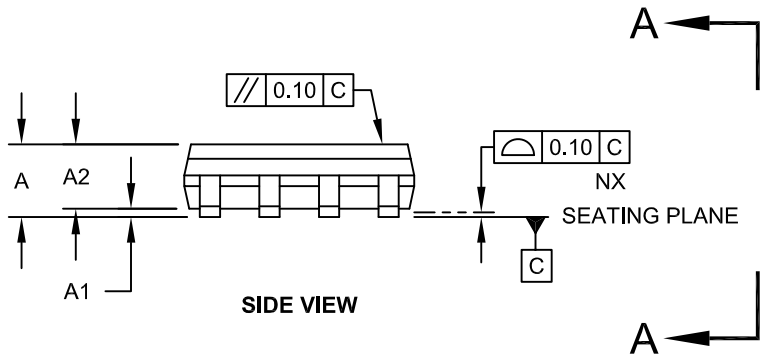
© 2010-2011 Microchip Technology Inc.

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

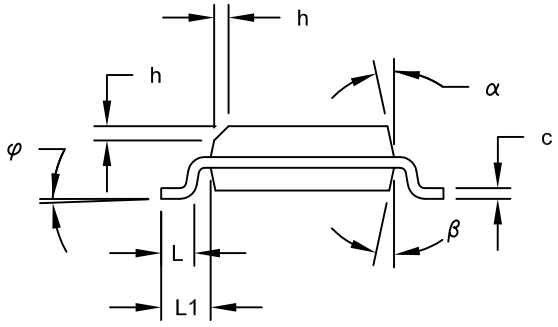
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

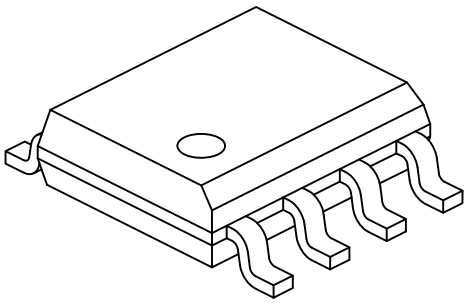


VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

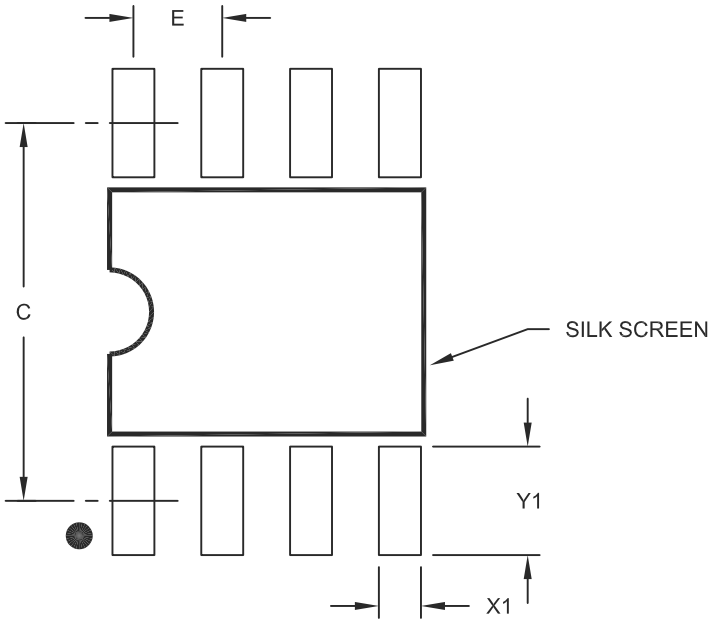
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

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8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

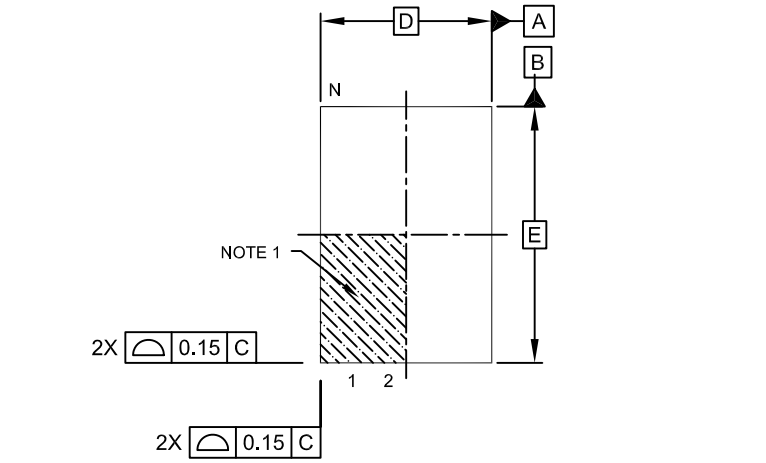
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

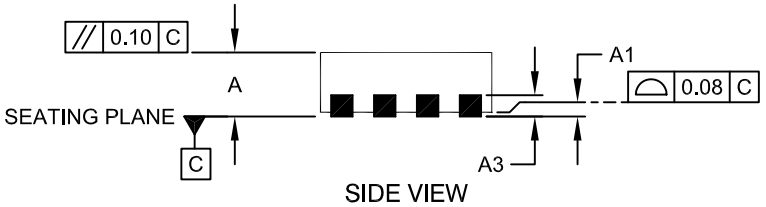
Microchip Technology Drawing No. C04-2057A

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

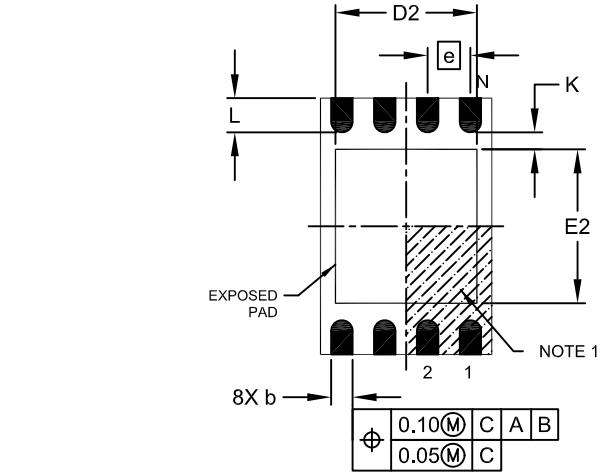
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



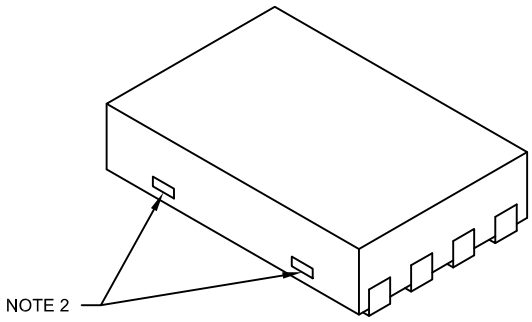
BOTTOM VIEW

Microchip Technology Drawing No. C04-129C

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8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.20	-	1.60
Exposed Pad Width	E2	1.20	-	1.60
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.25	0.30	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

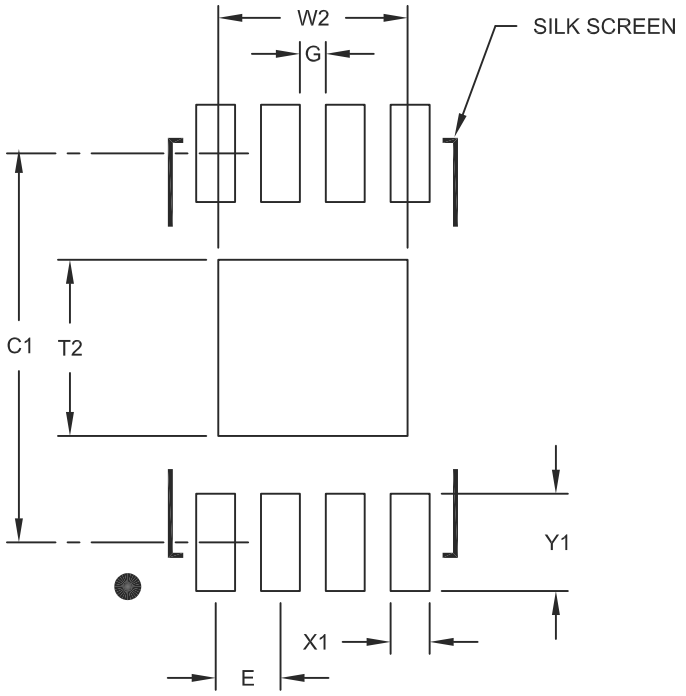
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129C Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75 mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			1.46
Optional Center Pad Length	T2			1.36
Contact Pad Spacing	C1		3.00	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

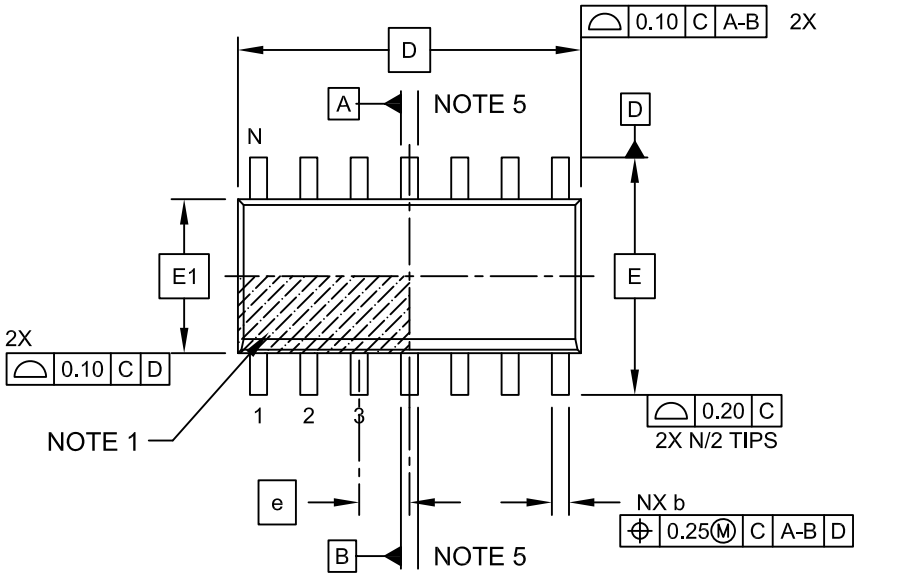
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2129A

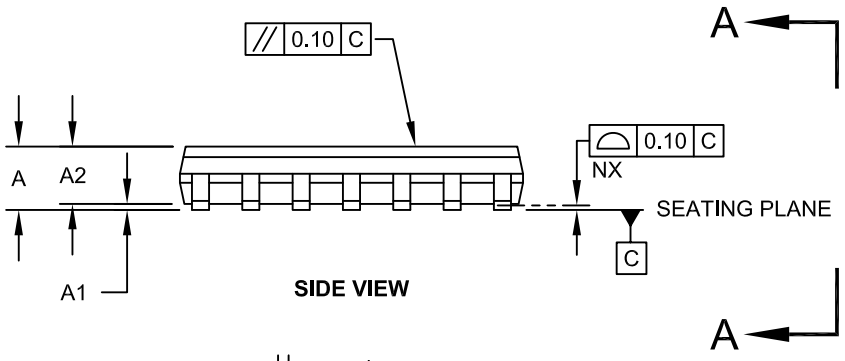
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14-Lead Plastic Small Outline (OD) - Narrow, 3.90 mm Body [SOIC]

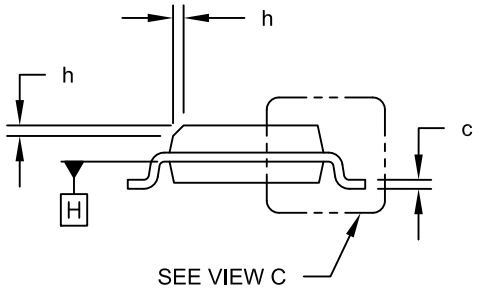
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

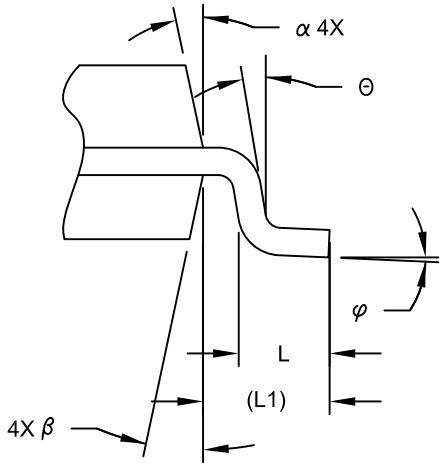


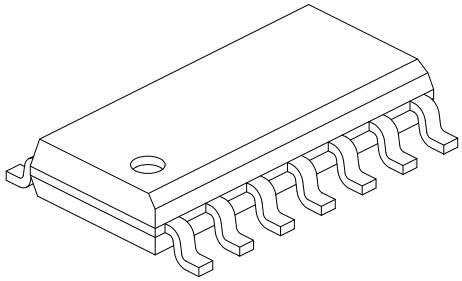
VIEW A-A

Microchip Technology Drawing No. C04-065C Sheet 1 of 2

14-Lead Plastic Small Outline (OD) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





VIEW C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

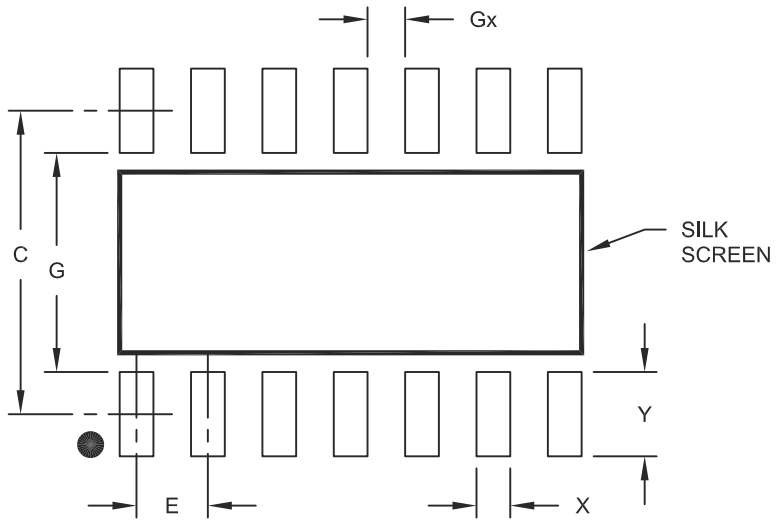
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065C Sheet 2 of 2

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14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

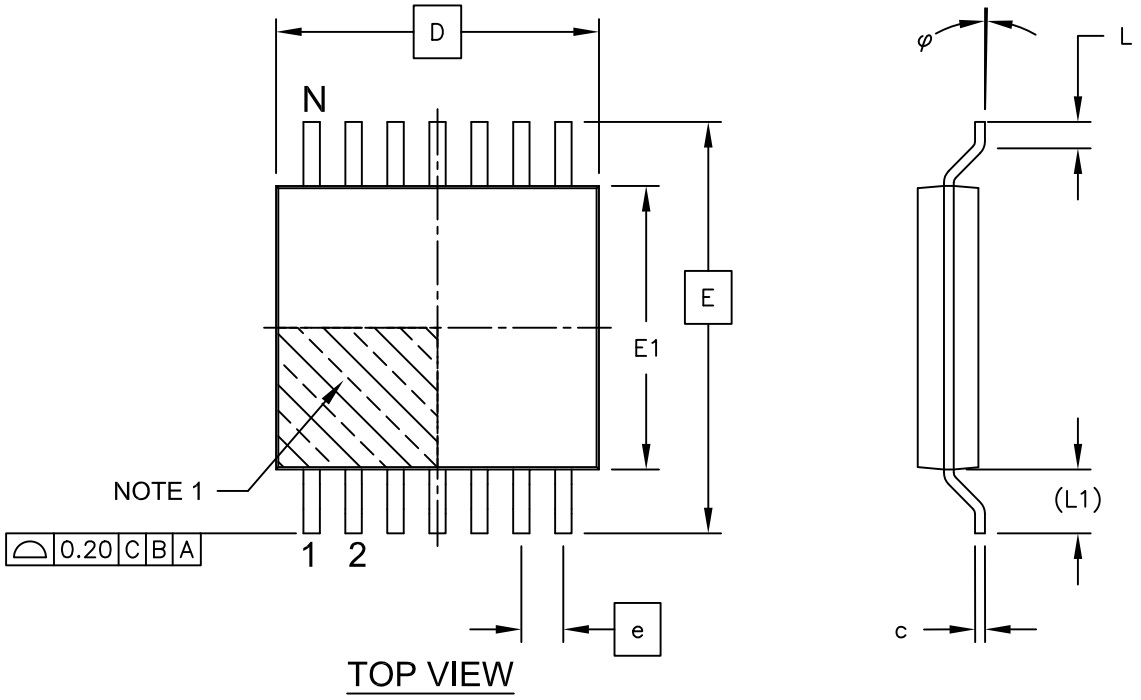
1. Dimensioning and tolerancing per ASME Y14.5M

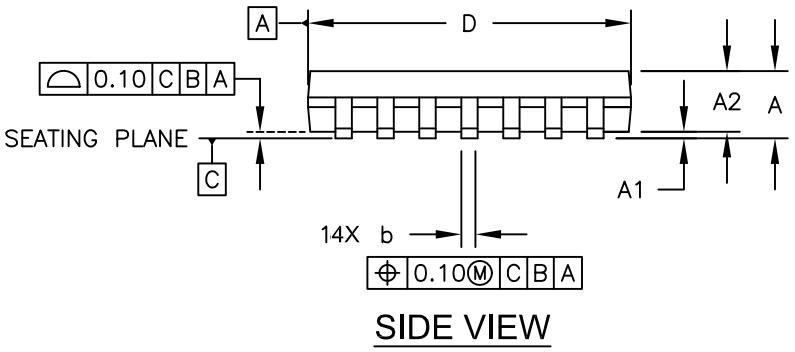
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



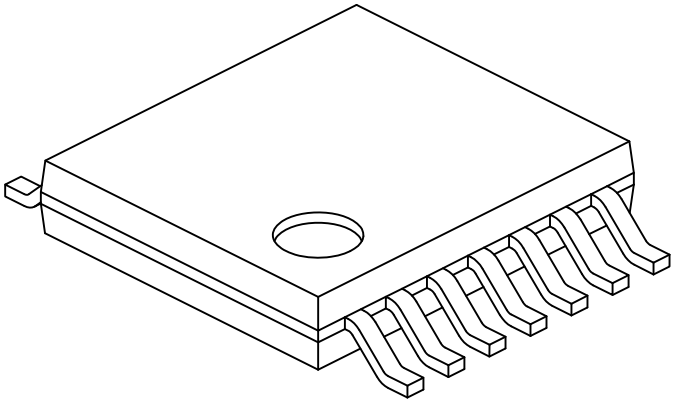


Microchip Technology Drawing C04-087C Sheet 1 of 2

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14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	(L1)		1.00 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.19	-	0.30

Notes:

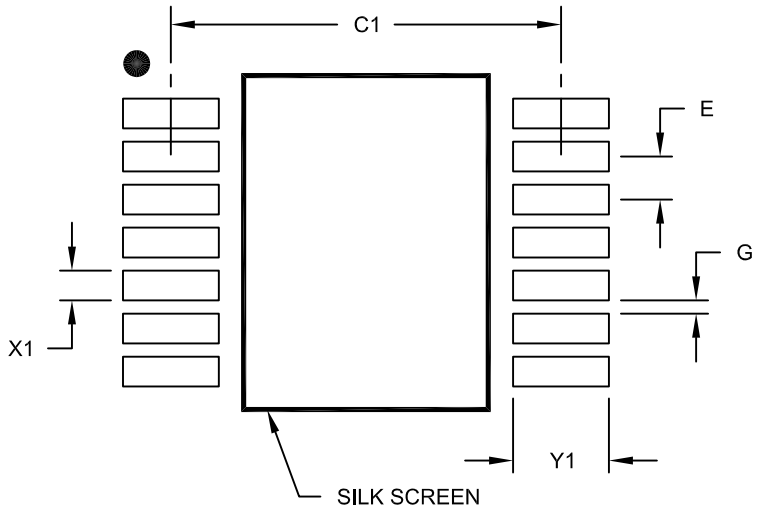
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-087C Sheet 2 of 2

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X14)	X1			0.45
Contact Pad Length (X14)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2087A

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APPENDIX A: REVISION HISTORY

Revision D (December 2011)

The following is the list of modifications:

1. Added the SC70-5 and SOT-23-5 packages for the MCP6H01 device and updated all related information throughout the document.

Revision C (March 2011)

The following is the list of modifications:

1. Added new device MCP6H04.
2. Updated Table 3-1 with MCP6H04 pin names and details.

Revision B (October 2010)

The following is the list of modifications:

1. Updated **Section 4.1 “Inputs”.**

Revision A (March 2010)

- Original Release of this Document.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-X	/XX
Device	Temperature Range	Package

Device:

MCP6H01T:	Single Op Amp (Tape and Reel) (SC-70, SOT-23)
MCP6H01:	Single Op Amp
MCP6H01T:	Single Op Amp (Tape and Reel) (SOIC and 2x3 TDFN)
MCP6H02:	Dual Op Amp
MCP6H02T:	Dual Op Amp (Tape and Reel) (SOIC and 2x3 TDFN)
MCP6H04:	Quad Op Amp
MCP6H04T:	Quad Op Amp (Tape and Reel) (SOIC and TSSOP)

Temperature Range: E = -40°C to +125°C

Package:

LT	=	Plastic Package (SC-70), 5-lead
OT	=	Plastic Small Outline Transistor (SOT-23), 5-lead
MNY *	=	Plastic Dual Flat, No Lead, (2x3 TDFN) 8-lead
SN	=	Lead Plastic Small Outline (150 mil Body), 8-lead
SL	=	Plastic Small Outline, (150 mil Body), 14-lead
ST	=	Plastic Thin Shrink Small Outline (150 mil Body), 14-lead

* Y = Nickel palladium gold manufacturing designator. Only available on the TDFN package.

Examples:

a)	MCP6H01T-E/LT:	Tape and Reel, 5LD SC70 pkg
b)	MCP6H01T-E/OT:	Tape and Reel, 5LD SOT-23 pkg
c)	MCP6H01-E/SN:	8LD SOIC pkg
d)	MCP6H01T-E/SN:	Tape and Reel, 8LD SOIC pkg
e)	MCP6H01T-E/MNY:	Tape and Reel, 8LD 2x3 TDFN pkg
f)	MCP6H02-E/SN:	8LD SOIC pkg
g)	MCP6H02T-E/SN:	Tape and Reel, 8LD SOIC pkg
h)	MCP6H02T-E/MNY:	Tape and Reel 8LD 2x3 TDFN pkg
i)	MCP6H04-E/SL:	14LD SOIC pkg
j)	MCP6H04T-E/SL:	Tape and Reel, 14LD SOIC pkg
k)	MCP6H04-E/ST:	14LD SOIC pkg
l)	MCP6H04T-E/ST:	Tape and Reel, 14LD TSSOP pkg

NOTES:

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