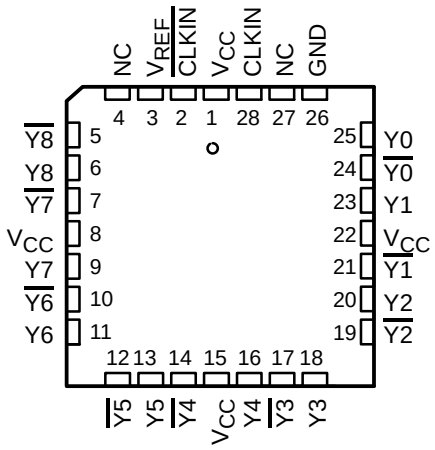
- **Low-Output Skew for Clock-Distribution Applications**
- **Differential Low-Voltage Pseudo-ECL (LVPECL) Compatible Inputs and Outputs**
- **Distributes Differential Clock Inputs to Nine Differential Clock Outputs**
- **Output Reference Voltage (V_{REF}) Allows Distribution From a Single-Ended Clock Input**
- **Packaged In a 28-Pin Plastic Chip Carrier**

FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The differential LVPECL clock-driver circuit distributes one pair of differential LVPECL clock inputs (CLKIN, $\overline{\text{CLKIN}}$) to nine pairs of differential clock (Y, $\overline{\text{Y}}$) outputs with minimum skew for clock distribution. It is specifically designed for driving 50-Ω transmission lines.

The V_{REF} output can be strapped to the $\overline{\text{CLKIN}}$ input for a single-ended CLKIN input.

The CDCVF111 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

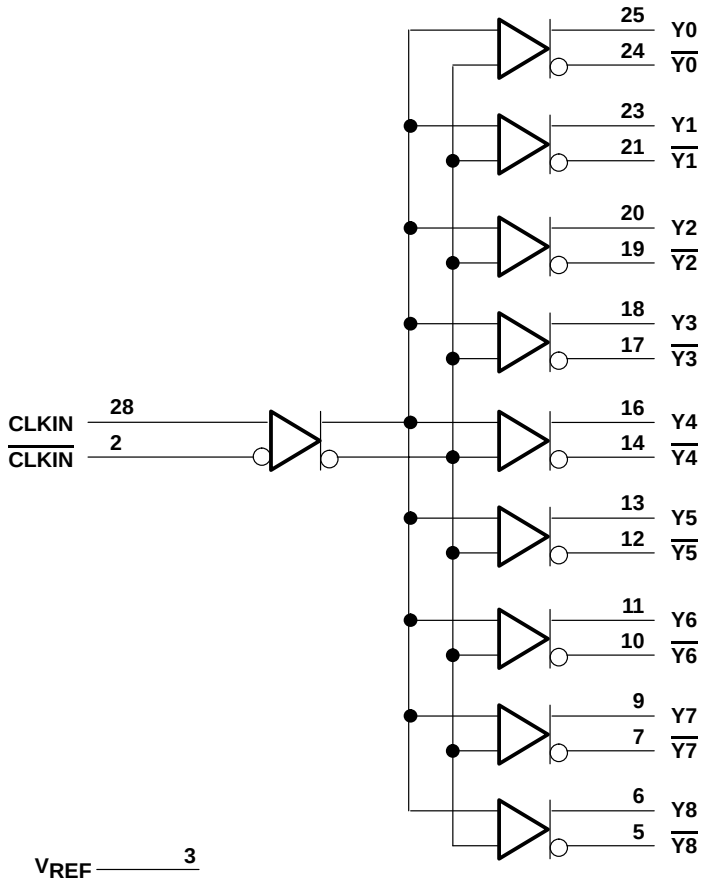
INPUTS		OUTPUTS	
CLKIN	$\overline{\text{CLKIN}}$	Yn	$\overline{\text{Yn}}$
X	X	L	H
L	H	L	H
H	L	H	L
L	V_{REF}	L	H
H	V_{REF}	H	L
V_{REF}	L	H	L
V_{REF}	H	L	H

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . –18 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . –50 mA
Continuous current through V_{CC} or GND . . . . . ± 80 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) . . . . . 525 mW
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 3 V to 3.6 V	V_{CC}–1.165	V_{CC}–0.88	V
		V_{CC} = 3.3 V	2.135	2.42	V
V_{IL}	Low-level input voltage	V_{CC} = 3 V to 3.6 V	V_{CC}–1.81	V_{CC}–1.475	V
		V_{CC} = 3.3 V	1.49	1.825	V
T_A	Operating free-air temperature		–40	85	°C
f_{clock}	Input frequency			650	MHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
V_{REF}	V_{CC} = 3 V to 3.6 V	I_{REF} = 100 µA	V_{CC}–1.38	V_{CC}–1.26	V
	V_{CC} = 3.3 V		1.92	2.04	
V_{OH}	V_{CC} = 3 V to 3.6 V, T_A = 0°C to 85°C, $f_{(max)}$ = 650 MHz		V_{CC}–1.12	V_{CC}–0.83	V
	V_{CC} = 3 V to 3.6 V, T_A = –40°C to 85°C, $f_{(max)}$ = 650 MHz		V_{CC}–1.15	V_{CC}–0.83	
	V_{CC} = 3.3 V		2.275	2.42	
V_{OL}	V_{CC} = 3 V to 3.6 V T_A = 0°C to 85°C, $f_{(max)}$ = 650 MHz		V_{CC}–1.86	V_{CC}–1.49	
	V_{CC} = 3 V to 3.6 V, T_A = –40°C to 85°C, $f_{(max)}$ = 650 MHz		V_{CC}–1.86	V_{CC}–1.52	
	V_{CC} = 3.3 V		1.49	1.68	
I_I	V_I = 2.4 V,	V_{CC} = 3 .6 V		150	µA
I_{CC} (Internal)	I_O = 0,	V_{CC} = 3 .6 V		100	mA

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (see Figure 1 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{PLH}	CLKIN, $\overline{\text{CLKIN}}$	Y, $\overline{\text{Y}}$	450	600	ps
t_{PHL}					
$t_{sk(o)}$		Y, $\overline{\text{Y}}$		50	ps
$t_{sk(pr)}$		Y, $\overline{\text{Y}}$		150	ps
t_r		Y, $\overline{\text{Y}}$	200	600	ps
t_f					

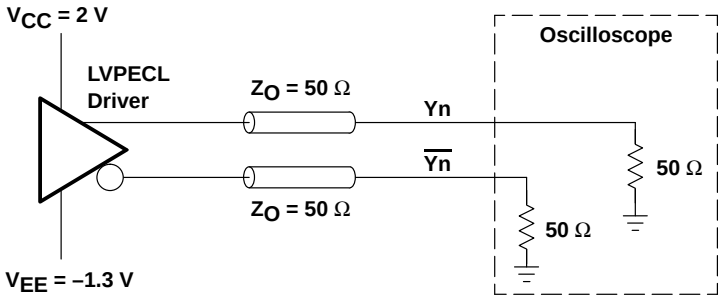
ESD information

ESD MODELS	LIMIT
Human Body Model (HBM)	2.0 kV
Machine Model (MM)	200 V
Charge Device Model (CDM)	2.0 kV

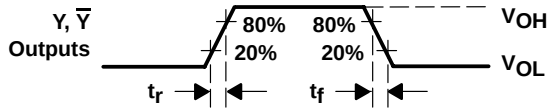
thermal information

CDCVF111 28-PIN PLCC			THERMAL AIR FLOW (CFM)				UNIT
			0	150	250	500	
$R_{\theta JA}$	High K		48	44	42	39	°C/W
$R_{\theta JA}$	Low K		70	58	52	46	°C/W
$R_{\theta JC}$	High K	22					°C/W
$R_{\theta JC}$	Low K	28					°C/W

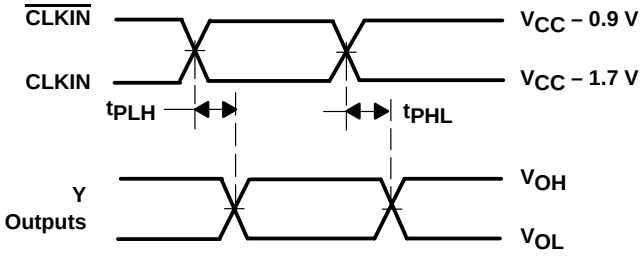
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT (See Note B)



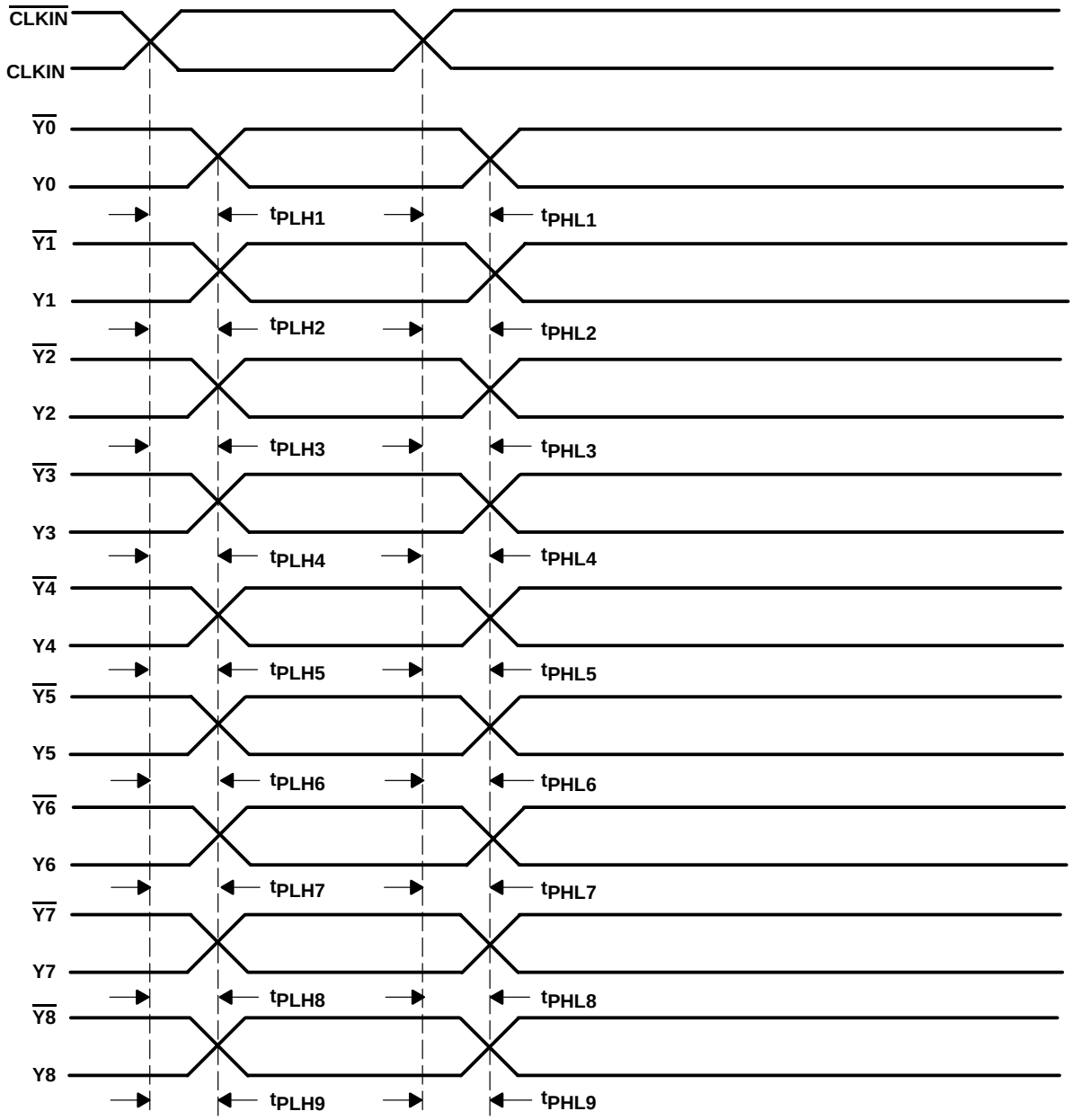
VOLTAGE WAVEFORMS
RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 45 MHz, Z_O = 50 Ω, t_r ≤ 1 ns, t_f ≤ 1 ns.
B. For additonal signal interface, see the *Interfacing Between LVPECL, LVDS, and CML* application note, Literature Number SCAA056.

Figure 1. Load Circuit and Voltage Waveforms



NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest t_{PLHn} (n = 1, 2, . . . 9)
- The difference between the fastest and slowest t_{PHLn} (n = 1, 2, . . . 9)

B. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
- The difference between the fastest and slowest t_{PLHn} (n = 1, 2, . . . 9)
- The difference between the fastest and slowest t_{PHLn} (n = 1, 2, . . . 9) across multiple devices

C. For additional information on skew and propagation delay parameters, see the *Defining Skew, Propagation Delay, Phase-Offset (Phase Error)* application note, literature number SCAA055.

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(pr)}$

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CDCVF111FN	ACTIVE	PLCC	FN	28	37	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCVF111	Samples
CDCVF111FNG4	ACTIVE	PLCC	FN	28	37	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCVF111	Samples
CDCVF111FNR	ACTIVE	PLCC	FN	28	750	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCVF111	Samples
CDCVF111FNRG4	ACTIVE	PLCC	FN	28	750	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCVF111	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

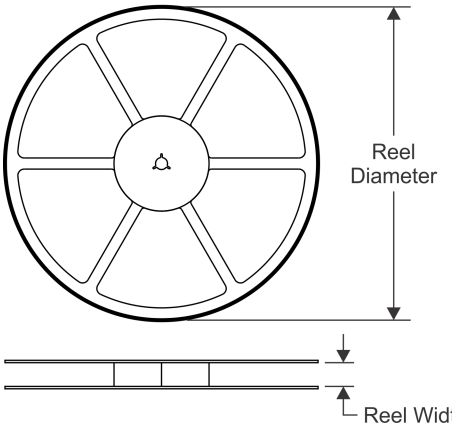
(4) Only one of markings shown within the brackets will appear on the physical device.

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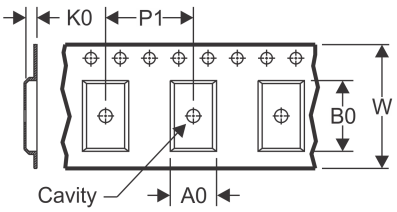
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

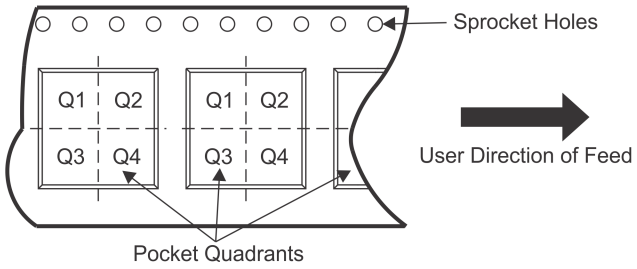


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

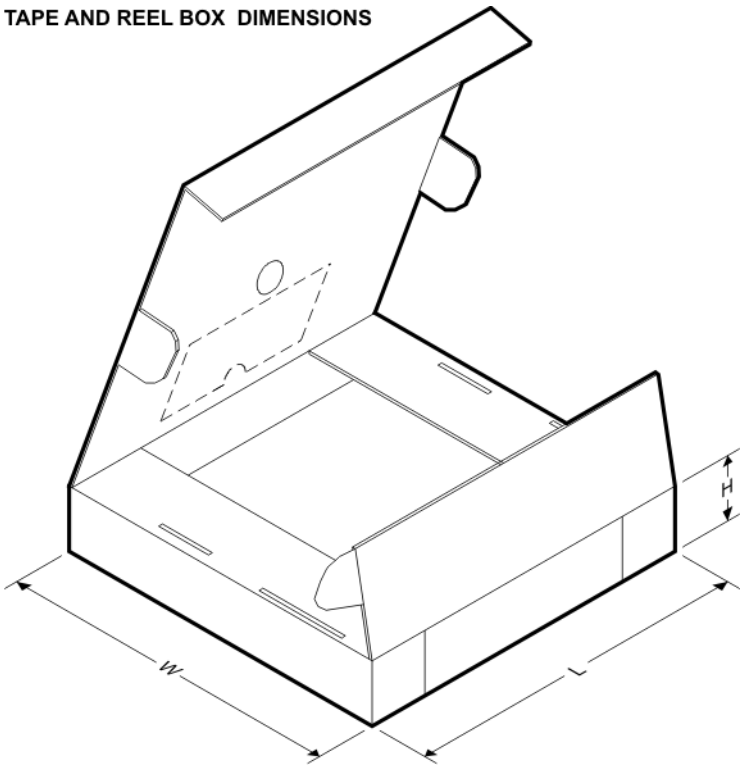
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCVF111FNR	PLCC	FN	28	750	330.0	24.4	12.95	12.95	5.0	16.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

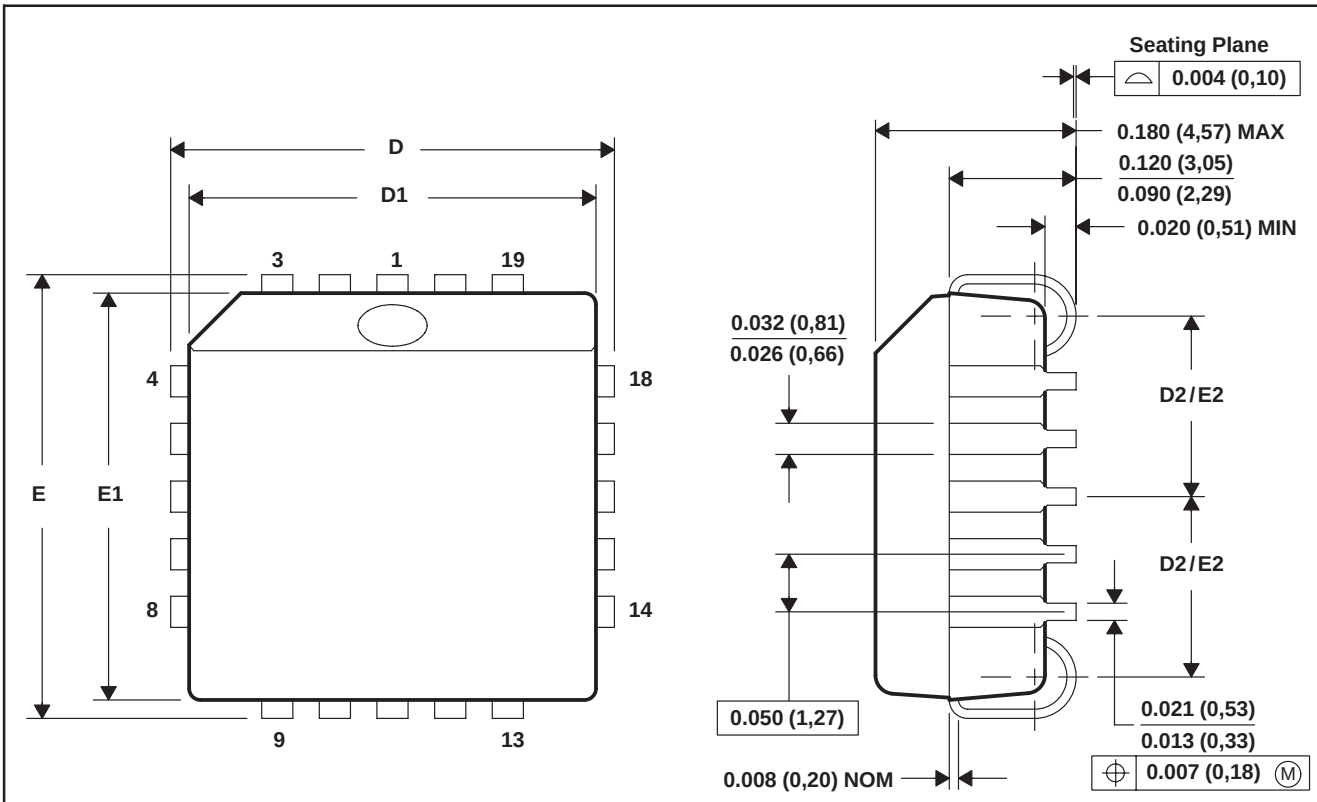
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCVF111FNR	PLCC	FN	28	750	346.0	346.0	41.0

MPLC004A – OCTOBER 1994

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

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