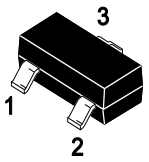
LP2128LT1G

20V P-Channel Enhancement-Mode MOSFET

1. FEATURES

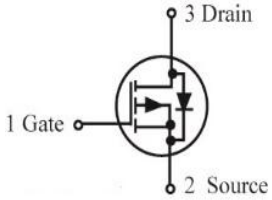
- VDS =-20V
- Advanced trench process technology
- High Density Cell Design For Ultra Low On-Resistance
- Fully Characterized Avalanche Voltage and Current
- Improved Shoot-Through FOM
- We declare that the material of product compliance with RoHS requirements and Halogen Free.



SOT23(TO-236)

2. APPLICATIONS

- Simple Drive Requirement
- Small Package Outline
- Surface Mount Device



3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LP2128LT1G	PA2	3000/Tape&Reel
LP2128LT3G	PA2	10000/Tape&Reel

4. MAXIMUM RATINGS(Ta = 25ºC)

Parameter	Symbol	Limits	Unit
Drain–Source Voltage	VDSS	-20	V
Gate–to–Source Voltage	VGS	±12	V
Drain Current(Note 1) – Continuous TA = 25°C – Pulsed	 ID IDM	 -6 -24	A
Avalanche Current(L=0.1mH)	IAS	12	A
Avalanche Energy(L=0.1mH)	EAS	7.3	mJ

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Total Device Dissipation FR–5 Board@Ta=25℃	PD	1100	mW
Thermal Resistance, Junction–to–Ambient	RΘJA	110	ºC/W
Junction and Storage temperature	TJ,Tstg	−55~+150	°C

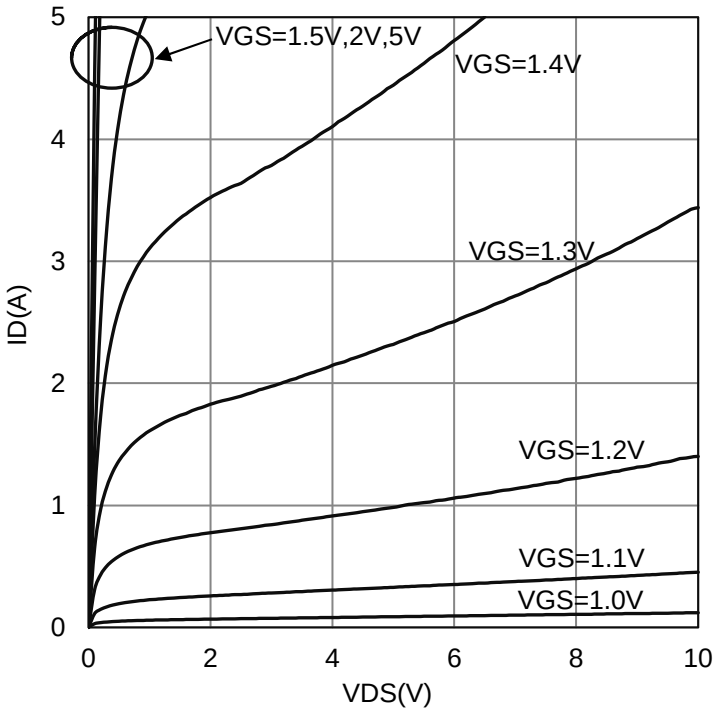
1.Repetitive Rating: Pulse width limited by the maximum junction temperature

6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

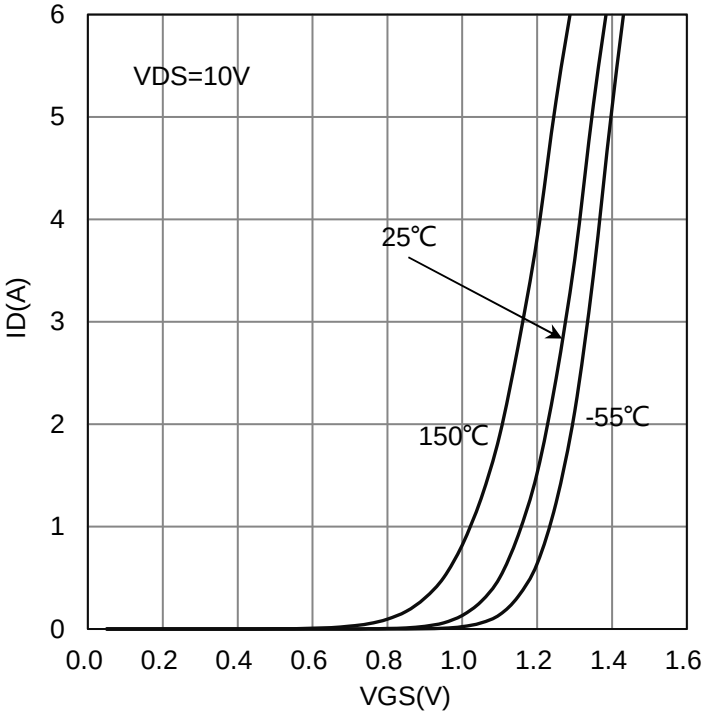
Characteristic		Symbol	Min.	Typ.	Max.	Unit
Static						
Drain–Source Breakdown Voltage (VGS = 0, ID = -250μA)		VBRDSS	-20	-	-	V
Zero Gate Voltage Drain Current (VGS = 0, VDS = -6.4 V)		IDSS	-	-	-1	μA
Gate–Body Leakage Current (VGS = ±12 V,VDS=0V)		IGSS	-	-	±100	nA
Gate Threshold Voltage (VDS = VGS, ID = -250μA)		VGS(th)	-0.45	-	-0.9	V
Static Drain–Source On–State Resistance (VGS = -4.5 V, ID = -2.4 A) (VGS = -2.5 V, ID = -2 A) (VGS = -1.8 V, ID = -1 A)		RDS(on)	- - -	17 25 47	28 41 78	mΩ
Forward Transconductance (VDS = -5V, ID = -3.5A)		gfs	-	8.5	-	S
On-State Drain Current (VDS≤ –5 V, VGS = –4.5 V) (VDS≤ –5 V, VGS = –2.5 V)		ID(on)	-6 -3	- -	- -	A
Source-Drain Diode						
Max. Diode Forward Current		IS	-	-1.6	-	A
Diode Forward Voltage (IS = -1.6A, VGS = 0V)		VSD	-	-	-1.2	V
Dynamic(Note 2)						
Input Capacitance (VGS = 0 V, f = 1.0MHz,VDS= -4 V)		Ciss	-	1038	-	pF
Output Capacitance (VGS = 0 V, f = 1.0MHz,VDS= -4 V)		Coss	-	110	-	pF
Reverse Transfer Capacitance (VGS = 0 V, f = 1.0MHz,VDS= -4 V)		Crss	-	92	-	pF
Total Gate Charge	(VDS=-10V,VGS=-4.5V,ID=-2.4A)	Qg	-	11	-	nC
Gate to Source Charg		Qgs	-	1.7	-	
Gate to Drain Charge		Qgd	-	2.5	-	
Gate Resistance (VDS=0V,VGS=0V,f=1.0MHz)		Rg	-	9.3	-	Ω
Switching(Note 2)						
Turn-On Delay Time	(VDD=-4V,RL=4Ω,RG=6.2Ω,VGEN=-4.5V,ID=-1A)	td(on)	-	6.2	-	ns
Rise Time		tr	-	14.4	-	
Turn-Off Delay Time		td(off)	-	46	-	
Fall Time		tf	-	24	-	

2.Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

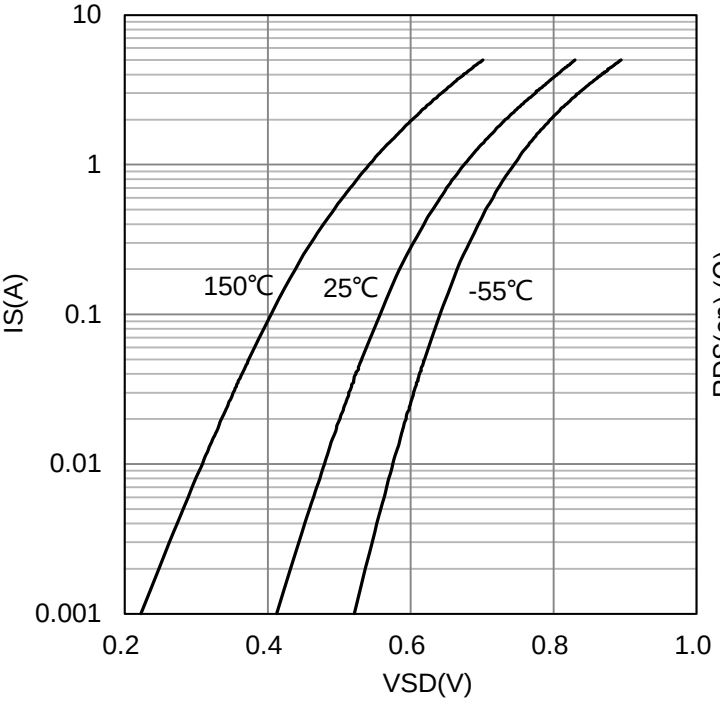
7.ELECTRICAL CHARACTERISTICS CURVES



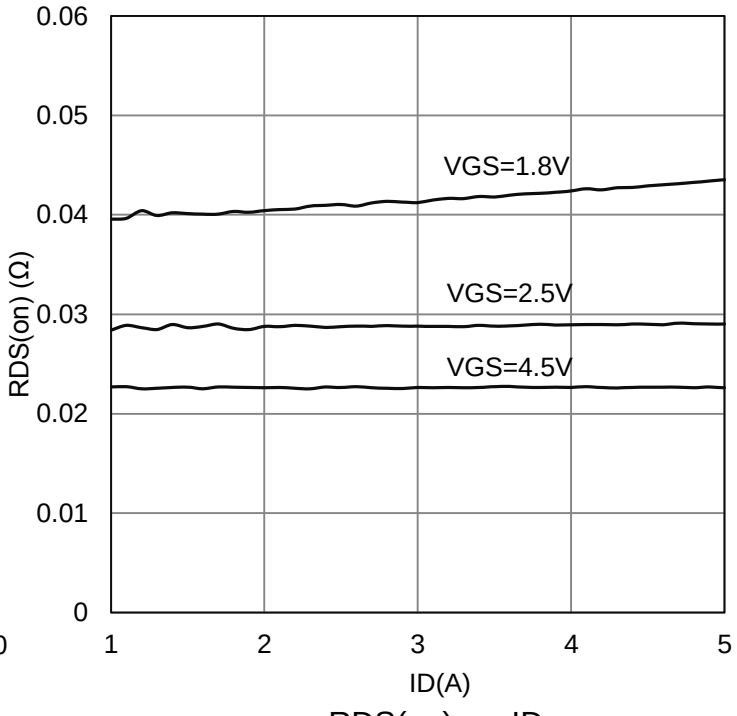
ID vs. VDS



ID vs. VGS

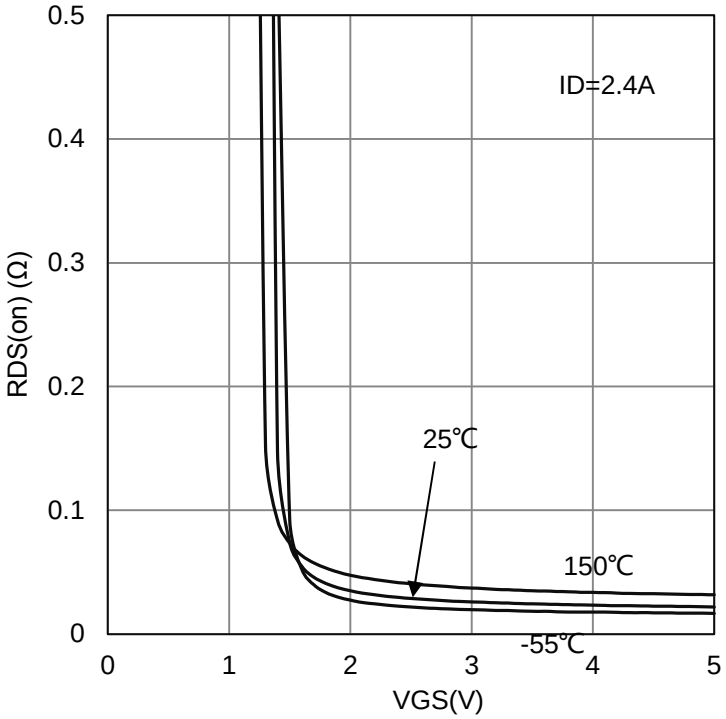


IS vs. VSD

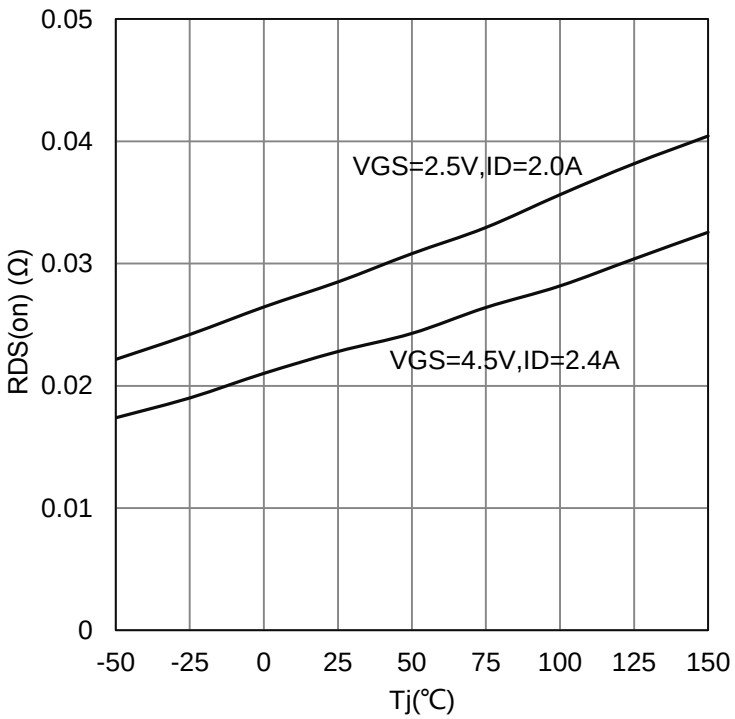


RDS(on) vs. ID

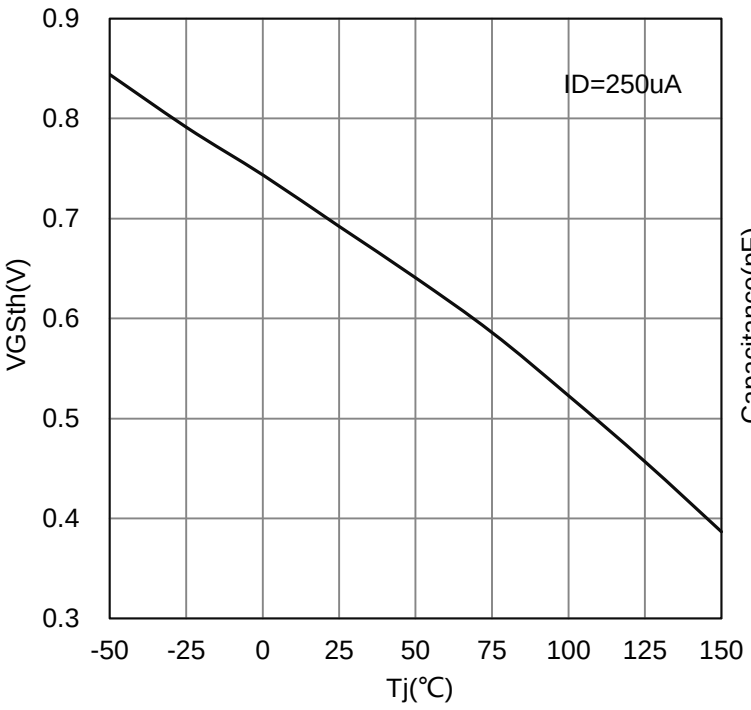
7.ELECTRICAL CHARACTERISTICS CURVES(Con.)



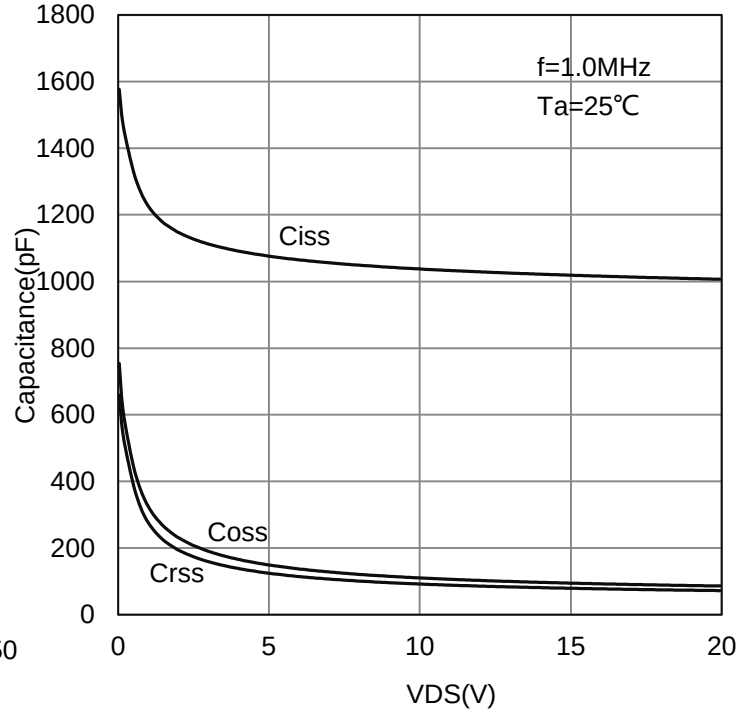
RDS(on) vs. VGS



RDS(on) vs. Tj

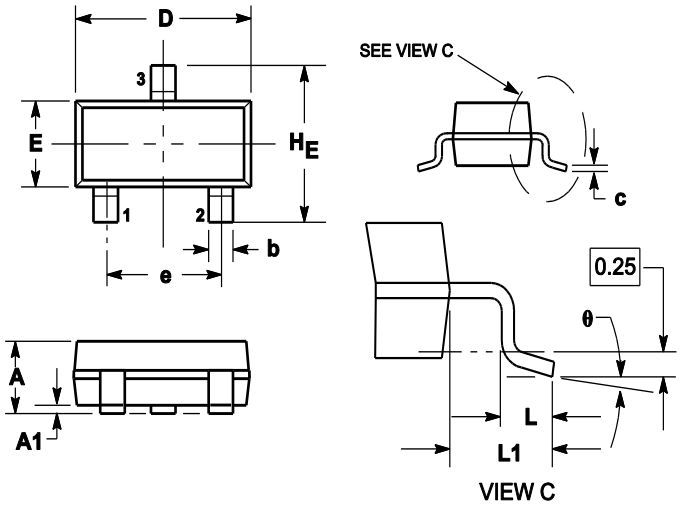


VGSth vs. Tj



Capacitance

8.OUTLINE AND DIMENSIONS



Notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1	1.11	0.035	0.04	0.044
A1	0.01	0.06	0.1	0.001	0.002	0.004
b	0.37	0.44	0.5	0.015	0.018	0.02
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.9	3.04	0.11	0.114	0.12
E	1.20	1.3	1.4	0.047	0.051	0.055
e	1.78	1.9	2.04	0.07	0.075	0.081
L	0.10	0.2	0.3	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.4	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

9.SOLDERING FOOTPRINT

