Current Mode PWM Controller

FEATURES

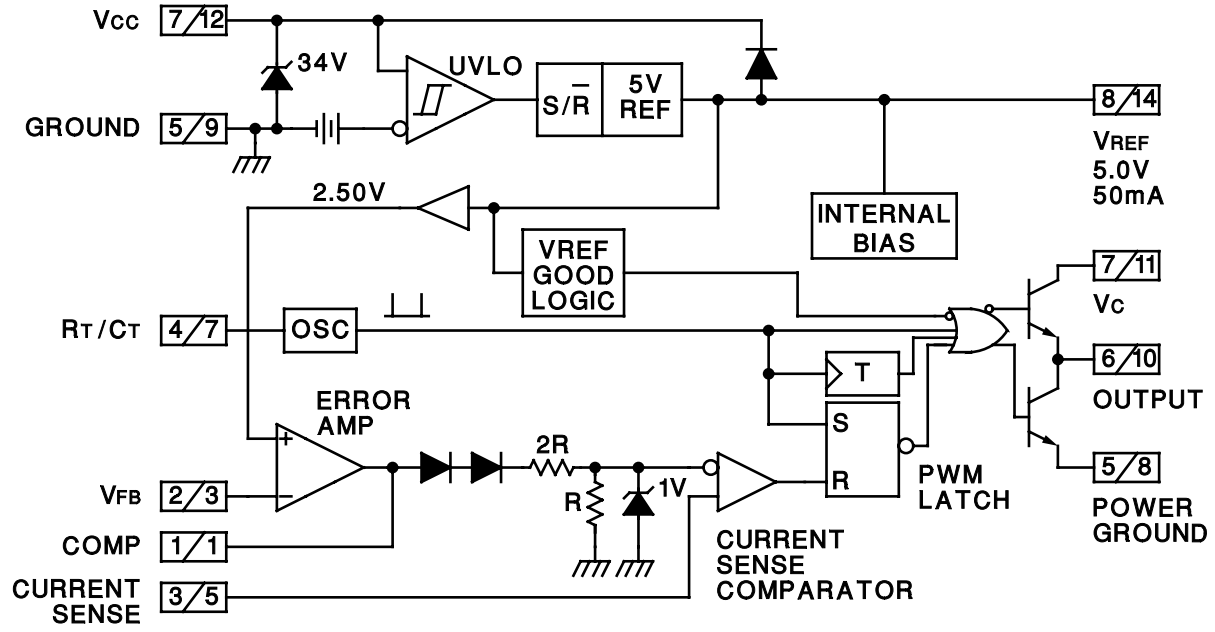
- Optimized For Off-line And DC To DC Converters
- Low Start Up Current (<1mA)
- Automatic Feed Forward Compensation
- Pulse-by-pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-voltage Lockout With Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500khz Operation
- Low RO Error Amp

DESCRIPTION

The UC1842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N Channel MOSFETs, is low in the off state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of 16V (on) and 10V (off), ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.4V and 7.6V. The UC1842 and UC1843 can operate to duty cycles approaching 100%. A range of zero to 50% is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

BLOCK DIAGRAM



Note 1: A/B A = DIL-8 Pin Number. B = SO-14 and CFP-14 Pin Number.
Note 2: Toggle flip flop used only in 1844 and 1845.

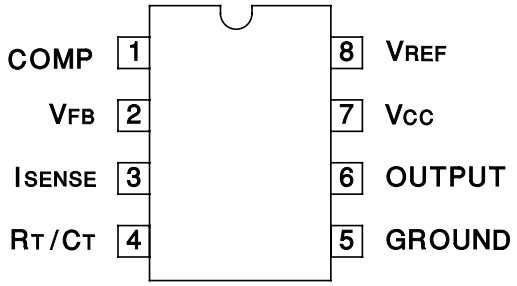
ABSOLUTE MAXIMUM RATINGS(Note 1)

Supply Voltage (Low Impedance Source) 30V
Supply Voltage (I_{CC} < 30mA) . . . . . Self Limiting
Output Current. . . . . ±1A
Output Energy (Capacitive Load) . . . . . 5 µJ
Analog Inputs (Pins 2, 3). . . . . -0.3V to +6.3V
Error Amp Output Sink Current . . . . . 10 mA
Power Dissipation at $T_A \leq 25°C$ (DIL–8) . . . . . 1 W
Power Dissipation at $T_A \leq 25°C$ (SOIC-14) . . . . . 725 mW
Storage Temperature Range. . . . . -65°C to +150°C
Junction Temperature Range . . . . . -55°C to +150°C
Lead Temperature (soldering, 10 seconds). . . . . 300°C

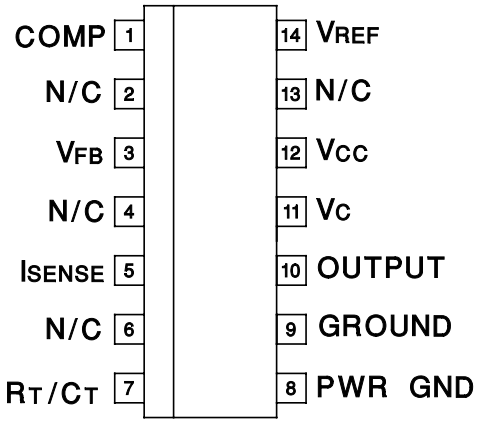
Note 1: All voltages are with respect to Pin 5.
All currents are positive into the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

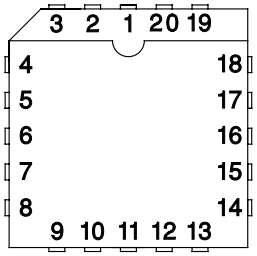
DIL-8, SOIC-8 (TOP VIEW)
N or J Package, D8 Package



SOIC-14, CFP-14. (TOP VIEW)
D or W Package



PLCC-20 (TOP VIEW)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
N/C	1
COMP	2
N/C	3
N/C	4
V_{FB}	5
N/C	6
I_{SENSE}	7
N/C	8
N/C	9
R_T/C_T	10
N/C	11
PWR GND	12
GROUND	13
N/C	14
OUTPUT	15
N/C	16
V_C	17
V_{CC}	18
N/C	19
V_{REF}	20

DISSIPATION RATING TABLE

Package	TA ≤ 25°C Power Rating	Derating Factor Above TA ≤ 25°C	TA ≤ 70°C Power Rating	TA ≤ 85°C Power Rating	TA ≤ 125°C Power Rating
W	700 mW	5.5 mW/°C	452 mW	370 mW	150 mW

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for -55°C ≤ T_A ≤ 125°C for the UC184X; -40°C ≤ T_A ≤ 85°C for the UC284X; 0°C ≤ T_A ≤ 70°C for the 384X; V_{CC} = 15V (Note 5); R_T = 10k; C_T = 3.3nF, T_A=T_J.

PARAMETER	TEST CONDITIONS	UC1842/3/4/5 UC2842/3/4/5			UC3842/3/4/5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T_J = 25°C, I_O = 1mA	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	12 ≤ V_{IN} ≤ 25V		6	20		6	20	mV
Load Regulation	1 ≤ I_O ≤ 20mA		6	25		6	25	mV
Temp. Stability	(Note 2) (Note 7)		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temp. (Note 2)	4.9		5.1	4.82		5.18	V
Output Noise Voltage	10Hz ≤ f ≤ 10kHz, T_J = 25°C (Note2)		50			50		µV
Long Term Stability	T_A = 125°C, 1000Hrs. (Note 2)		5	25		5	25	mV
Output Short Circuit		-30	-100	-180	-30	-100	-180	mA
Oscillator Section								
Initial Accuracy	T_J = 25°C (Note 6)	47	52	57	47	52	57	kHz
Voltage Stability	12 ≤ V_{CC} ≤ 25V		0.2	1		0.2	1	%
Temp. Stability	T_{MIN} ≤ T_A ≤ T_{MAX} (Note 2)		5			5		%
Amplitude	$V_{PIN\ 4}$ peak to peak (Note 2)		1.7			1.7		V
Error Amp Section								
Input Voltage	$V_{PIN\ 1}$ = 2.5V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			-0.3	-1		-0.3	-2	µA
A_{VOL}	2 ≤ V_O ≤ 4V	65	90		65	90		dB
Unity Gain Bandwidth	(Note 2) T_J = 25°C	0.7	1		0.7	1		MHz
PSRR	12 ≤ V_{CC} ≤ 25V	60	70		60	70		dB
Output Sink Current	$V_{PIN\ 2}$ = 2.7V, $V_{PIN\ 1}$ = 1.1V	2	6		2	6		mA
Output Source Current	$V_{PIN\ 2}$ = 2.3V, $V_{PIN\ 1}$ = 5V	-0.5	-0.8		-0.5	-0.8		mA
V_{OUT} High	$V_{PIN\ 2}$ = 2.3V, R_L = 15k to ground	5	6		5	6		V
V_{OUT} Low	$V_{PIN\ 2}$ = 2.7V, R_L = 15k to Pin 8		0.7	1.1		0.7	1.1	V
Current Sense Section								
Gain	(Notes 3 and 4)	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal	$V_{PIN\ 1}$ = 5V (Note 3)	0.9	1	1.1	0.9	1	1.1	V
PSRR	12 ≤ V_{CC} ≤ 25V (Note 3) (Note 2)		70			70		dB
Input Bias Current			-2	-10		-2	-10	µA
Delay to Output	$V_{PIN\ 3}$ = 0 to 2V (Note 2)		150	300		150	300	ns

Note 2: These parameters, although guaranteed, are not 100% tested in production.
Note 3: Parameter measured at trip point of latch with $V_{PIN\ 2}$ = 0.
Note 4: Gain defined as

$$A = \frac{\Delta\ VPIN\ 1}{\Delta\ VPIN\ 3},\ 0 \le VPIN\ 3 \le 0.8V$$

Note 5: Adjust V_{CC} above the start threshold before setting at 15V.
Note 6: Output frequency equals oscillator frequency for the UC1842 and UC1843.
Output frequency is one half oscillator frequency for the UC1844 and UC1845.
Note 7: Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

$$Temp\ Stability = \frac{V_{REF}\ (max) - VREF\ (min)}{TJ\ (max) - TJ\ (min)}$$

V_{REF} (max) and V_{REF} (min) are the maximum and minimum reference voltages measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for –55°C ≤ T_A ≤ 125°C for the UC184X; –40°C ≤ T_A ≤ 85°C for the UC284X; 0°C ≤ T_A ≤ 70°C for the 384X; V_{CC} = 15V (Note 5); R_T = 10k; C_T = 3.3nF, T_A=T_J.

PARAMETER	TEST CONDITION	UC1842/3/4/5 UC2842/3/4/5			UC3842/3/4/5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Section								
Output Low Level	I_{SINK} = 20mA		0.1	0.4		0.1	0.4	V
	I_{SINK} = 200mA		1.5	2.2		1.5	2.2	V
Output High Level	I_{SOURCE} = 20mA	13	13.5		13	13.5		V
	I_{SOURCE} = 200mA	12	13.5		12	13.5		V
Rise Time	T_J = 25°C, C_L = 1nF (Note 2)		50	150		50	150	ns
Fall Time	T_J = 25°C, C_L = 1nF (Note 2)		50	150		50	150	ns
Under-voltage Lockout Section								
Start Threshold	X842/4	15	16	17	14.5	16	17.5	V
	X843/5	7.8	8.4	9.0	7.8	8.4	9.0	V
Min. Operating Voltage After Turn On	X842/4	9	10	11	8.5	10	11.5	V
	X843/5	7.0	7.6	8.2	7.0	7.6	8.2	V
PWM Section								
Maximum Duty Cycle	X842/3	95	97	100	95	97	100	%
	X844/5	46	48	50	47	48	50	%
Minimum Duty Cycle				0			0	%
Total Standby Current								
Start-Up Current			0.5	1		0.5	1	mA
Operating Supply Current	$V_{PIN\ 2}$ = $V_{PIN\ 3}$ = 0V		11	17		11	17	mA
V_{CC} Zener Voltage	I_{CC} = 25mA	30	34		30	34		V

Note 2: These parameters, although guaranteed, are not 100% tested in production.

Note 3: Parameter measured at trip point of latch with $V_{PIN\ 2}$ = 0

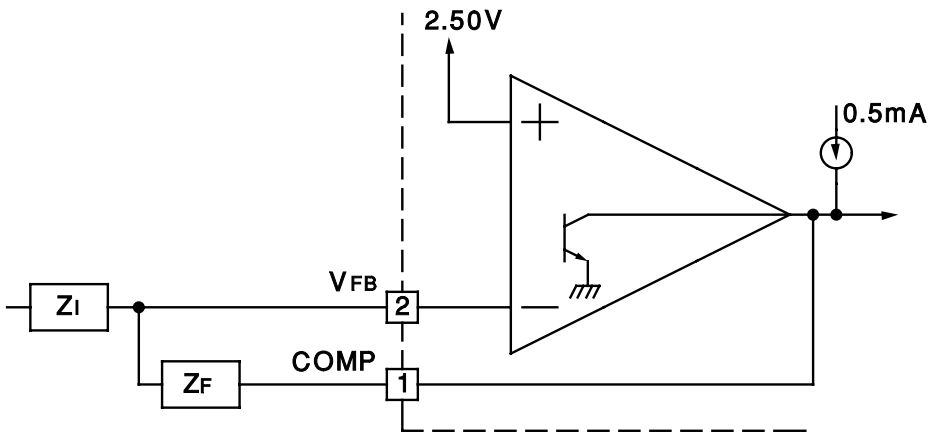
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Note 4: Gain defined as: $A = \frac{\Delta\ VPIN\ 1}{\Delta\ VPIN\ 3}; 0 \le VPIN\ 3 \le 0.8V$.

Note 5: Adjust V_{CC} above the start threshold before setting at 15V.

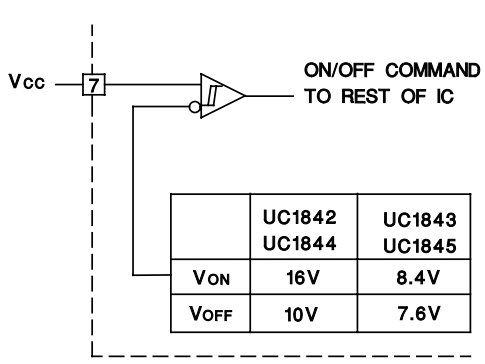
Note 6: Output frequency equals oscillator frequency for the UC1842 and UC1843.
Output frequency is one half oscillator frequency for the UC1844 and UC1845.

ERROR AMP CONFIGURATION

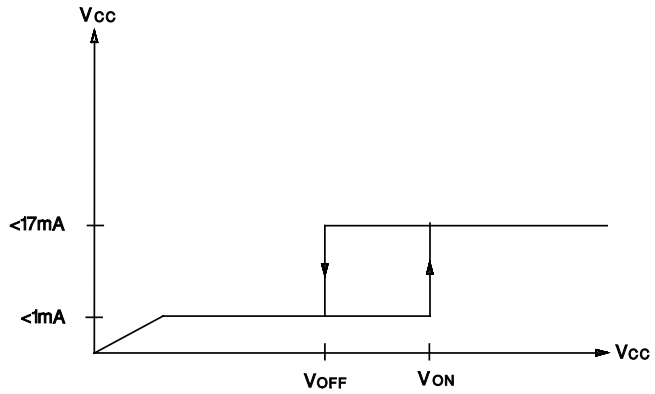


Error Amp can Source or Sink up to 0.5mA

UNDER-VOLTAGE LOCKOUT

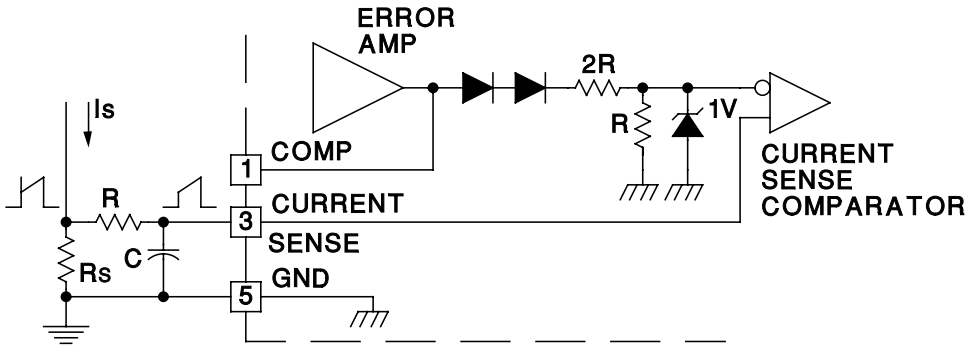


	UC1842 UC1844	UC1843 UC1845
VON	16V	8.4V
VOFF	10V	7.6V



During under-voltage lock-out, the output driver is biased to sink minor amounts of current. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with extraneous leakage currents.

CURRENT SENSE CIRCUIT

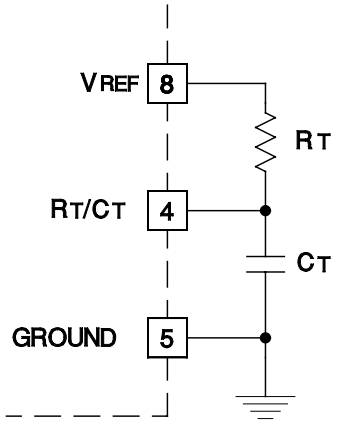


Peak Current (Is) is Determined By The Formula

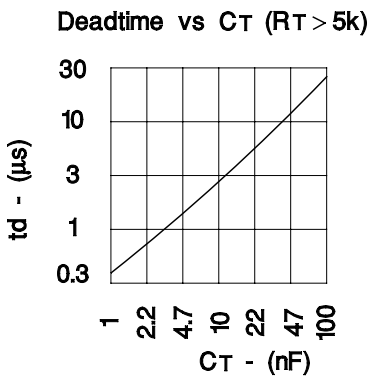
$$I_{SMAX} \approx \frac{1.0V}{RS}$$

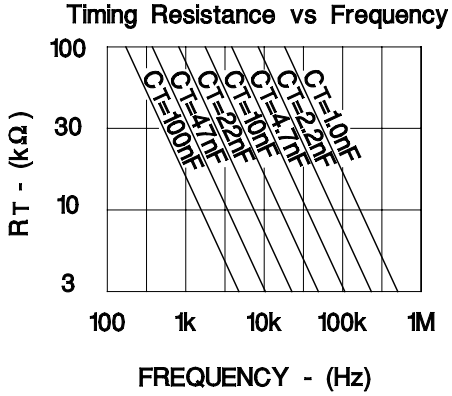
A small RC filter may be required to suppress switch transients.

OSCILLATOR SECTION

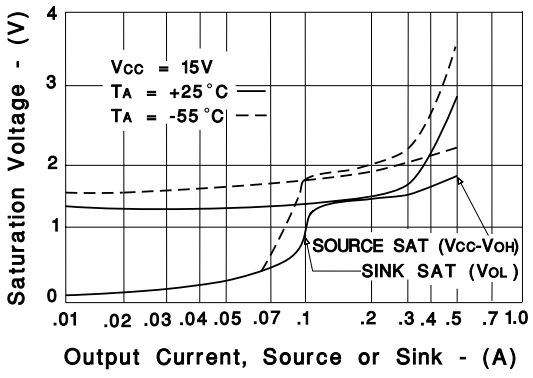


For $R_T > 5k$ $f \approx \frac{1.72}{R_T C_T}$

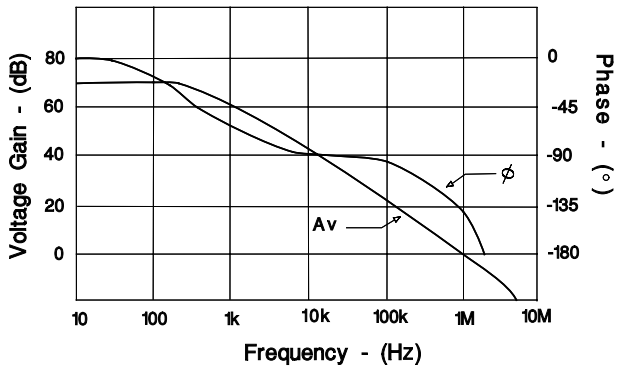




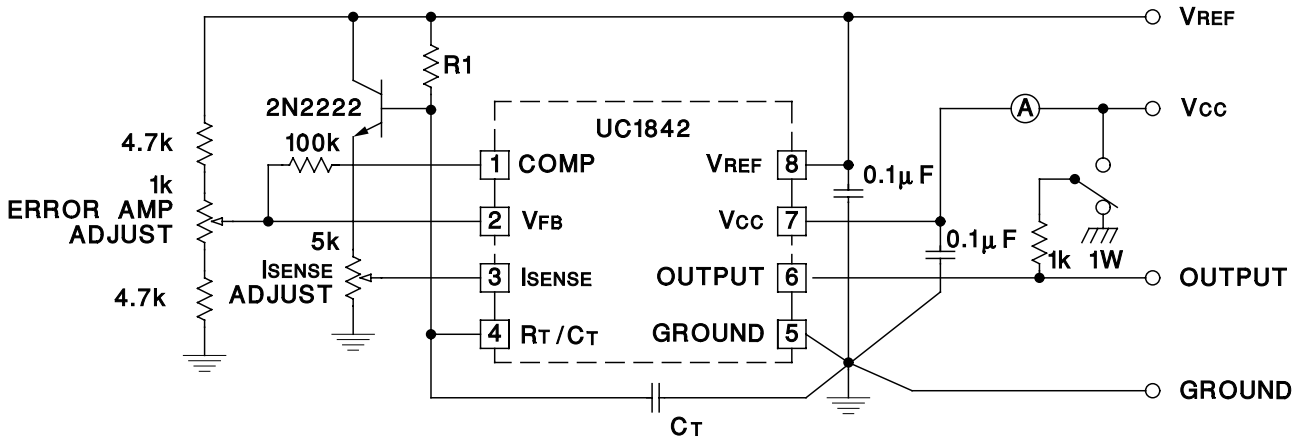
OUTPUT SATURATION CHARACTERISTICS



ERROR AMPLIFIER OPEN-LOOP FREQUENCY RESPONSE

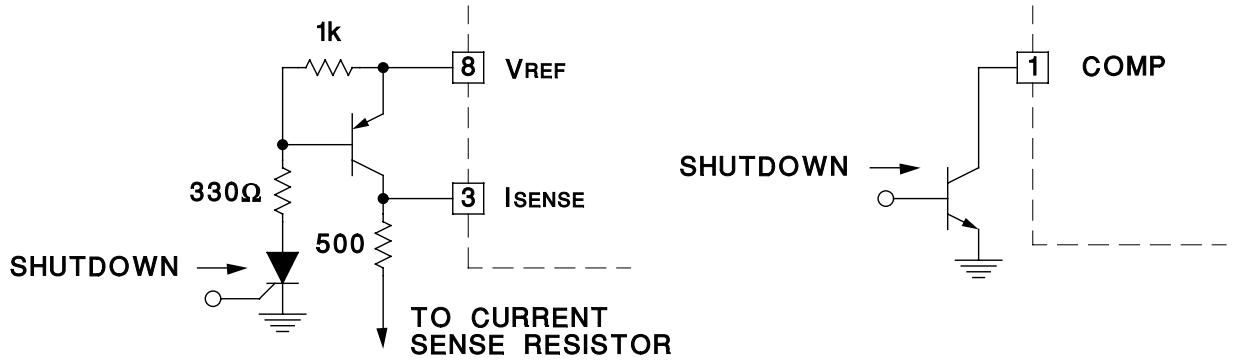


OPEN-LOOP LABORATORY FIXTURE



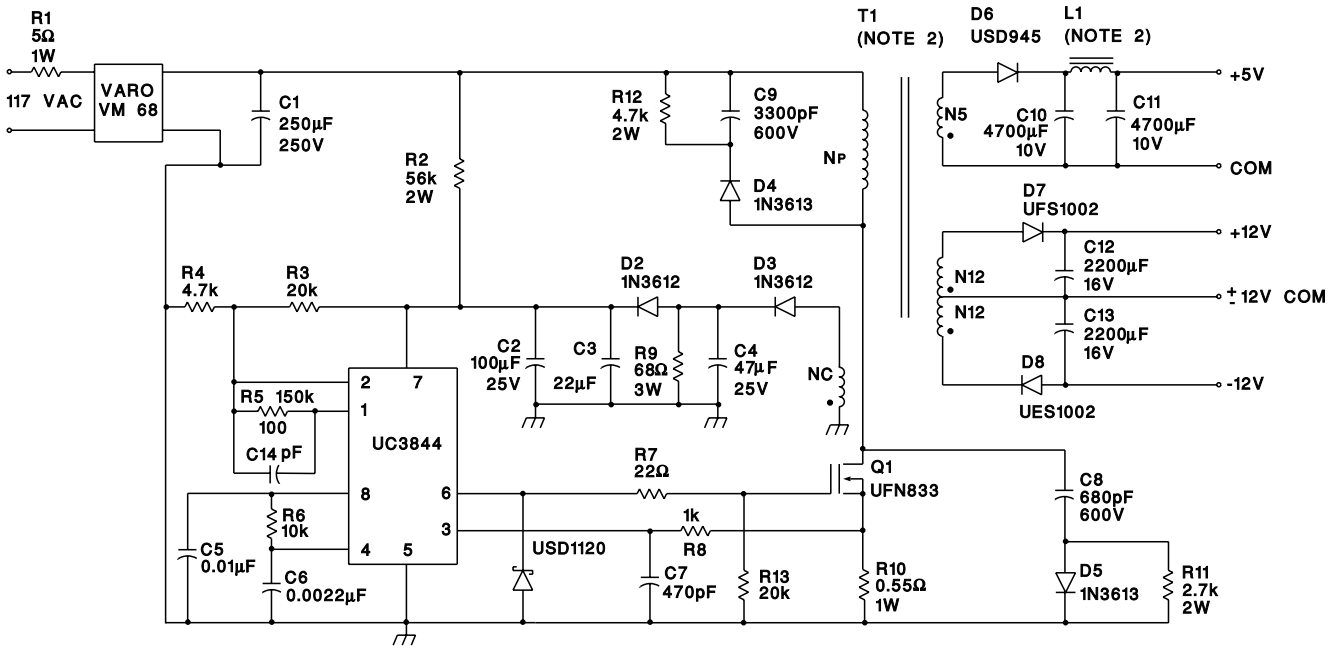
High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

SHUT DOWN TECHNIQUES



Shutdown of the UC1842 can be accomplished by two methods; either raise pin 3 above 1V or pull pin 1 below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pin 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling Vcc below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.

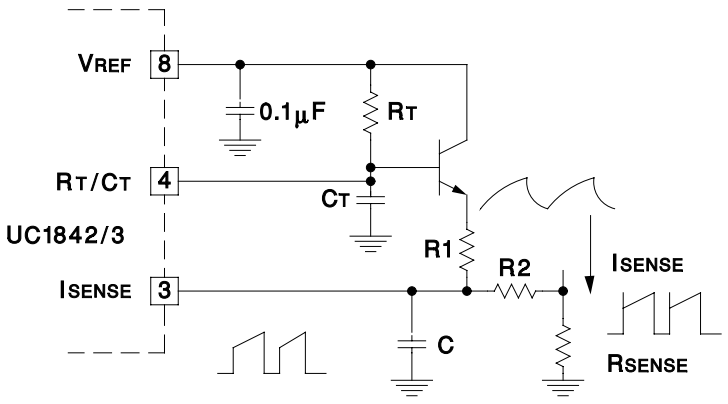
OFFLINE FLYBACK REGULATOR



Power Supply Specifications

1. Input Voltages 5VAC to 130VA (50 Hz/60Hz)
2. Line Isolation 3750V
3. Switching Frequency 40kHz
4. Efficiency at Full Load 70%
5. Output Voltage:
   A. +5V, ±5%; 1A to 4A load
   Ripple voltage: 50mV P-P Max
   B. +12V, ±3%; 0.1A to 0.3A load
   Ripple voltage: 100mV P-P Max
   C. -12V ,±3%; 0.1A to 0.3A load
   Ripple voltage: 100mV P-P Max

SLOPE COMPENSATION



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-8670401PA	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
5962-8670401VPA	ACTIVE	CDIP	JG	8	1	None	Call TI	Level-NC-NC-NC
5962-8670401VXA	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-8670401XA	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
5962-8670402PA	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
5962-8670402VPA	ACTIVE	CDIP	JG	8	1	None	Call TI	Level-NC-NC-NC
5962-8670402VXA	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-8670402XA	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
5962-8670403PA	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
5962-8670403VPA	ACTIVE	CDIP	JG	8	1	None	Call TI	Level-NC-NC-NC
5962-8670403VXA	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-8670403XA	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
5962-8670404PA	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
5962-8670404VPA	ACTIVE	CDIP	JG	8	1	None	Call TI	Level-NC-NC-NC
5962-8670404VXA	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-8670404XA	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
UC1842J	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
UC1842J883B	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
UC1842JQMLV	ACTIVE	CDIP	JG	8		None	Call TI	Call TI
UC1842L883B	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
UC1842W	ACTIVE	CFP	W	14	1	None	A42 SNPB	Level-NC-NC-NC
UC1843J	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
UC1843J883B	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
UC1843JQMLV	ACTIVE	CDIP	JG	8		None	Call TI	Call TI
UC1843L	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
UC1843L883B	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
UC1843LQMLV	ACTIVE	LCCC	FK	20		None	Call TI	Call TI
UC1843W	ACTIVE	CFP	W	14	1	None	A42 SNPB	Level-NC-NC-NC
UC1844J	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
UC1844J883B	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
UC1844JQMLV	ACTIVE	CDIP	JG	8		None	Call TI	Call TI
UC1844L	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
UC1844L883B	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
UC1844LQMLV	ACTIVE	LCCC	FK	20		None	Call TI	Call TI
UC1844W	ACTIVE	CFP	W	14	1	None	A42 SNPB	Level-NC-NC-NC
UC1845J	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
UC1845J883B	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
UC1845JQMLV	ACTIVE	CDIP	JG	8		None	Call TI	Call TI
UC1845L	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
UC1845L883B	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
UC1845LQMLV	ACTIVE	LCCC	FK	20		None	Call TI	Call TI
UC1845W	ACTIVE	CFP	W	14	1	None	A42 SNPB	Level-NC-NC-NC

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UC2842D	ACTIVE	SOIC	D	14	50	None	CU NIPDAU	Level-1-220C-UNLIM
UC2842D8	ACTIVE	SOIC	D	8	75	None	CU NIPDAU	Level-1-220C-UNLIM
UC2842D8TR	ACTIVE	SOIC	D	8	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC2842DR	ACTIVE	SOIC	D	14		None	Call TI	Call TI
UC2842DTR	ACTIVE	SOIC	D	14	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC2842DW	ACTIVE	SOIC	DW	16	40	None	CU NIPDAU	Level-2-220C-1 YEAR
UC2842DWTR	ACTIVE	SOIC	DW	16	2000	None	CU NIPDAU	Level-2-220C-1 YEAR
UC2842J	OBSOLETE	CDIP	JG	8		None	Call TI	Call TI
UC2842N	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU SNPB	Level-NC-NC-NC
UC2842P	OBSOLETE	PDIP	P	8		None	Call TI	Call TI
UC2843D	ACTIVE	SOIC	D	14	50	None	CU NIPDAU	Level-1-220C-UNLIM
UC2843D8	ACTIVE	SOIC	D	8	75	None	CU NIPDAU	Level-1-220C-UNLIM
UC2843D8TR	ACTIVE	SOIC	D	8	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC2843DR	OBSOLETE	SOIC	D	14		None	Call TI	Call TI
UC2843DTR	ACTIVE	SOIC	D	14	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC2843J	OBSOLETE	CDIP	JG	8		None	Call TI	Call TI
UC2843N	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU SNPB	Level-NC-NC-NC
UC2844D	ACTIVE	SOIC	D	14	50	None	CU NIPDAU	Level-1-220C-UNLIM
UC2844D8	ACTIVE	SOIC	D	8	75	None	CU NIPDAU	Level-1-220C-UNLIM
UC2844D8TR	ACTIVE	SOIC	D	8	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC2844DTR	ACTIVE	SOIC	D	14	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC2844N	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU SNPB	Level-NC-NC-NC
UC2845D	ACTIVE	SOIC	D	14	50	None	CU NIPDAU	Level-1-220C-UNLIM
UC2845D8	ACTIVE	SOIC	D	8	75	None	CU NIPDAU	Level-1-220C-UNLIM
UC2845D8TR	ACTIVE	SOIC	D	8	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC2845DTR	ACTIVE	SOIC	D	14	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC2845J	OBSOLETE	CDIP	JG	8		None	Call TI	Call TI
UC2845N	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU SNPB	Level-NC-NC-NC
UC3842D	ACTIVE	SOIC	D	14	50	None	CU NIPDAU	Level-1-220C-UNLIM
UC3842D8	ACTIVE	SOIC	D	8	75	None	CU NIPDAU	Level-1-220C-UNLIM
UC3842D8TR	ACTIVE	SOIC	D	8	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC3842DTR	ACTIVE	SOIC	D	14	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC3842J	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
UC3842N	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU SNPB	Level-NC-NC-NC
UC3842P	OBSOLETE	PDIP	P	8		None	Call TI	Call TI
UC3843D	ACTIVE	SOIC	D	14	50	None	CU NIPDAU	Level-1-220C-UNLIM
UC3843D8	ACTIVE	SOIC	D	8	75	None	CU NIPDAU	Level-1-220C-UNLIM
UC3843D8TR	ACTIVE	SOIC	D	8	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC3843DTR	ACTIVE	SOIC	D	14	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC3843J	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
UC3843N	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU SNPB	Level-NC-NC-NC
UC3843P	OBSOLETE	PDIP	P	8		None	Call TI	Call TI
UC3843QTR	OBSOLETE	PLCC	FN	20		None	Call TI	Call TI
UC3844D	ACTIVE	SOIC	D	14	50	None	CU NIPDAU	Level-1-220C-UNLIM
UC3844D8	ACTIVE	SOIC	D	8	75	None	CU NIPDAU	Level-1-220C-UNLIM
UC3844D8TR	ACTIVE	SOIC	D	8	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC3844DTR	ACTIVE	SOIC	D	14	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC3844J	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
UC3844N	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU SNPB	Level-NC-NC-NC
UC3844P	OBSOLETE	PDIP	P	8		None	Call TI	Call TI
UC3845D	ACTIVE	SOIC	D	14	50	None	CU NIPDAU	Level-1-220C-UNLIM
UC3845D8	ACTIVE	SOIC	D	8	75	None	CU NIPDAU	Level-1-220C-UNLIM
UC3845D8TR	ACTIVE	SOIC	D	8	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC3845DTR	ACTIVE	SOIC	D	14	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC3845J	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
UC3845N	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU SNPB	Level-NC-NC-NC
UC3845P	OBSOLETE	PDIP	P	8		None	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

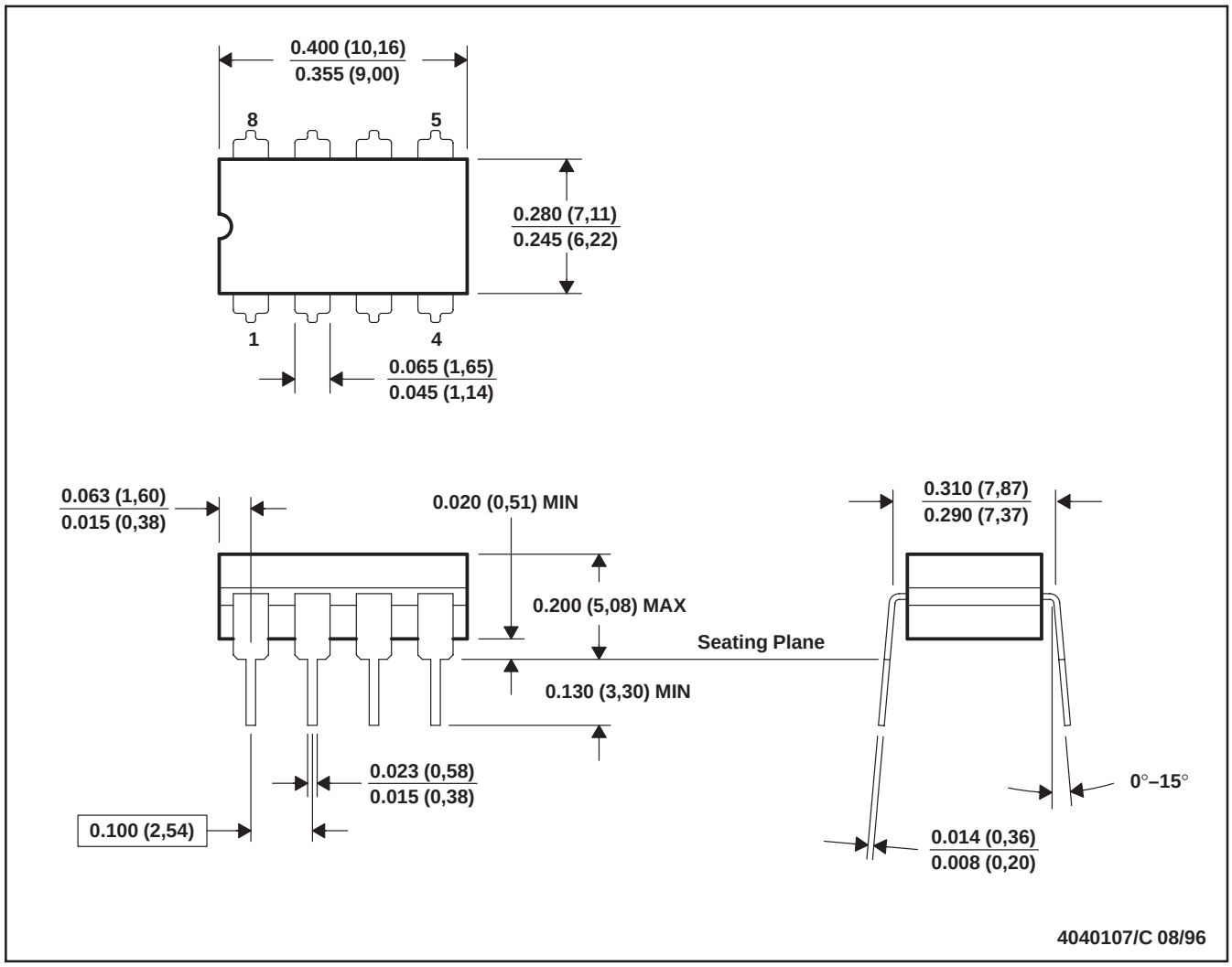
[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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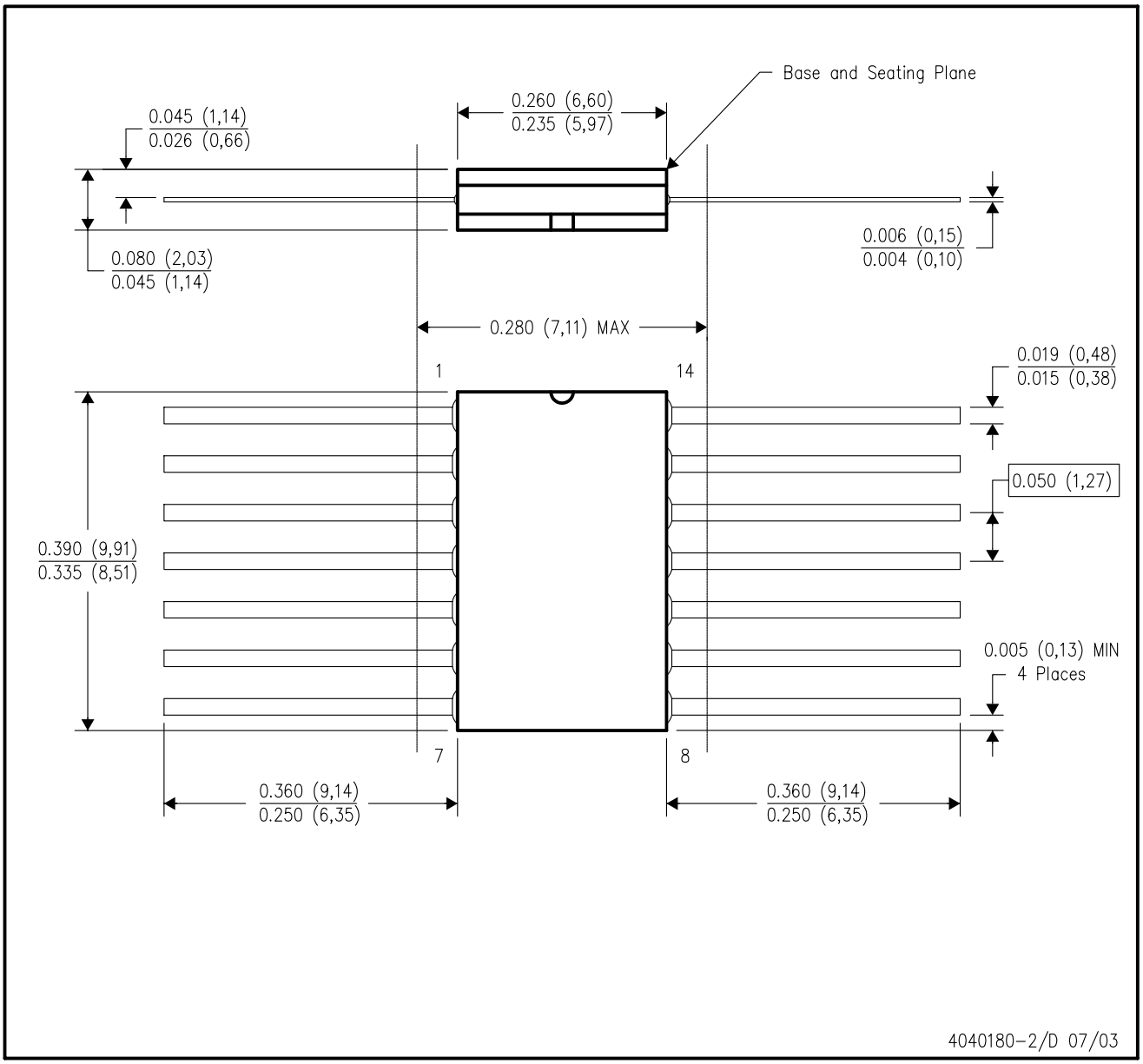
MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

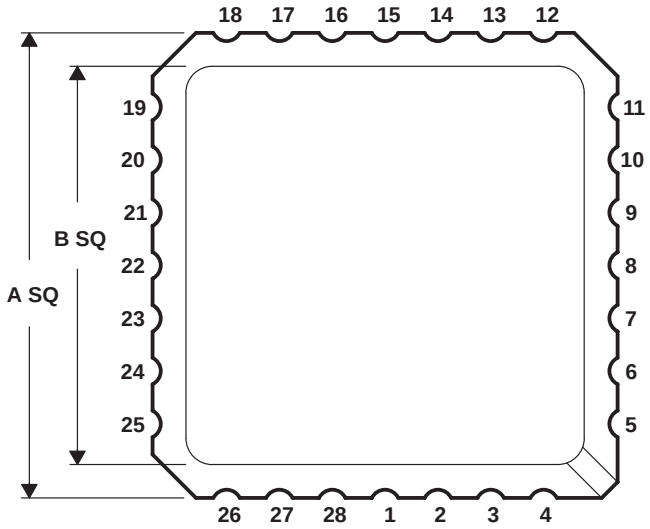
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



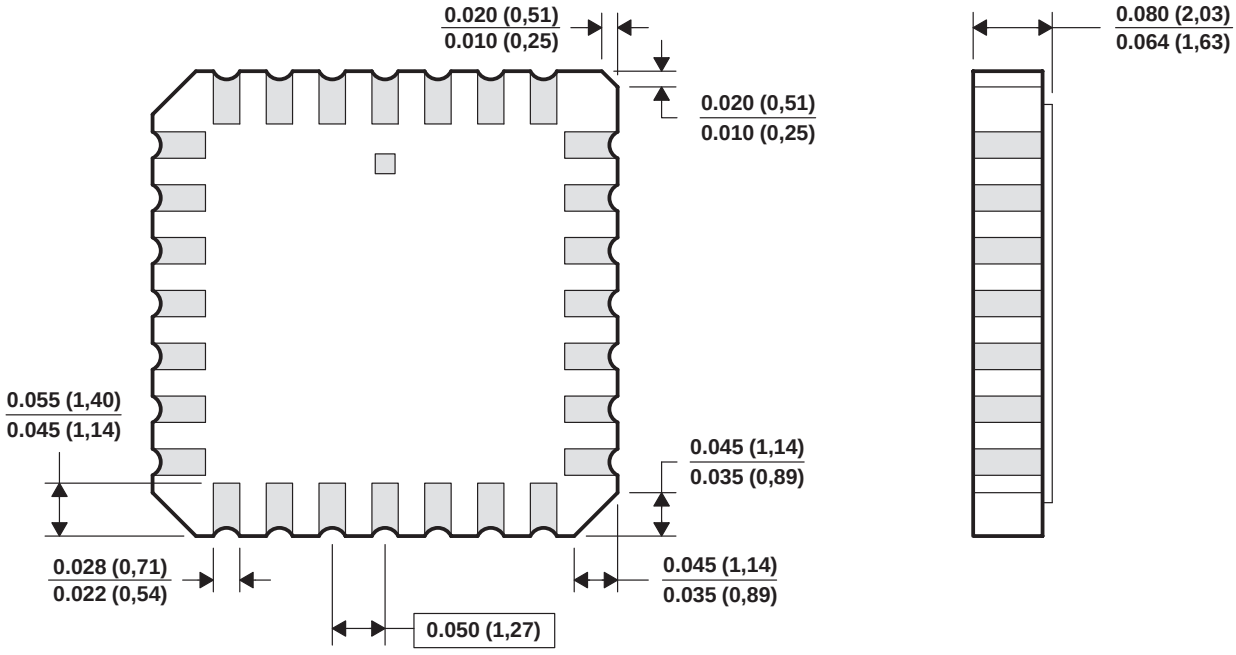
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14 and JEDEC MO–092AB

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

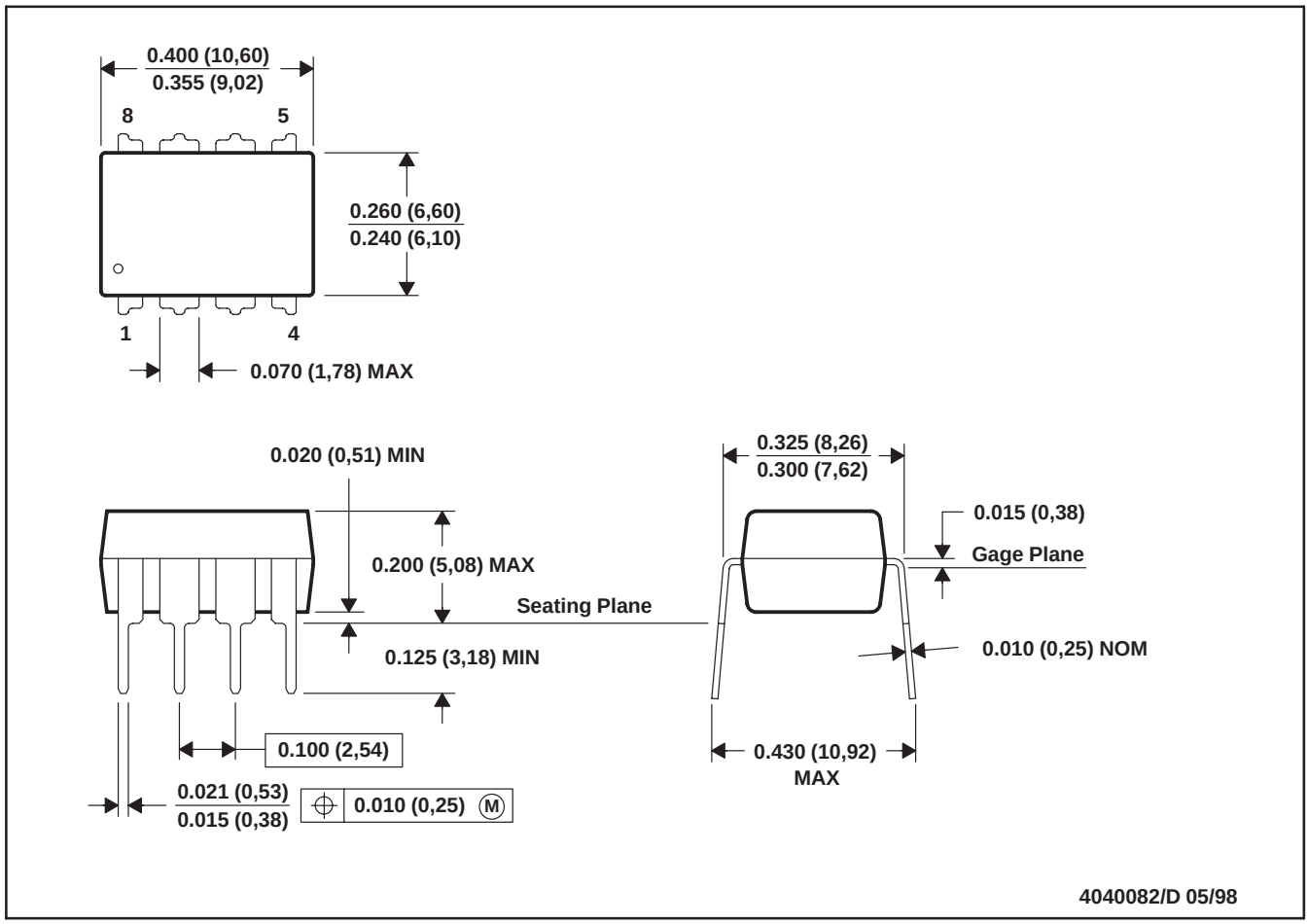


4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

MPDI001A – JANUARY 1995 – REVISED JUNE 1999

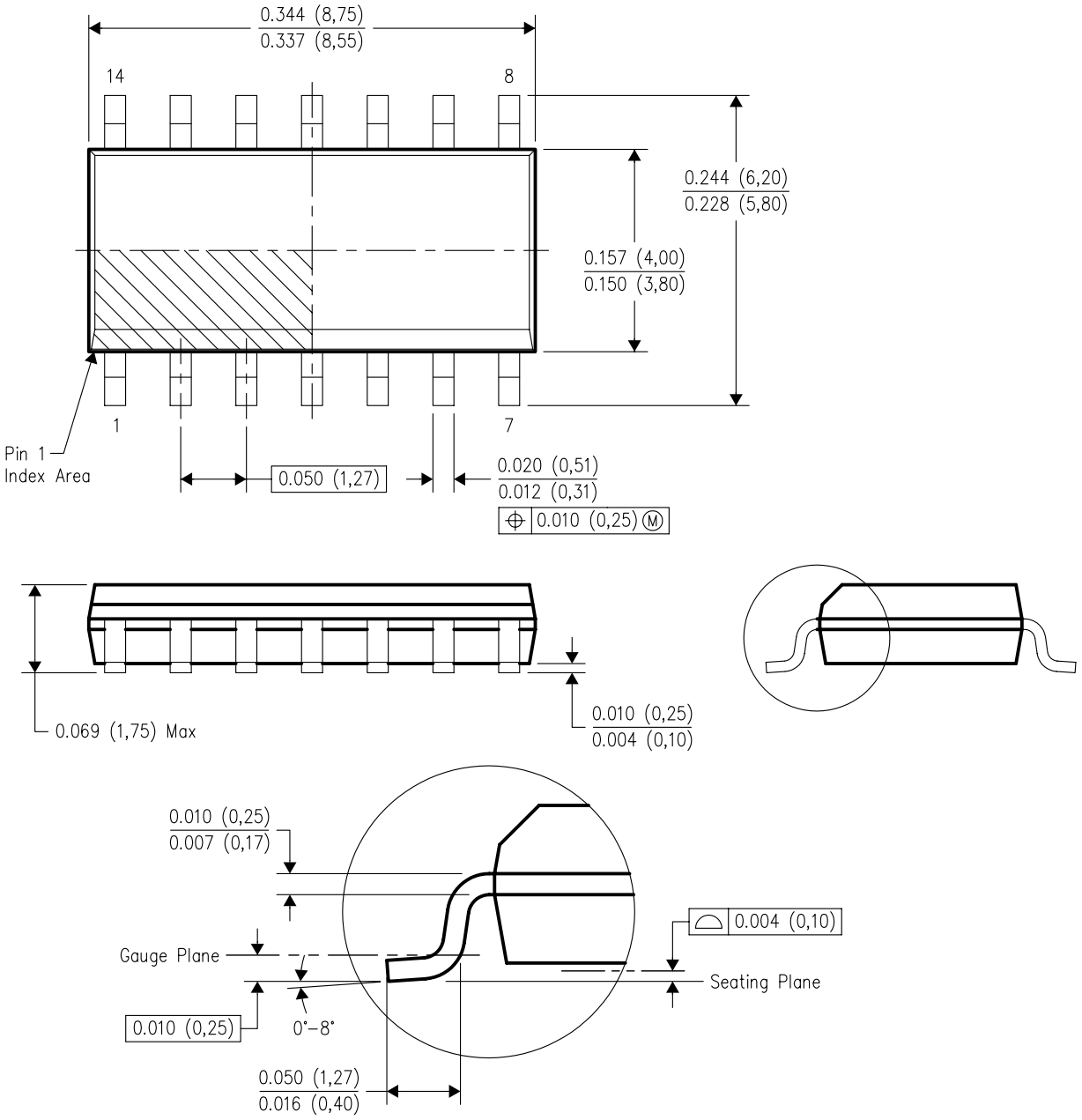
P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



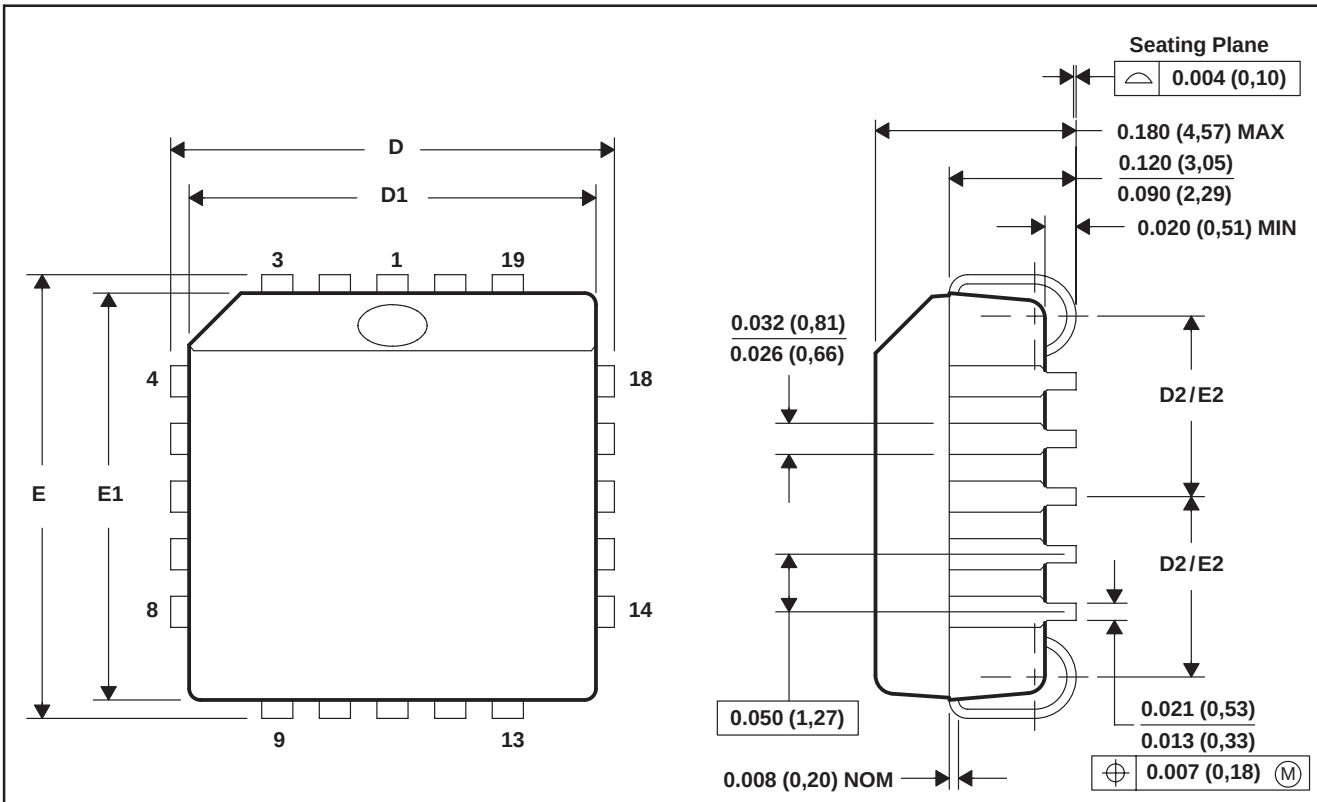
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AB.

MPLC004A – OCTOBER 1994

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN

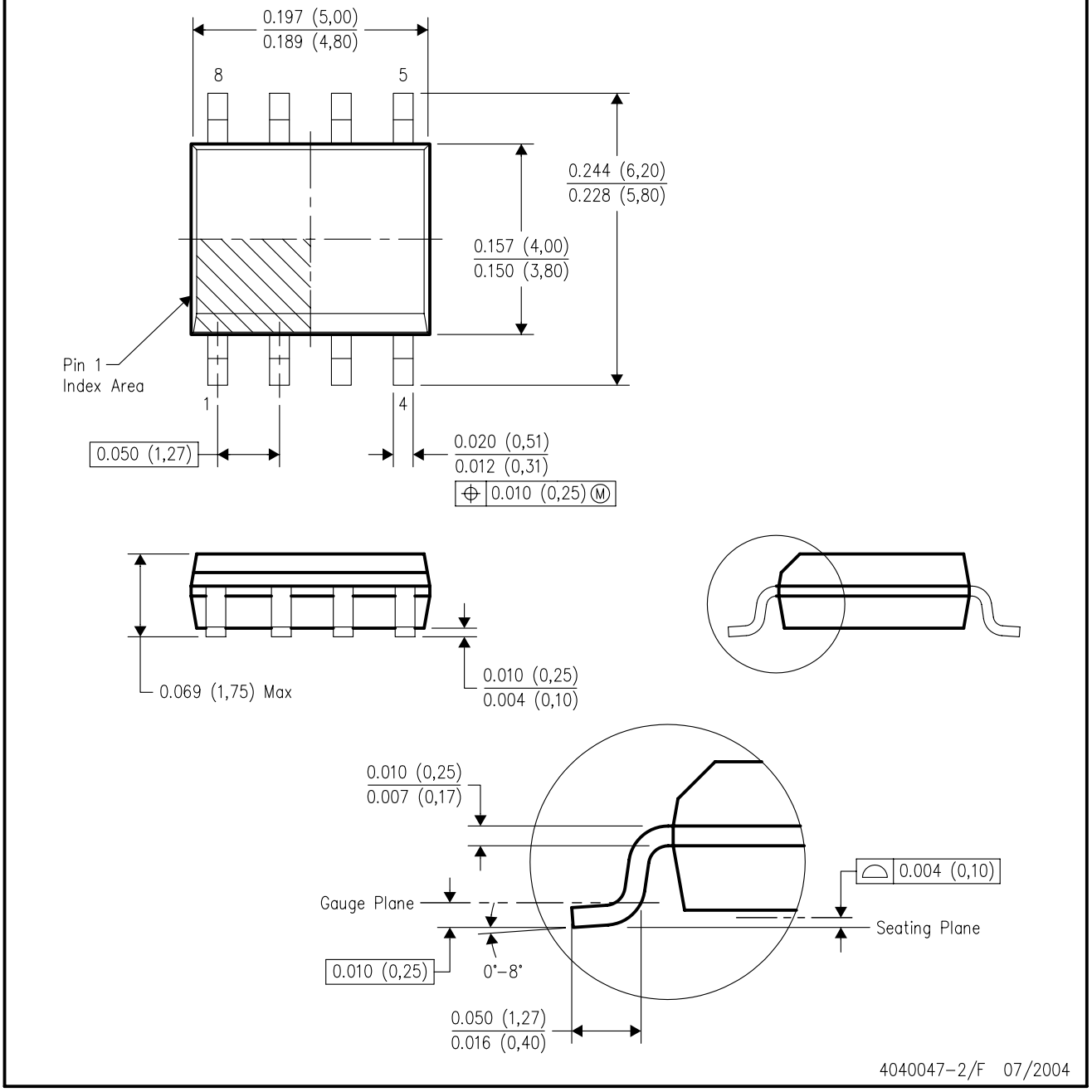


NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

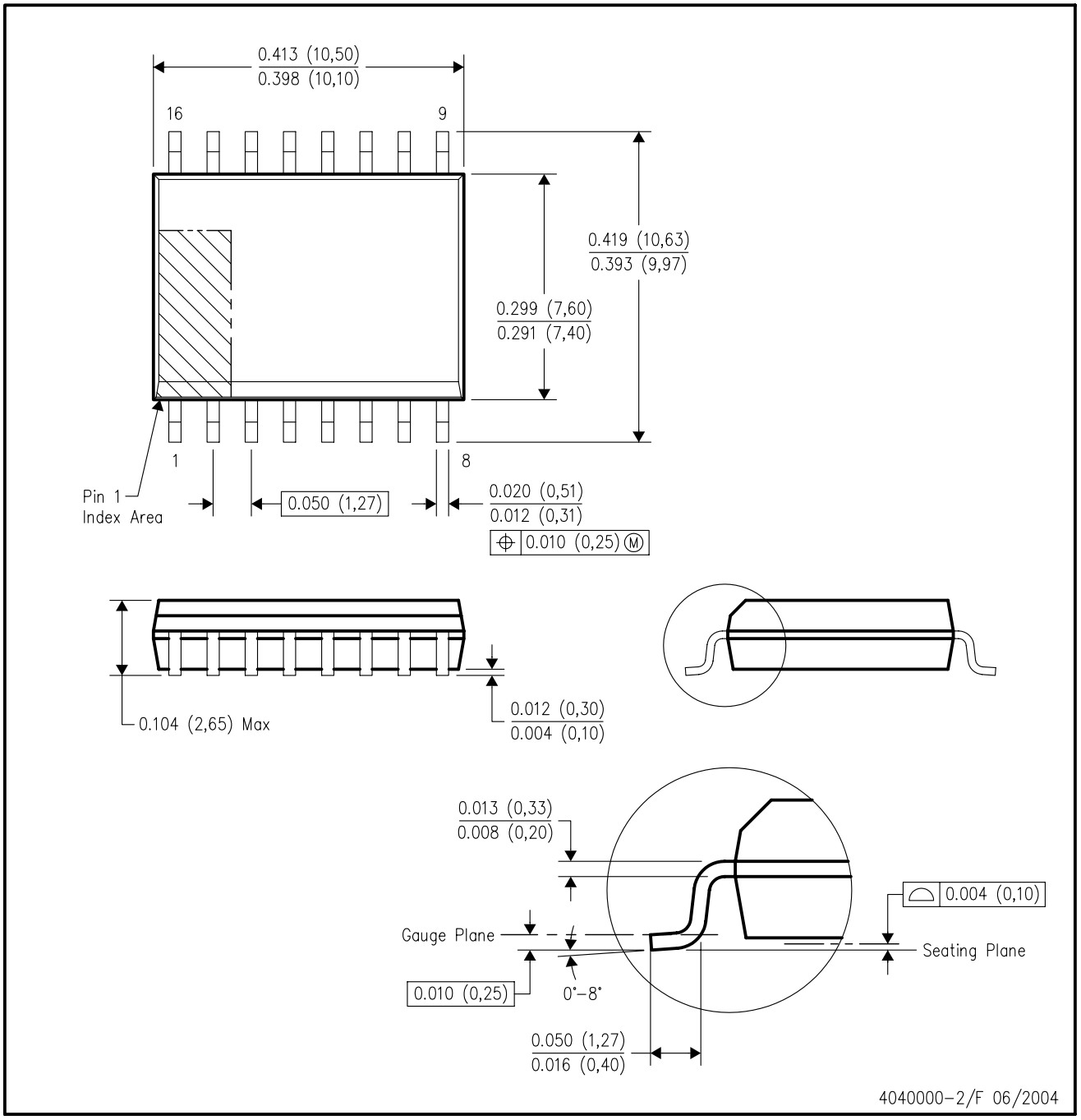
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AA.

DW (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

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