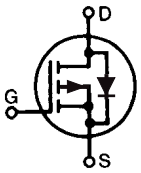
IXYS

PolarP™ Power MOSFET

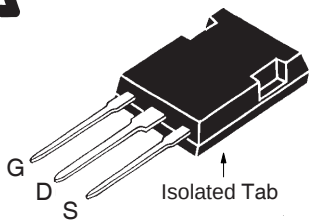
IXTR170P10P

V_{DSS} = -100V
I_{D25} = -108A
$R_{DS(on)}$ ≤ 13mΩ

P-Channel Enhancement Mode
Avalanche Rated



ISOPLUS247
E153432



G = Gate D = Drain
S = Source

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	-100	V
V_{DGR}	T_J = 25°C to 150°C, R_{GS} = 1MΩ	-100	V
V_{GSS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_C = 25°C	-108	A
I_{DM}	T_C = 25°C, Pulse Width Limited by T_{JM}	- 510	A
I_A	T_C = 25°C	-170	A
E_{AS}	T_C = 25°C	3.5	J
dV/dt	I_S ≤ I_{DM}, V_{DD} ≤ V_{DSS}, T_J ≤ 150°C	10	V/ns
P_D	T_C = 25°C	312	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6mm (0.062 in.) from Case for 10s	300	°C
T_{SOLD}	Plastic Body for 10s	260	°C
V_{ISOL}	50/60 H_Z ,RMS, t= 1min	2500	V~
M_d	Mounting Force	20..120/4.5..27	N/lb.
Weight		5	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0V, I_D = - 250μA	-100			V
$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1mA	- 2.0		- 4.0	V
I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V			±100	nA
I_{DSS}	V_{DS} = V_{DSS}, V_{GS}= 0V			- 50	μA
	T_J = 125°C			- 250	μA
$R_{DS(on)}$	V_{GS} = -10V, I_D = - 85A, Note 1			13	mΩ

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
  - UL Recognized Package
  - Isolated Mounting Surface
  - 2500V Electrical Isolation
- Dynamic dv/dt Rating
- High Current Handling Capability
- Avalanche Rated
- Fast Intrinsic Diode
- The Rugged PolarP™ Process
- Low Q_G
- Low Drain-to-Tab Capacitance
- Low Package Inductance

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- High-Side Switches
- Push Pull Amplifiers
- DC Choppers
- Automatic Test Equipment
- Current Regulators

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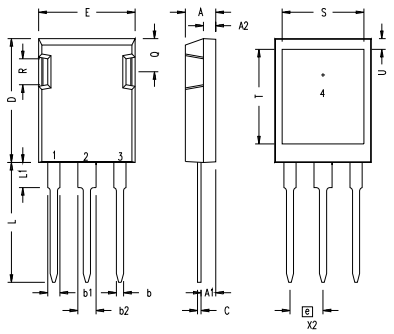
Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	V_{DS} = -10V, I_D = - 85A, Note 1	35	58		S
C_{iss}	V_{GS} = 0V, V_{DS} = - 25V, f = 1MHz		12.6		nF
C_{oss}			4190		pF
C_{rss}			930		pF
$t_{d(on)}$	**Resistive Switching Times**		32		ns
t_r	V_{GS} = -10V, V_{DS} = 0.5 • V_{DSS}, I_D = - 85A		75		ns
$t_{d(off)}$	R_G = 1Ω (External)		82		ns
t_f			45		ns
$Q_{g(on)}$	V_{GS} = -10V, V_{DS} = 0.5 • V_{DSS}, I_D = - 85A		240		nC
Q_{gs}			45		nC
Q_{gd}			120		nC
R_{thJC}				0.40	°C/W
R_{thCS}			0.15		°C/W

Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
I_S	V_{GS} = 0V			-170	A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			- 680	A
V_{SD}	I_F = - 85A, V_{GS} = 0V, Note 1			- 3.3	V
t_{rr}	I_F = - 85A, -di/dt = -100A/μs		176		ns
Q_{RM}	V_R = - 50V, V_{GS} = 0V		1.25		μC
I_{RM}			-14.2		A

Note 1: Pulse Test, t ≤ 300μs; Duty Cycle, d ≤ 2%.

ISOPLUS247 (IXTR) Outline



1 - Gate
2,4 - Drain
3 - Source

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.084	1.91	2.13
b2	.115	.123	2.92	3.12
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,931,844 5,049,961 5,237,481 6,162,665 6,404,065 B1 6,683,344 6,727,585 7,005,734 B2 7,157,338B2 4,850,072 5,017,508 5,063,307 5,381,025 6,259,123 B1 6,534,343 6,710,405 B2 6,759,692 7,063,975 B2 4,881,106 5,034,796 5,187,117 5,486,715 6,306,728 B1 6,583,505 6,710,463 6,771,478 B2 7,071,537

Fig. 1. Output Characteristics @ T_J = 25ºC

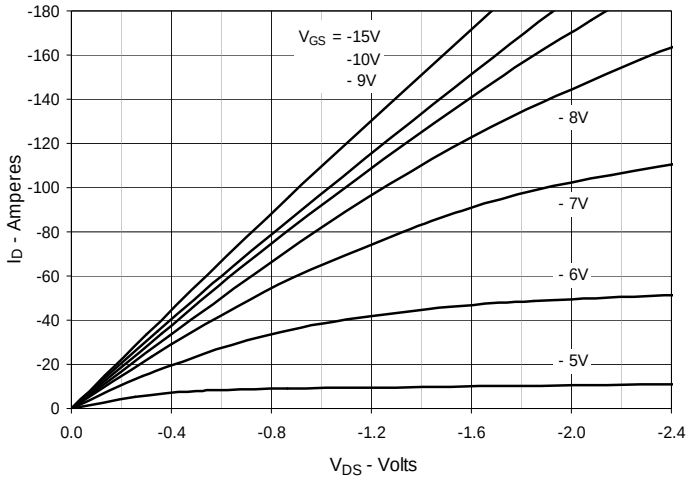


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

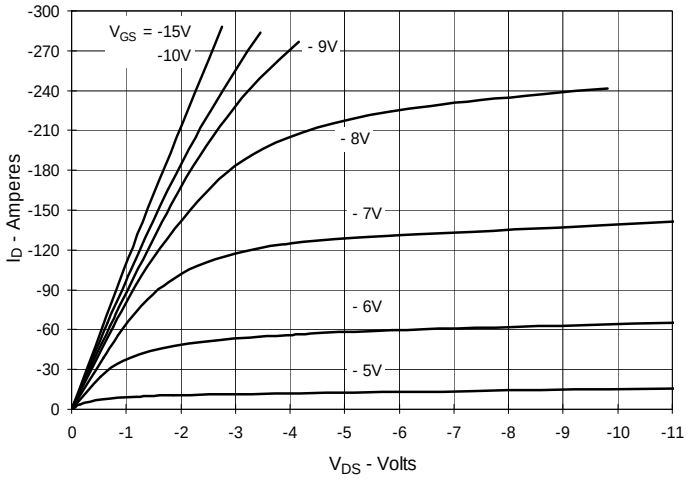


Fig. 3. Output Characteristics @ T_J = 125ºC

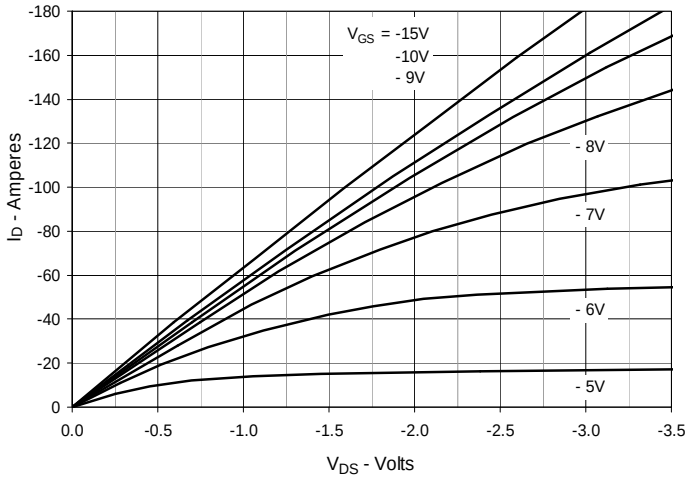


Fig. 4. $R_{DS(on)}$ Normalized to I_D = - 85A Value vs. Junction Temperature

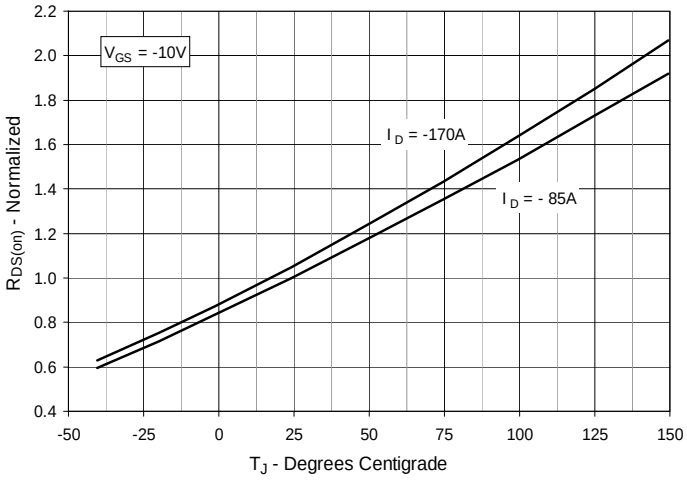


Fig. 5. $R_{DS(on)}$ Normalized to I_D = - 85A Value vs. Drain Current

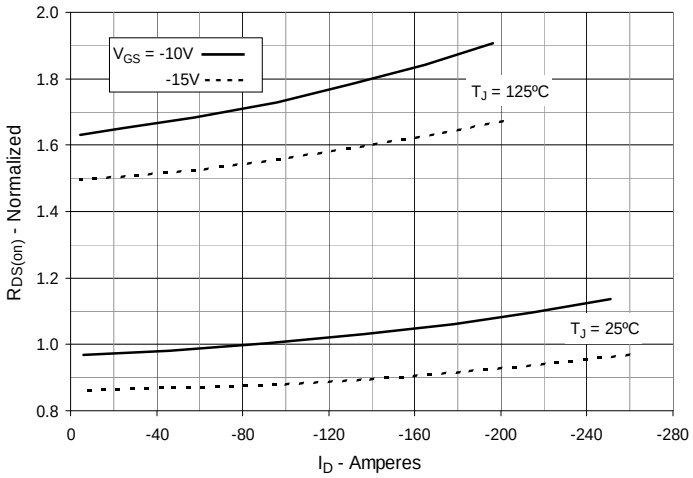


Fig. 6. Maximum Drain Current vs. Case Temperature

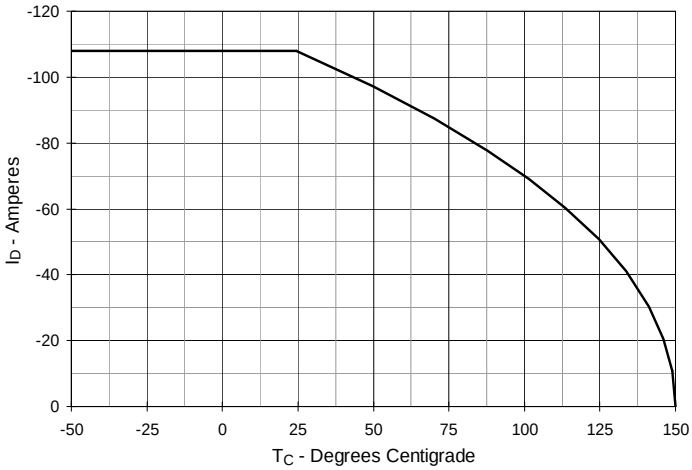


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Fig. 7. Input Admittance

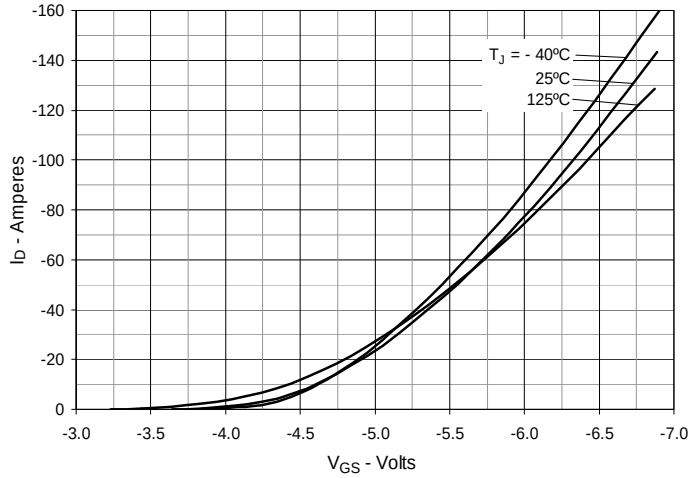

Fig. 8. Transconductance

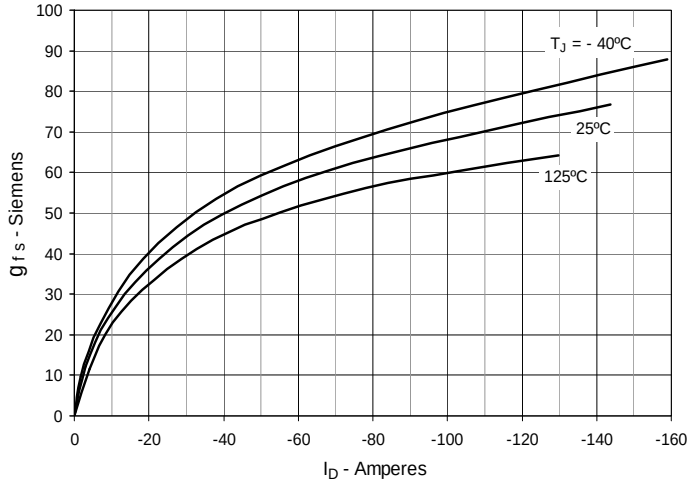

Fig. 9. Forward Voltage Drop of Intrinsic Diode

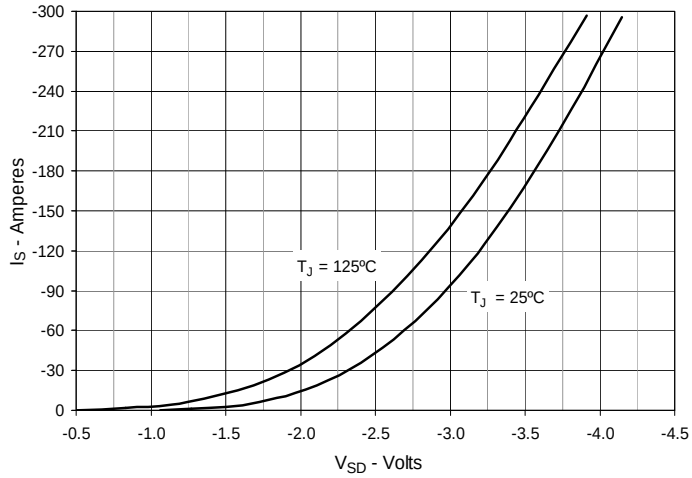

Fig. 10. Gate Charge

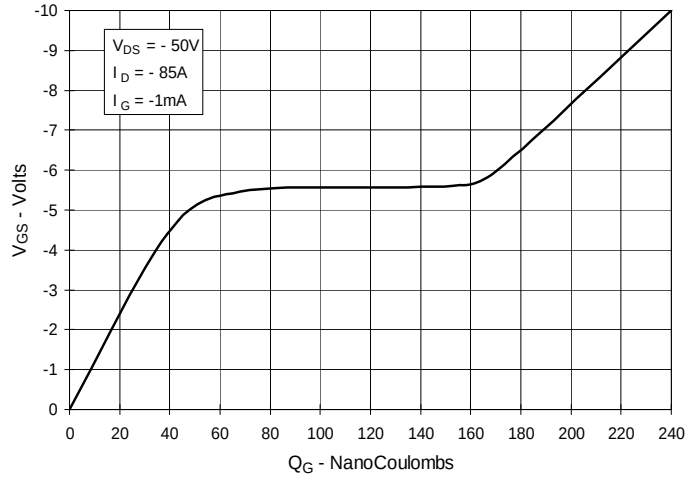

Fig. 11. Capacitance

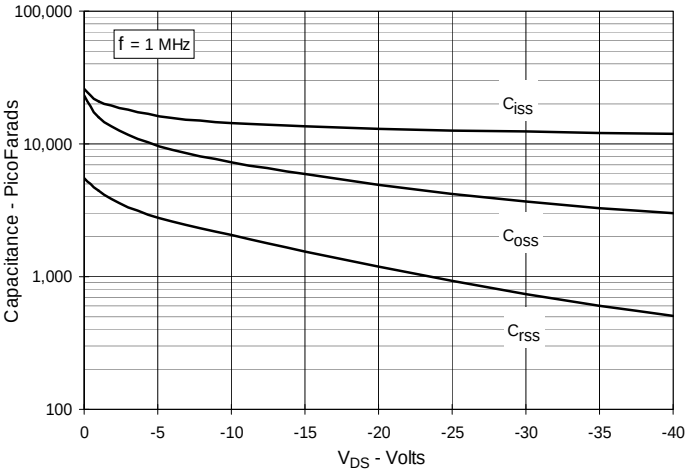

Fig. 12. Forward-Bias Safe Operating Area

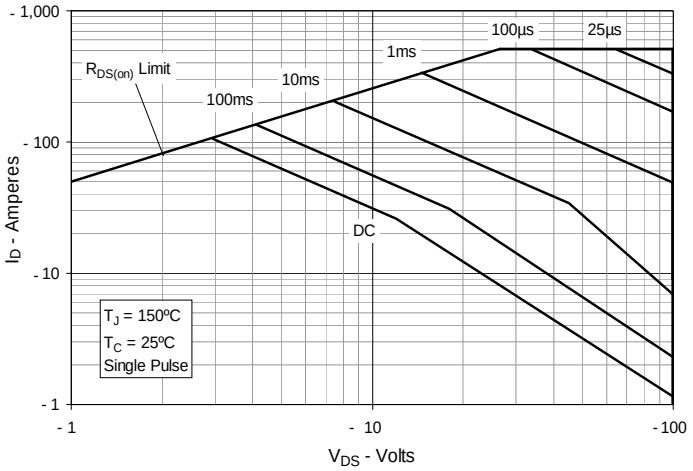

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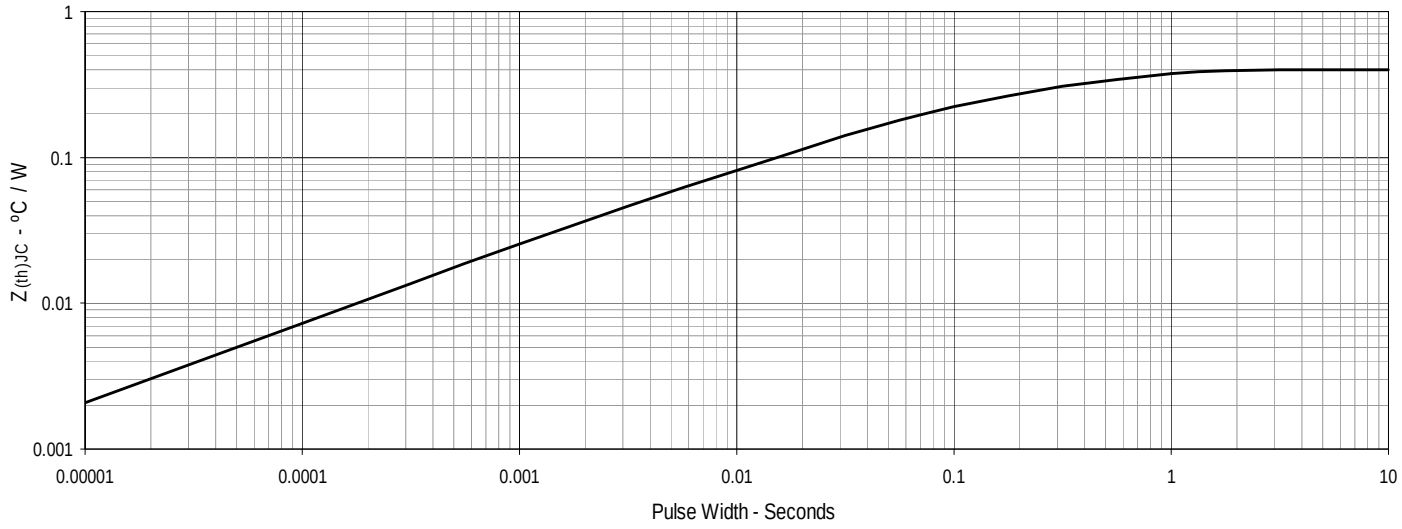
Fig. 13. Maximum Transient Thermal Impedance



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